SILICON GATE CMOS

524,288 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC518512PL is a 4M bit high speed CMOS pseudo static RAM organized as 524,288 words by 8 bits. The TC518512PL utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC518512PL-LV operates from a single 3.0V ~ 5.5V power supply. Refreshing is supported by a refresh ($\overline{OE}$/$\overline{RFSH}$) input which enables two types of refreshing - auto refresh and self refresh. The TC518512PL features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

The TC518512PL is available in a 32-pin, 0.6 inch width plastic DIP, a small outline plastic flat package, and a thin small outline package (forward type, reverse type).

Features

- Organization: 524,288 words x 8 bits
- Low voltage operation: 3.0V ~ 5.5V
- Data retention supply voltage: 3.0V ~ 5.5V
- Fast access time

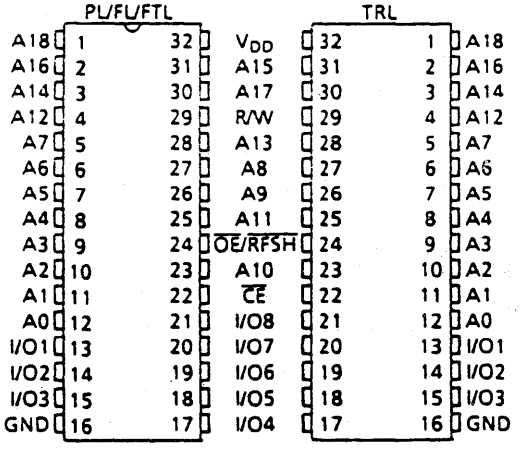
		TC518512PL-LV Family		
		-70	-80	-10
t_{CEA} $\overline{CE}$ Access Time		70ns	80ns	100ns
t_{OEA} $\overline{OE}$ Access Time		30ns	30ns	40ns
t_{RC} Cycle Time		115ns	130ns	160ns
Power Dissipation		385mW	330mW	275mW
Self Refresh Current	5.5V	200μA		
Self Refresh Current	3.0V	100μA		

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 2048 refresh cycles/32ms
- Package
  - TC518512PL: DIP32-P-600
  - TC518512FL: SOP32-P-525
  - TC518512FTL: TSOP32-P-400
  - TC518512TRL: TSOP32-P-400A

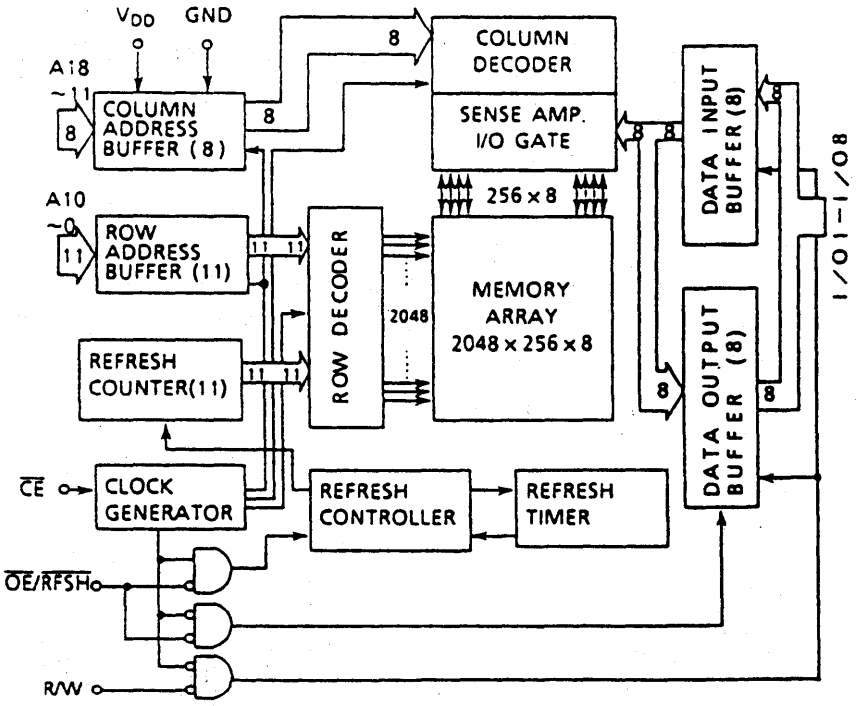
Pin Names

A0 ~ A18	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$/$\overline{RFSH}$	Output Enable Input Refresh Input
$\overline{CE}$	Chip Enable Input
I/O1 ~ I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

Pin Connection (Top View)



Block Diagram



Operating Mode

MODE \ PIN	$\overline{CE}$	$\overline{OE}$/$\overline{RFSH}$	R/W	A0 ~ A18	I/O1 ~ 8
Read	L	L	H	V*	OUT
Write	L	*	L	V*	IN
$\overline{CE}$ only Refresh	L	H	H	V*	HZ
Auto/Self Refresh	H	L	*	*	HZ
Standby	H	H	*	*	HZ

H = High level input (V_{IH})
L = Low level input (V_{IL})
* = V_{IH} or V_{IL}
V* = At the falling edge of $\overline{CE}$, all address inputs are latched. At all other times, the address inputs are "*".
HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	0 ~ 70	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	V_{DD} + 1.0	V	
V_{IL}	Input Low Voltage	-1.0	–	0.8	V	

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) $\overline{CE}$, Address cycling: t_{RC} = t_{RC} min.	70ns version	–	50	70	mA	3,4
		80ns version	–	45	60		
		100ns version	–	35	50		
I_{DDS1}	Standby Current $\overline{CE}$ = V_{IH}, $\overline{OE}/\overline{RFSH}$ = V_{IH}		–	–	1	mA	
I_{DDS2}	Standby Current $\overline{CE}$ = V_{DD} - 0.2V, $\overline{OE}/\overline{RFSH}$ = V_{DD} - 0.2V		–	–	200	µA	
I_{DDF1}	Self Refresh Current (Average) $\overline{CE}$ = V_{IH}, $\overline{OE}/\overline{RFSH}$ = V_{IL}		–	–	1	mA	
I_{DDF2}	Self Refresh Current (Average) $\overline{CE}$ = V_{DD} - 0.2V, $\overline{OE}/\overline{RFSH}$ = 0.2V		–	–	200	µA	
I_{DDF3}	Auto Refresh Current (Average) $\overline{OE}/\overline{RFSH}$ cycling: t_{FC} = t_{FC} min.	70ns version	–	–	70	mA	3
		80ns version	–	–	60		
		100ns version	–	–	50		
I_{DDF4}	$\overline{CE}$ only Refresh Current (Average) $\overline{CE}$, Address cycling: t_{RC} = t_{RC} min.	70ns version	–	–	70	mA	3
		80ns version	–	–	60		
		100ns version	–	–	50		
$I_{I(L)}$	Input Leakage Current 0V ≤ V_{IN} ≤ V_{DD}, All other Inputs not under test = 0V		–	–	±10	µA	
$I_{O(L)}$	Output Leakage Current Output Disabled ($\overline{CE}$ = V_{IH} or $\overline{OE}/\overline{RFSH}$ = V_{IH} or R/W = V_{IL}) 0V ≤ V_{OUT} ≤ V_{DD}		–	–	±10	µA	
V_{OH}	Output High Level I_{OH} = -1.0mA		2.4	–	–	V	
V_{OL}	Output Low Level I_{OL} = 2.1mA		–	–	0.4	V	

Capacitance* (V_{DD} = 5V, Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A18)	–	5	pF
C_{I2}	Input Capacitance ($\overline{CE}$, $\overline{OE}/\overline{RFSH}$, R/W)	–	7	
C_{IO}	Input/Output Capacitance	–	7	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	-70		-80		-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	115	–	130	–	160	–	ns	
t_{RMW}	Read Modify Write Cycle Time	165	–	180	–	220	–		
t_{CE}	$\overline{CE}$ Pulse Width	70	10,000	80	10,000	100	10,000		
t_P	$\overline{CE}$ Precharge Time	35	–	40	–	50	–		
t_{CEA}	$\overline{CE}$ Access Time	–	70	–	80	–	100		
t_{OEA}	$\overline{OE}$ Access Time	–	30	–	30	–	40		
t_{CLZ}	$\overline{CE}$ to Output in Low -Z	20	–	20	–	20	–		
t_{OLZ}	$\overline{OE}$ to Output in Low -Z	0	–	0	–	0	–		
t_{WLZ}	Output Active from End of Write	0	–	0	–	0	–		
t_{CHZ}	Chip Disable to Output in High-Z	0	20	0	20	0	25		9
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	20	0	20	0	25		9
t_{WHZ}	Write Enable to Output in High-Z	0	20	0	20	0	25		9
t_{OSC}	$\overline{OE}$ Setup Time Referenced to $\overline{CE}$	10	–	10	–	10	–		9
t_{OHC}	$\overline{OE}$ Hold Time Referenced to $\overline{CE}$	0	–	0	–	0	–		9
t_{RCS}	Read Command Setup Time	0	–	0	–	0	–		
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–		
t_{WP}	Write Pulse Width	25	–	25	–	30	–		
t_{WCH}	Write Command Hold Time	40	–	40	–	50	–		
t_{CWL}	Write Command to $\overline{CE}$ Lead Time	25	–	25	–	30	–		
t_{DSW}	Data Setup Time from R/W	20	–	20	–	25	–		10
t_{DSC}	Data Setup Time from $\overline{CE}$	20	–	20	–	25	–		10
t_{DHW}	Data Hold Time from R/W	0	–	0	–	0	–		10
t_{DHC}	Data Hold Time from $\overline{CE}$	0	–	0	–	0	–		10
t_{ASC}	Address Setup Time	0	–	0	–	0	–		11
t_{AHC}	Address Hold Time	15	–	20	–	25	–		11
t_{FC}	Auto Refresh Cycle Time	130	–	130	–	160	–		
t_{RFD}	$\overline{RFSH}$ Delay Time from $\overline{CE}$	40	–	40	–	50	–		
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000		12
t_{FP}	$\overline{RFSH}$ Precharge Time	30	–	30	–	30	–		12
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	–	8,000	–	8,000	–		12
t_{FRS}	$\overline{CE}$ Delay Time from $\overline{RFSH}$ (Self Refresh)	160	–	160	–	190	–		12
t_{REF}	Refresh Period (2048 cycles, A0 ~ A10)	–	32	–	32	–	32	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

3.3V Operation

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V	2
V_{IH}	Input High Voltage	V_{DD} - 0.2V	–	V_{DD} + 1. 0	V	
V_{IL}	Input Low Voltage	-0.5	–	0.2	V	

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 3.3V±0.3V)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) $\overline{CE}$, Address cycling: t_{RC} = t_{RC} min.	–	15	20	mA	3,4
I_{DDS2}	Standby Current	–	–	100	µA	
I_{DDF2}	Self Refresh Current (Average)	–	50	100	µA	
I_{DDF3}	Auto Refresh Current (Average) $\overline{RFSH}$ cycling: t_{FC} = t_{FC} min.	–	–	20	mA	3
I_{DDF4}	$\overline{CE}$ only Refresh Current (Average) $\overline{CE}$, Address cycling: t_{RC} = t_{RC} min.	–	–	20	mA	3
$I_{I(L)}$	Input Leakage Current 0V ≤ V_{IN} ≤ V_{DD}, All other Inputs not under test = 0V	–	–	±10	µA	
$I_{O(L)}$	Output Leakage Current Output Disabled, 0V ≤ V_{OUT} ≤ V_{DD}	–	–	±10	µA	
V_{OH}	Output High Level, I_{OH} = -100µA	V_{DD} - 0.2V	–	–	V	
V_{OL}	Output Low Level, I_{OL} = 100µA	–	–	0.2	V	

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 3.3V±0.3V) (Notes: 5, 6, 8)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTES
t_{RC}	Random Read, Write Cycle Time	230	–		
t_{RMW}	Read Modify Write Cycle Time	305	–		
t_{CE}	$\overline{CE}$ Pulse Width	150	10,000		
t_P	$\overline{CE}$ Precharge Time	80	–		
t_{CEA}	$\overline{CE}$ Access Time	–	150		
t_{OEA}	$\overline{OE}$ Access Time	–	80		
t_{CLZ}	$\overline{CE}$ to Output in Low -Z	20	–		
t_{OLZ}	$\overline{OE}$ to Output in Low -Z	5	–		
t_{WLZ}	Output Active from End of Write	5	–		
t_{CHZ}	Chip Disable to Output in High-Z	0	30		9
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	30		9
t_{WHZ}	Write Enable to Output in High-Z	0	30		9
t_{OSC}	$\overline{OE}$ Setup Time Referenced to $\overline{CE}$	10	–		9
t_{OHC}	$\overline{OE}$ Hold Time Referenced to $\overline{CE}$	15	–		9
t_{RCS}	Read Command Setup Time	0	–		
t_{RCH}	Read Command Hold Time	0	–	ns	
t_{WP}	Write Pulse Width	35	–		
t_{WCH}	Write Command Hold Time	70	–		
t_{CWL}	Write Command to $\overline{CE}$ Lead Time	35	–		
t_{DSW}	Data Setup Time from R/W	30	–		10
t_{DSC}	Data Setup Time from $\overline{CE}$	30	–		10
t_{DHW}	Data Hold Time from R/W	0	–		10
t_{DHC}	Data Hold Time from $\overline{CE}$	0	–		10
t_{ASC}	Address Setup Time	0	–		11
t_{AHC}	Address Hold Time	30	–		11
t_{FC}	Auto Refresh Cycle Time	230	–		
t_{RFD}	$\overline{RFSH}$ Delay Time from $\overline{CE}$	80	–		
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	80	8,000		12
t_{FP}	$\overline{RFSH}$ Precharge Time	50	–		12
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	–		12
t_{FRS}	$\overline{CE}$ Delay Time from $\overline{RFSH}$ (Self Refresh)	300	–		12
t_{REF}	Refresh Period (2048 cycles, A0 ~ A10)	–	32	ms	
t_T	Transition Time (Rise and Fall)	3	50	ns	

Timing Reference Levels:
Input Reference Levels: 1.5V/1.5V
Output Reference Levels: 1.5V/1.5V

Notes:

1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.

2) All voltages are referenced to GND.

3) I_{DDO}, I_{DDF3}, and I_{DDF4} depend on the cycle time.

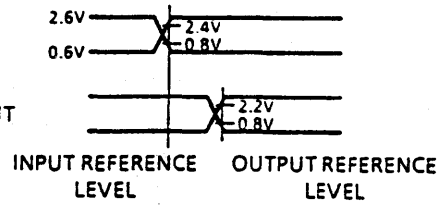
4) I_{DDO} depends on the output loading. Specified values are obtained with the outputs open.

5) An initial pause of 100μs with high $\overline{CE}$ is required after power-up before proper device operation is achieved.

6) AC measurements assume t_T = 5ns.

7) Timing reference levels

Input Levels	: V_{IH} = 2.6V V_{IL} = 0.6V	INPUT
Input Reference Levels	: V_{IH} = 2.4V V_{IL} = 0.8V	OUTPUT
Output Reference Levels	: V_{OH} = 2.2V V_{OL} = 0.8V	



8) Measured with a load equivalent to 1 TTL load and 100pF.

9) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

10) For write cycles, the input data is latched at the earlier of R/W or $\overline{CE}$ rising edge. Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).

11) All address inputs are latched at the falling edge of $\overline{CE}$. Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC}.

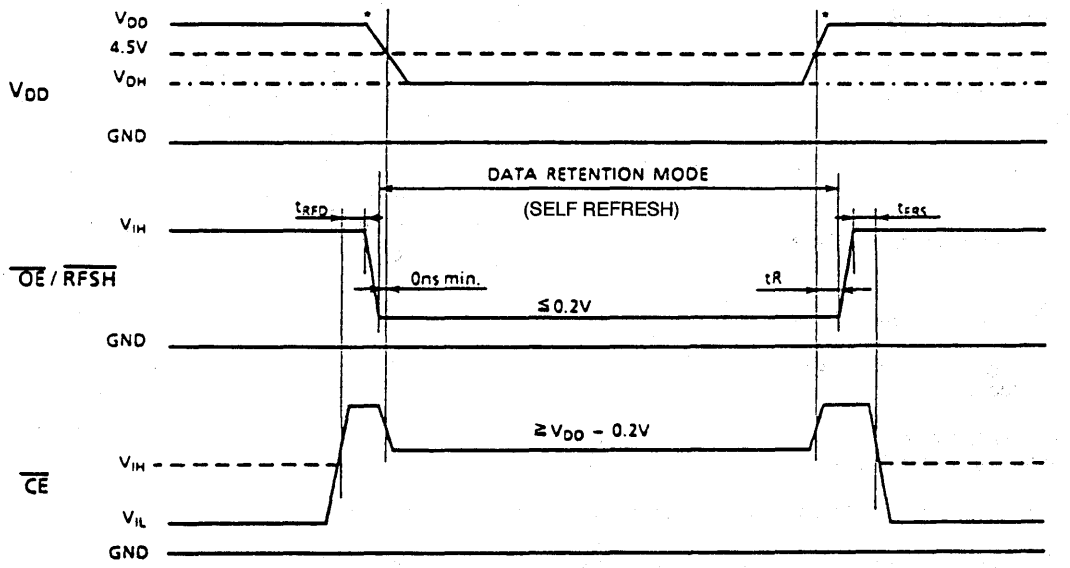
12) The two refresh operations, auto refresh and self refresh, are defined by the $\overline{RFSH}$ pulse width under the condition $\overline{CE}$ = V_{IH}.
Auto refresh : $\overline{RFSH}$ pulse width ≤ t_{FAP} (max.)
Self refresh : $\overline{RFSH}$ pulse width ≥ t_{FAS} (min.)

The timing parameter t_{FRS} must be met for proper device operation under the following conditions:
- after self refresh
- if $\overline{OE}$/$\overline{RFSH}$ = "L" after power-up

Data Retention Characteristics (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		3.0	–	5.5	V
I_{DDF2}	Self Refresh Current	V_{DH} = 3.0V	–	50	100	µA
		V_{DH} = 5.5V	–	100	200	
t_R	Recovery Time		5	–	–	ms

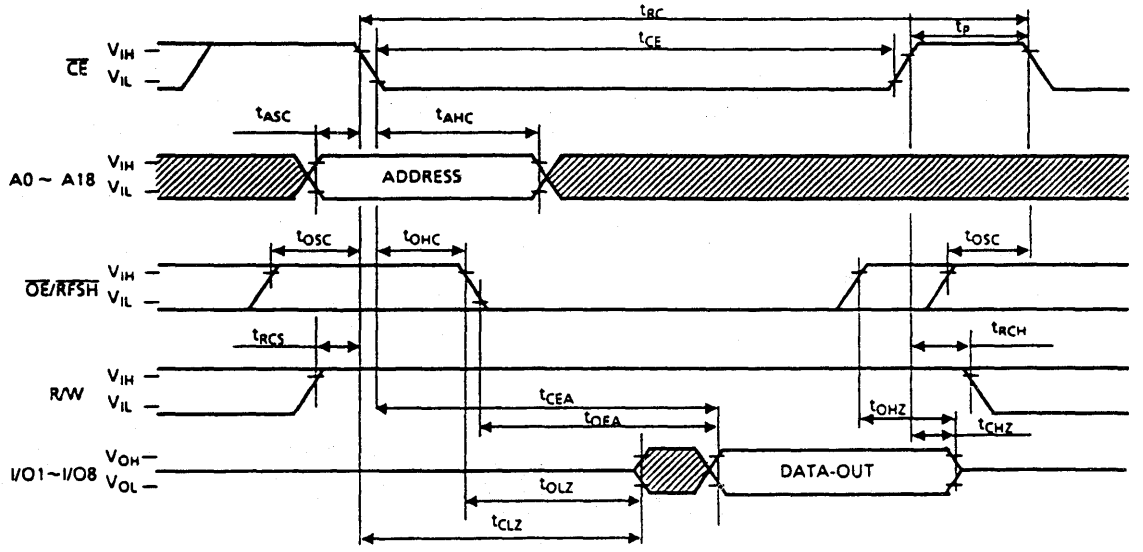
*The rising and falling slope of V_{DD} must be more than 50ms for proper device operation (20ms/V).



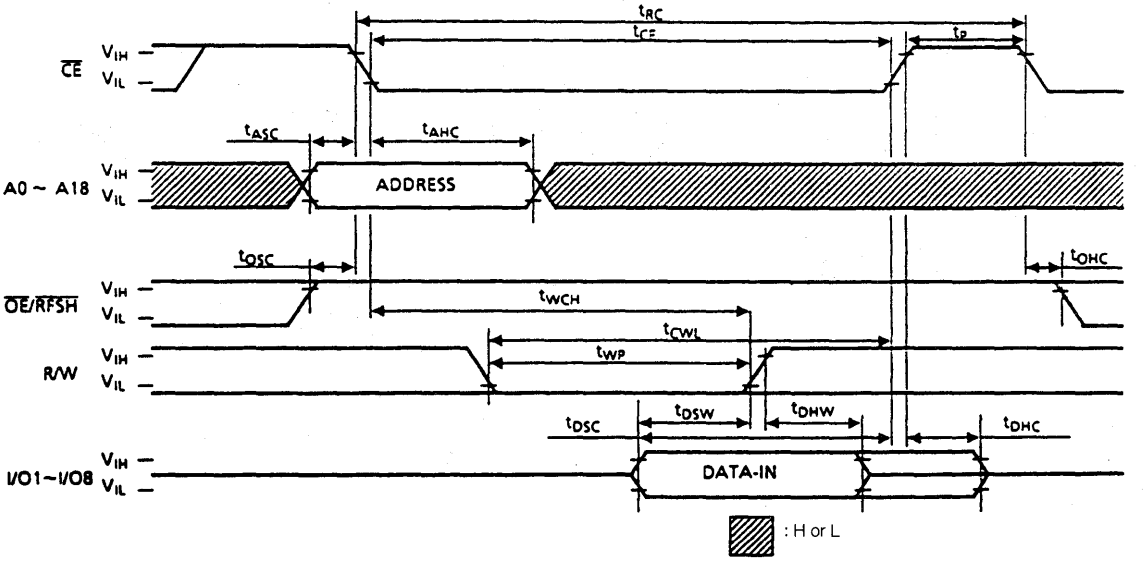
Notes: R/W, A0 ~ A18 = V_{IH} or V_{IL}
I_{DDF1} is applicable when $\overline{OE}/\overline{RFSH}$ = V_{IL} (max.), $\overline{CE}$ = V_{IH} (min.).

Timing Waveforms

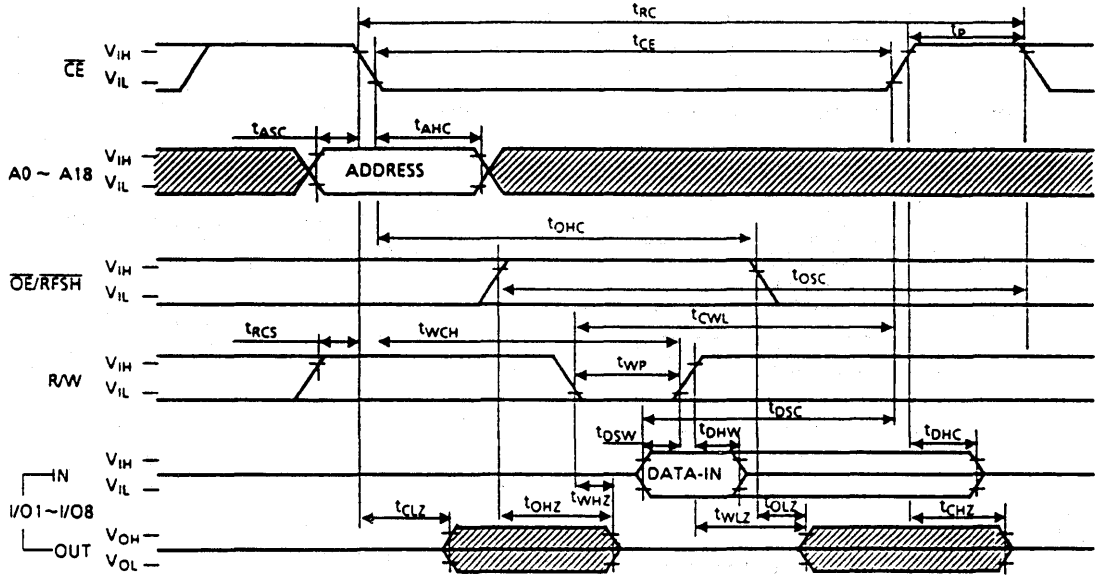
Read Cycle



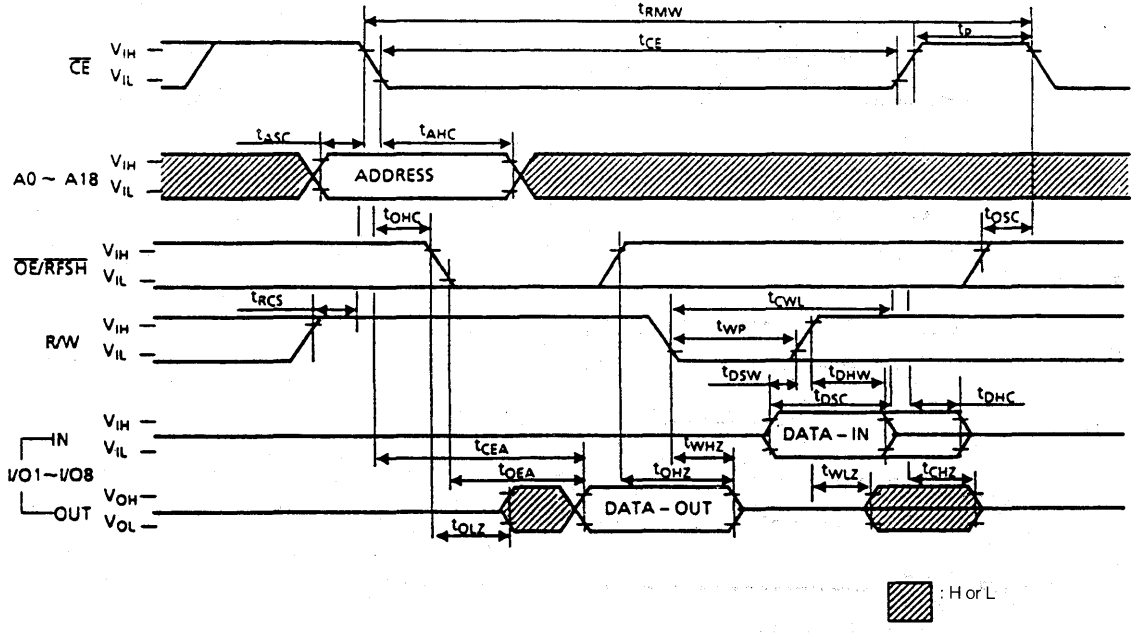
Write Cycle 1 ($\overline{OE}$ Fixed High)



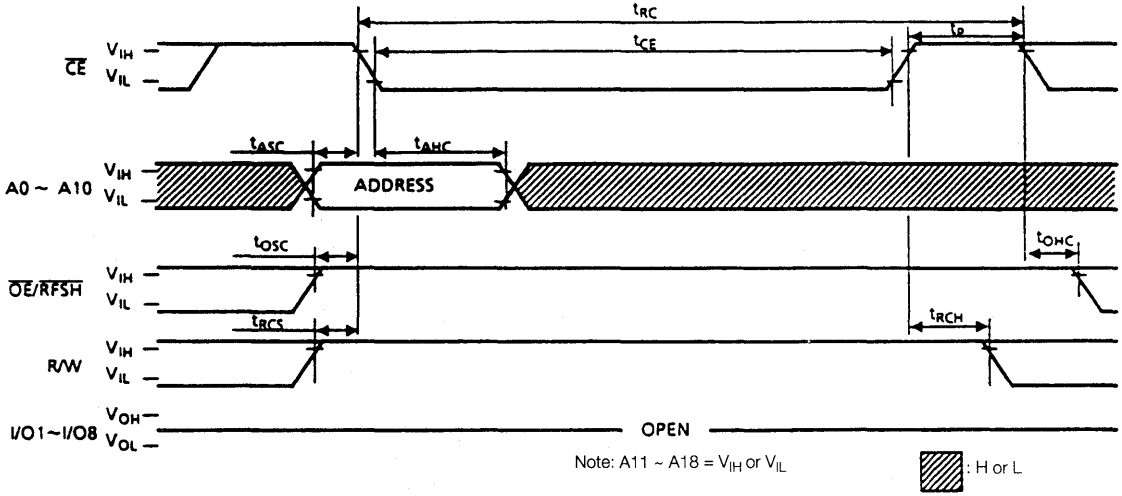
Write Cycle 2 ($\overline{OE}$ Clocked or Fixed Low)



Read Modify Write Cycle

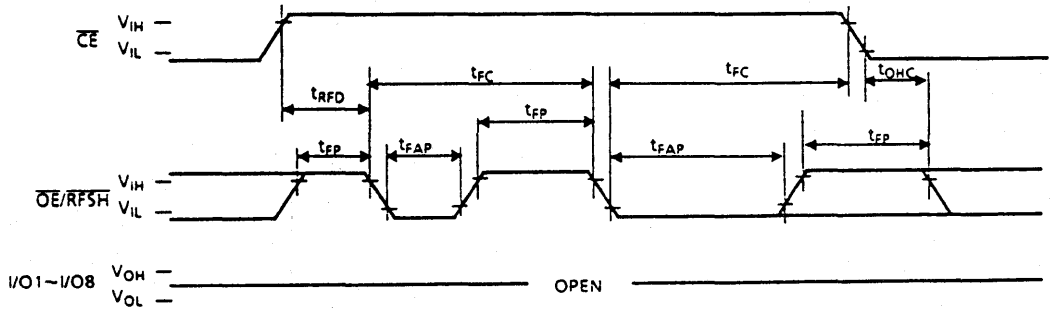


$\overline{CE}$ Only Refresh



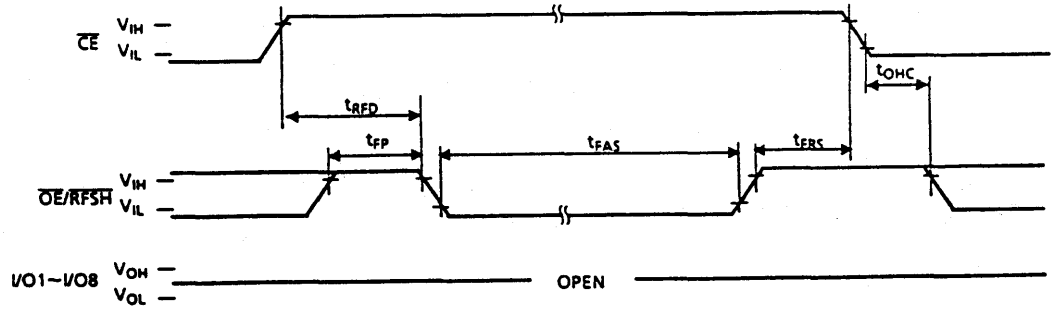
Note: A11 ~ A18 = V_{IH} or V_{IL} : H or L

Auto Refresh



Note: R/W, A0 ~ A18 = V_{IH} or V_{IL}

Self Refresh



Note: R/W, A0 ~ A18 = V_{IH} or V_{IL}