

TENTATIVE**TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS****16,777,216-WORD × 4-BIT EDO (HYPER PAGE) DYNAMIC RAM****DESCRIPTION**

The TC5164(5)405BJ/BFT/BJS/BFTS is an EDO (hyper page) dynamic RAM organized as 16,777,216 words by 4 bits. TC5164(5)405BJ/BFT/BJS/BFTS utilizes TOSHIBA's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC5164(5)405BJ/BFT/BJS/BFTS to be packaged in either a 32-pin plastic SOJ or a 32-pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. Other features include a single power supply of $3.3V \pm 0.3V$ tolerance and direct interfacing with high performance logic families such as LVTTL.

FEATURES

- 16,777,216-word by 4-bit organization
- Fast access time and cycle time
- Single power supply of $3.3V \pm 0.3V$ with a built-in V_{BB} generator
- Low power dissipation (max)
 - Operating : 306mW (TC5164405BJ/BFT/BJS/BFTS-40)
 - 252mW (TC5164405BJ/BFT/BJS/BFTS-50)
 - 432mW (TC5165405BJ/BFT/BJS/BFTS-40)
 - 360mW (TC5165405BJ/BFT/BJS/BFTS-50)
 - Standby : 1.8mW
 - 0.72mW (S-version)
- Outputs unlatched at cycle end, allowing two-dimensional chip selection
- Read-Modify-Write and EDO (Hyper Page mode) capability
- All inputs and outputs LVTTL-compatible
- Packages
 - BJ/BJS : SOJ32-P-400-1.27B, 1.27 grams
 - BFT/BFTS : TSOP II 32-P-400-1.27B, 0.50grams

		TC5164(5)405 BJ/BFT/BJS/BFTS	
		-40	-50
t_{RAC}	$\overline{RAS}$ Access Time	40ns	50ns
t_{AA}	Column Address Access Time	20ns	25ns
t_{CAC}	$\overline{CAS}$ Access Time	11ns	13ns
t_{RC}	Cycle Time	69ns	84ns
t_{HPC}	Hyper Page Mode Cycle Time	16ns	20ns

Part No.	Row Add.	Col. Add.	Refresh	Refresh Cycle
TC5164405BJ/BFT	A0 to A12	A0 to A10	$\overline{RAS}$ -Only refresh	8192/64 ms
			$\overline{CAS}$ -before- $\overline{RAS}$ refresh, Hidden refresh	4096/64 ms
TC5165405BJ/BFT	A0 to A11	A0 to A11	$\overline{RAS}$ -Only refresh, $\overline{CAS}$ -before- $\overline{RAS}$ refresh, Hidden refresh	4096/64 ms
TC5164405BJS/BFTS (S-version)	A0 to A12	A0 to A10	$\overline{RAS}$ -Only refresh	8192/128 ms
			$\overline{CAS}$ -before- $\overline{RAS}$ refresh, Hidden refresh, Self-refresh	4096/128 ms
TC5165405BJS/BFTS (S-version)	A0 to A11	A0 to A11	$\overline{RAS}$ -Only refresh, $\overline{CAS}$ -before- $\overline{RAS}$ refresh, Hidden refresh, Self-refresh	4096/128 ms

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TC5164405BJ/BFT/BJS/BFTS**PIN ASSIGNMENT (TOP VIEW)****Plastic SOJ**

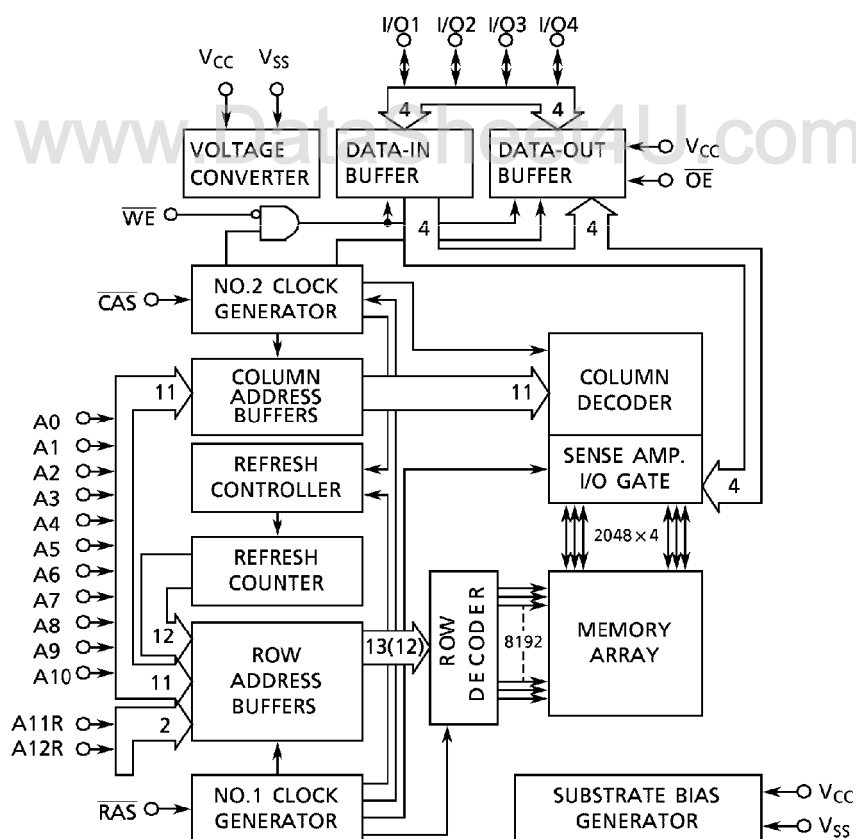
V _{CC}	1	32	V _{SS}
I/O1	2	31	I/O4
I/O2	3	30	I/O3
NC	4	29	NC
NC	5	28	NC
NC	6	27	NC
NC	7	26	CAS
WE	8	25	OE
RAS	9	24	A12R
A0	10	23	A11R
A1	11	22	A10
A2	12	21	A9
A3	13	20	A8
A4	14	19	A7
A5	15	18	A6
V _{CC}	16	17	V _{SS}

**Plastic TSOP
(Normal Bend Type)**

V _{CC}	1	32	V _{SS}
I/O1	2	31	I/O4
I/O2	3	30	I/O3
NC	4	29	NC
NC	5	28	NC
NC	6	27	NC
NC	7	26	CAS
WE	8	25	OE
RAS	9	24	A12R
A0	10	23	A11R
A1	11	22	A10
A2	12	21	A9
A3	13	20	A8
A4	14	19	A7
A5	15	18	A6
V _{CC}	16	17	V _{SS}

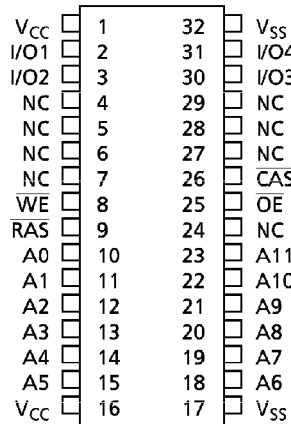
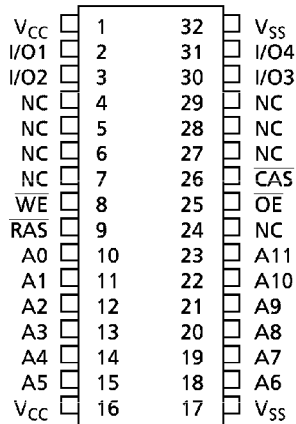
PIN NAMES

A0 to A12	Address Inputs
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
OE	Output Enable
I/O1 to I/O4	Data Input/Output
V _{CC}	Power (+ 3.3V)
V _{SS}	Ground
NC	No Connection

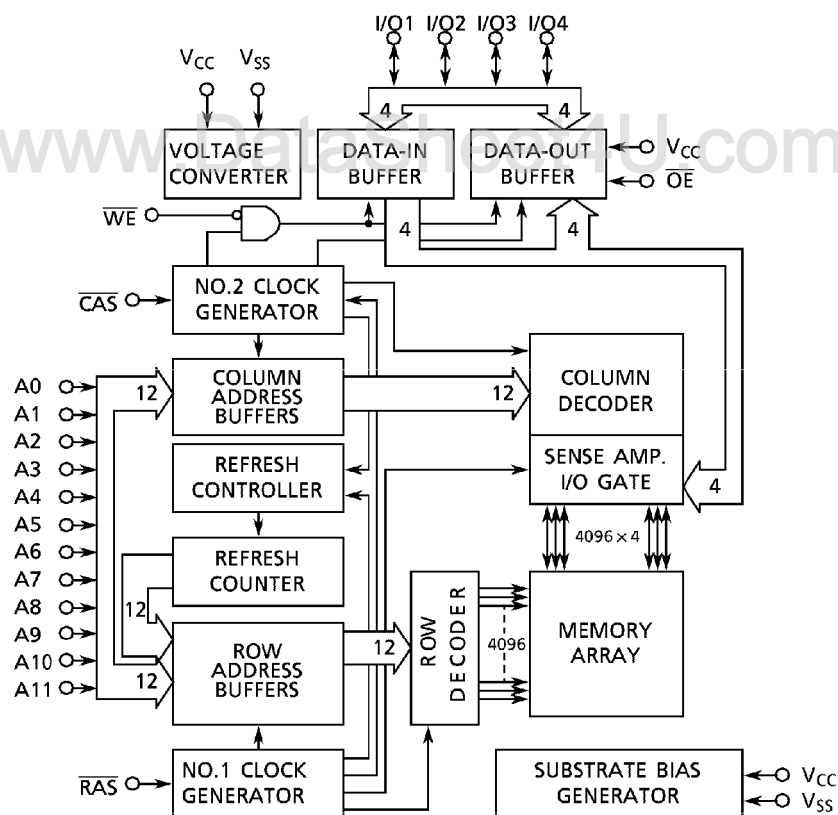
BLOCK DIAGRAM

TC5165405BJ/BFT/BJS/BFTS**PIN ASSIGNMENT (TOP VIEW)**

Plastic SOJ

Plastic TSOP
(Normal Bend Type)**PIN NAMES**

A0 to A11	Address Inputs
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
OE	Output Enable
I/O1 to I/O4	Data Input/Output
V _{CC}	Power (+ 3.3V)
V _{SS}	Ground
NC	No Connection

BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTES
Input Voltage	V_{IN}	- 0.3 to $V_{CC} + 0.3$	V	1
Output Voltage	V_{OUT}	- 0.3 to $V_{CC} + 0.3$	V	1
Power Supply Voltage	V_{CC}	- 0.3 to 4.6	V	1
Operating Temperature	T_{OPR}	0 to 70	°C	1
Storage Temperature	T_{STG}	- 55 to 150	°C	1
Soldering Temperature (10 s)	T_{SOLDER}	260	°C	1
Power Dissipation	P_D	1.0	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to 70°C)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	2
V_{IH}	Input High Voltage	2.0	–	$V_{CC} + 0.3^*$	V	2
V_{IL}	Input Low Voltage	- 0.3**	–	0.8	V	2

* $V_{CC} + 1.2V$ at pulse width $\leq 20ns$ (pulse width is measured at V_{CC})** - 1.2V at pulse width $\leq 20ns$ (pulse width is measured at V_{SS})**CAPACITANCE ($V_{CC} = 3.3V \pm 0.3V$, $f = 1$ MHz, $T_a = 0$ to 70°C)**

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (Address)	–	5	pF
C_{I2}	Input Capacitance (RAS, CAS, WE, OE)	–	7	pF
C_O	I/O Capacitance (I/O1 to I/O4)	–	7	pF

DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 0.3V$, $T_a = 0$ to 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC \text{ min}}$)	TC5164405BJ/BFT/BJS/BFTS-40	–	85	mA 3, 4, 5
		TC5164405BJ/BFT/BJS/BFTS-50	–	70	
		TC5165405BJ/BFT/BJS/BFTS-40	–	120	
		TC5165405BJ/BFT/BJS/BFTS-50	–	100	
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)	–	1	mA	
I_{CC3}	$\overline{RAS}$ -ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ -Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC \text{ min}}$)	TC5164405BJ/BFT/BJS/BFTS-40	–	85	mA 3, 5
		TC5164405BJ/BFT/BJS/BFTS-50	–	70	
		TC5165405BJ/BFT/BJS/BFTS-40	–	120	
		TC5165405BJ/BFT/BJS/BFTS-50	–	100	
I_{CC4}	HYPER PAGE MODE CURRENT Average Power Supply Current, Hyper Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address Cycling: $t_{HPC} = t_{HPC \text{ min}}$)	TC5164405BJ/BFT/BJS/BFTS-40	–	90	mA 3, 4, 5
		TC5164405BJ/BFT/BJS/BFTS-50	–	75	
		TC5165405BJ/BFT/BJS/BFTS-40	–	90	
		TC5165405BJ/BFT/BJS/BFTS-50	–	75	
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)	–	500	μA	
			200 (S-version)		
I_{CC6}	$\overline{CAS}$ -BEFORE- $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ -before- $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC \text{ min}}$)	TC5164405BJ/BFT/BJS/BFTS-40	–	120	mA 3, 5
		TC5164405BJ/BFT/BJS/BFTS-50	–	100	
		TC5165405BJ/BFT/BJS/BFTS-40	–	120	
		TC5165405BJ/BFT/BJS/BFTS-50	–	100	
I_{CC7}	BATTERY BACK-UP CURRENT Average Power Supply Current, Battery Back-up Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = \overline{CAS}$ -before- $\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$, $\overline{WE}$, Address = $V_{CC} - 0.2V$ or 0.2V, I/O1 to I/O4 = $V_{CC} - 0.2V$, 0.2V or Hi-Z: $t_{RC} = 31.2\mu\text{s}$ $t_{RAS} = t_{RAS \text{ min}}$ to 300ns)	–	500 (S-version)	μA	
I_{CCS}	SELF-REFRESH CURRENT Average Power Supply Current, Self-Refresh Mode ($\overline{RAS} = \overline{CAS} = V_{IL}$, $\overline{OE}$, $\overline{WE}$, Address = $V_{CC} - 0.2V$ or 0.2V, I/O1 to I/O4 = $V_{CC} - 0.2V$, 0.2V or Hi-Z)	–	400 (S-version)	μA	
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, Any Input ($0V \leq V_{IN} \leq V_{CC}$, All Other Pins Not under Test = 0V)	– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} Is Disabled, $0V \leq V_{OUT} \leq V_{CC}$)	– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output H Level Voltage ($I_{OUT} = -2\text{mA}$)	2.4	–	V	
V_{OL}	OUTPUT LEVEL Output L Level Voltage ($I_{OUT} = 2\text{mA}$)	–	0.4	V	

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS(V_{CC} = 3.3V ± 0.3V, Ta = 0 to 70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC5164(5)405BJ/BFT/BJ5/BFTS				UNIT	NOTES
		-40		-50			
		MIN	MAX	MIN	MAX		
t _{RC}	Random Read-or-Write Cycle Time	69	–	84	–	ns	
t _{RMW}	Read-Modify-Write Cycle Time	92	–	111	–	ns	
t _{RAC}	Access Time from RAS	–	40	–	50	ns	9, 14, 15
t _{CAC}	Access Time from CAS	–	11	–	13	ns	9, 14
t _{AA}	Access Time from Column Address	–	20	–	25	ns	9, 15
t _{CPA}	Access Time from $\overline{\text{CAS}}$ Precharge	–	22	–	28	ns	9
t _{CLZ}	CAS to Output in Low-Z	0	–	0	–	ns	
t _{OFF}	Output Buffer Turn-off Delay	0	11	0	13	ns	10, 16
t _T	Transition Time (Rise and Fall)	1	50	1	50	ns	8
t _{RP}	RAS Precharge Time	25	–	30	–	ns	
t _{RAS}	RAS Pulse Width	40	10,000	50	10,000	ns	
t _{RASP}	RAS Pulse Width (Hyper Page Mode)	40	100,000	50	100,000	ns	
t _{RSH}	RAS Hold Time	6	–	8	–	ns	
t _{RHCP}	RAS Hold Time from $\overline{\text{CAS}}$ Precharge (Hyper Page Mode)	22	–	28	–	ns	
t _{CSH}	$\overline{\text{CAS}}$ Hold Time	30	–	35	–	ns	
t _{CAS}	$\overline{\text{CAS}}$ Pulse Width	6	10,000	8	10,000	ns	
t _{RCD}	RAS-to-CAS Delay Time	10	29	12	37	ns	14
t _{RAD}	RAS-to-Column-Address Delay Time	8	20	10	25	ns	15
t _{CRP}	CAS-to-RAS Precharge Time	5	–	5	–	ns	
t _{CP}	$\overline{\text{CAS}}$ Precharge Time	6	–	8	–	ns	
t _{ASR}	Row Address Set up Time	0	–	0	–	ns	
t _{RAH}	Row Address Hold Time	6	–	8	–	ns	
t _{ASC}	Column Address Set up Time	0	–	0	–	ns	
t _{CAH}	Column Address Hold Time	6	–	8	–	ns	
t _{RAL}	Column-Address-to-RAS Lead Time	20	–	25	–	ns	
t _{RCS}	Read Command Set up Time	0	–	0	–	ns	
t _{RCH}	Read Command Hold Time	0	–	0	–	ns	11
t _{RRH}	Read Command Hold Time Referenced to RAS	0	–	0	–	ns	11
t _{WCH}	Write Command Hold Time	6	–	8	–	ns	
t _{WP}	Write Command Pulse Width	6	–	8	–	ns	
t _{RWL}	Write-Command-to-RAS Lead Time	6	–	8	–	ns	
t _{CWL}	Write-Command-to-CAS Lead Time	6	–	8	–	ns	
t _{DS}	Data Set up Time	0	–	0	–	ns	12
t _{DH}	Data Hold Time	6	–	8	–	ns	12

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(Continued)

SYMBOL	PARAMETER	TC5164(5)405BJ/BFT/BJ5/BFTS				UNIT	NOTES
		-40		-50			
		MIN	MAX	MIN	MAX		
t _{REF}	Refresh Period	–	64	–	64	ms	
		–	128 (S-version)	–	128 (S-version)		
t _{WCS}	Write Command Set up Time	0	–	0	–	ns	13
t _{CWD}	$\overline{\text{CAS}}$ -to- $\overline{\text{WE}}$ Delay Time	26	–	30	–	ns	13
t _{RWD}	$\overline{\text{RAS}}$ -to- $\overline{\text{WE}}$ Delay Time	55	–	67	–	ns	13
t _{AWD}	Column-Address-to- $\overline{\text{WE}}$ Delay Time	35	–	42	–	ns	13
t _{CPWD}	$\overline{\text{CAS}}$ -Precharge-to- $\overline{\text{WE}}$ Delay Time	37	–	45	–	ns	13
t _{CSR}	CAS Set up Time (CAS-before-RAS Cycle)	5	–	5	–	ns	
t _{CHR}	$\overline{\text{CAS}}$ Hold Time (CAS-before-RAS Cycle)	6	–	8	–	ns	
t _{RPC}	$\overline{\text{RAS}}$ -to- $\overline{\text{CAS}}$ Precharge Time	5	–	5	–	ns	
t _{ROH}	$\overline{\text{RAS}}$ Hold Time Referenced to $\overline{\text{OE}}$	6	–	8	–	ns	
t _{OEA}	$\overline{\text{OE}}$ Access Time	–	11	–	13	ns	9
t _{OED}	$\overline{\text{OE}}$ -to-Data Delay	11	–	13	–	ns	
t _{OLZ}	$\overline{\text{OE}}$ to Output in Low-Z	0	–	0	–	ns	
t _{OEZ}	Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$	0	11	0	13	ns	10
t _{OEH}	$\overline{\text{OE}}$ Command Hold Time	6	–	8	–	ns	
t _{ODS}	Output Disable Set up Time	0	–	0	–	ns	
t _{WRP}	$\overline{\text{WE}}$ -to-RAS Precharge Time (CAS-before-RAS Cycle)	5	–	5	–	ns	
t _{WRH}	$\overline{\text{WE}}$ -to-RAS Hold Time (CAS-before-RAS Cycle)	6	–	8	–	ns	
t _{RNCD}	RAS-to-Next-CAS Delay Time (Hyper Page Mode)	40	–	50	–	ns	
t _{HPC}	Hyper Page Mode Cycle Time	16	–	20	–	ns	
t _{HPRWC}	Hyper Page Mode Read-Modify-Write Cycle Time	47	–	57	–	ns	
t _{COH}	Output Data Hold Time	5	–	5	–	ns	
t _{REZ}	Output Buffer Turn-off Delay from RAS	0	11	0	13	ns	10, 16
t _{WEZ}	Output Buffer Turn-off Delay from $\overline{\text{WE}}$	0	11	0	13	ns	10
t _{WED}	$\overline{\text{WE}}$ -to-Data Delay	11	–	13	–	ns	
t _{OE}	$\overline{\text{OE}}$ Pulse Width	11	–	13	–	ns	
t _{OEP}	$\overline{\text{OE}}$ Precharge Time	6	–	8	–	ns	
t _{CPO}	CAS-to- $\overline{\text{OE}}$ Precharge Time	5	–	5	–	ns	
t _{OCH}	$\overline{\text{CAS}}$ Hold Time Referenced to $\overline{\text{OE}}$	6	–	8	–	ns	
t _{RASS}	RAS Pulse Width (CAS-before-RAS Self-Refresh) (S-version only)	100	–	100	–	μs	
t _{RPS}	$\overline{\text{RAS}}$ Precharge Time (CAS-before-RAS Self-Refresh) (S-version only)	69	–	84	–	ns	
t _{CHS}	$\overline{\text{CAS}}$ Hold Time (CAS-before-RAS Self-Refresh) (S-version only)	-50	–	-50	–	ns	

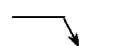
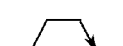
NOTES:

1. Conditions outside the limits listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS} .
3. I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} depend on the cycle rate.
4. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. The address can be changed once at most while $\overline{RAS}=V_{IL}$. In the case of I_{CC4} , it can be changed once at most during a Hyper Page Mode cycle (t_{HPC}).
6. An initial pause of $200\mu s$ is required after power-up followed by a minimum of eight $\overline{RAS}$ -Only refresh cycles before proper device operation is achieved. When using the internal refresh counter, a minimum of eight $\overline{CAS}$ -before- $\overline{RAS}$ refresh cycles instead of eight $\overline{RAS}$ -Only refresh cycles is required.
7. AC measurements assume $t_T=2ns$.
8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Also, transition times are measured between the V_{IH} and V_{IL} levels.
9. This is measured with a load equivalent to $100pF$ at $V_{OH} = 2.0V$ ($I_{OUT} = -2mA$), $V_{OL} = 0.8V$ ($I_{OUT} = 2mA$).
10. t_{OFF} (max), t_{OEZ} (max), t_{REZ} (max) and t_{WEZ} (max) define the time at which the output goes open circuit and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a Read cycle.
12. These parameters are referenced to the leading edge of $\overline{CAS}$ in Early Write cycles and to the leading edge of $\overline{WE}$ in Read-Modify-Write cycles.
13. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$, the cycle is an Early Write cycle and the Data-out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}(\min)$, $t_{CWD} \geq t_{CWD}(\min)$, $t_{AWD} \geq t_{AWD}(\min)$ and $t_{CPWD} \geq t_{CPWD}(\min)$ (Hyper Page mode), the cycle is a Read-Modify-Write cycle and the data output will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the data output (at access time) is indeterminate.
14. Operation within the $t_{RCD}(\max)$ limit ensures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then the access time is determined by t_{CAC} .
15. Operation within the $t_{RAD}(\max)$ limit ensures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then the access time is determined by t_{AA} .
16. If $\overline{RAS}$ goes high before $\overline{CAS}$ goes high, the output goes open circuit when $\overline{CAS}$ goes high (t_{OFF}). If $\overline{CAS}$ goes high before $\overline{RAS}$ goes high, the output goes open circuit when $\overline{RAS}$ goes high (t_{REZ}).

DATA-OUT HI-Z CONTROL LOGIC

$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Timing Specification
H		L	H	t_{OFF}
	H	L	H	t_{REZ}
L	L		H	t_{OEZ}
L	H	L		t_{WEZ}

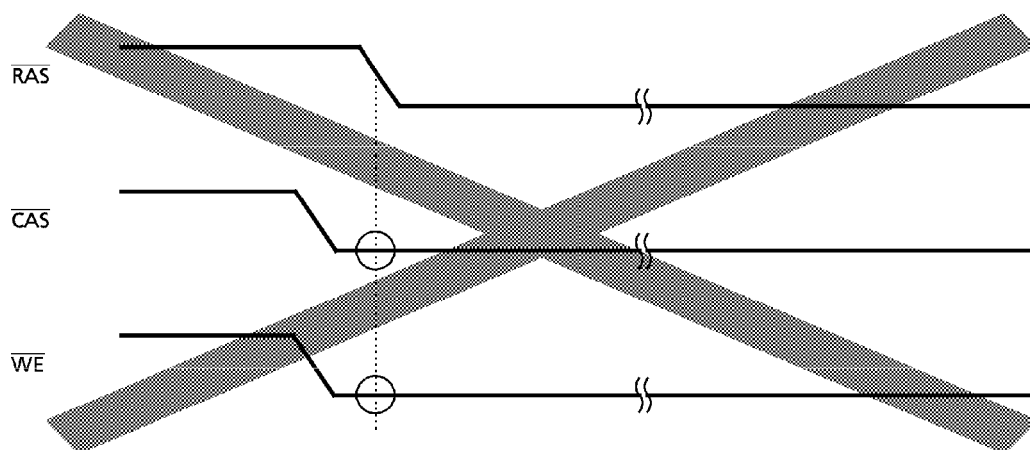
DATA-OUT LO-Z CONTROL LOGIC

$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Timing Specification
L		L	H	t_{CLZ}
L	L		H	t_{OLZ}
L	L		H	t_{OLZ}

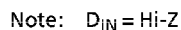
CAUTION

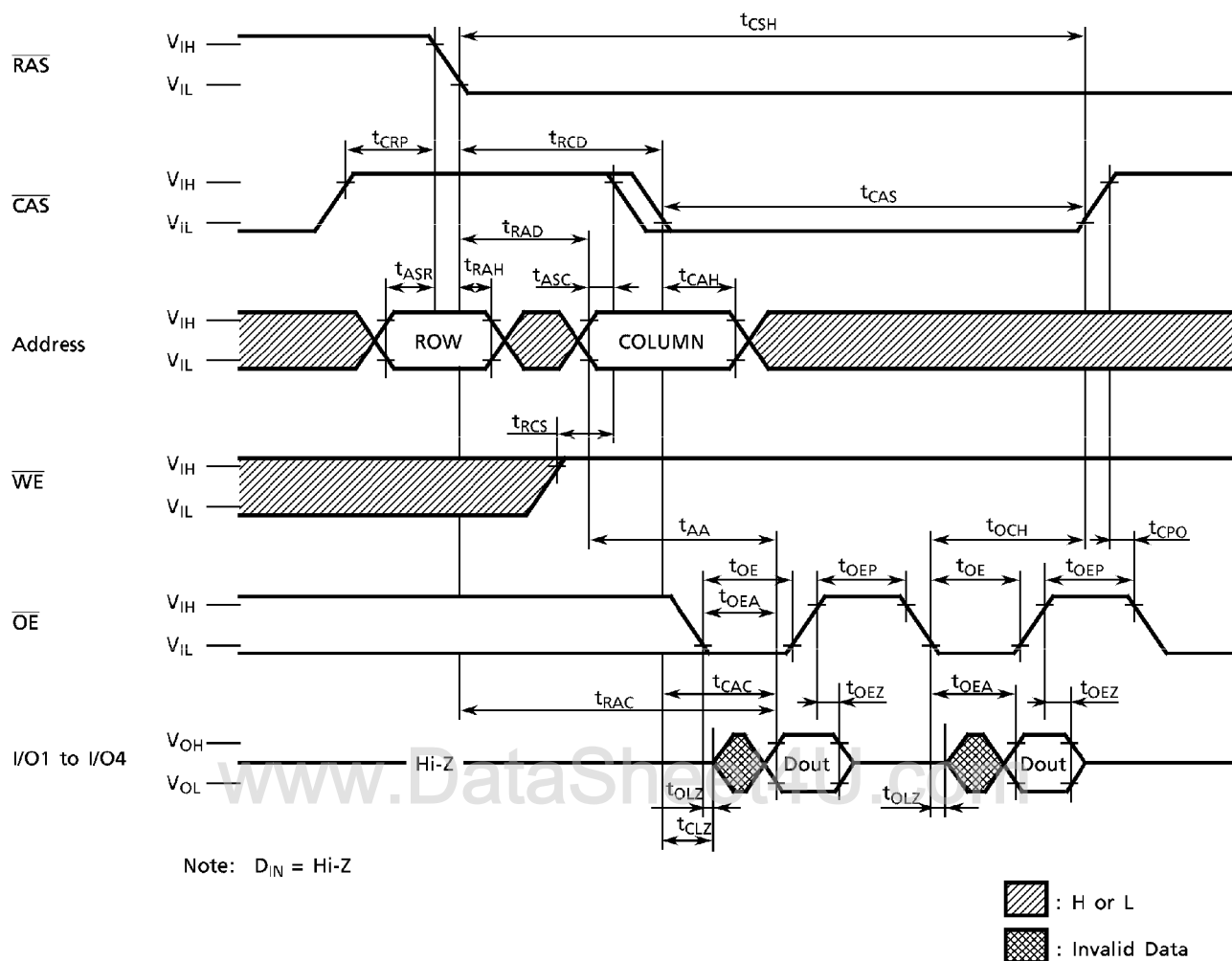
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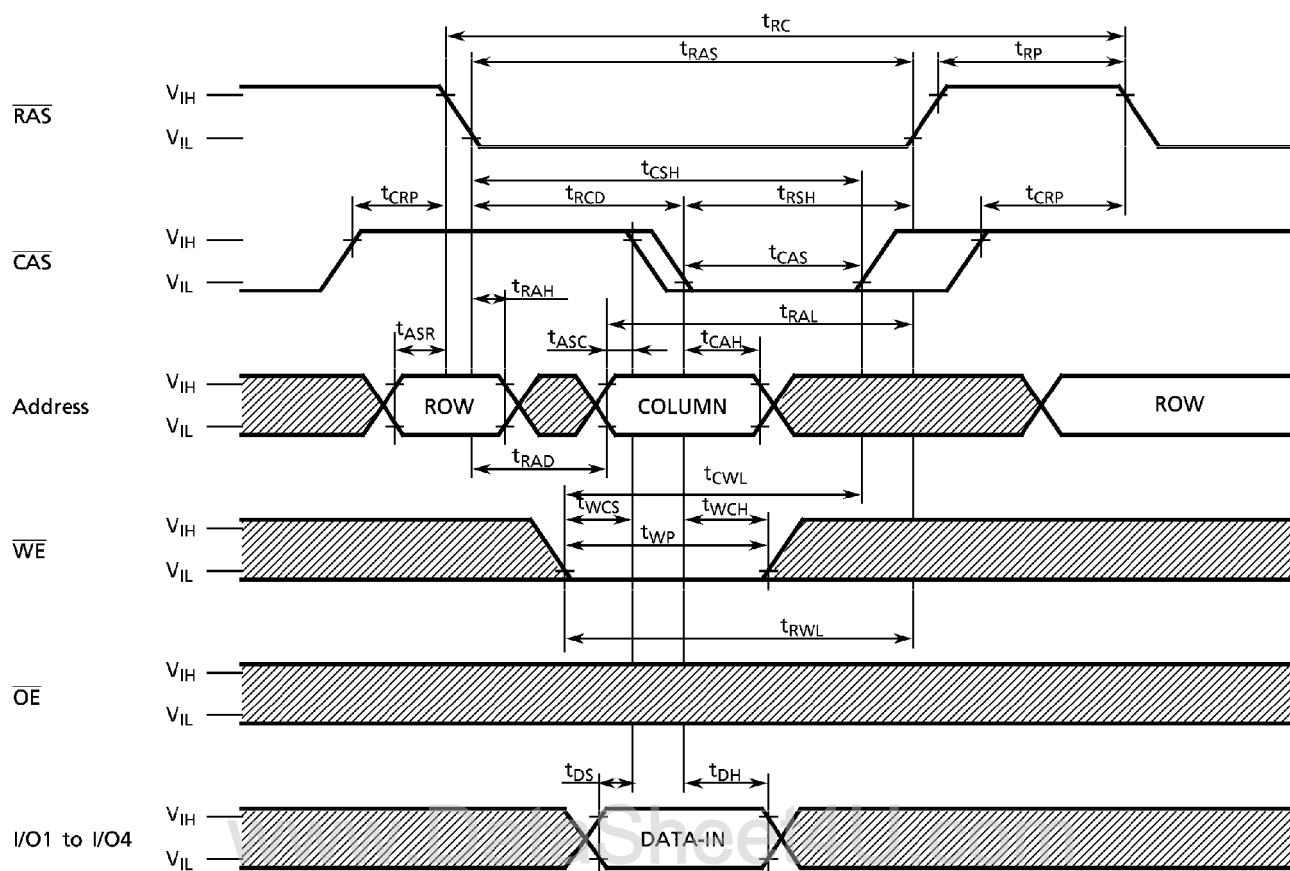
The WCBR ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$) timing shown below is not allowed during normal operation, such as during Read, Write and Refresh operations. When WCBR is input, a malfunction may occur due to the change in internal circuit operation status.

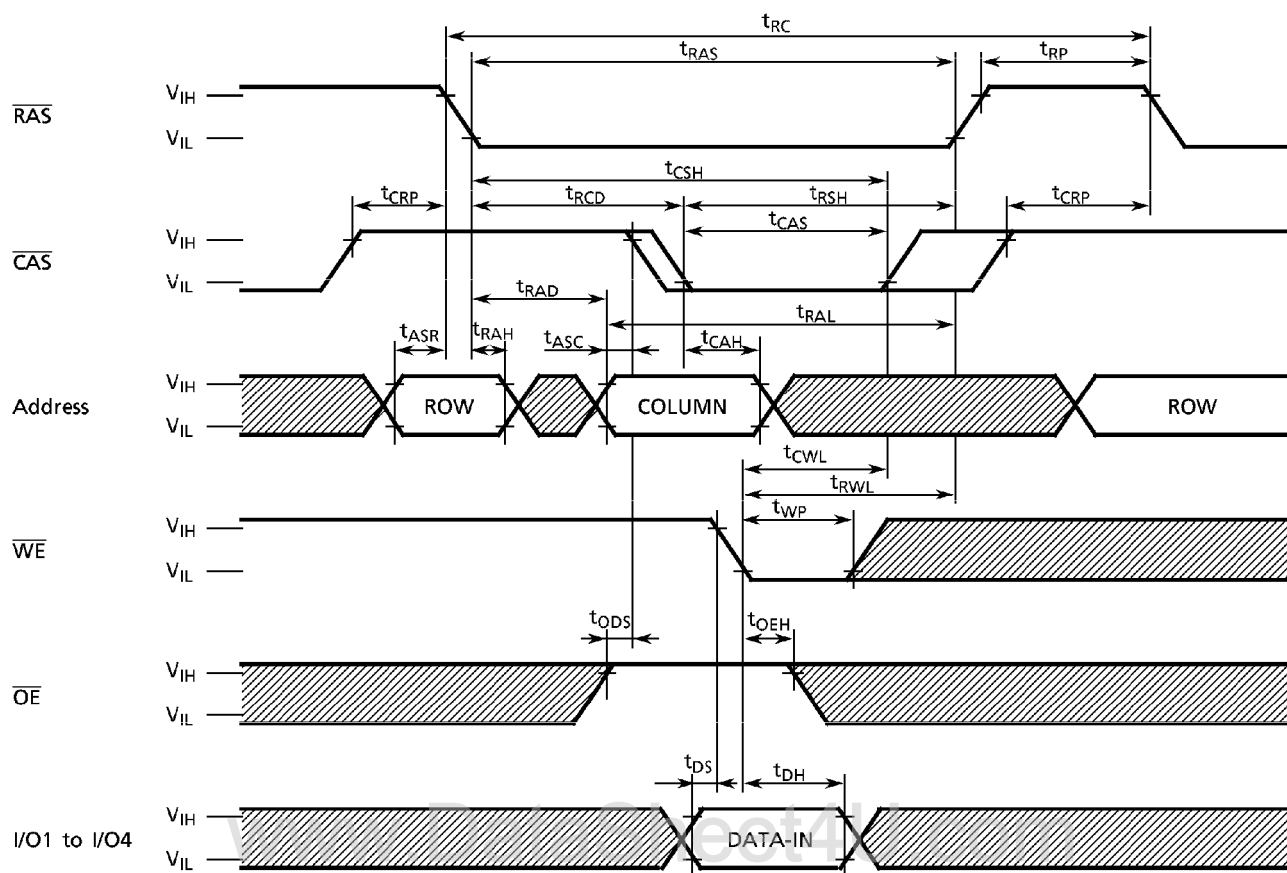
**WCBR timing**

READ CYCLE



OE-CONTROLLED READ CYCLE

WRITE CYCLE (EARLY WRITE)

OE-CONTROLLED WRITE CYCLE

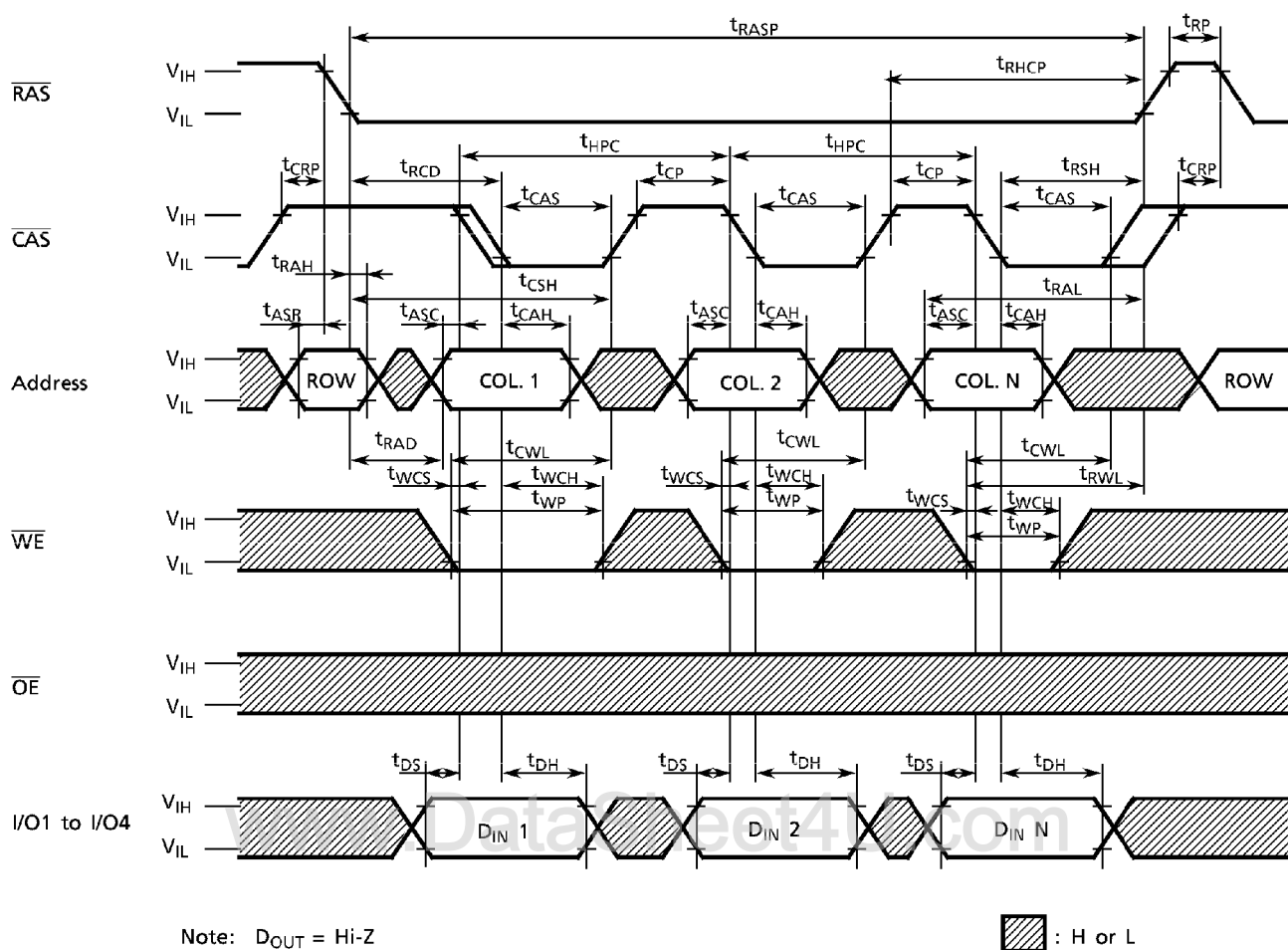
The diagram illustrates the timing relationships for a memory device. The signals shown are $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address, $\overline{\text{WE}}$, $\overline{\text{OE}}$, and I/O data (I/O1 to I/O4). The timing parameters are defined as follows:

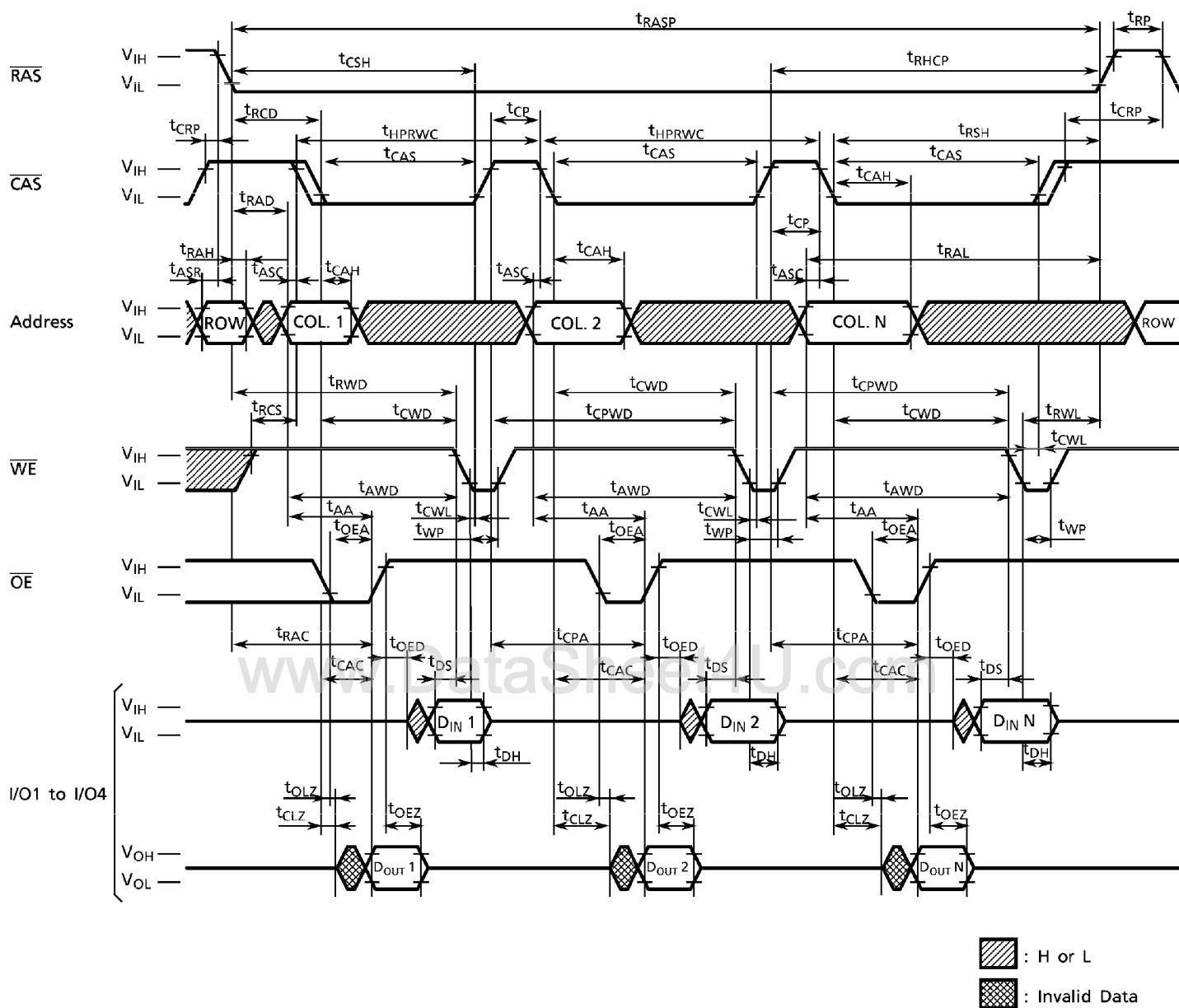
- t_{RAS} : RAS pulse width
- t_{RCD} : RAS to CAS delay
- t_{CAS} : CAS pulse width
- t_{RSH} : RAS to SH (Sense Amplifier) delay
- t_{CRP} : RAS to CAS precharge delay
- t_{ASR} : Address to RAS delay
- t_{RAH} : Address to RAS hold delay
- t_{ASC} : Address to CAS delay
- t_{CAH} : Address to CAS hold delay
- t_{RAD} : RAS to Address delay
- t_{RCS} : RAS to CAS delay
- t_{AWD} : Address to WE delay
- t_{CWD} : CAS to WE delay
- t_{CWL} : CAS to WE delay
- t_{RWL} : RAS to WE delay
- t_{VVP} : WE to VVP delay
- t_{RWD} : RAS to WE delay
- t_{AA} : Address to WE delay
- t_{OA} : OE to WE delay
- t_{RAC} : RAS to OE delay
- t_{CAC} : CAS to OE delay
- t_{OLZ} : OE to OLZ delay
- t_{CLZ} : OE to CLZ delay
- t_{OED} : OE to OE delay
- t_{OEZ} : OE to OEZ delay
- t_{PS} : OE to PS delay
- t_{DH} : OE to DH delay

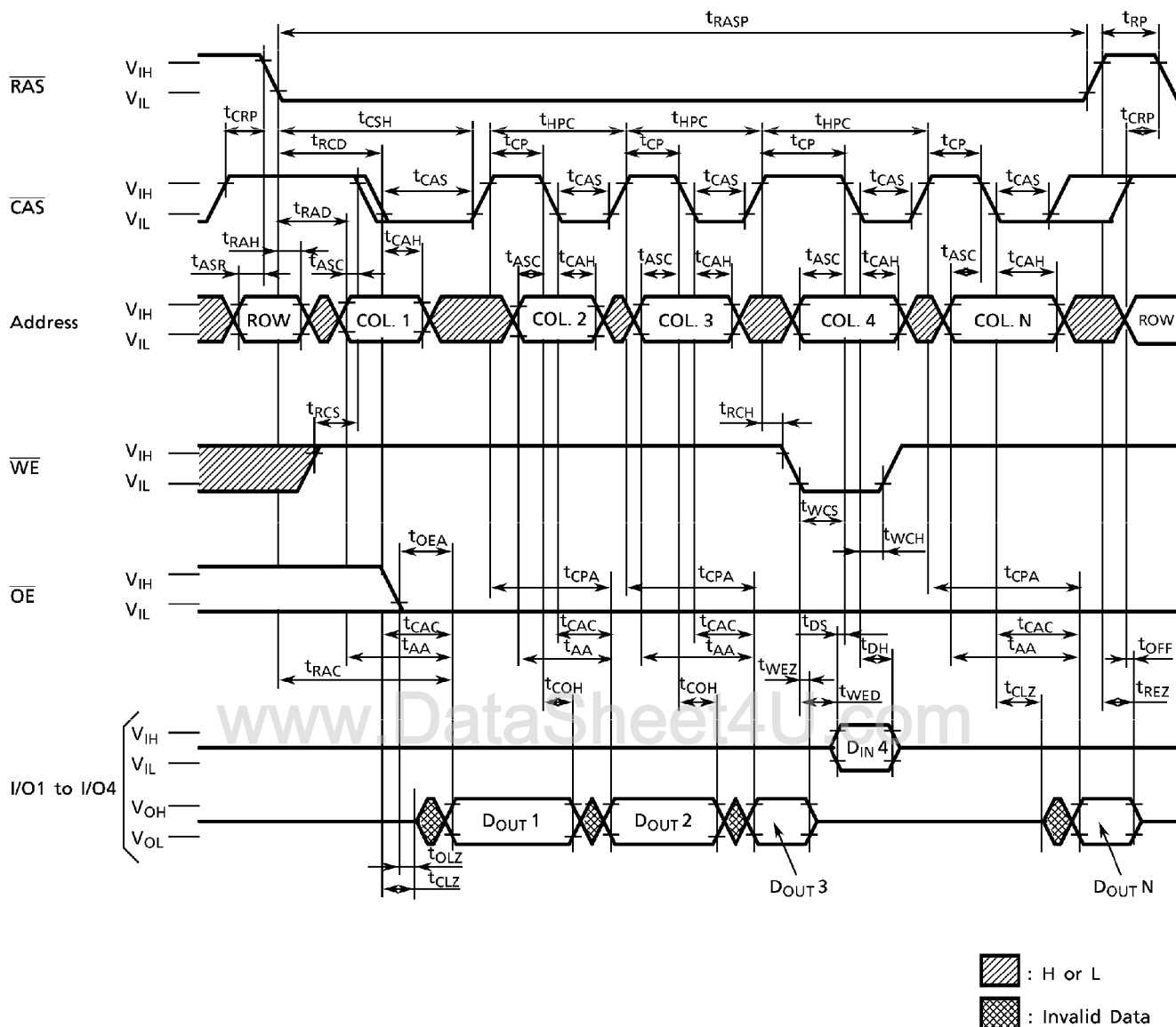
The diagram also shows the data bus (D_{IN} and D_{OUT}) and the output enable signal (OE) during the read cycle. The data bus is shown in a Hi-Z state during the precharge phase. The output enable signal (OE) is shown in a Hi-Z state during the precharge phase.

 : H or L
 : Invalid Data

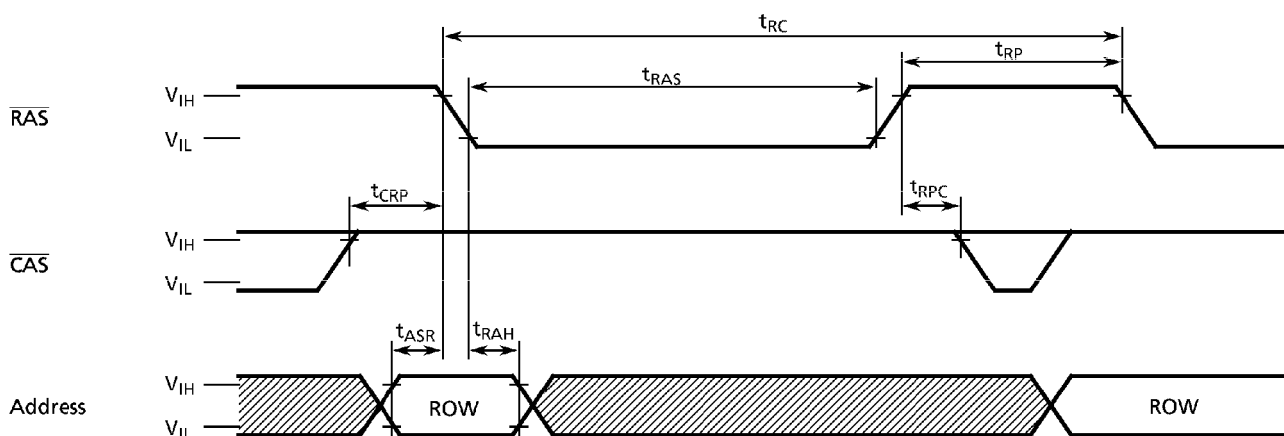
HYPER PAGE MODE WRITE CYCLE (EARLY WRITE)



HYPER PAGE MODE READ-MODIFY-WRITE CYCLE

HYPER PAGE MODE READ-WRITE MIXED CYCLE

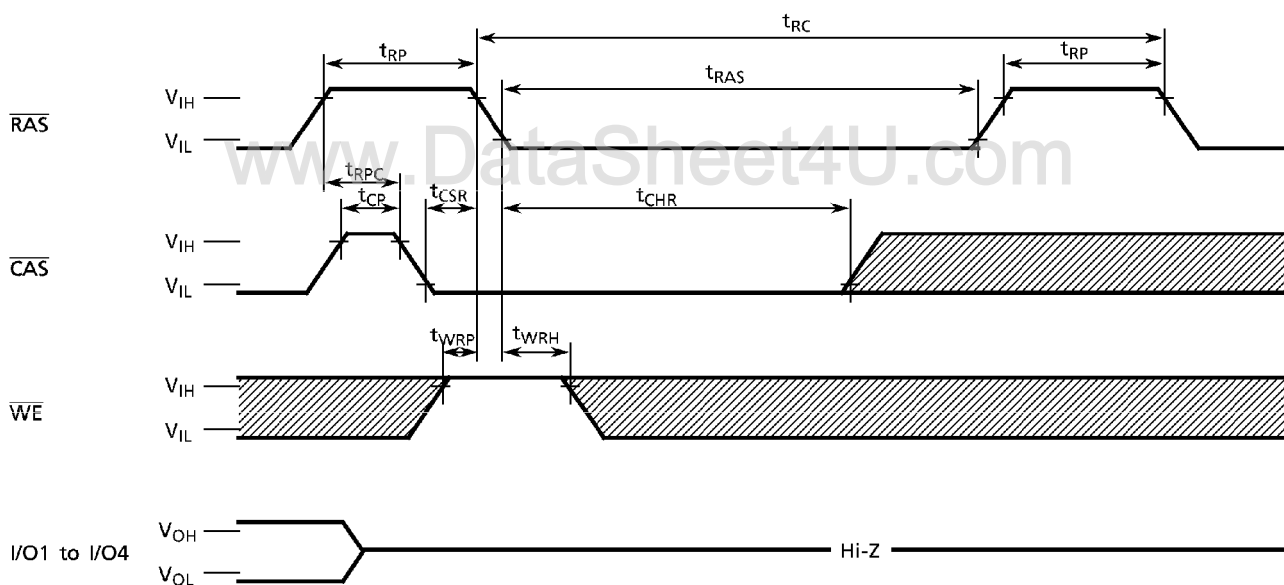
RAS-ONLY REFRESH CYCLE



Note: $\overline{\text{WE}}$, $\overline{\text{OE}}$ and $D_{\text{IN}} = \text{H or L}$

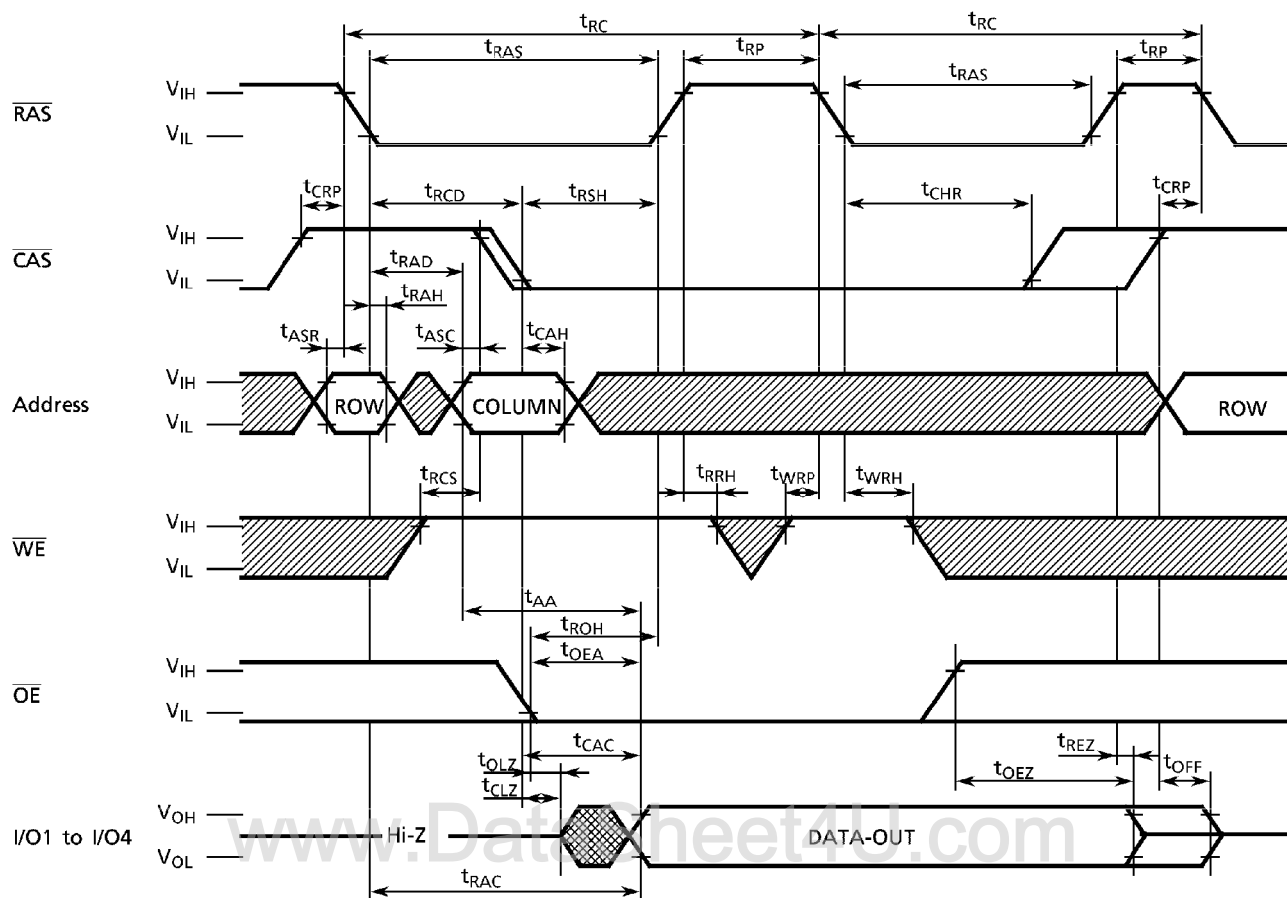
▨ : H or L

CAS-BEFORE-RAS REFRESH CYCLE

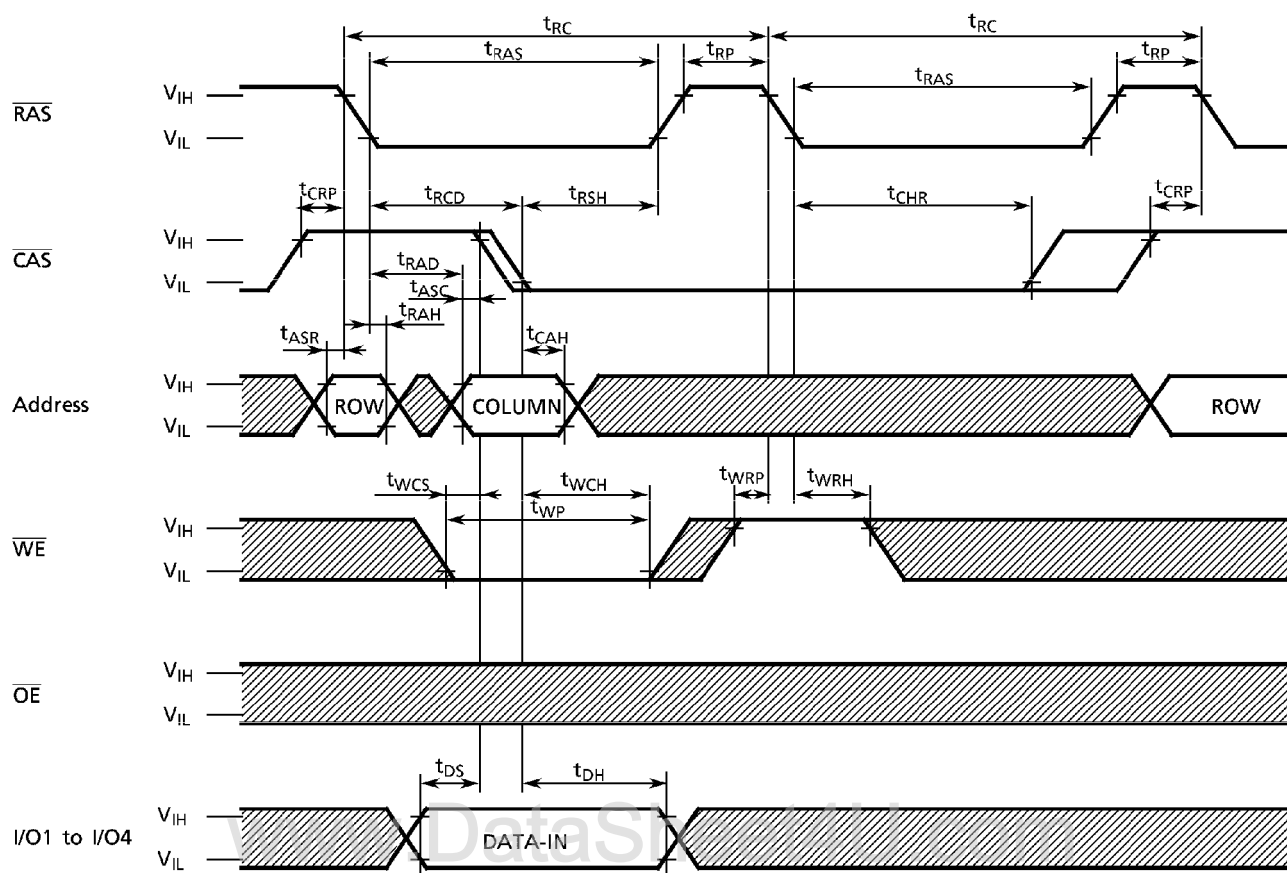


Note: D_{IN} , $\overline{\text{OE}}$ and Address = H or L

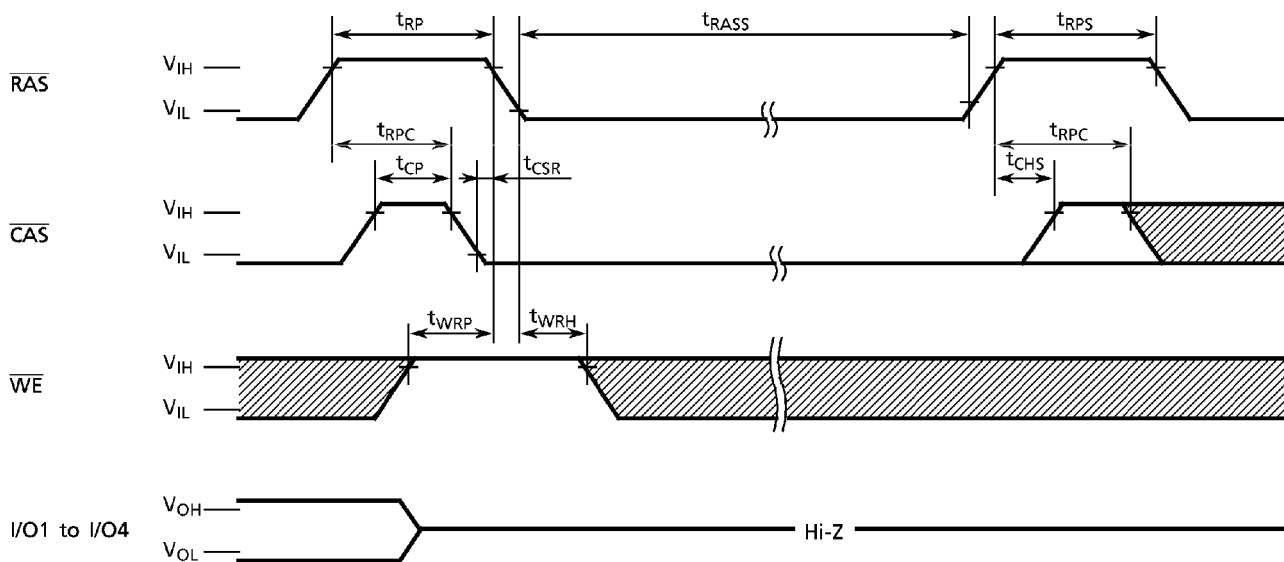
▨ : H or L

HIDDEN REFRESH CYCLE (READ)Note: D_{IN} = Hi-Z

 : H or L
 : Invalid Data

HIDDEN REFRESH CYCLE (WRITE)Note: D_{OUT} = Hi-Z

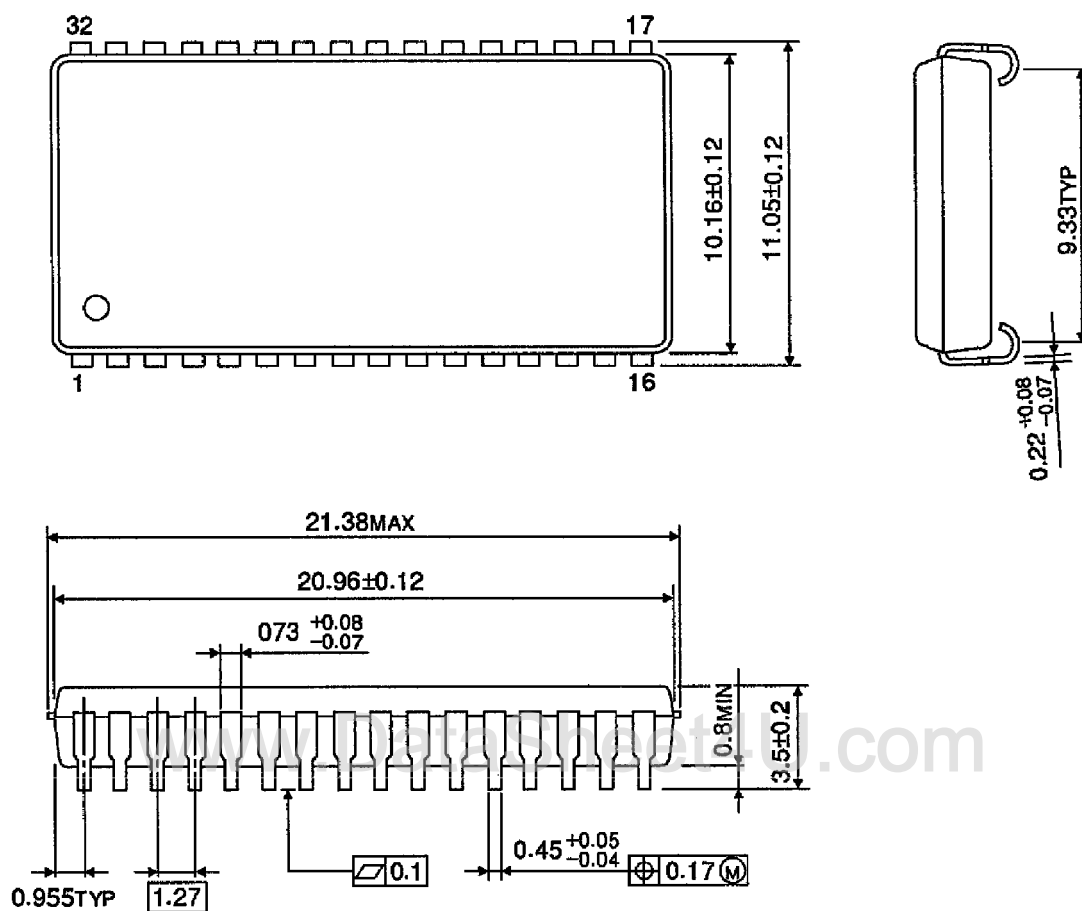
: H or L

CAS-BEFORE-RAS SELF-REFRESH CYCLE (S-version only)Note: D_{IN} , $\overline{\text{OE}}$ and Address = H or L
 : H or L

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Unit: mm



TOSHIBA**TC5164(5)405BJ/BFT/BJS/BFTS-40,-50****PACKAGE DIMENSIONS (TSOPII 32 – P – 400 – 1.27B)**

Unit: mm

