TOSHIBA

TC514800AJ/AZ/AFT-70/80

524,288 WORD X 8 BIT DYNAMIC RAM

DESCRIPTION

The TC514800AJ/AZ/AFT is the new generation dynamic RAM organized 524,288 word by 8 bit. The TC514800AJ/AZ/AFT utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514800AJ/AZ/AFT to be packaged in a standard 28 pin plastic SOJ, 28 pin plastic ZIP and 28 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL,

FEATURES

- 524,288 word by 8 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10% with a built-ion V_{BB} generator
- Low Power
  578mW MAX .Operating
  (TC514800AJ/AZ/AFT-70)
  495mW Max. Operating
  TC514800AJ/AZ/AFT-80
  5.5mW Max. Standby
- Outputs unlatched at cycle end allows two-di-mensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/16ms
- Package
  TC514800AJ :SOJ28-P-400
  TC514800AZ :ZIP28-P-400
  TC514800AFT :TSOP28-P-400

KEY PARAMETERS

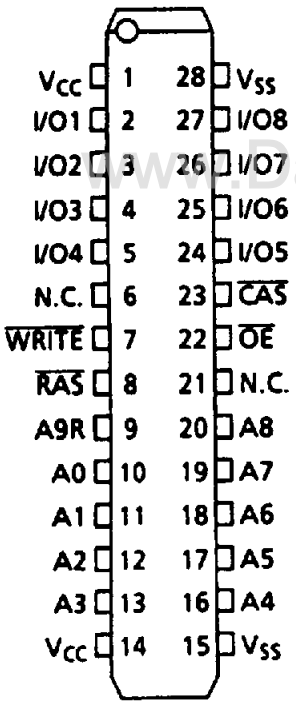
ITEM		TC514800AJ/AZ/AFT	
		-70	-80
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns
t_{AA}	Column Address Access Time	35ns	40ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns
t_{RC}	Cycle Time	130ns	150ns
t_{PC}	Fast Page Mode Cycle Time	45ns	50ns

PIN NAME

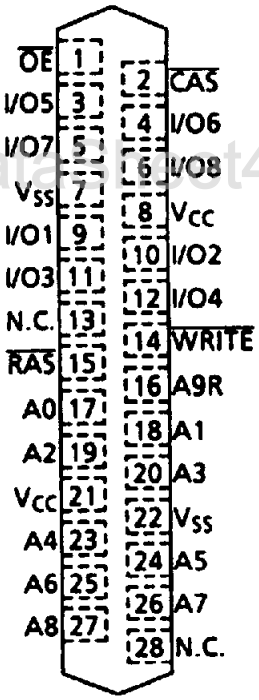
A0~A8 A9R	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O8	Data Input/Output
V_{CC}	Power (+ 5V)
V_{SS}	Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)

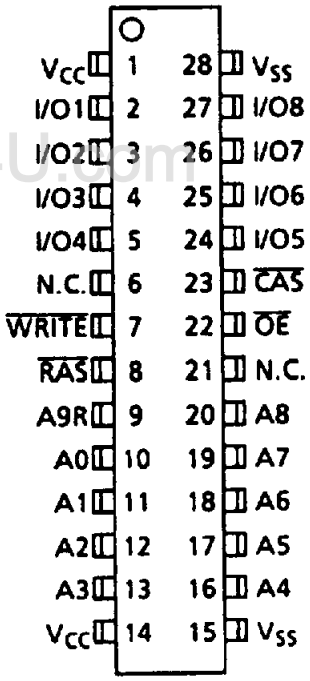
Plastic SOJ



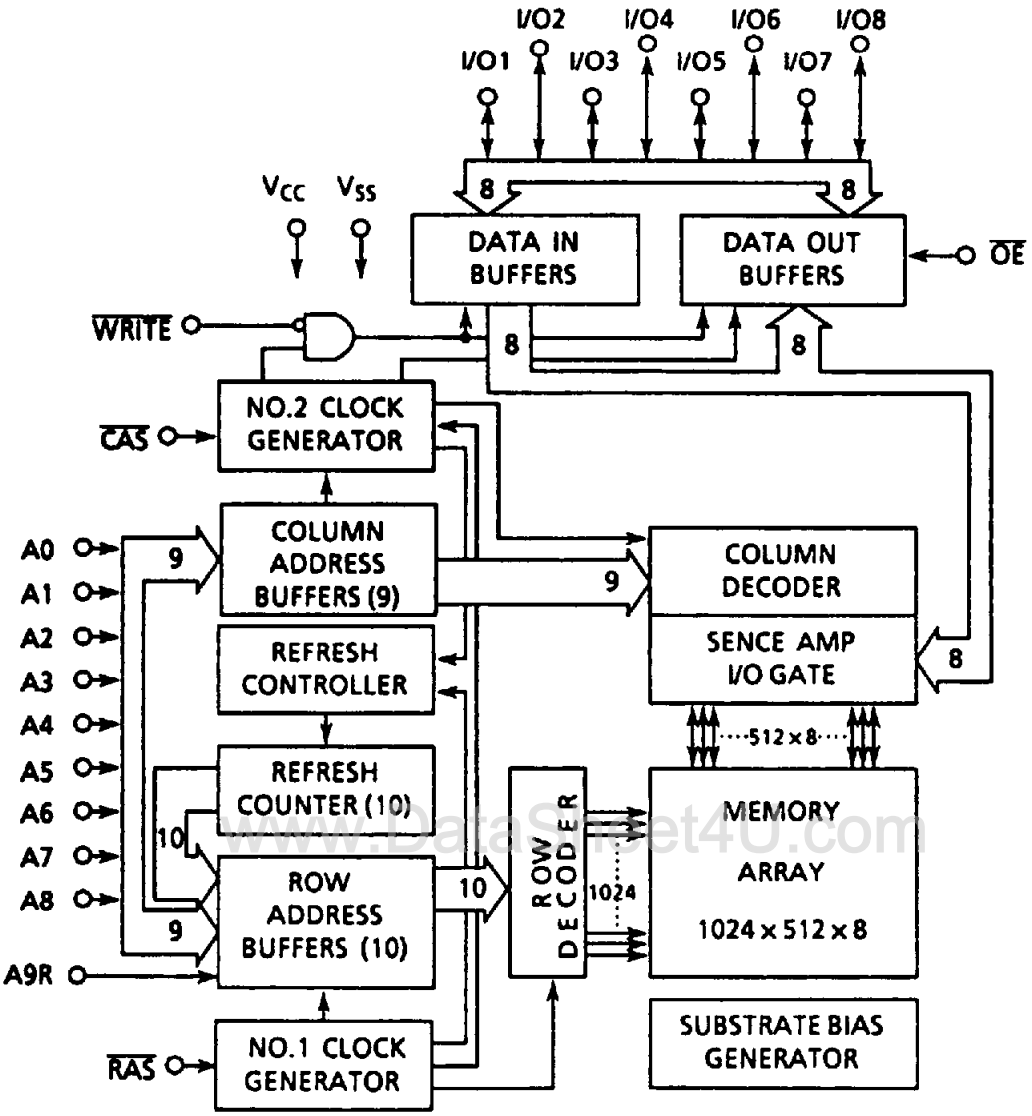
Plastic ZIP



Plastic TSOP
(Normal Bend Type)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	— 1~7	V	1
Output Voltage	V_{OUT}	— 1~7	V	1
Power Supply Voltage	V_{CC}	— 1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6..5	V	2
V_{IL}	Input Low Voltage (A0~A8,A9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	-1.0*1	-	0.8	V	2
V_{IL}	Input Low Voltage ($\overline{I/O}$~$\overline{I/O9}$)	-0.5*2	-	0.8	V	2

*1 -2.5V at pulse width ≤ 20ns
*2 -2.0V at pulse width ≤ 20ns

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC514800AJ/AZ/AFT-70	-	105	mA	3,4 5
		TC514800AJ/AZ/AFT-80	-	90		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514800AJ/AZ/AFT-70	-	105	mA	3,5
		TC514800AJ/AZ/AFT-80	-	90		
			-			
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$,Address Cycling:t_{PC}=t_{PC}MIN.)	TC514800AJ/AZ/AFT-70	-	75	mA	3,4 5
		TC514800AJ/AZ/AFT-80	-	65		
			-			
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$,Cycling: t_{RC}=t_{PC} MIN.)	TC514800AJ/AZ/AFT-70	-	105	mA	3
		TC514800AJ/AZ/AFT-80	-	90		
			-			
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤5.5V)		-10	10	μA	
V_{OH}	OUTPUT CURRENT Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT CURRENT Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	TC514800AJ/AZ/AFT				UNIT	NOTES
		-70		-80			
		MIN	MAX.	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	ns	
t_{RMW}	Read-Modify-Write Cycle	185	-	205	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	50	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	-	105	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	35	-	40	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	45	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Presharge Time	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100,000	80	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	-	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5		ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	ns	
t_{AR}	Column Address Hold Time	55	-	60	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	35	-	40	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	11
t_{WCH}	Write Command Hold TIme	15	-	15	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	-	60	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC514800AJ/AZ/AFT				UNIT	NOTES
		-70		-80			
		MIN	MAX	MIN	MAX		
t_{WP}	Write Command Pulse Width	15	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	12
t_{DHR}	Data Hold Time	15	-	15	-	ns	12
t_{DH}	Data Hold Time referenced to $\overline{RAS}$	55	-	60	-	ns	
t_{REF}	Refresh Period	-	16	-	16	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	-	50	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	100	-	110	-	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	65	-	70	-	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	70	-	75	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	-	40	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	-	10		ns	
t_{OEA}	$\overline{OE}$ Access TIme	-	20	0	20	ns	9
t_{OED}	$\overline{OE}$ to Data Delay	20	-	20	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	20	-	ns	
t_{ODS}	Output Disable Set-Up Time	0	-	0	-	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0~A8, A9)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$))	-	7	pF
C_O	Input Capacitance (I/O1~I/O8)	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume t_T=5ns.

8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieveS the open circuit condition and are not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

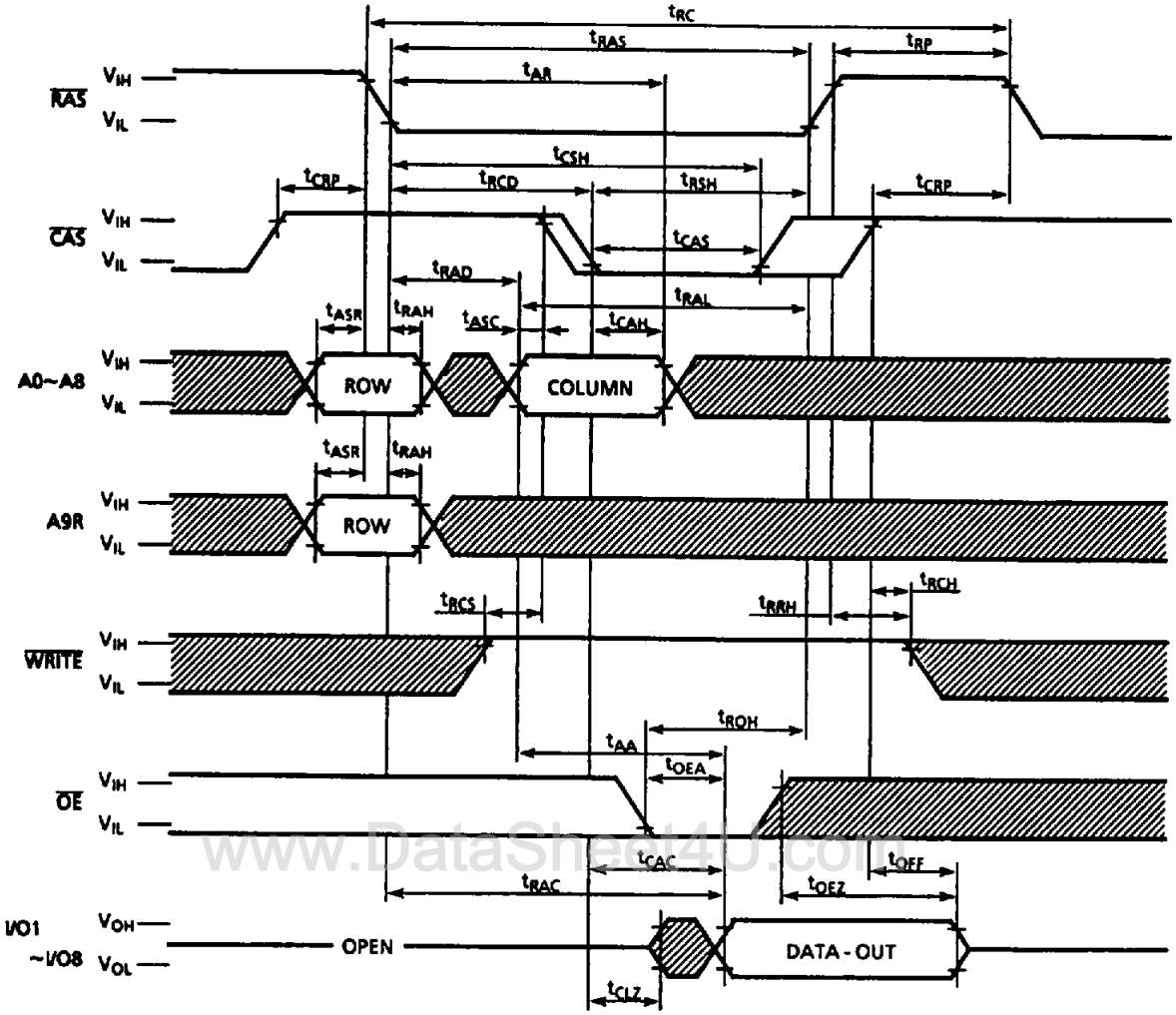
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.

13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the date sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.), $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CPWP} \geq t_{CPWD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.

14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

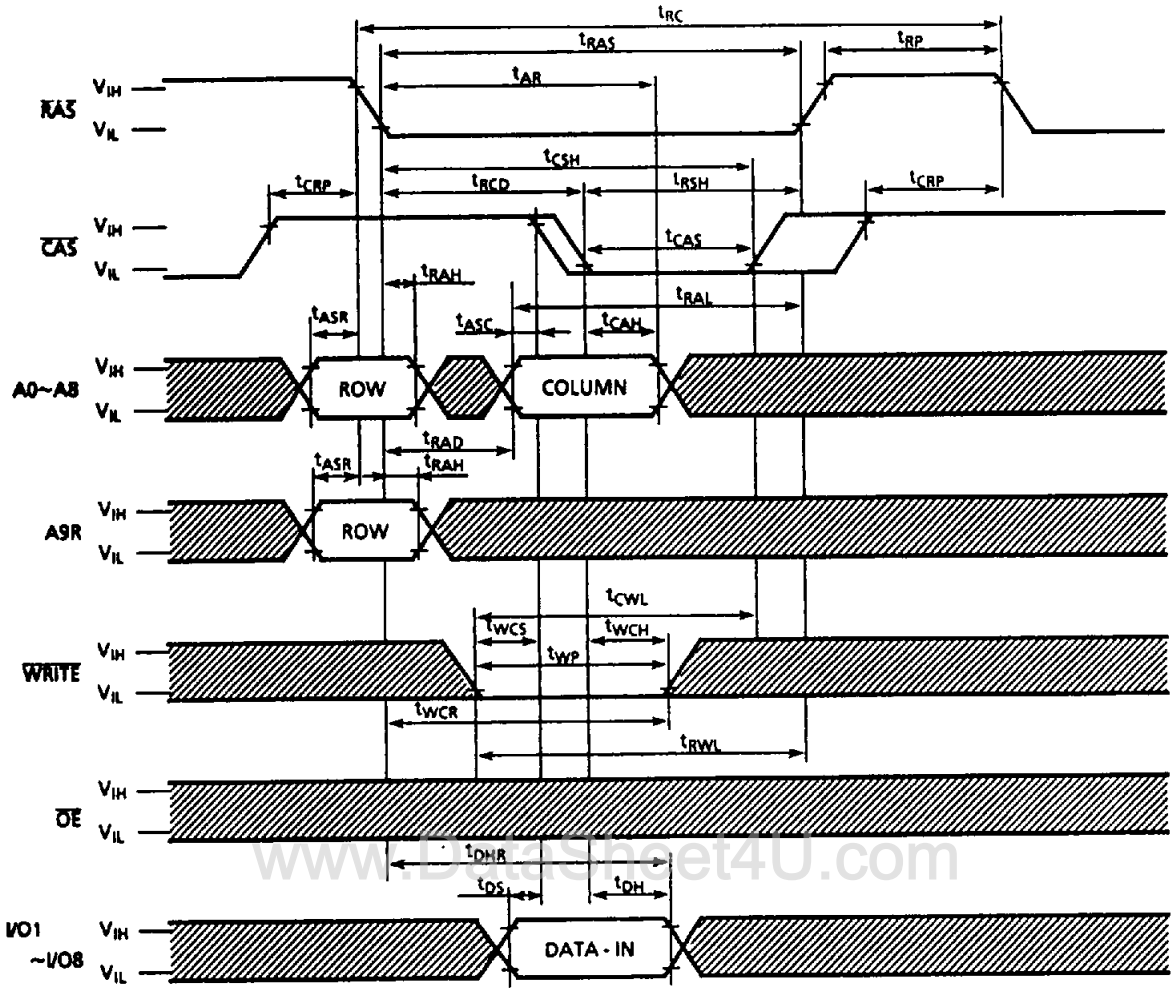
READ CYCLE



Note : D_{IN} = OPEN

▨ : "H" or "L"

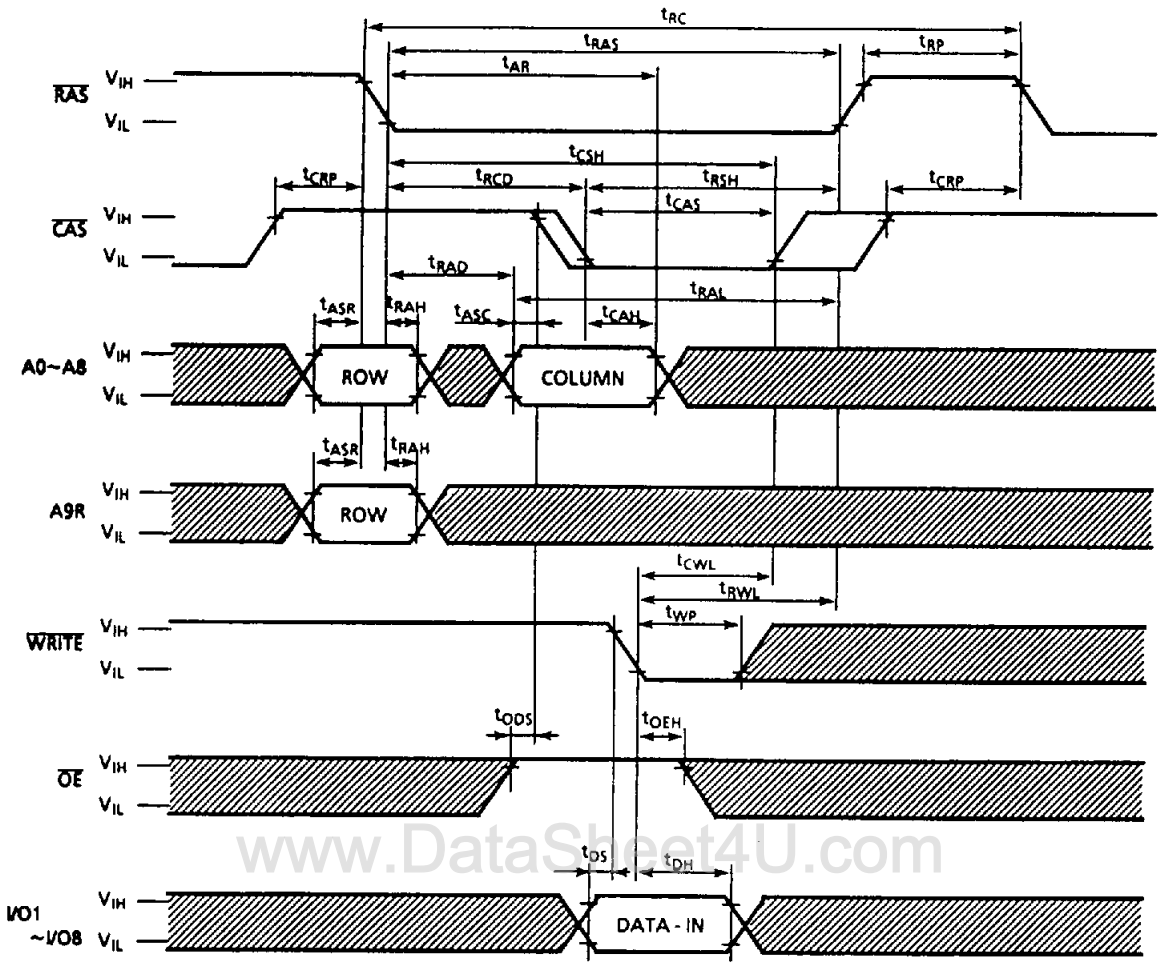
WRITE CYCLE (EARLY WRITE)



Note : D_{OUT} = OPEN

▨ : "H" or "L"

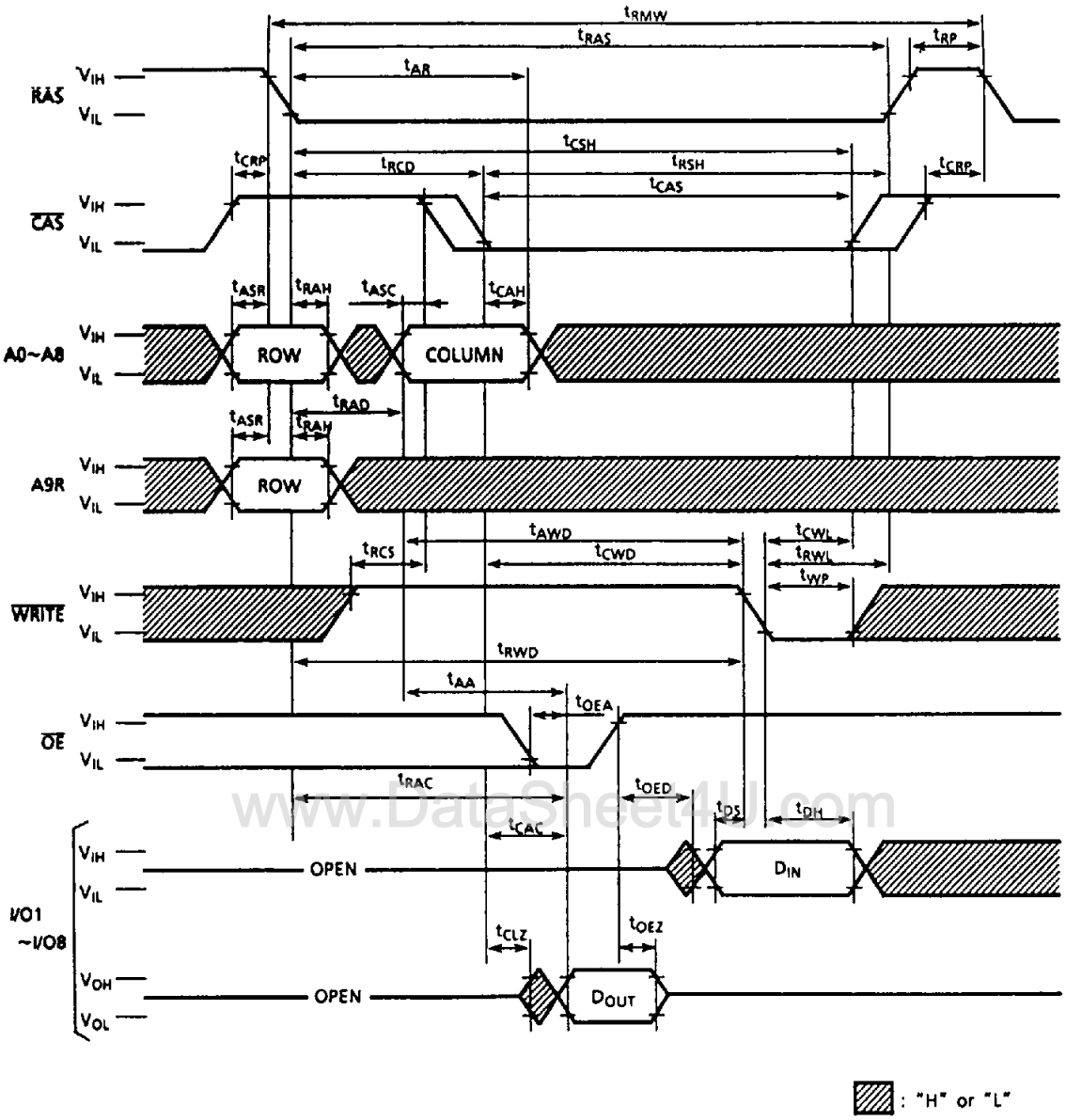
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



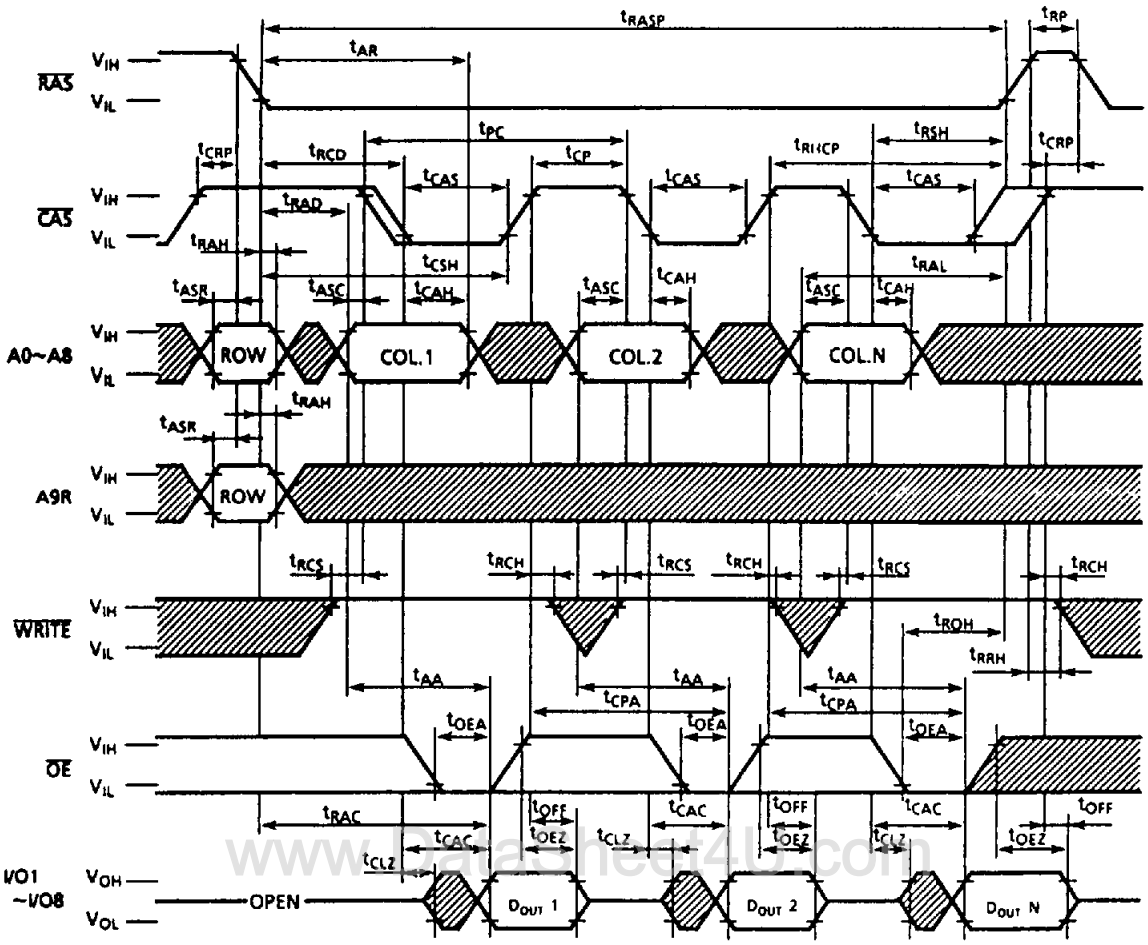
Note : D_{OUT} = OPEN

▨ : "H" or "L"

READ-MODIFY-WRITE CYCLE



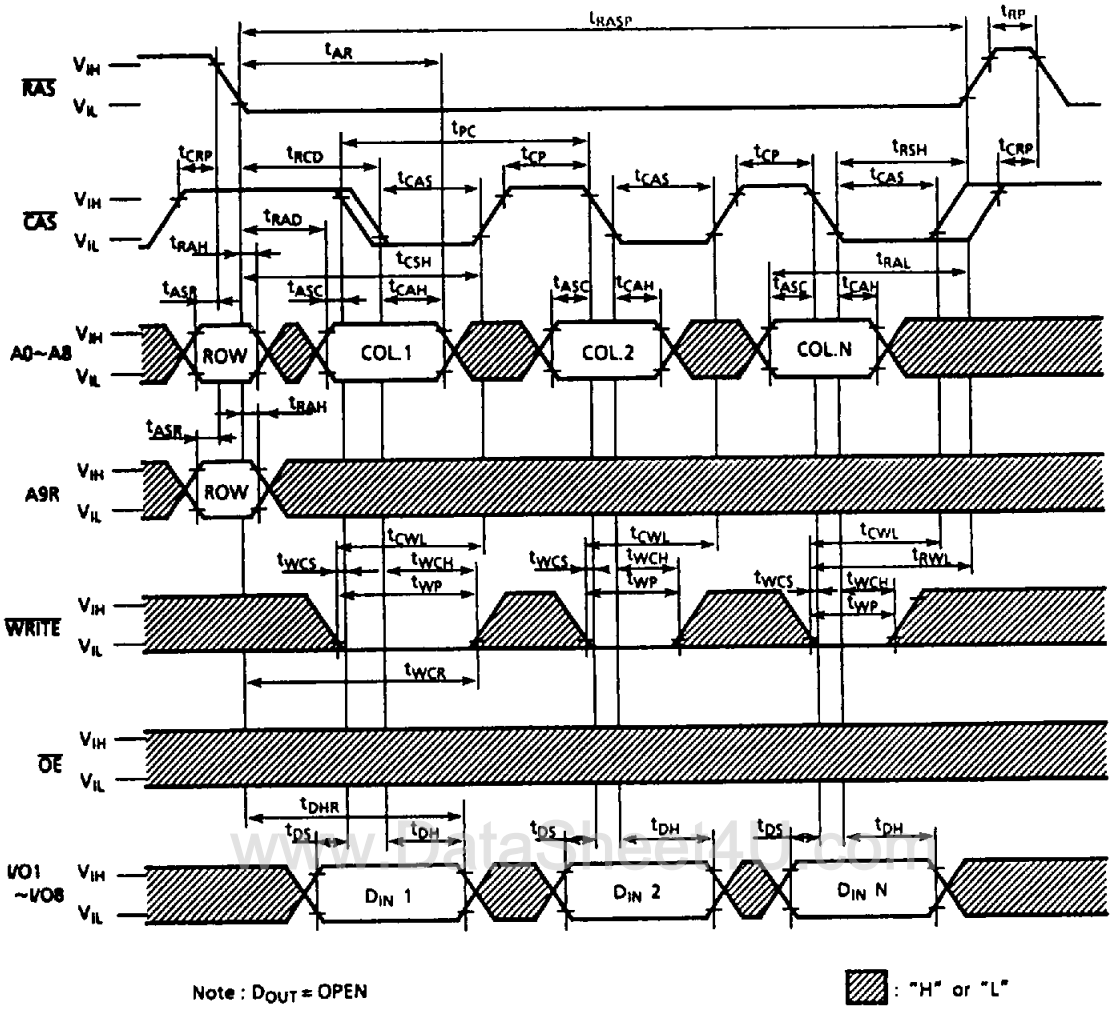
FAST PAGE MODE READ CYCLE



Note : D_{IN} = OPEN

▨ : "H" or "L"

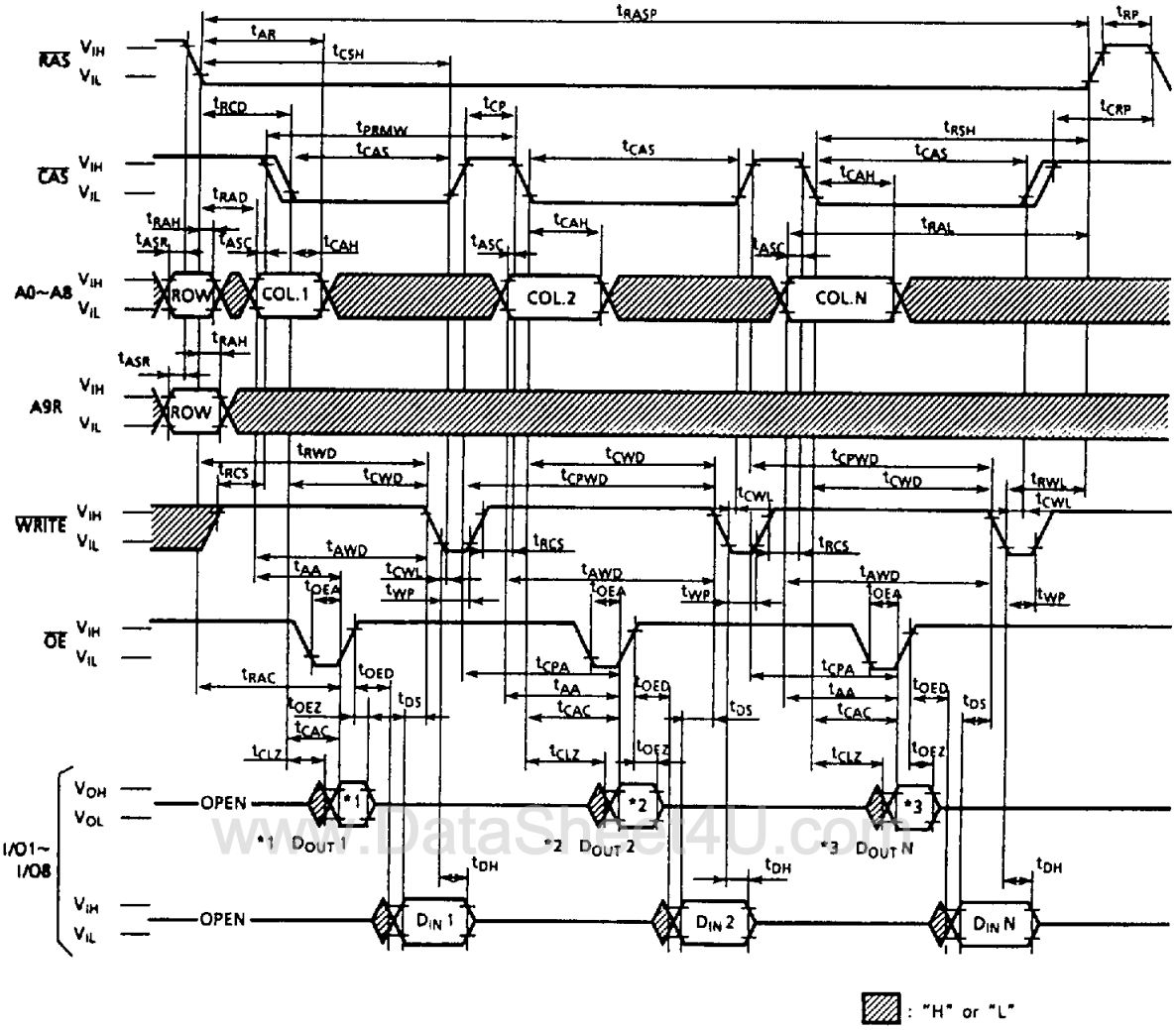
FAST PAGE MODE WRITE CYCLE



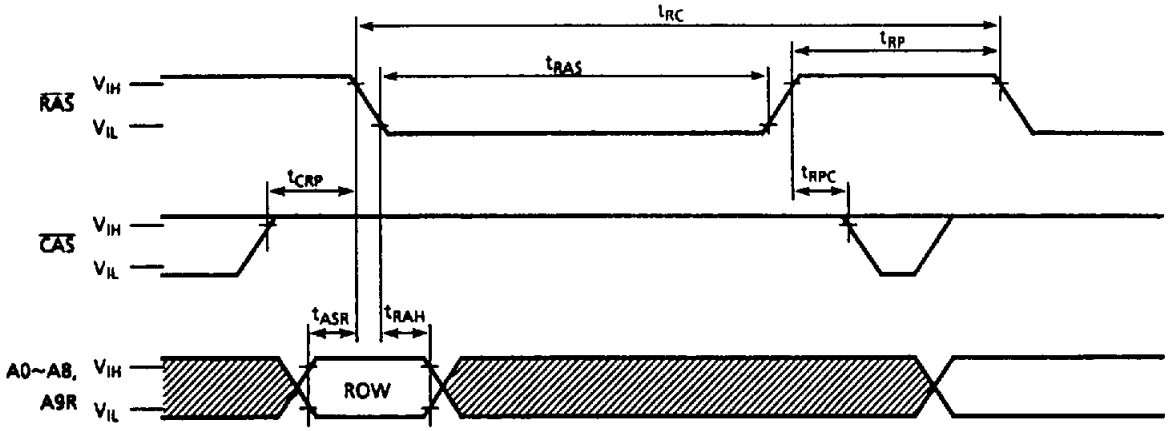
Note : D_{OUT} = OPEN

▨ : "H" or "L"

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



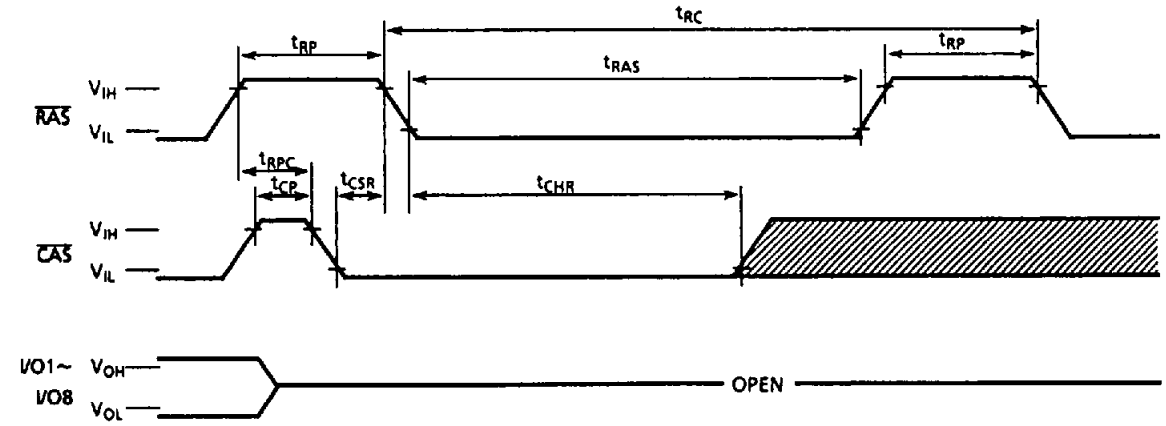
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, $\overline{OE}$, D_{IN} = "H" or "L"
D_{OUT} = OPEN

▨: "H" or "L"

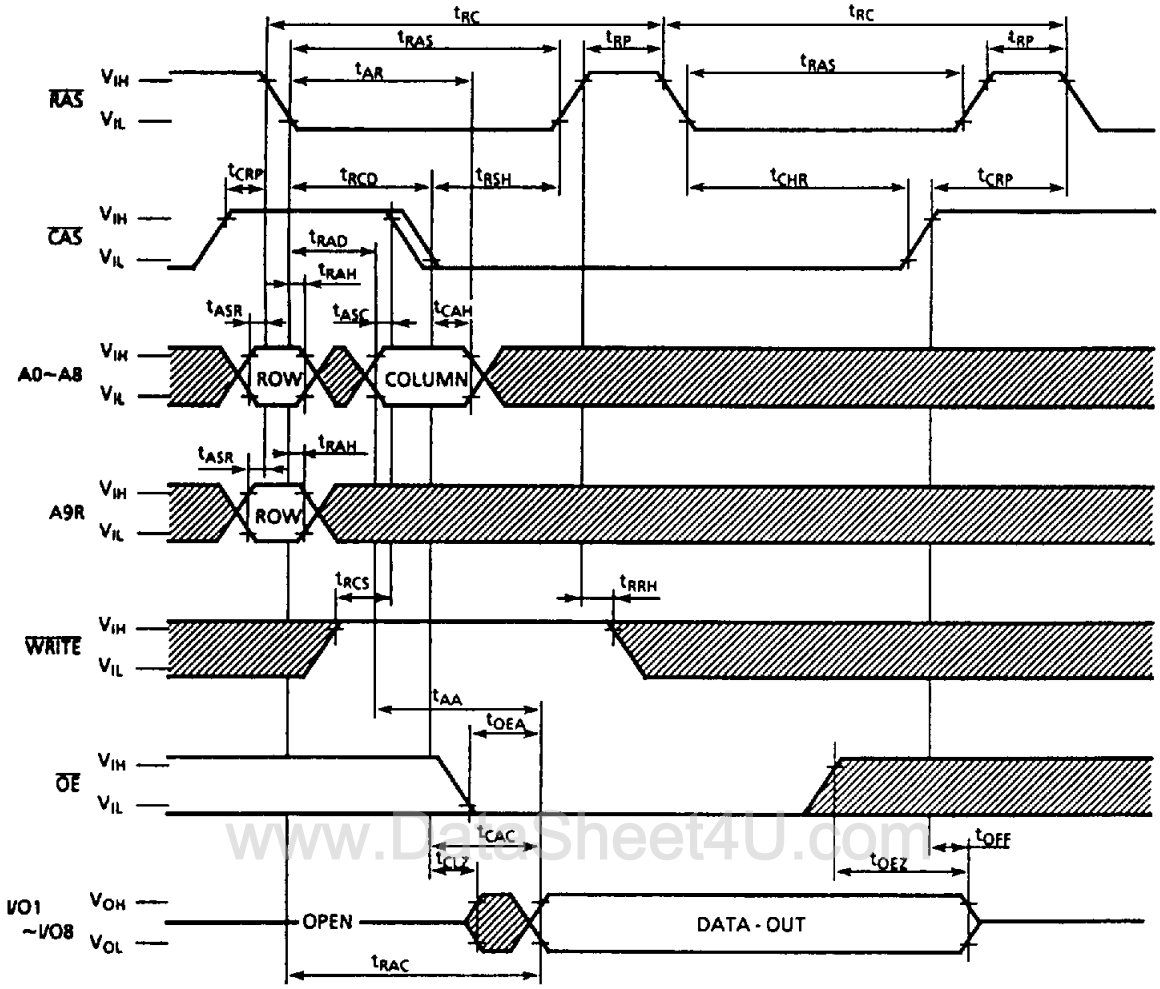
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{WRITE}$, $\overline{OE}$, A0~A8, A9R = "H" or "L"

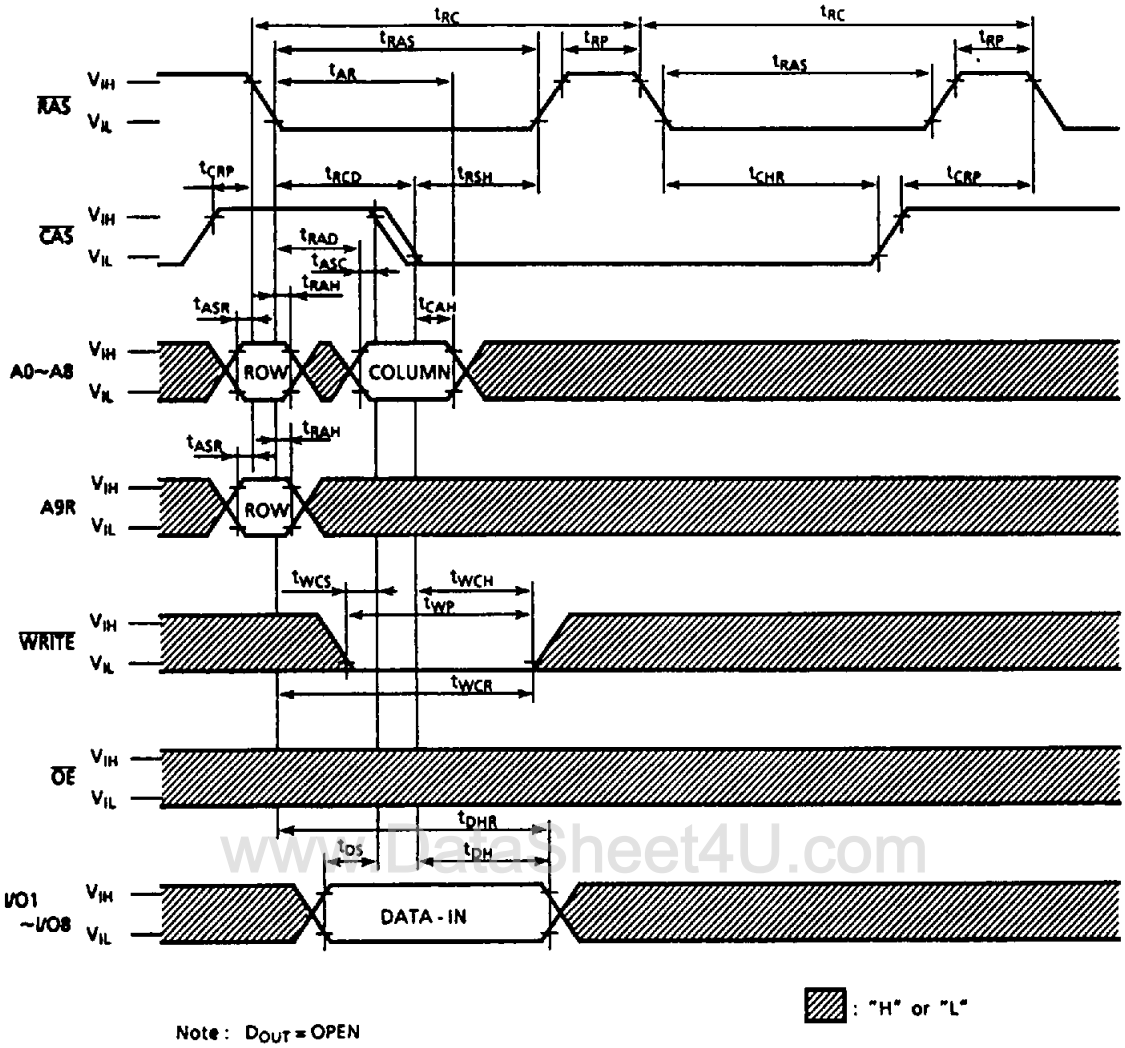
▨: "H" or "L"

HIDDEN REFRESH CYCLE (READ)



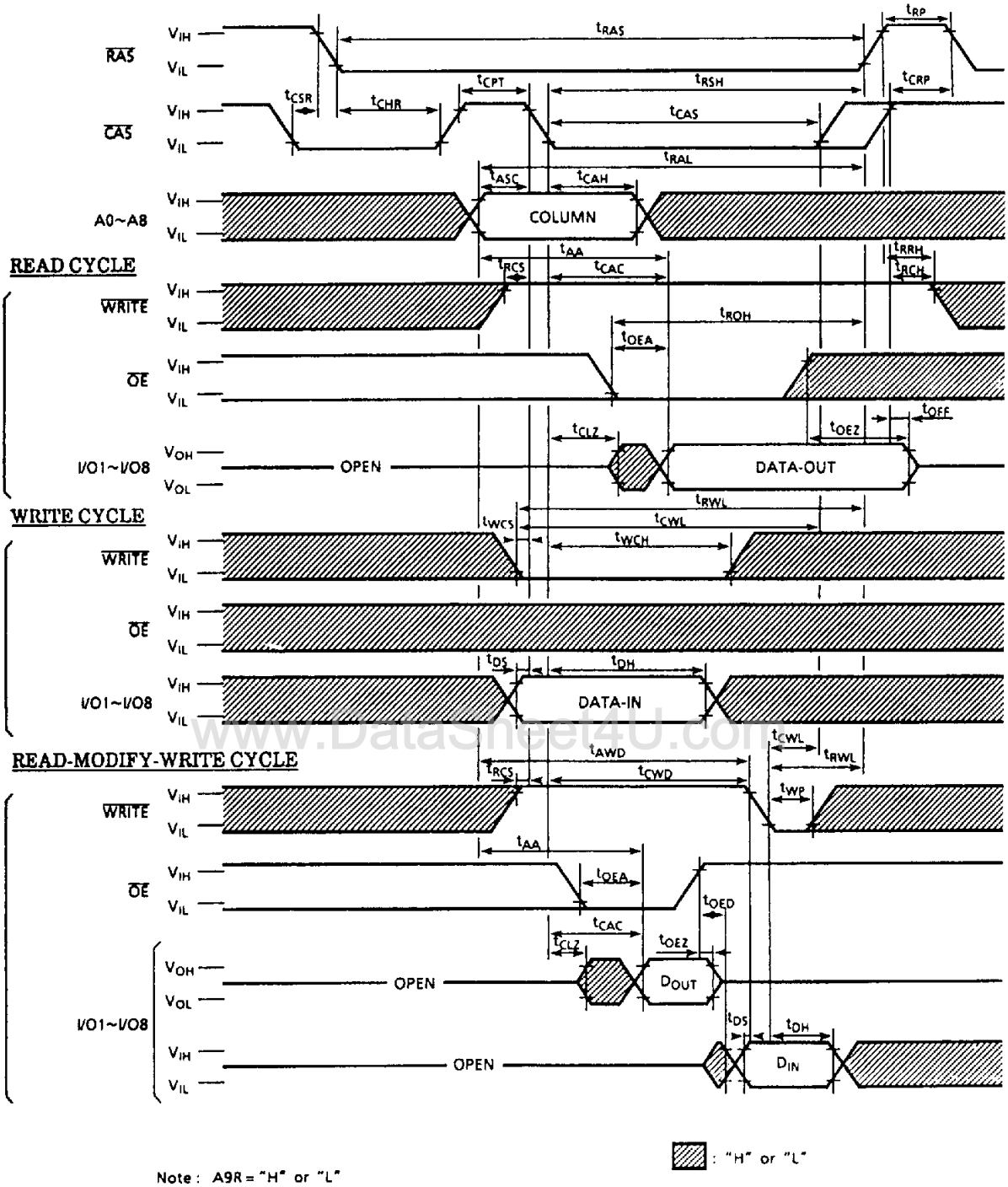
Note : D_{IN} = OPEN

HIDDEN REFRESH CYCLE (WRITE)



Note : D_{OUT} = OPEN

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



: "H" or "L"

Note : A9R = "H" or "L"

APPLICATION INFORMATION

ADDRESSING

The 19 address bits required to decode 1 of the 524,288 cell locations within the TC514800AJ/AZ/AFT are multiplexed onto the 10 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 10 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 9 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$ triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Data Inputs

A write cycle is performed by bringing $\overline{WRITE}$ low during the $\overline{RAS}/\overline{CAS}$ operation. The falling edge of $\overline{CAS}$ or $\overline{WRITE}$ stobes data on I/O1~I/O8 into the on-chip data latch. In an early write cycle, $\overline{WRITE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In delayed write or read modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{WRITE}$ with setup and hold times referenced to these signals.

In delayed or read modify write, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

Data Ouputs

The three state output buffers provide direct TTL compatibility with a fan-out of standard TTL load. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

The outputs become valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the output are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{OE}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state.

When the $\overline{OE}$ imput is brought to a logical low level, the output buffers are enabled. Both $\overline{CAS}$ and $\overline{OE}$ can control the outputs. Thus in read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high forces the outputs into the high impedance state.

$\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 1024 row addresses (A0~A8, A9R) within each 16 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished "$\overline{RAS}$-only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

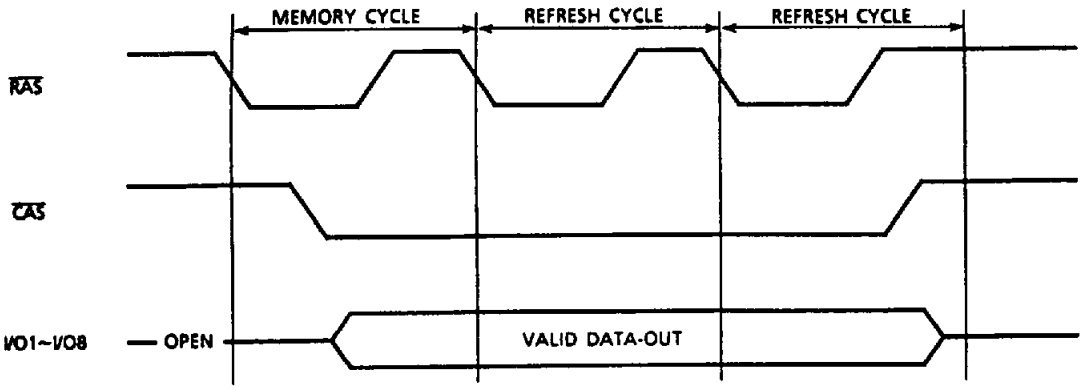
$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC514800AJ/AZ/AFT offers an alternate refresh method. If $\overline{CAS}$ is hold on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generations and the refresh address counter are enabled, and an internal refresh control clock generations and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh opeation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

FAST PAGE MODE

The "Fast Page Mode" feature of the TC514800AJ/AZ/AFT allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Fast page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

HIDDEN REFRESH

An optional feature of the TC514800AJ/AZ/AFT is that refresh cycles may be performed while maintaining valid data at the output pins. This is referred to as Hidden Refresh. Hidden Refresh is perfomed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "Hidden" among data cycles without affecting the data availability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC514800AJ/AZ/AFT can be tested by "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST". This cycle performs READ/WRITE operation taking internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycle as initialization cycles. The test procedure is as follows.

1. Write "0" into all the memory cells normal write mode.
2. Select one certain column address and read "0" out and write "1' in each cell be performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-MODIFY-WRITE CYCLE)". Repeat this operation 1024 times.
3. Check "1" out of 1024 bits at normal read mode , which was written at 2.
4. Using the same column as 2., read "1" out and write "0" in each cell performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST". Repeat This operation 1024 times.
5. Check "0" out of 1024 bits as normal read mode, which was written at 4.
6. Perform the above 1. to 5. to the complement data.