4,194,304 WORD x 1 BIT DYNAMIC RAM

* This is advanced information and specifications are subject to change without notice.

DESCRIPTION

The TC514101J/Z is the new generation dynamic RAM organized 4,194,304 words by 1 bit. The TC514101J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514101J/Z to be packaged in a standard 26/20 pin plastic SOJ and 20 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

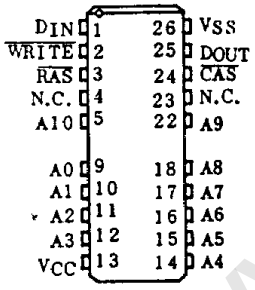
- 4,194,304 word by 1 bit organization
- Fast access time and cycle time

		TC514101J/Z-80/-10	
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{RC}	Cycle Time	150ns	180ns
t_{NC}	Nibble Mode Cycle Time	40ns	45ns

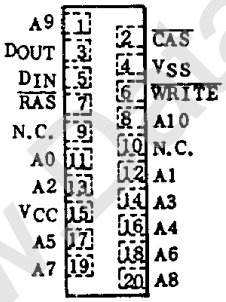
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low power
  578mW Operating (TC514101J/Z-80)
  495mW Operating (TC514101J/Z-10)
  5.5mW MAX. Standby
- Output unlatched at cylce end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Nibble Mode and Test Mode capability
- All inputs and output TTL compatible
- 1024 refresh cycles/16ms
- Package Plastic SOJ: TC514101J
  Plastic ZIP: TC514101Z

PIN CONNECTION (TOP VIEW)

Plastic SOJ



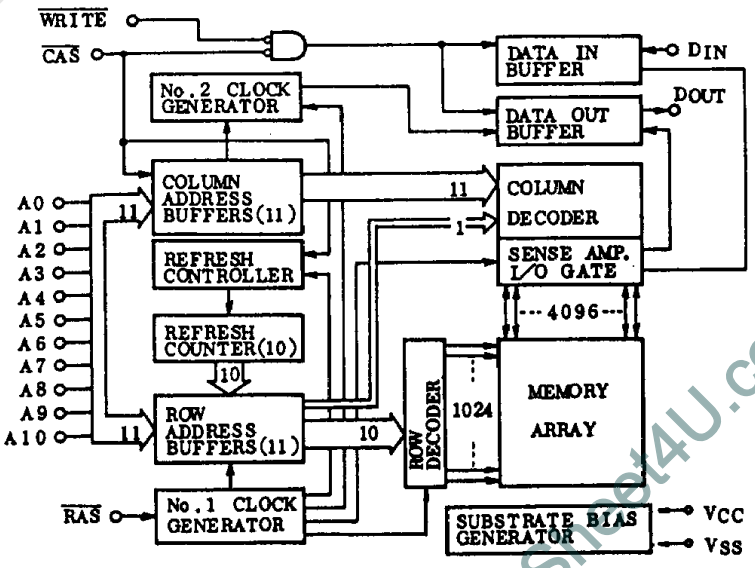
Plastic ZIP



PIN NAMES

A0 ~ A10	Address Inputs
$\overline{RAS}$	Row Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTE
Input Voltage	V_{IN}	-1 ~ 7	V	1
Output Voltage	V_{OUT}	-1 ~ 7	V	1
Power Supply Voltage	V_{CC}	-1 ~ 7	V	1
Operating Temperature	T_{OPR}	0 ~ 70	°C	1
Storage Temperature	T_{STG}	-55 ~ 150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C·sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (T_a=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, T_a=0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC514101J/Z-80	-	105	mA	3,4,5
		TC514101J/Z-10	-	90		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514101J/Z-80	-	105	mA	3,5
		TC514101J/Z-10	-	90		
I_{CC4}	NIBBLE MODE CURRENT Average Power Supply Current, Nibble Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling: t_{NC}=t_{NC} MIN.)	TC514101J/Z-80	-	60	mA	3,4,5
		TC514101J/Z-10	-	50		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC514101J/Z-80	-	105	mA	3
		TC514101J/Z-10	-	90		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins not under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ~ 70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514101J/Z -80		TC514101J/Z -10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150	-	180	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	175	-	210	-	ns	
t_{NC}	Nibble Mode Cycle Time	40	-	45	-	ns	
t_{NRMW}	Nibble Mode Read-Modify-Write Cycle Time	65	-	75	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	80	-	100	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	25	ns	9,14
t_{AA}	Access Time from Column Address	-	40	-	50	ns	9,15
t_{NCAC}	Nibble Mode Access Time	-	20	-	25	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	60	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	-	100	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	40	20	50	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	10	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	20	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	-	50	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	15	-	20	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{WP}	Write Command Pulse Width	15	-	20	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC514101J/Z -80		TC514101J/Z -10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	12
t_{DH}	Data Hold Time	15	-	20	-	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	60	-	75	-	ns	
t_{REF}	Refresh Period	-	16	-	16	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	-	25	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	80	-	100	-	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	40	-	50	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	20	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	-	50	-	ns	
t_{NCAS}	Nibble Mode Pulse Width	20	-	25	-	ns	
t_{NCP}	Nibble Mode $\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{NRSH}	Nibble Mode $\overline{RAS}$ Hold Time	20	-	25	-	ns	
t_{NCWD}	Nibble Mode $\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	-	25	-	ns	
t_{NRWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{RAS}$ Lead Time	20	-	25	-	ns	
t_{NCWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{CAS}$ Lead Time	20	-	25	-	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	10	-	10	-	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	-	10	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE

(V_{CC}=5V±10%, Ta=0∿70°C) (Note 6, 7, 8)

SYMBOL	PARAMETER	TC514101J/Z -80		TC514101J/Z -10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	155	-	185	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	105	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	-	25	-	30	ns	9,14
t_{AA}	Access Time from Column Address	-	45	-	55	ns	9,15
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	105	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	-	30	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	-	105	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	30	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	55	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0∿70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0∿A10, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	-	7	pF
C_O	Output Capacitance (D_{OUT})	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Column address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{CAS}$=V_{IH}.

6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume t_T=5ns.

8. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.

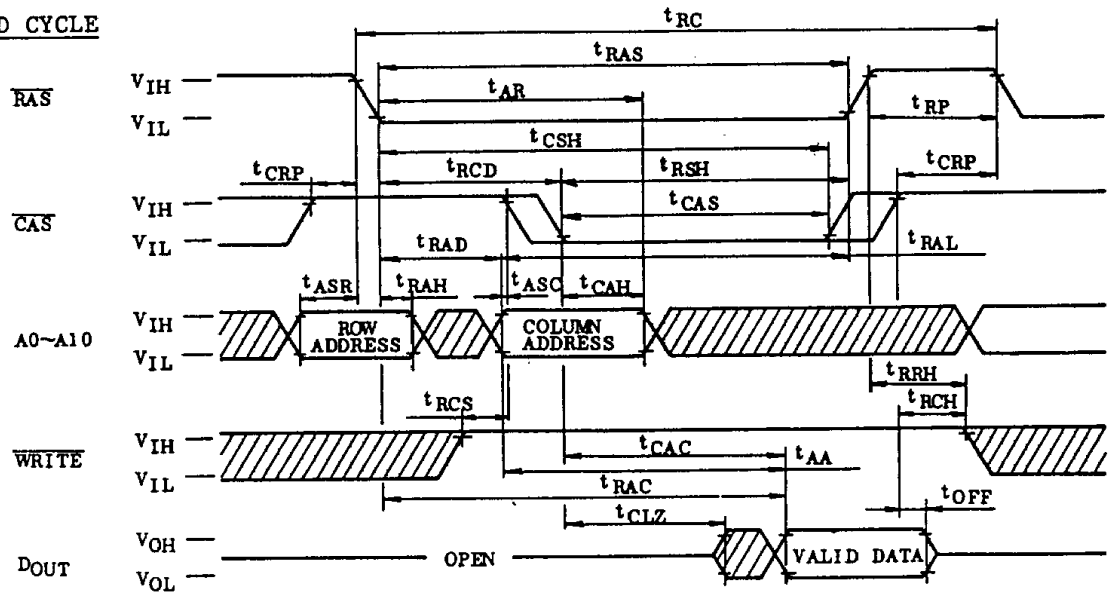
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a read-modify-write cycle and data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

14. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

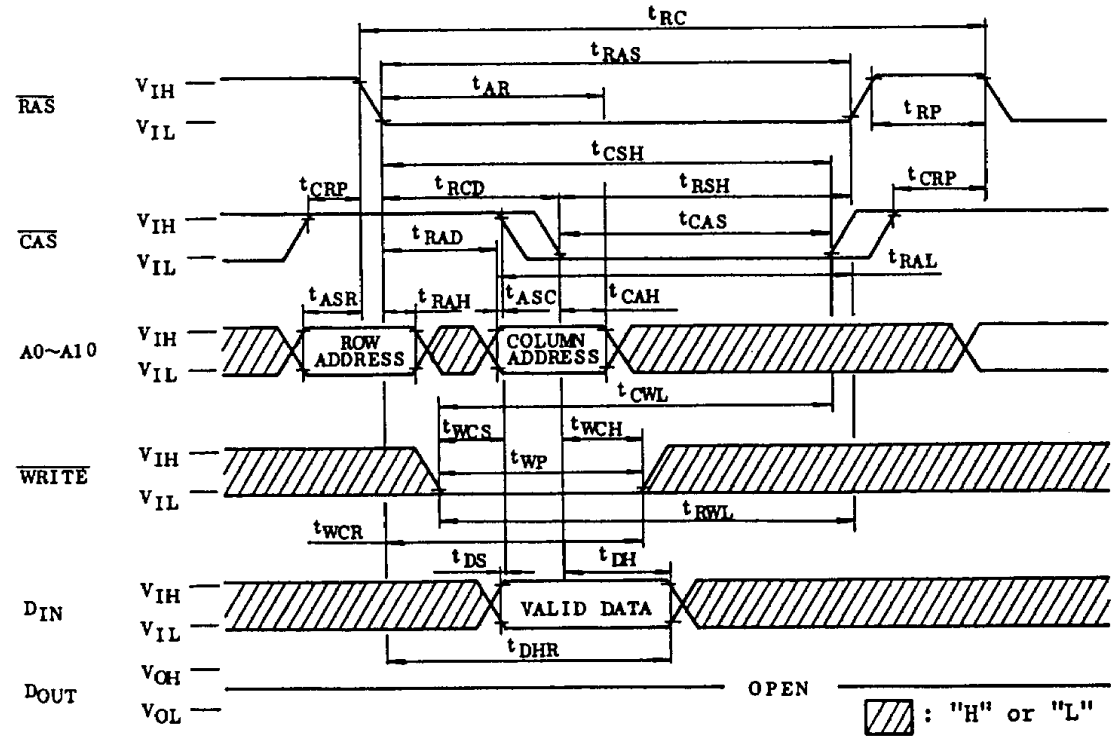
15. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

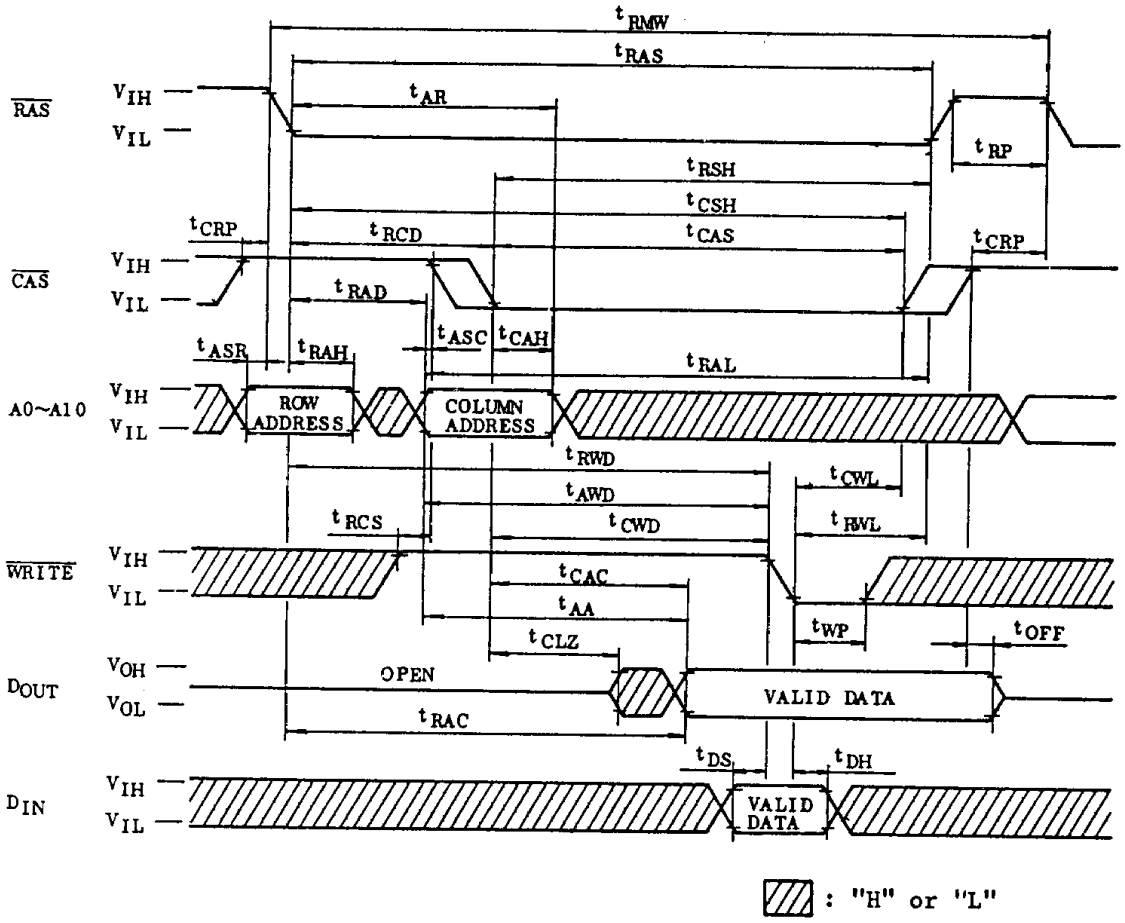
READ CYCLE



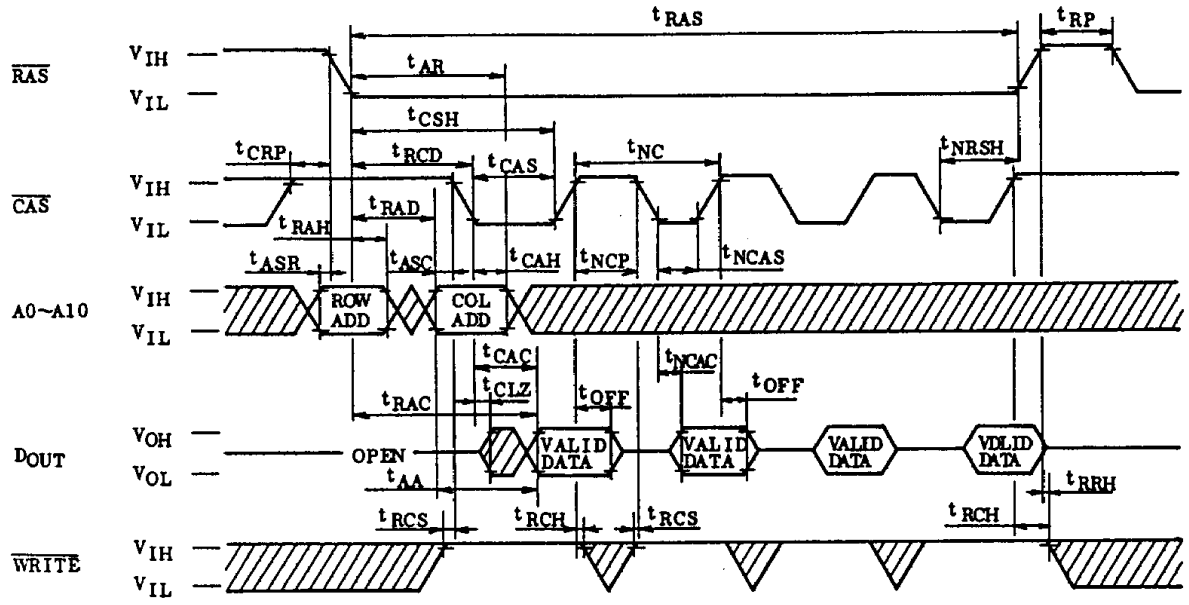
WRITE CYCLE (EARLY WRITE)



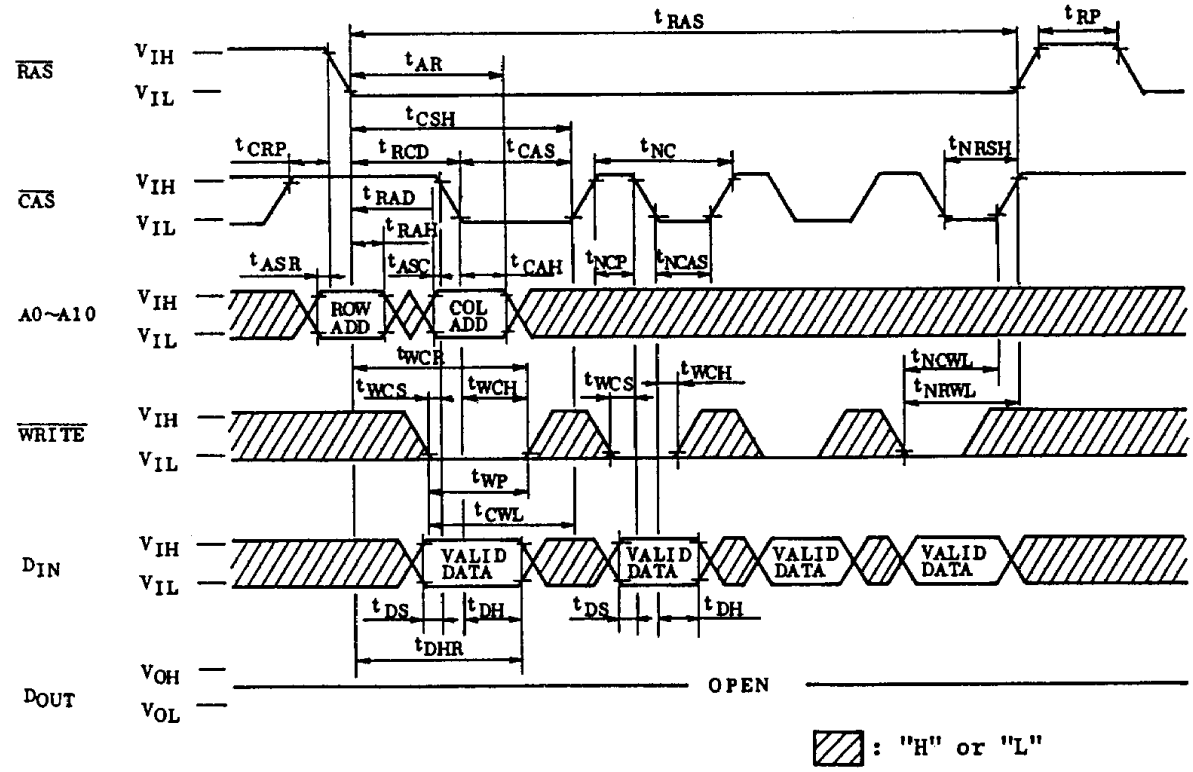
READ-MODIFY-WRITE CYCLE



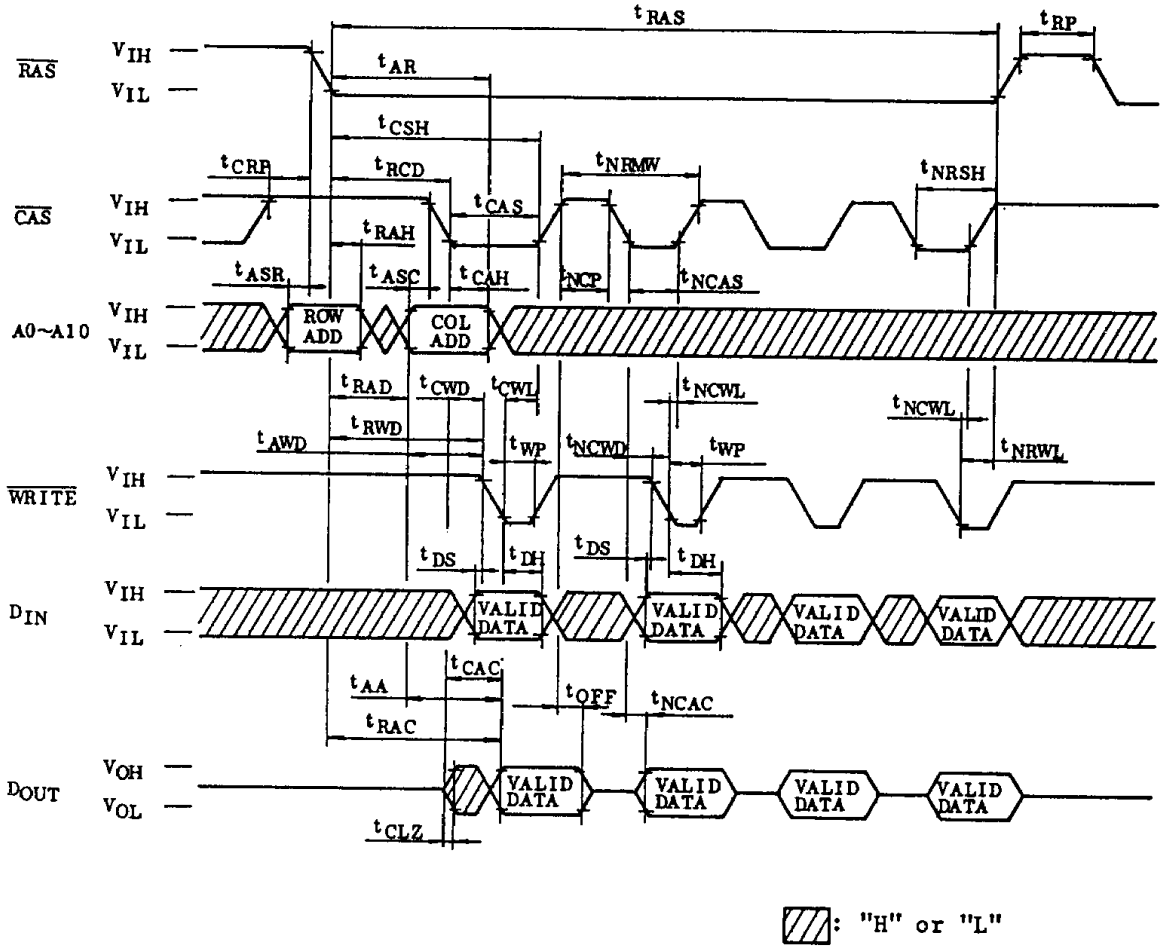
NIBBLE MODE READ CYCLE



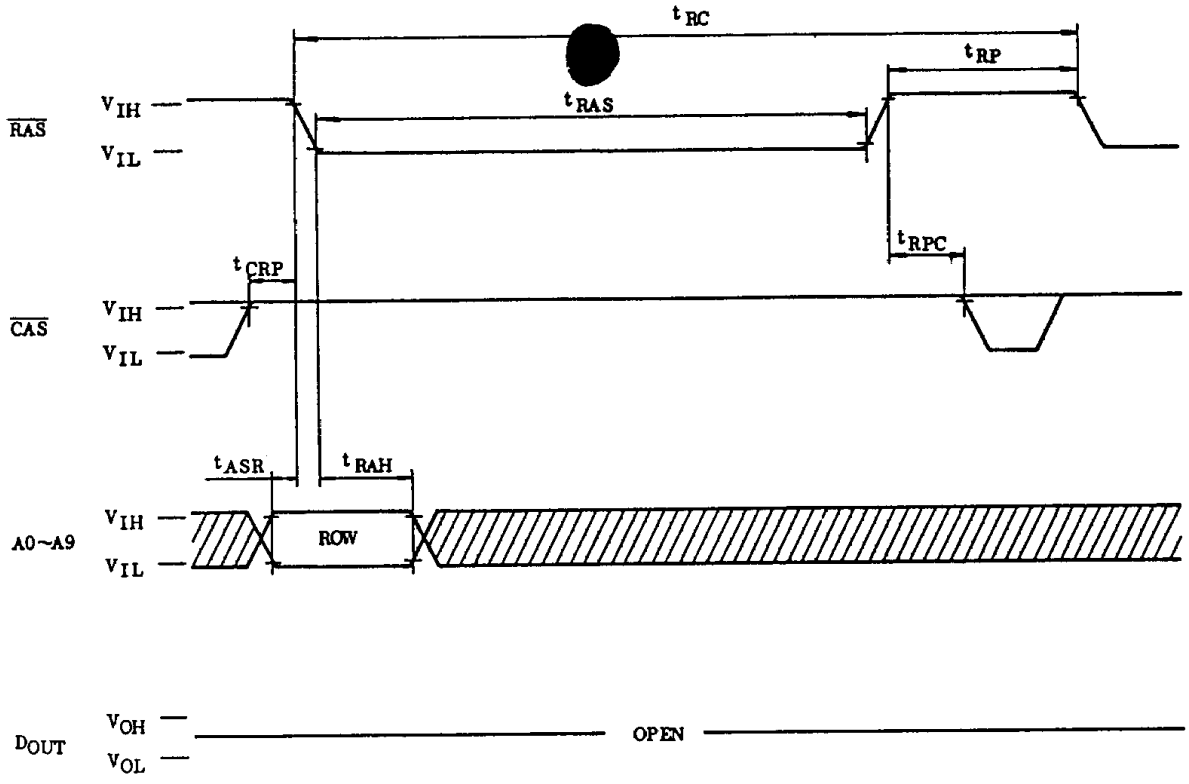
NIBBLE MODE WRITE CYCLE (EARLY WRITE)



NIBBLE MODE READ-MODIFY-WRITE CYCLE



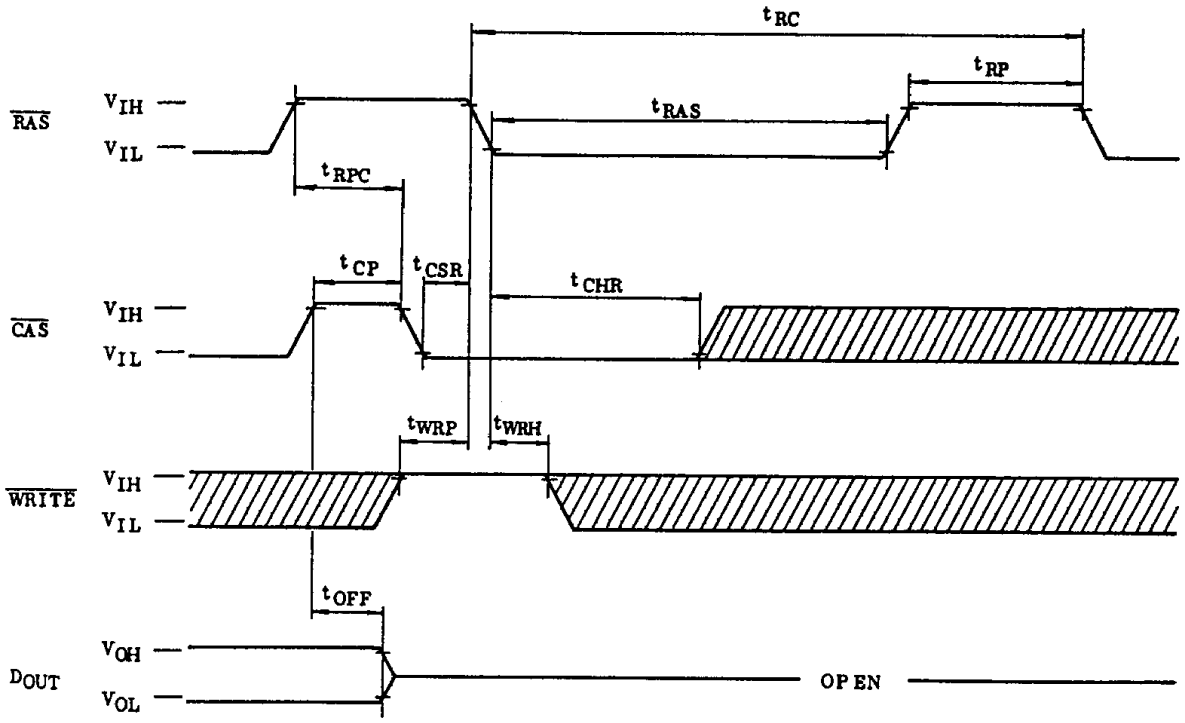
$\overline{RAS}$ ONLY REFRESH CYCLE



▨: "H" or "L"

NOTE: $\overline{WRITE}$="H" or "L" , A10="H" or "L"

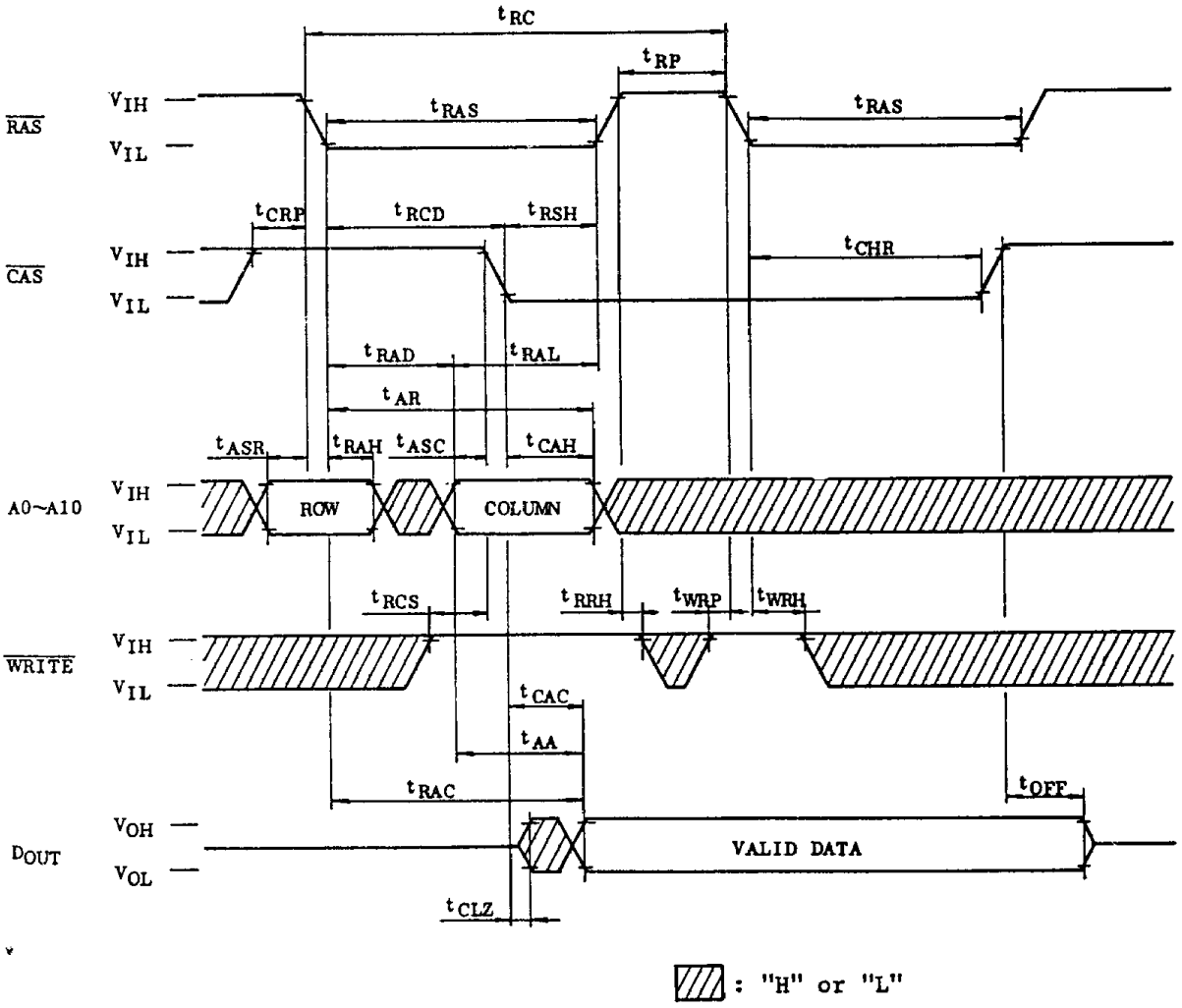
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



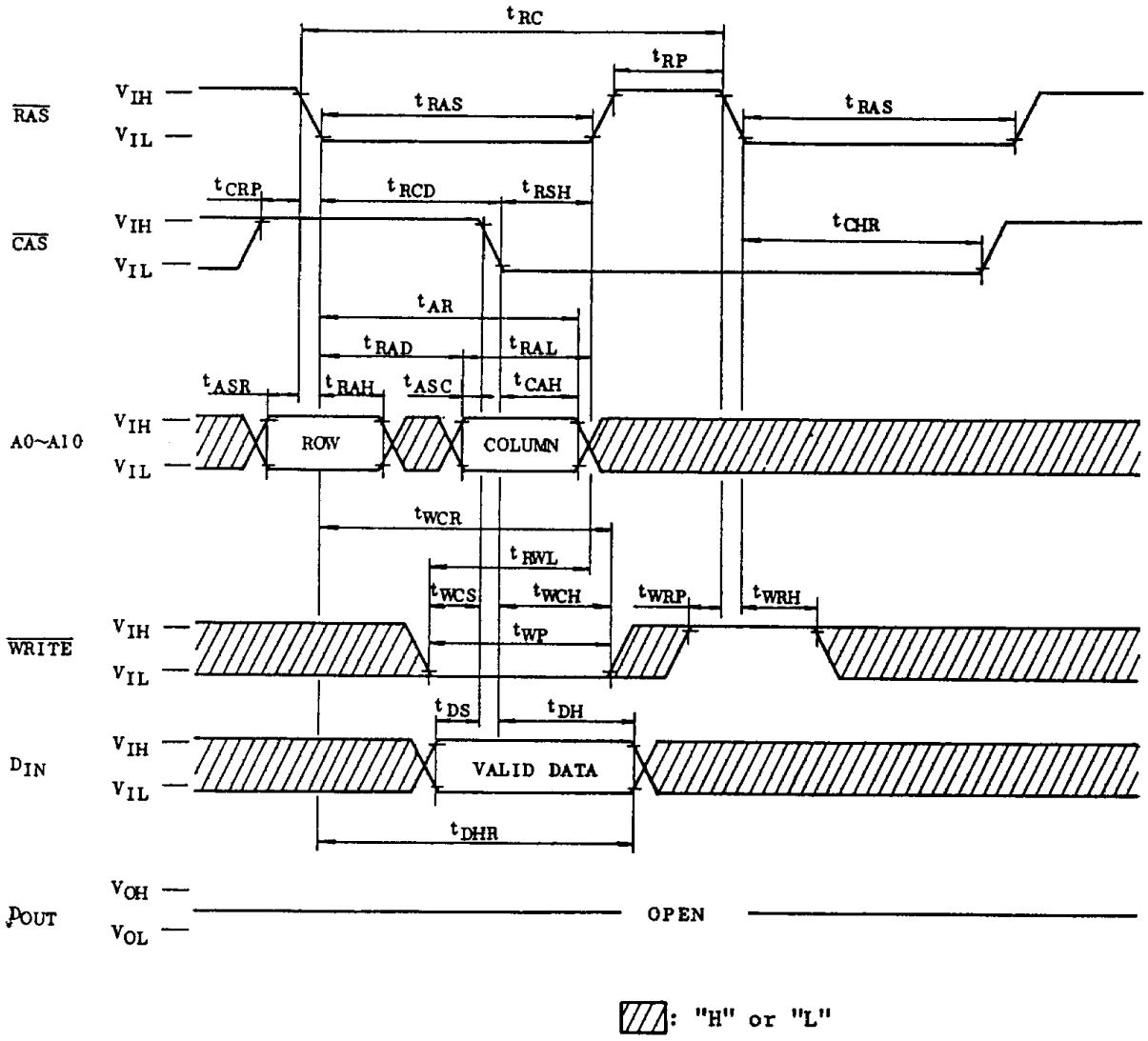
NOTE: A0 ∿ A10="H" or "L"

▨: "H" or "L"

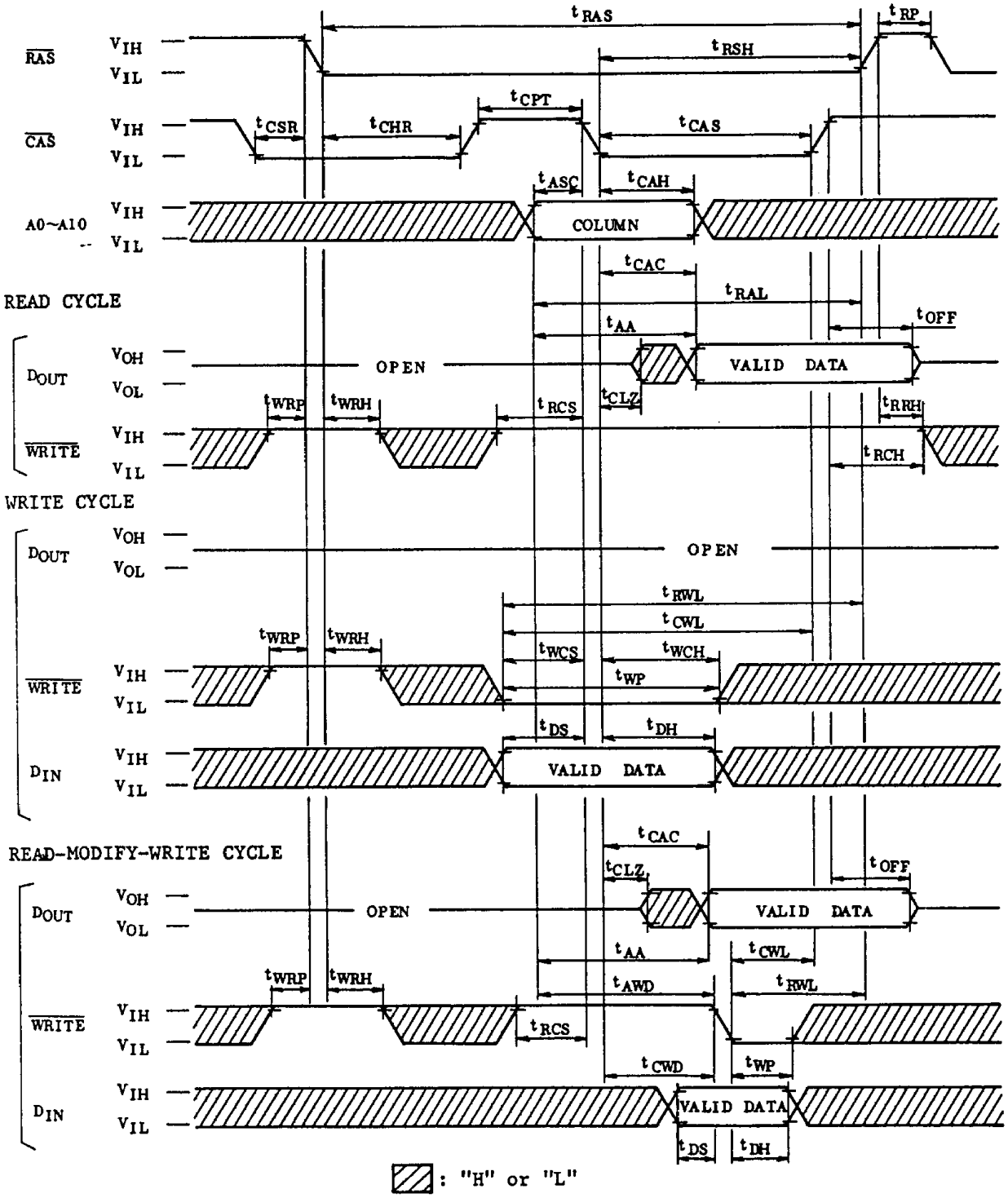
HIDDEN REFRESH CYCLE (READ)



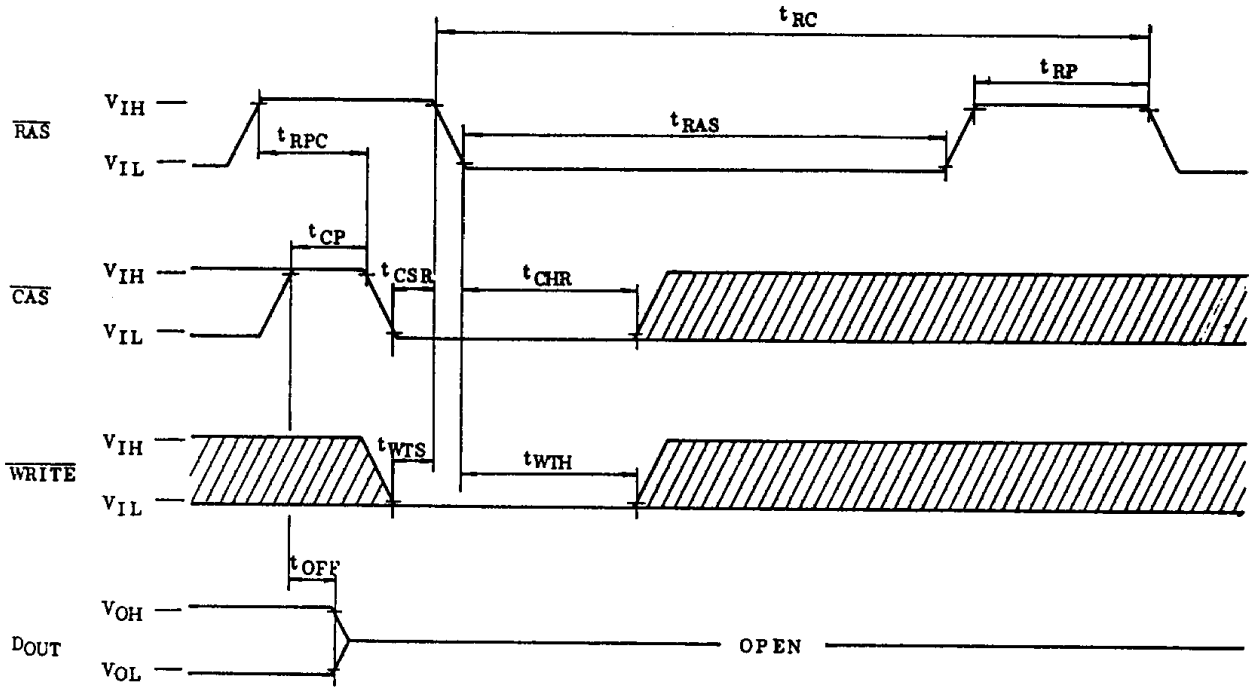
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE

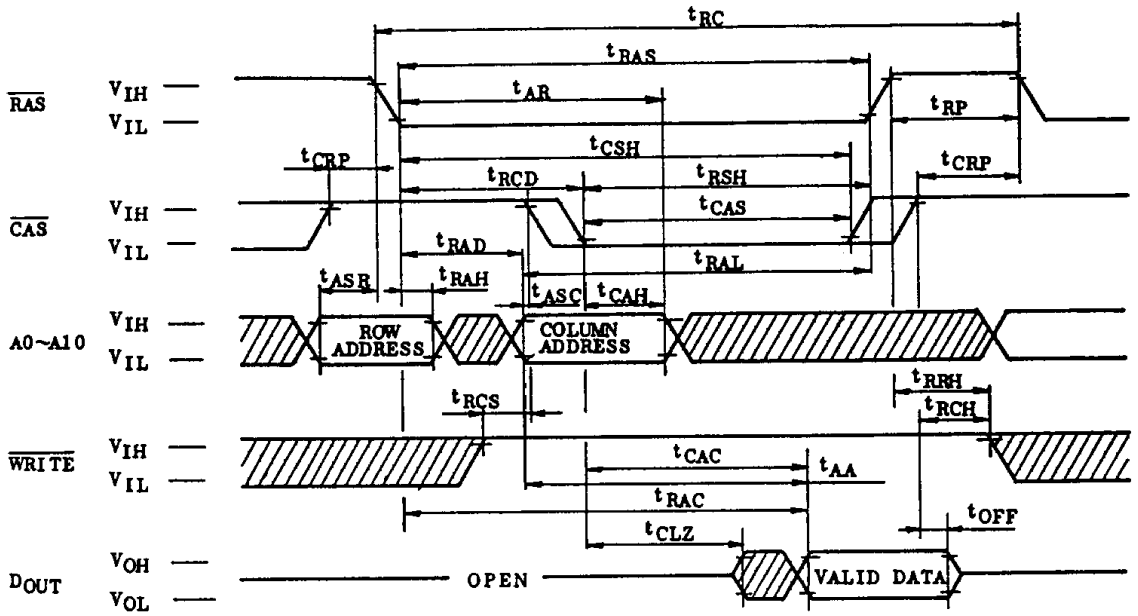


WRITE, CAS BEFORE RAS REFRESH CYCLE

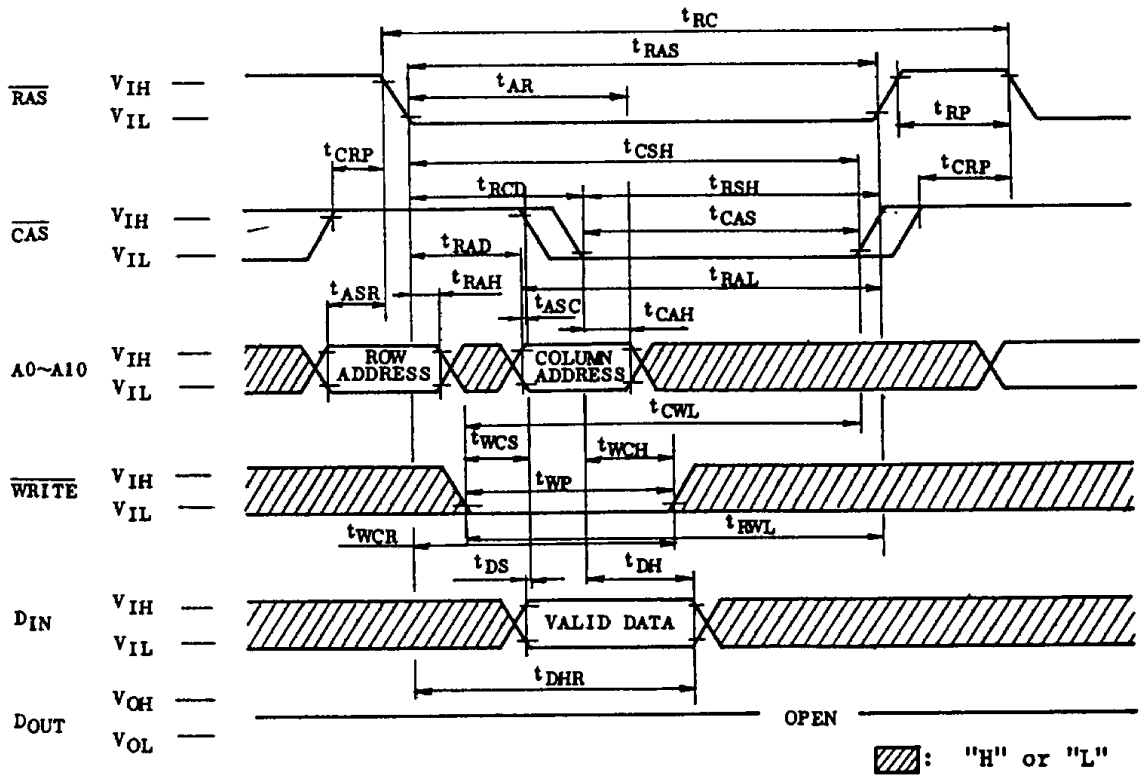


NOTE: D_{IN}, A0 ∿ A10: "H" or "L" ▨ : "H" or "L"

READ CYCLE IN THE TEST MODE



WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



APPLICATION INFORMATION

ADDRESSING

The 22 address bits required to decode 1 of the 4,194,304 cell locations within the TC514101J/Z are multiplexed onto the 11 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 11 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 11 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and nibble mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

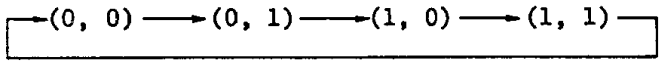
Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the ouptut within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TC514101J/Z is the high impedance (open circuit) state. This is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

NIBBLE MODE

Nibble mode operation allows faster successive data operation on 4 bits. The first of 4 bits is accessed in the usual manner with read data coming out at t_{CAC} time. By keeping $\overline{RAS}$ low, $\overline{CAS}$ can be cycled up and then down, to read or write the next three pages at high data rate. Row and column address need only be supplied for the first access of the cycles. From then on, the falling edge of $\overline{CAS}$ will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around method).



Address A10 determines the starting point of the circular 4 bits nibble. Row A10 and column A10 provide the two binary bits needed to select one of four bits. From then on, successive bits come out in a binary fashion; 00 → 01 → 10 → 11 with A10 row being the least significant address.

A nibble cycle can be a read, write, or delayed write cycle. Any combinations of reads and writes or late writes will be allowed. In addition, the circular wrap-around will continue for as long as $\overline{RAS}$ is kept low.

$\overline{RAS}$ ONLY REFRESH

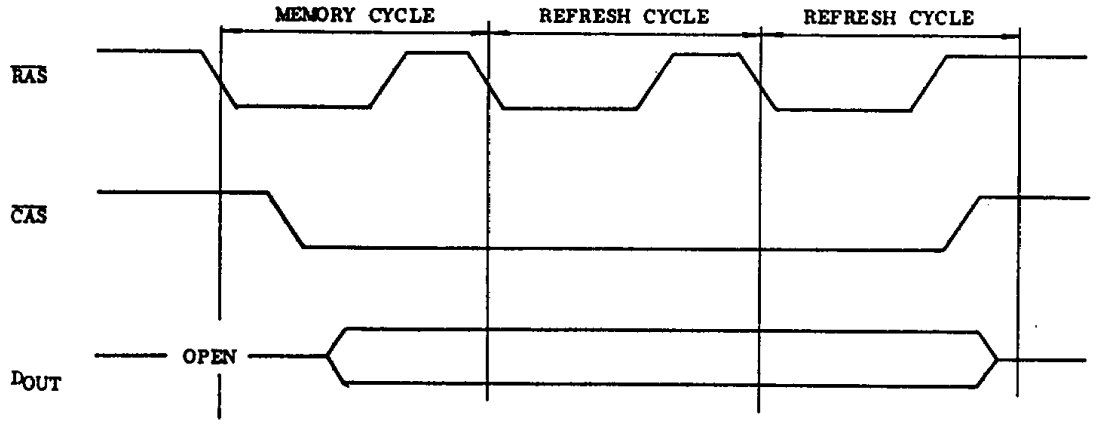
Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 1024 row address (A0 ∿ A9) within each 16 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC514101J/Z offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

HIDDEN REFRESH

An optional feature of the TC514101J/Z is that refresh cycles may be performed while maintaining valid data at the output pin. This referred to as Hidden Refersh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (See Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of TC514101J/Z can be tested by $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST (READ-WRITE CYCLE).
Repeat this operation 1024 times.

③ Check "1" out of 1024 bits at normal read mode, which was written at ②.

④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST.
Repeat this operation 1024 times.

⑤ Check "0" out of 1024 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ the complement data.

TEST MODE

The TC514101J/Z is the RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A10R, A10C and A0C are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0". Fig. 1 shows the block diagram of TC514101J/Z. In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/8 in case of N test pattern).

BLOCK DIAGRAM IN TEST MODE

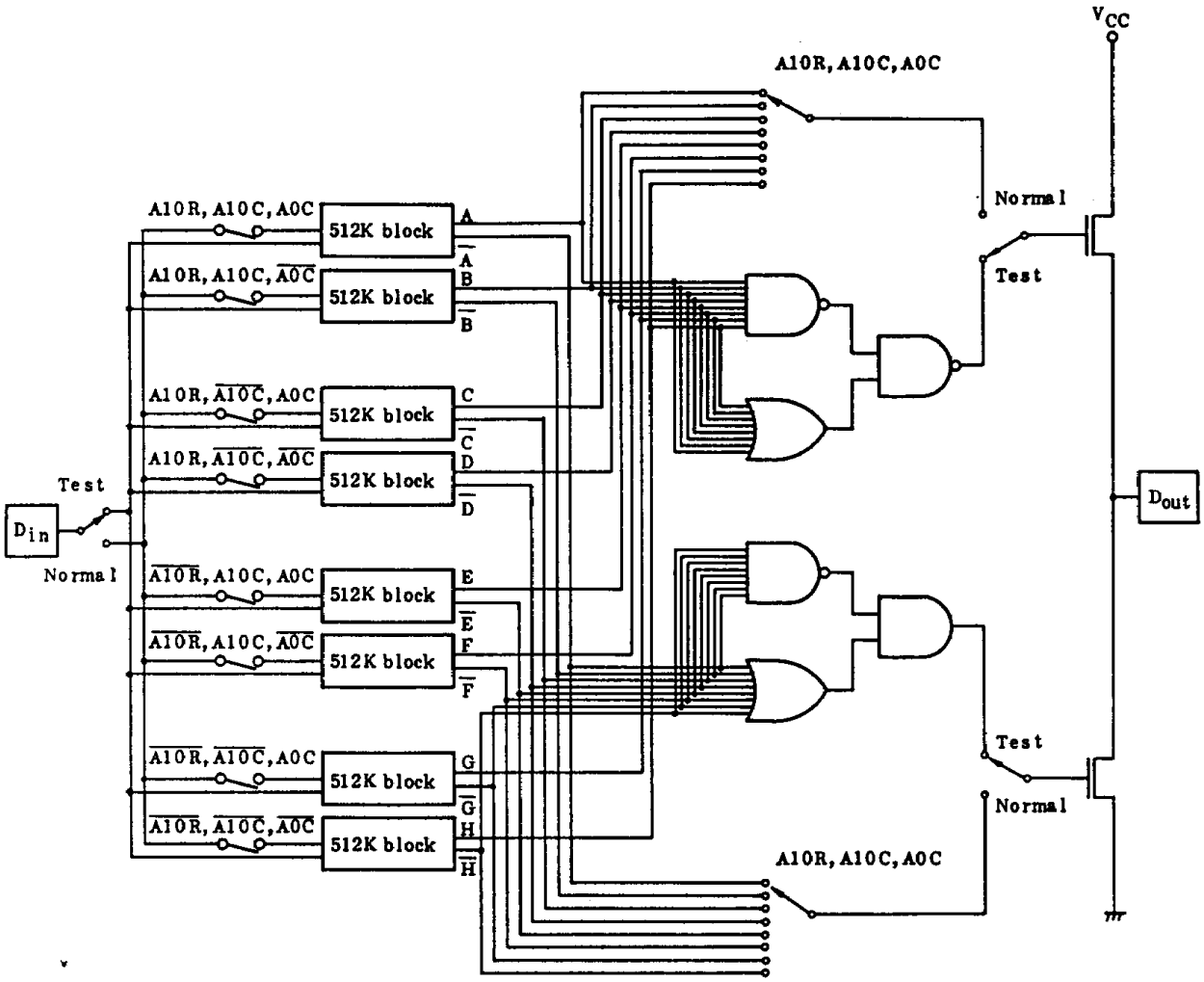


Fig. 1