TC40H390P/F

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

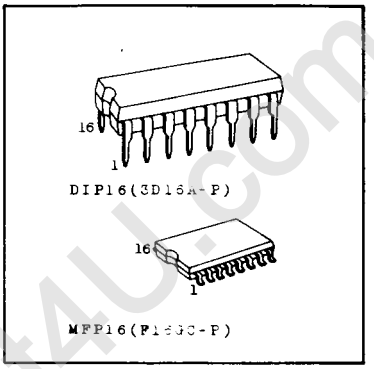
TC40H390 DUAL DECADE COUNTER

The TC40H390 is a dual decade counter with CLEAR function, and can be sued as a binary/quinary /decimal counter. The CLEAR input is active at "H" level, and the CLOCK input is triggered at the falling edge of CLOCK.

For using a TC40H390 as a decimal counter, output QA shall be connected to input $\overline{B}$ directly.

For using a TC40H390 as a quinary counter, input clock signal shall be applied to input $\overline{B}$ directly.

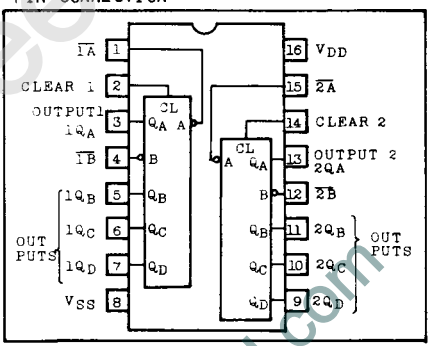
The function and pin assignment of this counter are the same as those of the TTL74390 and the LSTTL74LS390.



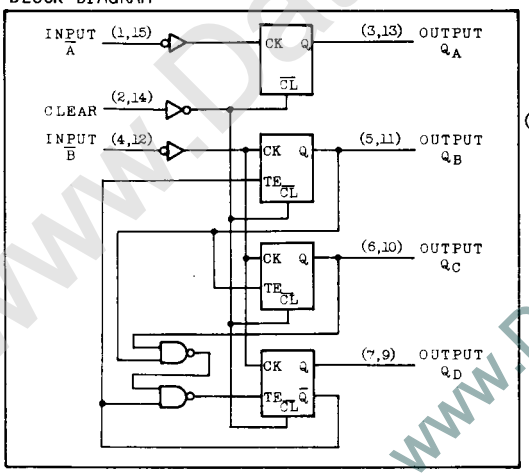
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN CONNECTION



BLOCK DIAGRAM



COUNT SEQUENCE

(1)QA,IN$_B$ Connection

COUNT	OUTPUT			
	Q_A	Q_B	Q_C	Q_D
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

(2)QD,IN$_A$ Connection

COUNT	OUTPUT			
	Q_B	Q_C	Q_D	Q_A
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	L	L	L	H
6	H	L	L	H
7	L	H	L	H
8	H	H	L	H
9	L	L	H	H

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	—	2.0	-	8.0	V
Input Voltage	V_{IN}	—	0	-	V_{DD}	V
Operating Temperature	T_{opr}	—	-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

CHARACTERISTIC	SYMBOL	TEST CONCITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High Level Output Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS}$	5	4.95	-	4.95		-	4.95	-	V
Low Level Output Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{DD}$	5	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current	I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS}$	5	-0.52	-	-0.44		-	-0.36	-	mA
Low Level Output Current	I_{OL}	V_{OL}=0.4V $V_{IN}=V_{DD}$	5	1.4	-	1.1		-	0.8	-	mA
High Level Input Voltage	V_{IH}	$\|I_{OUT}\|<1\mu A$ V_{OUT}=0.5V V_{OUT}=4.5V $V_{IN}=V_{SS},V_{DD}$	5	4.0	-	4.0		-	4.0	-	V
Low Level Input Voltage	V_{IL}		5	-	1.0	-		1.0	-	1.0	V
Input Current "H"Level	I_{IH}	V_{IH}=8.0	8	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L"Level	I_{IL}	V_{IL}=0.0V	8	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Supply Current	I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	12.5	-	10^{-3}	12.5	-	75	μA

* All valid input combinations.

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, V_{DD}=5V, C_L=15pF)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}		-	18	35	ns
Output Fall Time		t_{of}		-	15	30	ns
Propagation Delay Time	Low-High Level	t_{pLH}	CLCOK - Q	-	42	63	ns
	High-Low Level	t_{pHL}		-	36	54	ns
High-Low Level Propagation Delay Time		t_{pHL}	CLEAR - Q	-	36	54	ns
Maximum Clock Rise/Fall Time		$t_{r\phi}$ $t_{f\phi}$		1.0	100	-	μs
Minimum Clear Pulse Width		t_w		-	20	35	ns
Minimum Clear Removal Time		t_{rem}		-	10	20	ns
Maximum Clock Frequency		f_{MAX}		15	30	-	MHz
Input Capacitance		C_{IN}		-	5		

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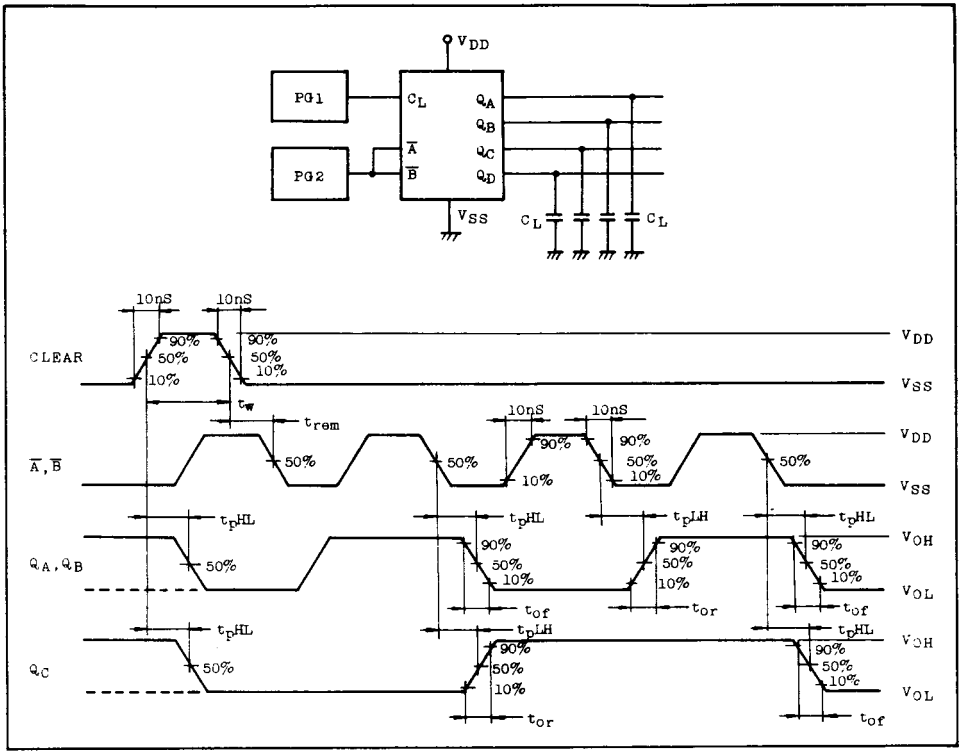
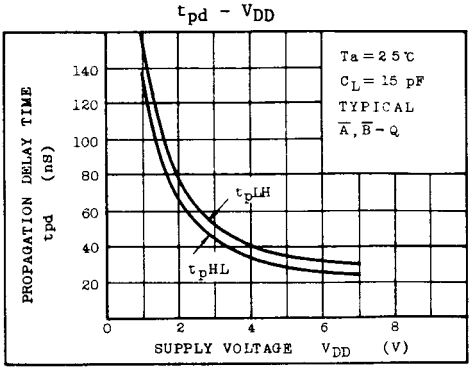
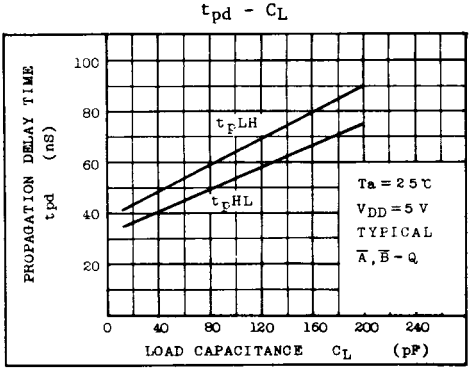
SWITCHING TIME TEST CIRCUIT AND WAVEFORM







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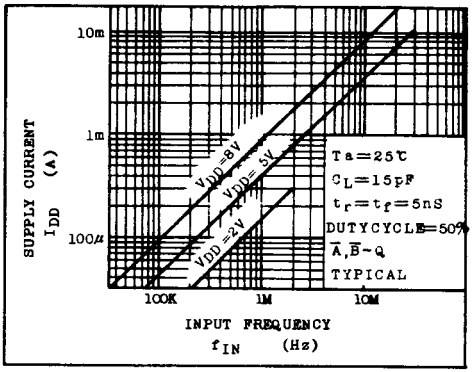
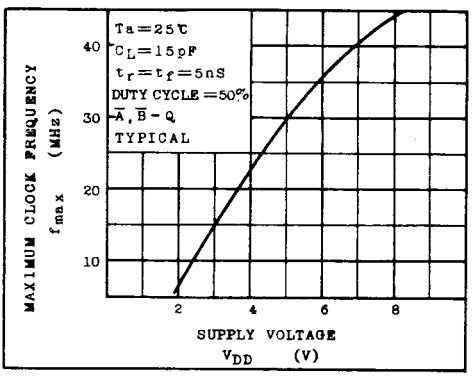
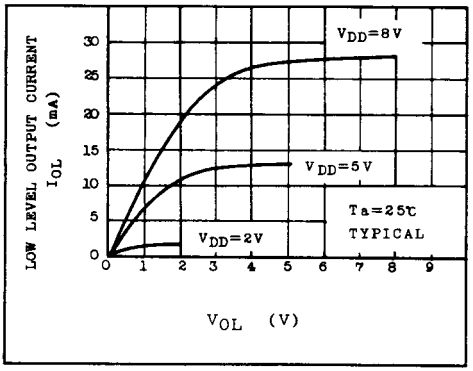
$I_{DD} - f_{IN}$



$f_{max} - V_{DD}$



$I_{OL} - V_{OL}$



$I_{OH} - (V_{DD} - V_{OH})$