

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC40H259P/F

TC40H259 8-BIT ADDRESSABLE LATCH

The TC40H259 is an 8-bit addressable latch having one common input line and eight independent output lines.

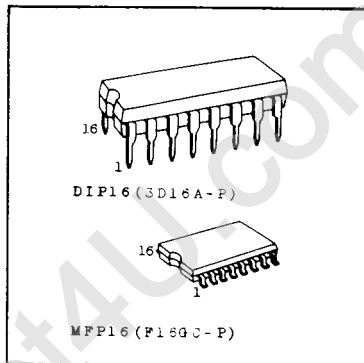
The respective bits are controlled by LATCH SELECT inputs (A, B and C).

When CLEAR input is at "H" level and ENABLE($\bar{G}$) input is at "L" level, the data is written into the bit selected by LATCH SELECT inputs (A, B and C). In this case, the other bits hold their previous conditions.

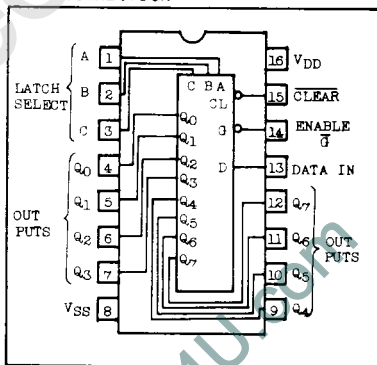
When both of CLEAR input and ENABLE($\bar{G}$) input go to "H" level, write of all bits is inhibited regardless of LATCH SELECT input, and their previous conditions are held.

When CLEAR input is set to "L" level and ENABLE($\bar{G}$) input is set to "H" level, all bits are reset to "L" level regardless of the other inputs.

The pin assignment and function of this latch are the same as those of the LSTTL 74LS259.



PIN CONNECTION



MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	V _{SS} -0.5 ~ V _{SS} +10	V
Input Voltage	V _{IN}	V _{SS} -0.5 ~ V _{DD} +0.5	V
Output Voltage	V _{OUT}	V _{SS} -0.5 ~ V _{DD} +0.5	V
Input Current	I _{IN}	±10	mA
Power Dissipation	P _D	300 (DIP) / 180 (MFP)	mW
Storage Temperature	T _{stg}	-65 ~ 150	°C
Lead Temp./Time	T _{sol}	260°C • 10 sec	

TRUTH TABLE

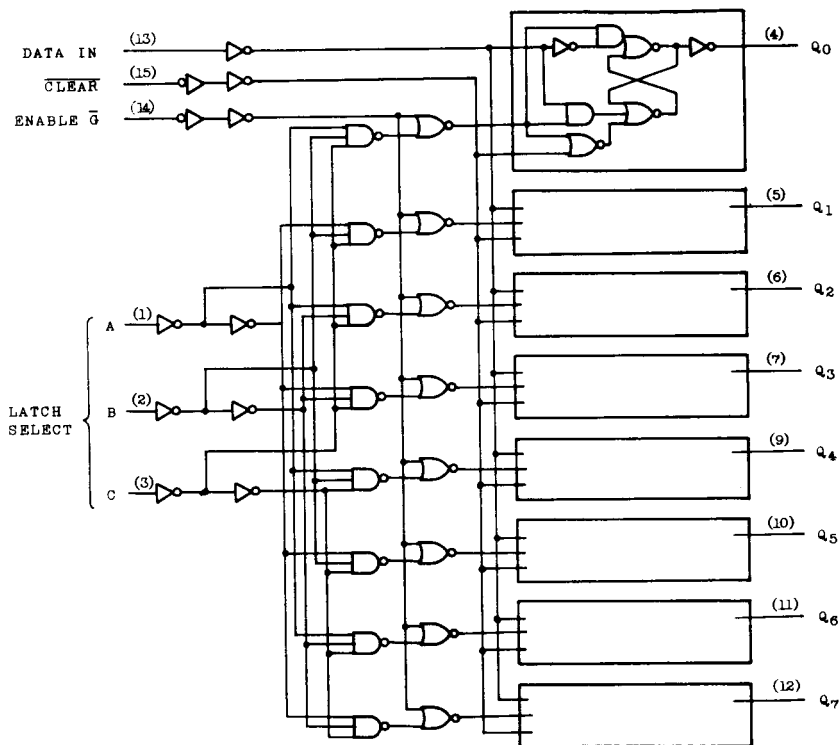
INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
CLEAR	G			
H	L	DATA IN	HOLD	ADDRESSABLE LATCH
H	H	HOLD	HOLD	MEMORY
L	L	DATA IN	L	8-LINE DEMULTIPLEXER
L	H	L	L	CLEAR

LATCH SELECTION

SELECT INPUTS			LATCH ADDRESSED
A	B	C	
L	L	L	Q ₀
H	L	L	Q ₁
L	H	L	Q ₂
H	H	L	Q ₃
L	L	H	Q ₄
H	L	H	Q ₅
L	H	H	Q ₆
H	H	H	Q ₇

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BLOCK DIAGRAM



* ALL INPUTS ARE EQUIPPED WITH PROTECTION CIRCUIT.

RECOMMENDED OPERATING CONDITIONS ($V_{SS}=0.0V$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	-	2.0	-	8.0	V
Input Voltage	V_{IN}	-	0	-	V_{DD}	V
Operating Temperature	T_{opr}	-	-40	-	85	°C

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ELECTRICAL CHARACTERISTICS ($V_{SS} = 0.0V$)

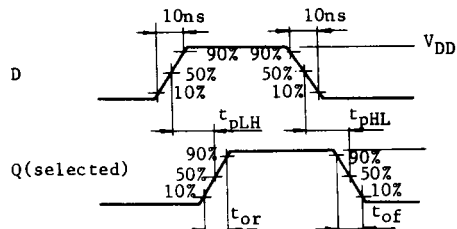
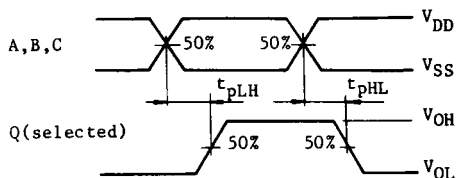
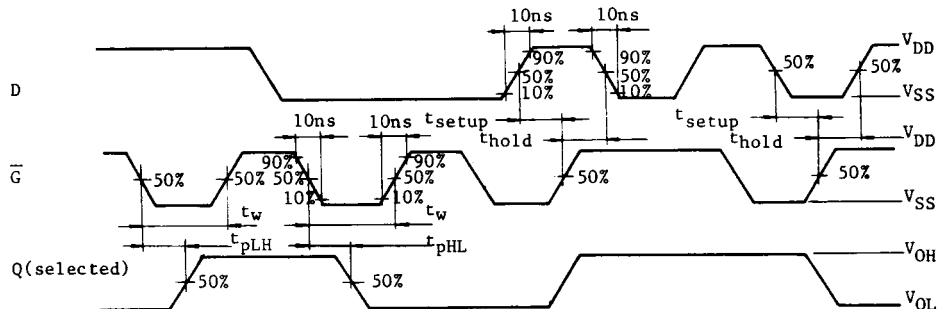
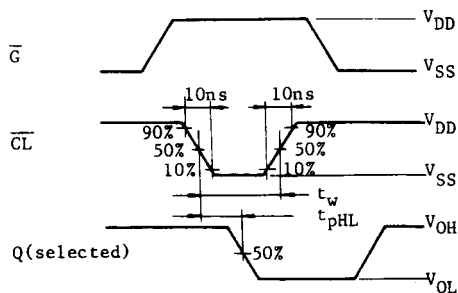
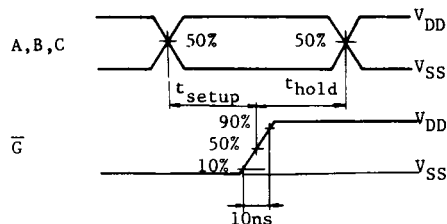
CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$ I_{OUT} < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$ I_{OUT} < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	-	0.05	-	0.0	0.05	-	0.05	
High Level Output Current		I_{OH}	$V_{OH} = 4.6V$ $V_{IN} = V_{SS}, V_{DD}$	5	-0.52	-	-0.44	-	-	-0.36	-	mA
Low Level Output Current		I_{OL}	$V_{OL} = 0.4V$ $V_{IN} = V_{SS}, V_{DD}$	5	1.4	-	1.1	-	-	0.8	-	
Input Voltage	"H" Level	V_{IH}	$ I_{OUT} < 1\mu A$ $V_{OUT} = 0.5V$ $V_{OUT} = 4.5V$	5	4.0	-	4.0	-	-	4.0	-	V
	"L" Level	V_{IL}		5	-	1.0	-	-	1.0	-	1.0	
Input Current	"H" Level	I_{IH}	$V_{IH} = 8.0V$	8	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"L" Level	I_{IL}	$V_{IL} = 0.0V$	8	-	-0.3	-	10^{-5}	-0.3	-	-1.0	
Quiescent Supply Current		I_{DD}	$*V_{IN} = V_{SS}, V_{VV}$	5	-	12.5	-	10^{-3}	12.5	-	75	μA

SWITCHING CHARACTERISTICS ($T_a = 25^\circ C$, $V_{SS} = 0V$, $V_{DD} = 5V$, $C_L = 15pF$)

CHARACTERISTICS		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}	Fig.1	-	20	40	ns
Output Fall Time		t_{of}		-	18	36	
Propagation Delay Time	Low-High	t_{pLH}	DATA - Q	Fig.1	-	42	ns
	High-Low	t_{pHL}			-	53	
Propagation Delay Time	Low-High	t_{pLH}	SELECT-Q	Fig.2	-	43	ns
	High-Low	t_{pHL}			-	64	
Propagation Delay Time	Low-High	t_{pLH}	ENABLE-Q	Fig.3	-	42	ns
	High-Low	t_{pHL}			-	53	
	High-Low	t_{pHL}	CLEAR-Q	Fig.4	-	48	ns
Minimum Clear Pulse Width		t_w	CLEAR	Fig.4	-	20	ns
Minimum Enable Pulse Width		t_w	ENABLE	Fig.3	-	20	ns
Min. Data Setup Time		t_{set-up}	ENA-DATA	Fig.3	-	30	ns
Min. Data Setup Time		t_{set-up}	SELECT-ENA	Fig.5	-	10	ns
Min. Data Hold Time		t_{hold}	ENA-DATA	Fig.3	-	10	ns
Min. Data Hold Time		t_{hold}	SELECT-ENA	Fig.5	-	10	ns
Input Capacitance		C_{IN}			-	5	pF

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SWITCHING TIME TEST WAVEFORM

CIRCUIT 1. ($\overline{G}=L$, $\overline{CL}=H$, $A^{\wedge}C=STABLE$)CIRCUIT 2. ($\overline{G}=L$, $\overline{CL}=L$, $D=H$)CIRCUIT 3. ($\overline{CL}=H$, $A^{\wedge}C=STABLE$)CIRCUIT 4. ($D=H$, $A^{\wedge}C=STABLE$)CIRCUIT 5. ($\overline{CL}=H$)

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