TC40H194P/F

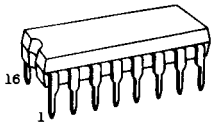
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC40H194 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

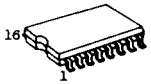
The TC40H194 is a 4-bit bidirectional bit register, which permits right shift (in the direction from Q_A to Q_D) and left shift (in the direction from Q_D to Q_A) operations.

When CLEAR terminal is set to "L" level, output goes to "L" level regardless of other inputs. All the other operations synchronize with the rising edge of CLOCK.

The function and pin assignment of this register are the same as those of the TTL74194 and the LSTTL74LS194.



DIP16(3D16A-P)

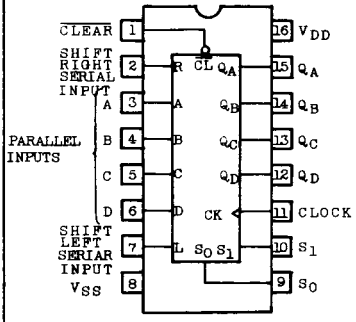


MFP16(F16GC-P)

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5 ∿ V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5 ∿ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ∿ V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Storage Temperature	Tstg	-65 ∿ 150	°C
Lead Temp./Time	Tsol	260°C • 10 sec	

PIN CONNECTION



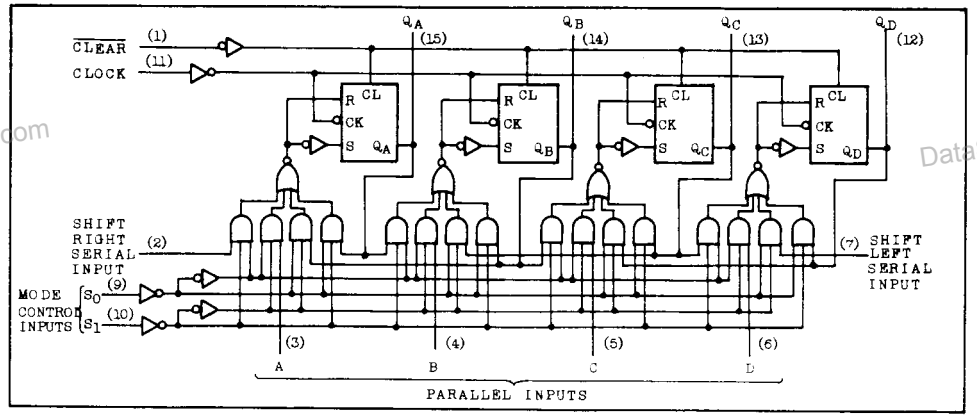
TRUTH TABLE

INPUTS										OUTPUTS			
CLEAR	MODE S_I	MODE S_O	CLOCK	SERIAL LEFT	SERIAL LIGHT	PARALLEL A	PARALLEL B	PARALLEL C	PARALLEL D	Q_A	Q_B	Q_C	Q_D
L	*	*	*	*	*	*	*	*	*	L	L	L	L
H	*	*	H	*	*	*	*	*	*	No Change			
H	H	H	↑	*	*	a	b	c	d	a	b	c	d
H	L	H	↑	*	H	*	*	*	*	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	*	L	*	*	*	*	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	*	*	*	*	*	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	*	*	*	*	*	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	*	*	*	*	*	*	*	No Change			

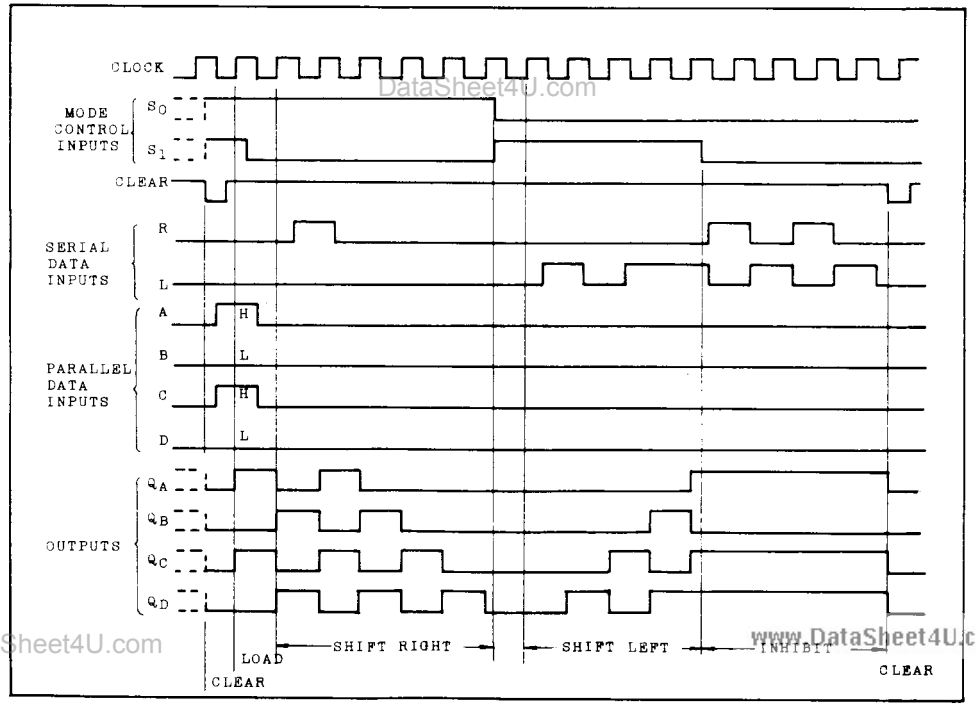
*=Don't Care

TC40H194P/F

BLOCK DIAGRAM



TIMING CHART



TC40H194P/F

RECOMMENDED OPERATING CONDITION (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	MAX.	MIN.	TYPE
Supply Voltage	V_{DD}	—	2.0	-	8.0	V
Input Voltage	V_{IN}	—	0	-	V_{DD}	V
Operating Temperature	T_{opr}	—	-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

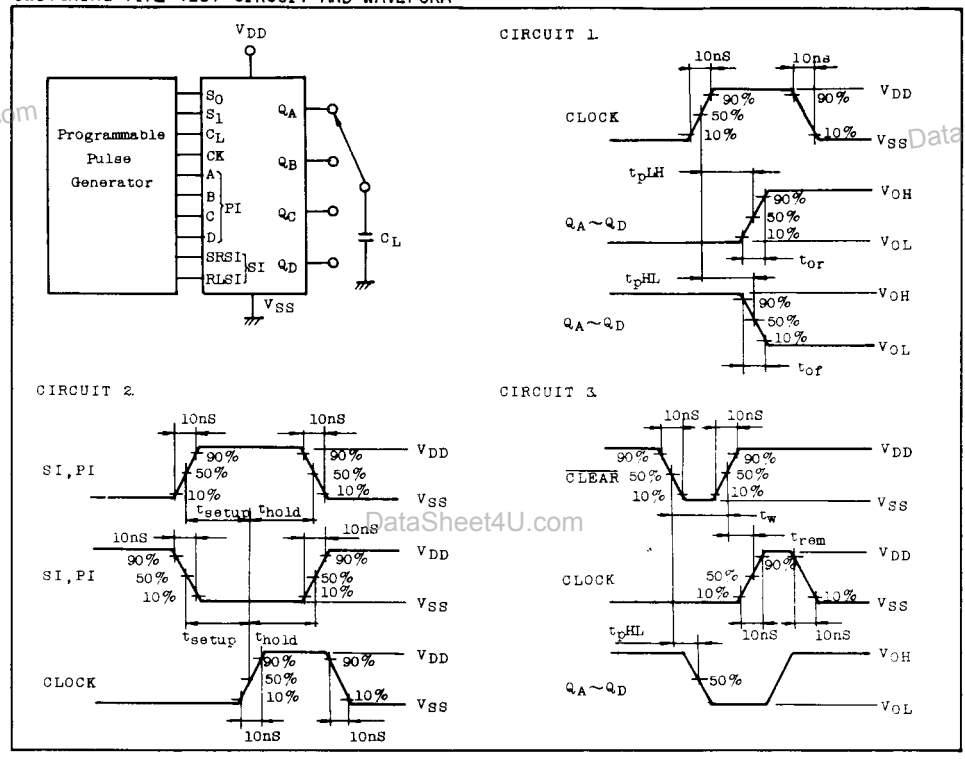
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA V_{IN}=V_{SS},V_{DD}	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA V_{IN}=V_{SS},V_{DD}	5	-	0.05	-	0.0	0.05		0.05	V
High Level Output Current	I_{OH}	V_{OH}=4.6V V_{IN}=V_{SS},V_{DD}	5	-0.52	-	-0.44		-	-0.36	-	mA
Low Level Output Current	I_{OL}	V_{OL}=0.4V V_{IN}=V_{SS},V_{DD}	5	1.4	-	1.1		-	0.8	-	mA
Input Voltage "H" Level	V_{IH}	$\|I_{OUT}\|$<1μA V_{OUT}=0.5V	5	4.0	-	4.0		-	4.0	-	V
Input Voltage "L" Level	V_{IL}	V_{OUT}=4.5V	5	-	1.0	-		1.0	-	1.0	V
Input Current "H"Level	I_{IH}	V_{IH}=8.0V	8	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L"Level	I_{IL}	V_{IL}=0.0V	8	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Supply Current	I_{DD}	*V_{IN}=V_{SS},V_{DD}	5	-	12.5	-	10^{-3}	12.5	-	75	μA

* All valid input combinations.

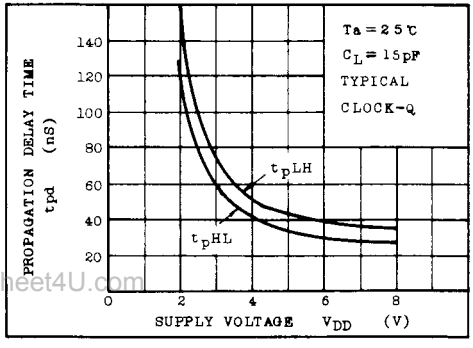
SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0.0V, V_{DD}=5V, C =15pF)

CHARACTERISTIC		SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}		Fig.1	-	21	40	ns
Output Fall Time		t_{of}		Fig.1	-	14	30	ns
Propagation Delay Time	Low-High	t_{pLH}	CLOCK-Q	Fig.1	-	43	65	ns
	High-Low	t_{pHL}	CLOCK-Q	Fig.1	-	34	52	ns
	High-Low	t_{pHL}	CLEAR-Q	Fig.3	-	35	52	ns
Minimum Clear Pulse Width		t_w	CLEAR	Fig.3	-	16	28	ns
Maximum Clock Frequency		$f_{MAX\phi}$			10	20	-	MHz
Maximum Clock Rise/Fall Time		$t_{r\phi}$,$t_{f\phi}$			1.0	20	-	μs
Minimum Clear Removal Time		t_{rem}		Fig.3	-	15	28	ns
Minimum Set-up Time		t_{set-up}	SI,PI	Fig.2	-	-	45	ns
Minimum Hold Time		t_{hold}		Fig.2	-	0	-	ns
Input Capacitance		C_{IN}			-	5		

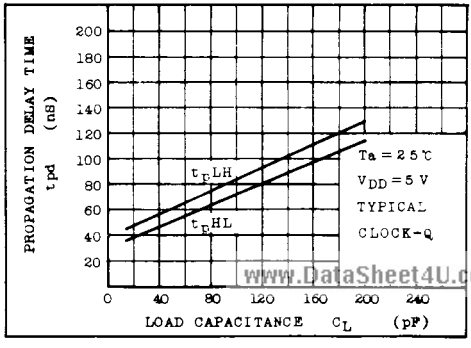
SWITCHING TIME TEST CIRCUIT AND WAVEFORM



t_{pd} - V_{DD}

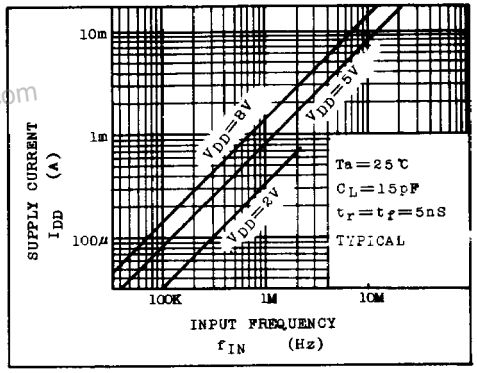


t_{pd} - C_L

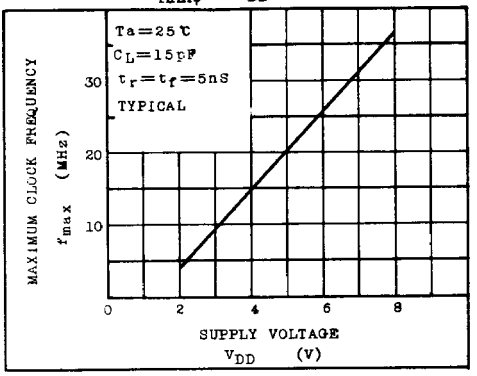


TC40H194P/F

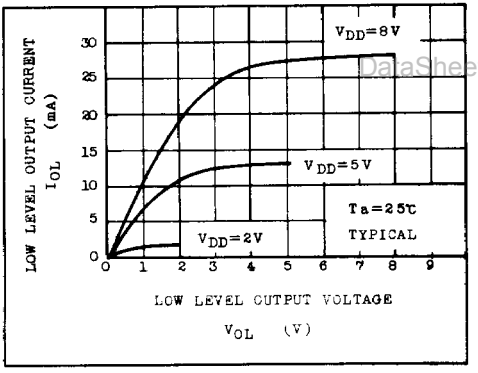
I_{DD} - f_{IN}



$f_{MAX\phi}$ - V_{DD}



I_{OL} - V_{OL}



I_{OH} - (V_{DD} - V_{OH})