C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

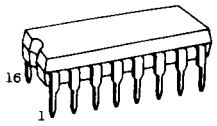
TC40H175P/F

TC40H175 QUAD D-TYPE FLIP-FLOP

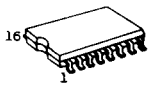
The TC40H175 is a quad D-type flip-flop having common CLOCK and common $\overline{CLEAR}$ input.

The logical input applied to data input is transmitted to outputs Q and $\overline{Q}$ at the rising edge of CLOCK input.

When $\overline{CLEAR}$ input is set to "L" level, output Q goes to "L" level and output $\overline{Q}$ to "H" level, respectively.



DIP16(3D16A-P)

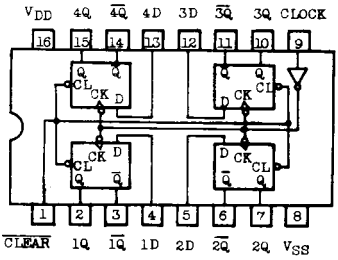


MFP16(F16GC-P)

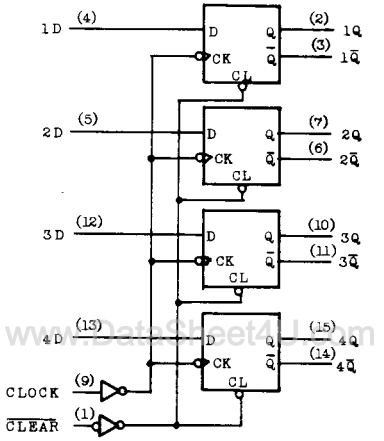
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5 ∿ V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5 ∿ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ∿ V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temp./Time	Tsol	260°C · 10 sec	

PIN CONNECTION



LOGIC DIAGRAM



※ ALL INPUTS ARE EQUIPPED WITH PROTECTION CIRCUIT.

TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{CLEAR}$	CLOCK	DATA	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	↓	X	No Change	

X = Don't Care

TC40H175P/F

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	–	2.0	–	8.0	V
Input Voltage	V_{IN}	–	0	–	V_{DD}	V
Operating Temperature	T_{opr}	–	-40	–	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

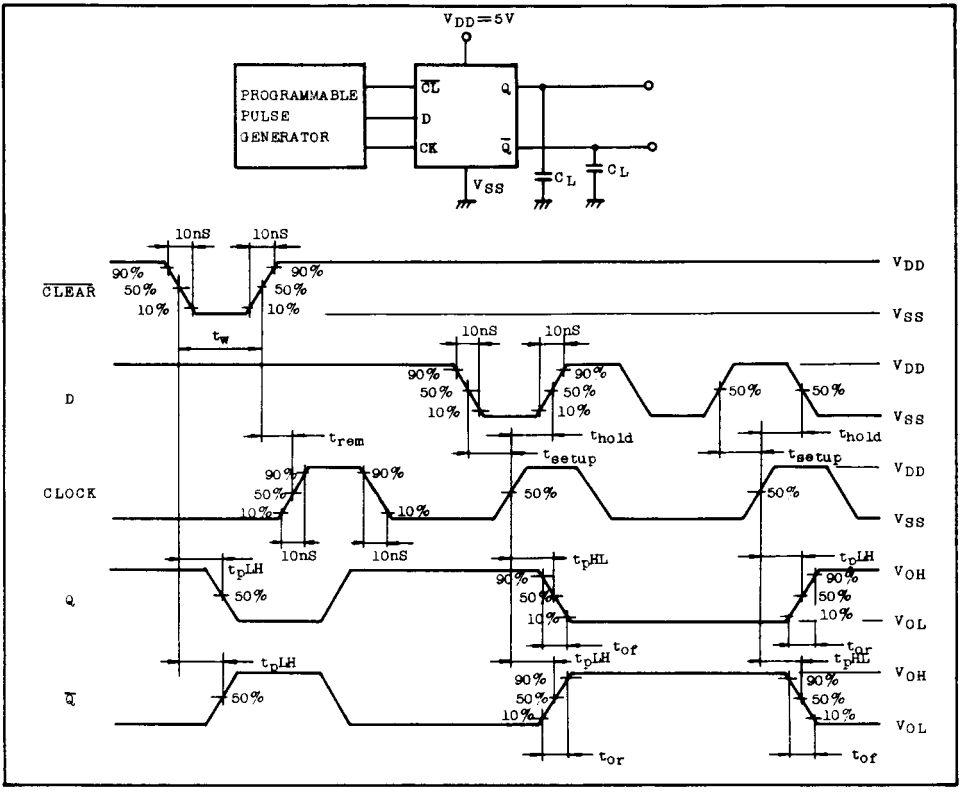
CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\|$<1μA V_{IN}=V_{SS}, V_{DD}	5	4.95	–	4.95	5.0	–	4.95	–	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\|$<1μA V_{IN}=V_{SS}, V_{DD}	5	–	0.05	–	0.0	0.05	–	0.05	
High Level Output Current		I_{OH}	V_{OH}=4.6V V_{IN}=V_{SS}, V_{DD}	5	-0.52	–	-0.44		–	-0.36	–	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V V_{IN}=V_{SS}, V_{DD}	5	1.4	–	1.1		–	0.8	–	
Input Voltage	"H" Level	V_{IH}	$\|I_{OUT}\|$<1μA V_{OUT}=0.5V V_{OUT}=4.5V	5	4.0	–	4.0		–	4.0	–	V
	"L" Level	V_{IL}		5	–	1.0	–		1.0	–	1.0	
Input Current	"H" Level	I_{IH}	V_{IH}=8.0V	8	–	0.3	–	10^{-5}	0.3	–	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0.0V	8	–	-0.3	–	-10^{-5}	-0.3	–	-1.0	
Quiescent Supply Current		I_{DD}	*V_{IN}=V_{SS}, V_{DD}	5	–	12.5	–	10^{-3}	12.5	–	75	μA

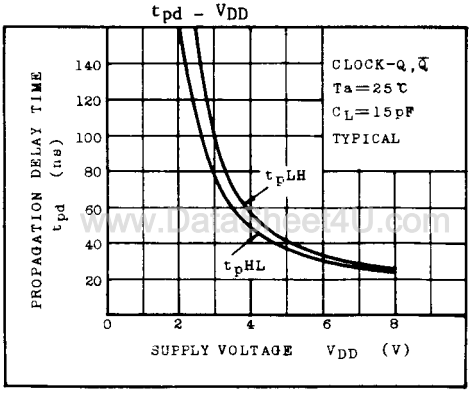
*All valid input combinations.

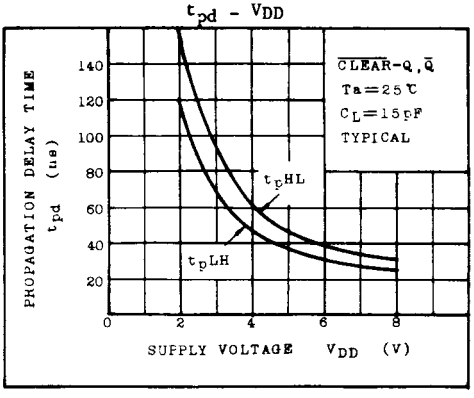
SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0.0V, C_L=15pF)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}		5	–	18	35	ns
Output Fall Time		t_{of}		5	–	17	30	
Propagation Delay Time	(Low-High)	t_{pLH}	CLOCK - Q, $\overline{Q}$	5	–	42	63	ns
	(High-Low)	t_{pHL}		5	–	38	57	
	(Low-High)	t_{pLH}	$\overline{CLEAR}$ - Q, $\overline{Q}$	5	–	35	53	
	(High-Low)	t_{pHL}		5	–	45	68	
Min. Width of Pulse		t_w	$\overline{CLEAR}$	5	–	13	24	ns
Max. Clock Rise Time / Fall Time		$t_{r\phi}$ $t_{f\phi}$		5	1.0	7.0	–	μs
Min. Data Hold Time		t_{hold}		5	–	–	5	ns
Min. Data Setup Time		t_{set-up}	D-CLOCK	5		–	25	ns
Input Capacitance		C_{IN}			–	5	–	pF
Max. Clock Frequency		$f_{MAX\phi}$		5	10	20	–	MHz
Min. Clear Removal Time		t_{rem}		5		17	25	ns

SWTITCHING TIME TEST CIRCUIT AND WAVEFORM

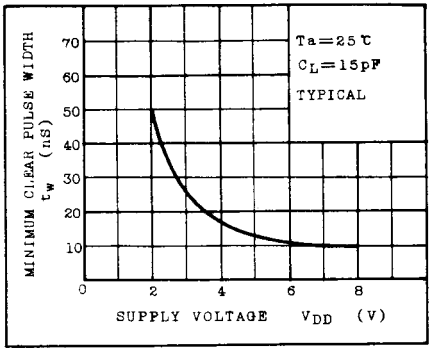




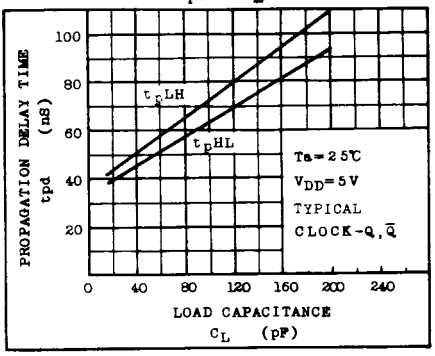


TC40H175P/F

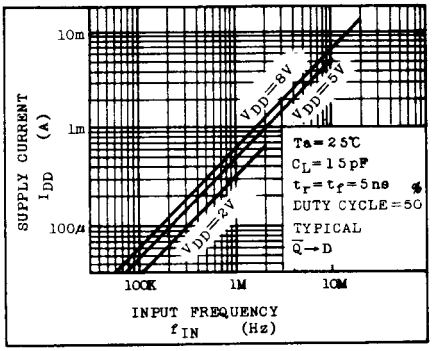
t_w - V_{DD}



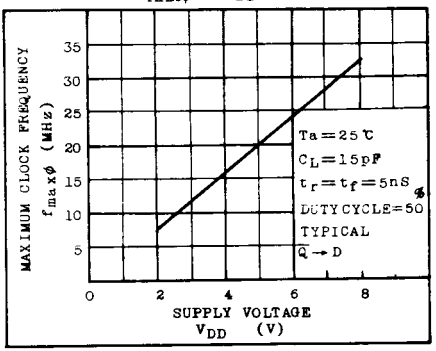
t_{pd} - C_L



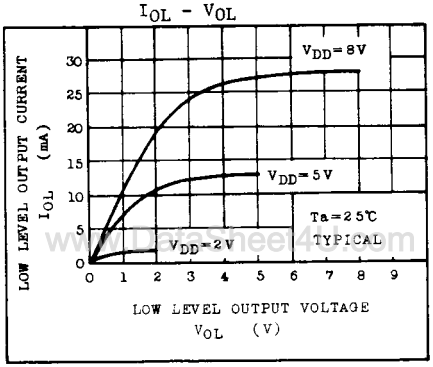
I_{DD} - f_{IN}



$f_{MAX\phi}$ - V_{DD}



I_{OL} - V_{OL}



I_{OH} - (V_{DD} - V_{OH})