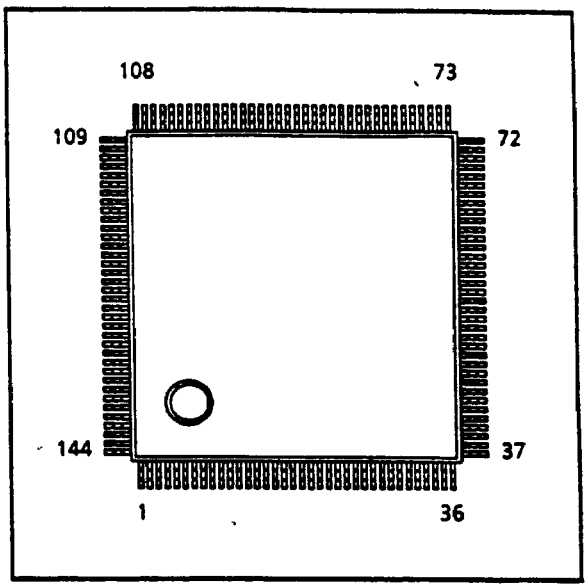
TC35108F
(9600bps MODEM PROCESSOR)

1. GENERAL DESCRIPTION

The TOSHIBA TC35108F is a 9600 bit per second facsimile modem processor. The half duplex modem required for facsimile use is composed by TC35108F and TC35103F. The TC35103F is an Analog Front End LSI (AFE) including ADC, DAC, PGA, Programmable Attenuator and filters. The AFE can be controlled via the modem processor. The modem satisfies the telecommunication requirement specified in CCITT recommendations V.29, V.27ter, T.30, T.4 and T.3. The modem is capable of framing/deframing HDLC (High level Data Link Control) which is required in T.30 binary procedure and T.30A Error Correction Mode (ECM). The TC35108F is designed for use in Group 3 and Group 2 facsimile machines.



2. FEATURES

- ☐ Half-Duplex
- ☐ CCITT V.29, V.27ter, V.21 Channel 2, Group 2
- ☐ HDLC framing/deframing
- ☐ DTMF dialing
- ☐ Programmable tone Generation and Detection
- ☐ Equalization
  - Automatic Adaptive (V.29,V.27ter)
  - Compromise cable (TC35103F)
  - Compromise link (TC35103F)
- ☐ DTE interface
  - Microprocessor bus
  - CCITT V.24 (RS-232-C Compatible)
- ☐ CMOS low power

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TOSHIBA CORPORATION

3. SYSTEM OVERVIEW

3.1 HARDWARE INTERFACE

The functional interconnection diagram (FIG 3.1) shows typical modem connection in a facsimile. The TC35108F has a CCITT V.24 compatible serial interface and 16 words of addressing space. The serial interface is provided for optional USRT. However, the facsimile system seldom needs USRT. Because, the modem provides similar function to USRT such as HDLC framing/deframing and parallel data interface using microprocessor bus.

The TC35108F can generate interrupt signal according to specified condition. This feature allows easy programming in T.30 procedure.

The EYE pattern is a monitor output in Group 3 configurations. The signal quality and modem circuitry performance such as SNR, can be evaluated by observing the EYE pattern. The TC35108F outputs EYE pattern signals by serial digital stream. This digital data must be converted to parallel form by an external shift register and then to analog form by two digital to analog converters (DAC). For display the pattern on the oscilloscope, connect these outputs to X axis and Y axis input respectively.

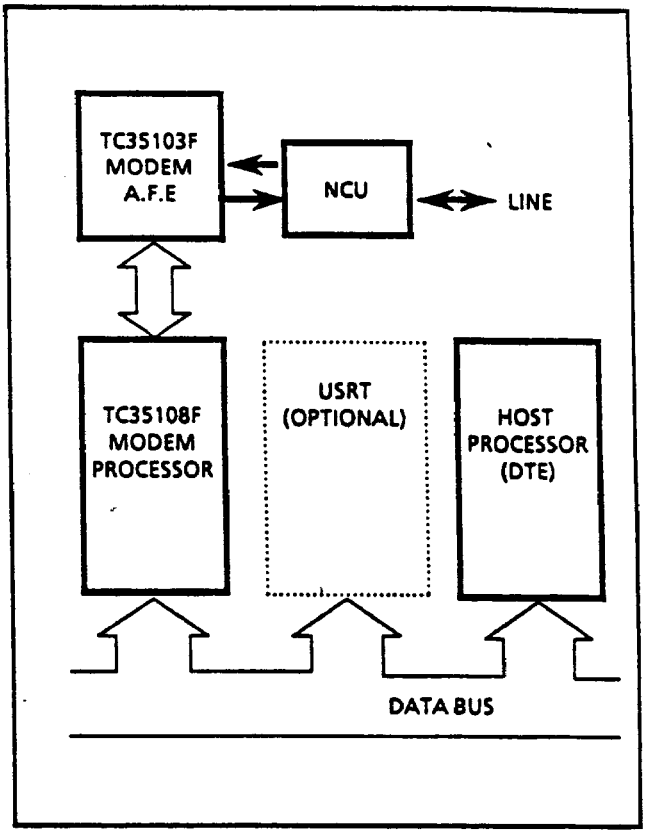


FIG 3.1
TYPICAL MODEM CONNECTION

3.1.1 AFE CONTROL

The TC35108F has a TC35103F control port controlled by its interface register. The AFE function such as Mute, Fixed equalization, and Programmable attenuation becomes available if the TC35103F is being installed.

3.1.2 PARALLEL INTERFACE

The modem via microprocessor bus. The modem has both parallel and serial interface including Request To Send (-RTS) control. Also, the modem provides -DREQ and -DACK terminals for DMA control.

3.2 SOFTWARE FEATURES

The TC35108F communicates with host processor through 16words×8bit of interface registers. The register map is shown in table 3.2. To keep compatibility with the TC35107F modem processor, register bit map assignment and configuration code are similar to the TC35107F. Since the TC35108F is enhanced modem processor based upon the TC35107F, controller program will easily be converted.
In addition to the default operation, the TC35108F enables coefficients writing in parallel form. Coefficients are valid in use of tone detection or tone generation.

3.2.1 CONFIGURATIONS

Table 3.2.1 shows selectable modem configuration. SETUP bit enables and disables configuration instead of hardware reset. Therefore, the TC35108F does not require -RST control while set up operation. The I/O port for modem -RST control will be reduced.

3.2.2 HDLC

Binary procedure in T.30 is performed by HDLC based data format. Also, T.30 Annex says Error Correction Mode (ECM) at high speed data transferring. In this optional mode, message data is framed by HDLC format. The TC35108F has framing and deframing capability at any speed. TOSHIBA TC35108F Application note describes detail.

3.2.3 TONE GENERATION

The TC35108F supports specified single tone generation for tonal procedure. Just writing a byte of code into configuration register, the modem begins to send single tone such as CED, GC, GI. DTMF generate function is convenient not only dialing but also certain applications. No longer the facsimile machine needs DTMF dialer IC.
The DTMF frequencies and output level are user programmable. Therefore, the TC35108F is capable of tuning its DTMF level to different countries specifications without external circuits. This feature also allows melody generation by the host program.

3.2.4 TONE DETECTION

Group 2 facsimile performs its procedure by tones. The TC35108F scans 4 frequencies in Group 2 configuration. This detection result is output to interface register by 4 bit.

TABLE 3.2 WRITE REGISTER MAP

ADDR	BIT CONTENTS								MNEMONIC
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
0H	CONF7	CONF6	CONF5	CONF4	CONF3	CONF2	CONF1	CONF0	CONF
1H	POL	CB	EQH	LPFS	AGCS1	AGCS0	FCDS1	FCDS0	ACR1
2H	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0	TXR
3H	0	0	SETUP	HALC	HDLC	LAGC	PDM	DEL	ACR2
4H	0	0	0	0	0	RSP	CLAMP	MARK	ACR3
5H	IM7	IM6	IM5	IM4	IM3	IM2	IM1	IM0	IMR
6H	MUTE	LEQL	CEQL2	CEQL1	ATT3	ATT2	ATT1	ATT0	AFER
7H	-	-	-	-	-	-	-	-	RESERVED
8H	CACC	CWR	0	0	0	0	0	0	ACR4
9H	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	CAR
AH	CD07	CD06	CD05	CD04	CD03	CD02	CD01	CD00	CDRL
BH	CD15	CD14	CD13	CD12	CD11	CD10	CD09	CD08	CDRM
CH	-	-	-	-	-	-	-	-	RESERVED
DH	-	-	-	-	-	-	-	-	RESERVED
EH	-	-	-	-	-	-	-	-	RESERVED
FH	-	-	-	-	-	-	-	-	RESERVED

SYMBOL DESCRIPTIONS

[0] This bit must be set to a zero. (Default value is also 0.)

[-] Reserved bit. Currently, writing has no meanings.

TABLE 3.2 (CONTINUED) READ REGISTER MAP

ADDR	BIT CONTENTS								MNEMONIC
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
0H	TX	CTS	SQD	G2POL	DCD	PN	P2	FCD	MSR
1H	-	-	-	-	-	-	-	-	
2H	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0	RXR
3H	0	0	AGC5	AGC4	AGC3	AGC2	AGC1	AGC0	AGCR
4H	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0	BCR
5H	CD	PN	EOFT	BOFR	EOFR	FABT	CRCER	DREQ	ITFR
6H	MUTE	LEQL	CEQL2	CEQL1	ATT3	ATT2	ATT1	ATT0	AFER
7H	-	-	-	-	-	-	-	-	RESERVED
8H	CACD	CWRD	0	0	0	HITP	GHIT	DET21	ESR1
9H	0	0	0	0	FR3	FR2	FR1	FR0	ESR2
AH	CD07	CD06	CD05	CD04	CD03	CD02	CD01	CD00	CDRL
BH	CD15	CD14	CD13	CD12	CD11	CD10	CD09	CD08	CDRM
CH	-	-	-	-	-	-	-	-	RESERVED
DH	-	-	-	-	-	-	-	-	RESERVED
EH	-	-	-	-	-	-	-	-	RESERVED
FH	-	-	-	-	-	-	-	-	RESERVED

TABLE 3.2.1 CONFIGURATION

GROUP 3 CONFIG.	BIT RATE (BPS)	ECHO PROTECT TONE TRAINING EXECUTION	CONFIG. CODE (HEX)	CB
V.29	9600	NO PROTECTION TRAINING ENABLE	C8H	1
		195ms CARRIER TRAINING DISABLE	C9H	
	7200	NO PROTECTION TRAINING ENABLE	CAH	
		195ms CARRIER TRAINING DISABLE	CBH	
	4800	NO PROTECTION TRAINING ENABLE	CCH	
		195ms CARRIER TRAINING DISABLE	CDH	
V.27ter LONG TRAINING	4800	NO PROTECTION TRAINING ENABLE	C0H	
		195ms CARRIER TRAINING DISABLE	C1H	
	2400	NO PROTECTION TRAINING ENABLE	C4H	
		195ms CARRIER TRAINING DISABLE	C5H	
V.27ter SHORT TRAINING	4800	NO PROTECTION TRAINING ENABLE	C2H	
		195ms CARRIER TRAINING DISABLE	C3H	
	2400	NO PROTECTION TRAINING ENABLE	C6H	
		195ms CARRIER TRAINING DISABLE	C7H	
V.21 (Channel 2)	300	NO PROTECTION NO TRAINING	E8H	

NOTE:

CB is an extension bit of CONF register. This bit is assigned to bit 6 of ACR1.

According to CCITT Recommendation T.4, facsimile performs picture transferring by V.27ter with Echo Protection. T4 does not describes echo protection in case of V.29.

V.27ter short training is not a standard modulation scheme of Group 3 facsimile. However, this configuration can be used as Non Standard Facilities (NSF) which is specified by facsimile manufacturer. The modem is capable of communicating by short training, if the Training Check (TCF) was successfully done by V.27ter long training.

TABLE 3.2.1 (CONTINUED)

CCITT REC.	CONFIGURATION CODE (HEX)	CB
GROUP 2	D0H	0

TABLE 3.2.1 (CONTINUED)

TONE (Hz)	CONFIGURATION CODE (HEX)	CB
462	F0H	0
540	F1H	0
1080	F2H	0
1100	F3H	0
1250	F4H	0
1300	F5H	0
1500	F6H	0
1650	F7H	0
1700	F8H	0
1800	F9H	0
1850	FAH	0
1900	FBH	0
2100	FCH	0
2400	FDH	0
3240	FEH	0
1600	FFH	0

NOTE:

Once the tone code was set to CONF register, the modem begins to transmit single tone regardless of RTS (Request To Send) status.

TABLE 3.2.1 (CONTINUED)

DTMF FREQ(HZ)		CONFIGURATION CODE(HEX)	CB
HIGH GROUP	LOW GROUP		
1209	697	70H	0
1209	770	71H	0
1209	852	72H	0
1209	941	73H	0
1336	697	74H	0
1336	770	75H	0
1336	852	76H	0
1336	941	77H	0
1477	697	78H	0
1477	770	79H	0
1477	852	7AH	0
1477	941	7BH	0
1633	697	7CH	0
1633	770	7DH	0
1633	852	7EH	0
1633	941	7FH	0

NOTE:

Once the DTMF code was set to CONF register, the modem begins to transmit DTMF regardless of the RTS (Request To Send) status.

Configuration code "30H (CB = 0)" is a NOP(Non Operation) code. The modem keeps silence when the code was set.

4 PIN DESCRIPTION

Signal names and descriptions of the TC35108F are listed in table 4.1. The signal names which begin with dash (-) are active low signals.

TABLE 4

PIN NAME	No.	I/O	DESCRIPTIONS
			MICROPROCESSOR INTERFACE
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7	34 33 30 29 28 27 26 25	IN/OUT	DATA BUS
A0 A1 A2 A3	125 124 123 122	IN IN IN IN	ADDRESS BUS
-CE -RD -WR	39 42 43	IN IN IN	CHIP ENABLE READ SIGNAL WRITE SIGNAL
-RST	47	IN	SYSTEM RESET
-INT -DREQ -DACK	41 120 121	OUT OUT IN	INTERRUPT DATA REQUEST (DMA INTERFACE) DATA ACKNOWLEDGE (DMA INTERFACE)
			CCITT V.24 COMPATIBLE INTERFACE
-RTS -CTS -DCD TXD RXD DTCK	46 50 51 49 52 53	IN OUT OUT IN OUT OUT	REQUEST TO SEND CLEAR TO SEND DATA CARRIER DETECT TRANSMISSION DATA RECEPTION DATA DATA CLOCK
			DIAGNOSTIC INTERFACE
EYESYC EYEDAT EYECLK	87 88 114	OUT* OUT IN	EYE PATTERN SYNCHRONIZATION (OPEN DRAIN) EYE PATTERN DATA EYE PATTERN CLOCK (CONNECT TO ADCK)

TABLE 4 (CONTINUED)

PIN NAME	No.	I/O	DESCRIPTIONS
			ANALOG FRONT END INTERFACE
ATT0	137	OUT	ATTENUATOR CONTROL 0
ATT1	136	OUT	ATTENUATOR CONTROL 1
ATT2	134	OUT	ATTENUATOR CONTROL 2
ATT3	133	OUT	ATTENUATOR CONTROL 3
CEQL1	132	OUT	CABLE EQUALIZER CONTROL 1
CEQL2	131	OUT	CABLE EQUALIZER CONTROL 2
LEQL	130	OUT	LINK EQUALIZER CONTROL
MUTE	129	OUT	MUTE CONTROL
SC	59	OUT	A/D START CONVERSION TRIGGER
ADCK	58	OUT	A/D CONVERSION CLOCK
BCTCK	40	IN	DIGITIZED WAVE SIGNAL
-AFIE	20	IN	AFE DATA INPUT ENABLE
AFDI	21	IN	AFE DATA INPUT
-AFOE	23	OUT*	AFE DATA OUTPUT ENABLE (OPEN DRAIN)
AFDO	22	OUT	AFE DATA OUTPUT
			CLOCK INPUT
CLK	IN	17	MASTER CLOCK (6.2208MHz)
			CLOSED CONNECTIONS
-RSTO	45	OUT	MODEM PROCESSOR RESET CONTROL
-MPRST	92	IN	MODEM PROCESSOR RESET (CONNECT TO RSTO)
AFICK	89	IN	AFE INPUT CLOCK (CONNECT TO ADCK)
AFOCK	140	IN	AFE OUTPUT CLOCK (CONNECT TO ADCK)
GBANK	85	OUT	CONNECT TO IBANK
IBANK	86	IN	CONNECT TO GBANK
GD0	83		
GD1	82		
GD2	81		INTERNAL BUS G
GD3	80	IN/OUT	INTERNAL BUS A,B, AND G MUST BE CONNECTED
GD4	77		BY EACH BIT.
GD5	76		
GD6	75		
GD7	71		

TABLE 4 (CONTINUED)

PIN NAME	No.	I/O	DESCRIPTIONS
			CLOSED CONNECTIONS
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7	6 7 10 11 12 13 14 15	IN/OUT	INTERNAL BUS A INTERNAL BUS A,B, AND G MUST BE CONNECTED BY EACH BIT.
PB0 PB1 PB2 PB3 PB4 PB5 PB6 PB7	104 103 100 99 98 97 96 95	IN/OUT	INTERNAL BUS B INTERNAL BUS A,B, AND G MUST BE CONNECTED BY EACH BIT.
-APDI -GPDI1	5 64	IN OUT	CONNECT EACH OTHER
-APDO -GPDO1	4 63	IN OUT	CONNECT EACH OTHER
-BPDI -GPDI2	105 68	IN OUT	CONNECT EACH OTHER
-BPDO -GPDO2	106 67	IN OUT	CONNECT EACH OTHER
-SES GFS	94 69	IN OUT	CONNECT EACH OTHER
GREQ AP1	70 143	IN OUT	CONNECT EACH OTHER
			CLAMP PINS
-TEST GTEST TESTAK -TESTAG	93 38 110 117	IN IN IN IN	CONNECT TO VDD CONNECT TO GND CONNECT TO VDD CONNECT TO VDD

5 FUNCTIONAL DESCRIPTION

5.1 REGISTERS

The TC35108F has 21 of user accessible registers. Since they have single port structure, two registers are located at same address. These different two registers are represented as WRITE REGISTER and READ REGISTER in this document. The bit location is represented using following format.

FORMAT:	[W/R : ADDRESS : BIT]
W/R	W (Write) or R (Read)
ADDRESS	0 to F (Hex-Decimal)
BIT	0 (LSB) to 7 (MSB)

EXAMPLE:

SETUP bit is located at bit 5 of write register address 3. Therefore, it is described as follows.

SETUP [W : 3 : 5]

5.2 WRITE REGISTERS

5.2.1 CONF (Configuration Register)

ADDR 0H		MNEMONIC	DESCRIPTIONS
BIT	DEF.		
7	1	CONF7	The most significant modem configuration is determined by this register and CB (Control Bit [W:1:6]). CB is an extension bit of CONF register. CB must be set while SETUP bit [W:3:5] is a one. SETUP assumes modem processor reset signal which can be generated by host processor writing. Refer to SETUP PROCEDURE for more information. Default value is V.29 9600bps no echo protection mode.
6	1	CONF6	
5	0	CONF5	
4	0	CONF4	
3	1	CONF3	
2	0	CONF2	
1	0	CONF1	
0	0	CONF0	

NOTE:

DEF. means default value at power on reset sequence.

5.2.2 ACR1 (Additional Control Register 1)

<table>
<tr><th colspan="2">ADDR 1H</th><th rowspan="2">MNEMONIC</th><th rowspan="2">DESCRIPTIONS</th></tr>
<tr><th>BIT</th><th>DEF.</th></tr>
<tr><td>7</td><td>0</td><td>POL</td><td>Polarity for Mini Facsimile mode.</td></tr>
<tr><td>6</td><td>1</td><td>CB</td><td>Control Bit. This bit is an extension bit of CONF register. CB must be set prior to CONF register.</td></tr>
<tr><td>5</td><td>0</td><td>EQH</td><td>Equalizer coefficients hold. Always set this bit to a zero.</td></tr>
<tr><td>4</td><td>0</td><td>LPFS</td><td>LPF Select. Set this bit to a one.</td></tr>
<tr><td>3
2</td><td>0
0</td><td>AGCS</td><td>AGC type select.
<table>
<tr><th colspan="2">BIT</th><th rowspan="2">AGC TYPE</th></tr>
<tr><th>3</th><th>2</th></tr>
<tr><td>0</td><td>0</td><td>Average</td></tr>
<tr><td>0</td><td>1</td><td>Peak</td></tr>
<tr><td>1</td><td>0</td><td>Hold</td></tr>
<tr><td>1</td><td>1</td><td>Hold</td></tr>
</table></td></tr>
<tr><td>1
0</td><td>0
0</td><td>FCDS</td><td>Fast Carrier Detect level select.
<table>
<tr><th colspan="2">BIT</th><th rowspan="2">FCD ON [dBm]</th><th rowspan="2">FCD OFF [dBm]</th></tr>
<tr><th>3</th><th>2</th></tr>
<tr><td>0</td><td>0</td><td>-43</td><td>-48</td></tr>
<tr><td>0</td><td>1</td><td>-26</td><td>-31</td></tr>
<tr><td>1</td><td>0</td><td>-16</td><td>-21</td></tr>
<tr><td>1</td><td>1</td><td>undefined</td><td>undefined</td></tr>
</table></td></tr>
</table>

5.2.3 TXR

ADDR 2H		MNEMONIC	DESCRIPTIONS
BIT	DEF.		
7	*	TXR	Transmission data register. This register is used in parallel data mode. The Data will be transmitted by LSB first. The first data must be written before -CTS goes to low. Refer to timing chart described later.
6	*		
5	*		
4	*		
3	*		
2	*		
1	*		
0	*		

NOTE:

Asterisk (*) means undefined at power on reset sequence. Power on reset sequence is described later.

5.2.4 ACR2

ADDR 3H		MNEMONIC	DESCRIPTIONS
BIT	DEF.		
5	0	SETUP	When this bit was set to a one, the modem processor holds its operation. Set this bit to a one, before configuration writing. After writing, set to a zero to enable configuration. This operation is called software reset sequence.
3	0	HDLC	The state of 1 of this bit means HDLC mode.
2	0	LAGC	Slow AGC. This bit must be set to a zero for facsimiles.
1	0	PDM	Set this bit to a one for parallel data mode or HDLC mode. When this bit was set to a zero, the modem inputs transmission data through V.24 compatible serial interface. PDM determines transmission data path.
0	0	DEL	Data clock reduction. Data clock frequency becomes 1/2 when this bit was set to a one.

5.2.5 ACR3

ADDR 4H		MNEMONIC	DESCRIPTIONS
BIT	DEF.		
2	0	RSP	Request to Send Parallel. Set this bit to a one instead of making the -RTS to low. The -RTS shall be clamped to high.
1	0	CLAMP	This bit determines transmission data path. Modem transmits MARK (described below) data instead of transmission data when this bit is set to a one in parallel mode. This feature is provided for sending abort sequence in HDLC mode.
0	0	MARK	Set this bit to a one to send abort sequence in HDLC mode. Abort sequence consists from at least 7 bits of continuous 1. The modem inputs MARK as transmission data in parallel mode. Zero insertion will not be performed.

5.2.6 IMR (Interrupt Mask Register)

ADDR 5H		MNEMONIC	DESCRIPTIONS
BIT	DEF.		
7	0	IMR7	This register masks interrupt factor which can be read through ITFR [R:5]. Interrupt factor becomes available when these bits are set to a one corresponding to ITFR bit location. Refer to ITFR descriptions for more information.
6	0	IMR6	
5	0	IMR5	
4	0	IMR4	
3	0	IMR3	
2	0	IMR2	
1	0	IMR1	
0	0	IMR0	

5.2.7 AFER (Analog Front End Register)

ADDR 6H		MNEMONIC	DESCRIPTIONS
BIT	DEF.		
7	0	MUTE	MUTE control. Transmission signal line will be disconnected when this bit is set to a one.
6	0	LEQL	Link Equalizer control. The modem employs fixed link equalizer when this bit is set to a one.
5	0	CEQL2	Cable Equalizer selection bits. The modem employs cable equalizers according to the setting of these two bits.
4	0	CEQL1	
3	1	ATT3	Transmitter Attenuator control. The host processor can control attenuation from 0dB to 15dB. by 1bB step. The default value (1111) means 15dB attenuation.
2	1	ATT2	
1	1	ATT1	
0	1	ATT0	

5.2.8 ACR4

ADDR 8H		MNEMONIC	DESCRIPTIONS
BIT	DEF.		
7	0	CACC	Coefficients ACCess. Host processor informs coefficients access by setting this bit.
6	0	CWR	Coefficients WRiting. This bit will be set after setting of coefficients and its writing address. When this bit is set to a one, the modem processor accepts written coefficients.

5.2.9 CAR (Coefficients Address Register)

ADDR 9H		MNEMONIC	DESCRIPTIONS
BIT	DEF.		
7	0	CA7	This register indicates coefficients address which will be accessed by the host processor.
6	0	CA6	
5	0	CA5	
4	0	CA4	
3	0	CA3	
2	0	CA2	
1	0	CA1	
0	0	CA0	

5.2.10 CDRL (Coefficients Data Register LSB)

ADDR AH		MNEMONIC	DESCRIPTIONS
BIT	DEF.		
7	0	CD07	This register contains Least Significant Byte of coefficient. Coefficients is available when the modem assumes tone generator, DTMF generator and tone detector.
6	0	CD06	
5	0	CD05	
4	0	CD04	
3	0	CD03	
2	0	CD02	
1	0	CD01	
0	0	CD00	

5.2.11 CDRM (Coefficients Data Register MSB)

ADDR BH		MNEMONIC	DESCRIPTIONS
BIT	DEF.		
7	0	CD15	This register contains Most Significant Byte of coefficient. Coefficients is available when the modem assumes tone generator, DTMF generator and tone detector.
6	0	CD14	
5	0	CD13	
4	0	CD12	
3	0	CD11	
2	0	CD10	
1	0	CD09	
0	0	CD08	

5.3 READ REGISTERS

5.3.1 MSR1 (Modem Status Register)

ADDR 0H	MNEMONIC	DESCRIPTIONS
BIT7	TX	Transmission status. TX indicates the modem is being transmitter.
BIT6	CTS	Clear To Send. This bit indicates data can be transmitted. CTS is active high.
BIT5	SQD	Signal Quality Detect. The state of 1 means poor signal quality. This bit is available in V.29 or V.27ter configuration.
BIT4	G2POL	Group 2 POLarity. This bit indicates polarity of Group 2 carrier in reception. The state of 0 means 0 degree, and 1 means 180 degrees.
BIT3	DCD	Data Carrier Detect. This bit indicates available data can be read from the modem. DCD is active high.
BIT2	PN	Pseudo random sequence. This bit becomes to high at V.29 or V.27ter equalizer training sequence when the modem is processing training.
BIT1	P2	Alternate symbol. This bit becomes to high prior to pseudo random sequence in V.29 or V.27ter training when the modem is processing training.
BIT0	FCD	Fast Carrier Detect. This bit becomes to high if any energy on the receiver line was detected.

5.3.2 RXR (Reception data Register)

ADDR 2H	MNEMONIC	DESCRIPTIONS
BIT7	RX7	Reception data appears to this register.
BIT6	RX6	
BIT5	RX5	
BIT4	RX4	
BIT3	RX3	
BIT2	RX2	
BIT1	RX1	
BIT0	RX0	

5.3.3 AGCR (AGC Register)

ADDR 3H	MNEMONIC	DESCRIPTIONS
BIT5	AGC5	The modem provides Auto Gain Controller (AGC). AGC range is 0dB (00H) to 47.5dB (3FH). Therefore, its resolution is 0.75dB.
BIT4	AGC4	
BIT3	AGC3	
BIT2	AGC2	
BIT1	AGC1	
BIT0	AGC0	

5.3.4 BCR (Binary Counter Register)

ADDR 4H	MNEMONIC	DESCRIPTIONS
BIT7	CT7	Wave digitized counter register. The register counts up on the rising edge of the BCTCK input signal. The host processor can not write a value into this register.
BIT6	CT6	
BIT5	CT5	
BIT4	CT4	
BIT3	CT3	
BIT2	CT2	
BIT1	CT1	
BIT0	CT0	

5.3.5 ITFR (InTerruput Factor Register)

ADDR 5H	MNEMONIC	DESCRIPTIONS
BIT7	DCD	Data Carrier Detected. Same as [R:0:3].
BIT6	PN	Pseudo random sequence. Same as [R:0:2]
BIT5	EOFT	End Of Frame Transmission. EOFT becomes to high when the last byte of user data in a HDLC frame has transmitted. It is reset at power on or writing to TXR was performed.
BIT4	BOFR	Begining Of Frame Reception. This bit becomes to a one at the end of flag sequence in HDLC. It is reset at power on or writing to TXR was performed.
BIT3	EOFR	End Of Frame Reception. This bit becomes to a one when a flag was detected in HDLC. It is reset at power on or writing to TXR was performed.
BIT2	FABT	Frame ABorT. This bit becomes to a one when abort sequence was detected in HDLC. It is reset at power on or writing to TXR was performed.
BIT1	CRCER	CRC ERror (FCS error). This bit becomes to a one with EOFR if FCS error occurred. It is reset at power on or writing to TXR was performed.
BIT0	DREQ	Data REQuest. This bit becomes to a one when the modem requests a byte of transmission data or informs a byte of reception data prepared in RXR to the host processor.

5.3.6 ESR1 (Extension Status Register 1)

ADDR 8H	MNEMONIC	DESCRIPTIONS
BIT7	CACD	Coefficient ACcess Done. This bit becomes to a one when the modem read or wrote a coefficients via CDRL, CDRM and CAR. The host processor observes the bit for handshaking.
BIT6	CWRD	Coefficients WRiting Done. This bit becomes to a one with CACD when the modem read a coefficients into its coefficients RAM.
BIT2	HITP	HIT Polarity. This bit indicates receiver line signal level hit polarity. It becomes to a one with GHIT bit when the level suddenly went up.
BIT1	GHIT	Gain HIT. This bit indicates receiver line signal level hit. It becomes to a one when the level suddenly went down or up. HITP bit indicates its polarity.
BIT0	DET21	V.21 detection. This bit becomes to a one when the receiver line signal modulated by V.21 modulation scheme was detected in V.29 or V.27ter configuration.

5.3.7 ESR2 (Extension Status Register 2)

ADDR 9H	MNEMONIC	DESCRIPTIONS
BIT3	FR3	FRequency detection indicator bit3. Default frequency is 2100Hz.
BIT2	FR2	FRequency detection indicator bit2. Default frequency is 1650Hz.
BIT1	FR1	FRequency detection indicator bit1. Default frequency is 1100Hz.
BIT0	FR0	FRequency detection indicator bit0. Default frequency is 462Hz.

5.3.8 CDRL (Coefficients Data Register LSB)

ADDR AH		MNEMONIC	DESCRIPTIONS
BIT	DEF.		
7	0	CD07	This register contains Least Significant Byte of coefficient. Coefficients is available when the modem assumes tone generator, DTMF generator and tone detector.
6	0	CD06	
5	0	CD05	
4	0	CD04	
3	0	CD03	
2	0	CD02	
1	0	CD01	
0	0	CD00	

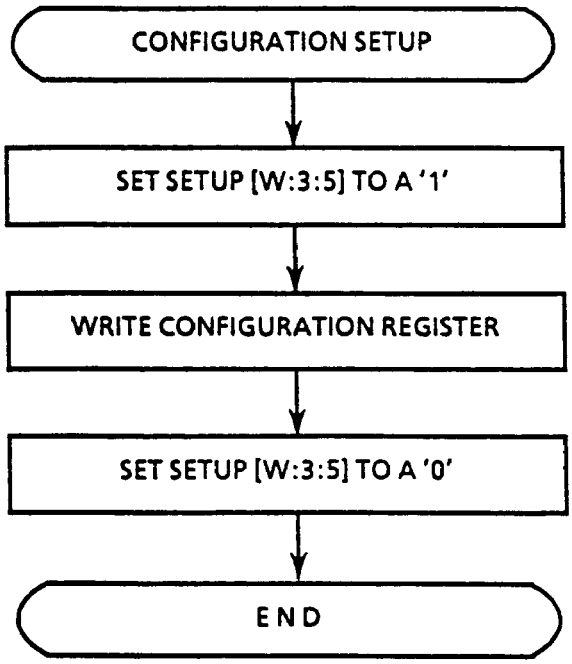
5.3.9 CDRM (Coefficients Data Register MSB)

ADDR BH		MNEMONIC	DESCRIPTIONS
BIT	DEF.		
7	0	CD15	This register contains Most Significant Byte of coefficient. Coefficients is available when the modem assumes tone generator, DTMF generator and tone detector.
6	0	CD14	
5	0	CD13	
4	0	CD12	
3	0	CD11	
2	0	CD10	
1	0	CD09	
0	0	CD08	

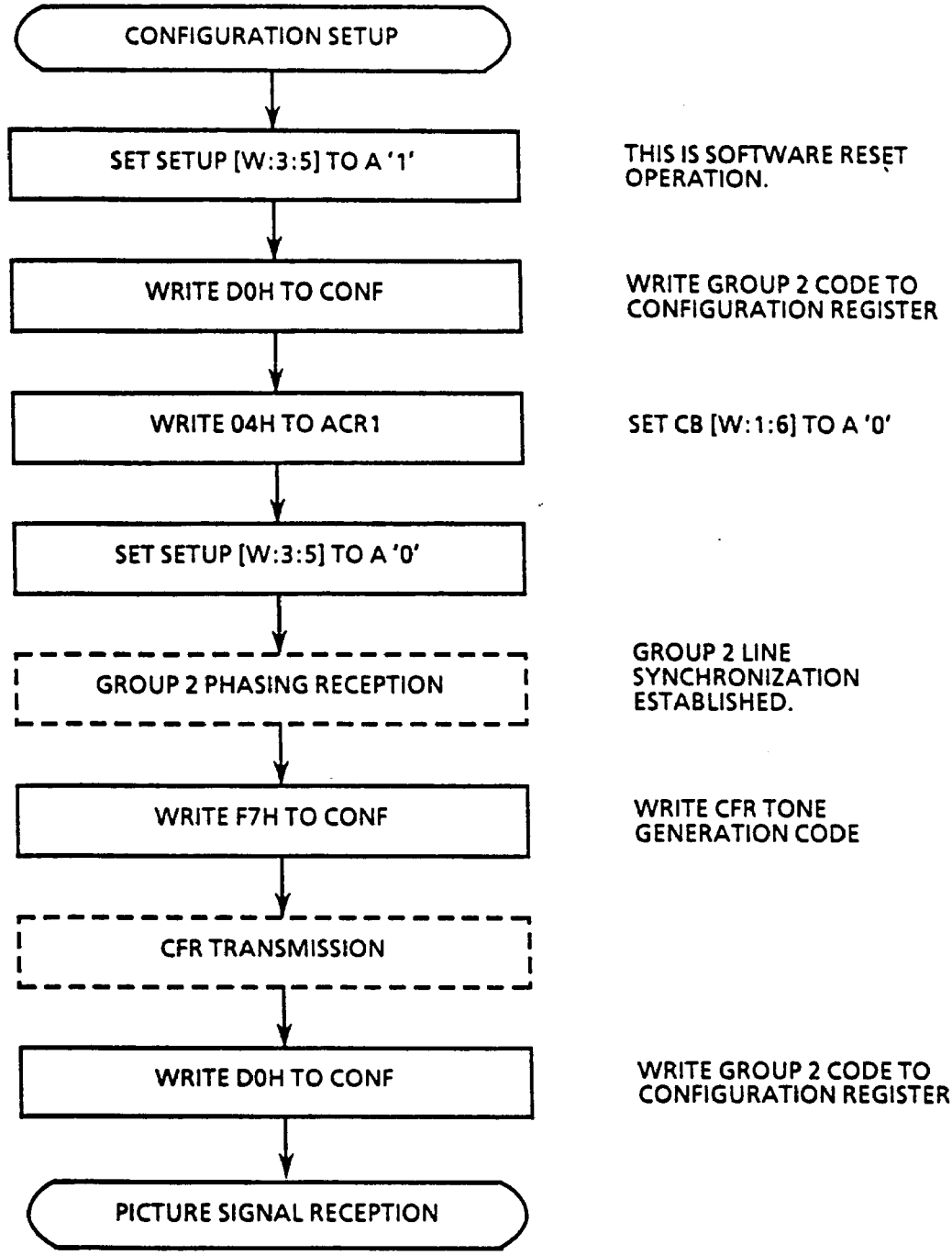
5.4 CONFIGURATION SETUP

The host processor performs setup procedure represented below. There are two different procedures. Because, the modem has to be reset at changing configuration to make sure its operation. The TC35108F stops data clock while the LSI is being reset by SETUP bit. Although in case of Group 2 CFR tone generation, scanning line synchronization will be lost if the data clock stops. Therefore, the host processor changes configuration without reset operation such as setting SETUP to a one in Group 2 facsimile procedure.

5.4.1 EXCEPT TONE GENERATION IN GROUP 2



5.4.2 OPERATION IN GROUP 2 (IN CASE OF CFR TRANSMISSION)



As the flow chart shows, do not perform reset operation while synchronization is establishing.

5.5 POWER ON RESET SEQUENCE

The TC35108F begins to initialize the registers when the -RST terminal is kept to logical low level for 450ns. This operation is called hardware reset sequence. The modem requires hardware reset at power-on.

The condition of the modem after hardware reset is described below. Refer to section 5 FUNCTIONAL DESCRIPTION for more information.

DEFAULT CONDITIONS

ITEM	CONDITION
DATA RATE	9600 bps (V.29)
ECHO	NO ECHO PROTECTION
TRAINING	ENABLE
TYPE OF AGC	AVERAGE TYPE
FCD ON LEVEL	ABOVE -43dBm
FCD OFF LEVEL	UNDER -48dBm
TX DATA PATH	SERIAL INTERFACE
HDLC MODE	INACTIVE

5.6 COMMUNICATION SPECIFICATIONS

The TC35108F supports Group 2, V.21, V.27ter and V.29 modulation scheme.

MODULATION SCHEME

FUNCTION	CARRIER FREQUENCY (Hz ± 0.01%)	MODULATION SCHEME
Group 2	2100	AM-PM-VSB
V.21 CHANNEL 2	1650 / 1850	FSK
V.27ter	1800	PSK
V.29	1700	QAM

SIGNALING AND DATA RATE

FUNCTION	SIGNALING (BAUD ± 0.01%)	DATA RATE (BPS ± 0.01%)	TRANSMISSION SPECTRUM SHAPING FILTER
Group 2	(10368)	(10368)	VSB FILTER
V.21 CHANNEL 2	300	300	NON
V.27ter	1200 1600	2400 4800	100% SQUARE ROOT ROLL OFF 50% SQUARE ROOT ROLL OFF
V.29	2400	4800 7200 9600	15% SQUARE ROOT ROLL OFF

TURN-ON SEQUENCE

FUNCTION		ECHO PROTECT TONE DISABLED	ECHO PROTECT TONE ENABLED
V.27ter	2400 BPS	943ms	1159ms
	4800 BPS	708ms	918ms
V.29	4800 BPS 7200 BPS 9600 BPS	253ms	449ms
V.21		≤ 100us	-
Group 2		≤ 100us	-

CLAMPING

(i) The RXD terminal is clamped to a '1' whenever -DCD is inactive.

(ii) The -DCD terminal is clamped to high whenever SQD is '1' in Group 3 configurations. The state of SQD = '1' indicates poor signal quality. SQD bit is located at [R :0:5].

(iii) When the host controls Request To Send by RSP bit in the interface register, clamp the -RSP terminal to logical high level.

5.7 DATA TRANSFER MODES

5.7.1 SERIAL MODE

The serial mode uses CCITT V.24 compatible serial interface to transfer channel data. The serial interface of the modem is a half duplex type. The -RTS terminal or RSP bit in the interface register changes its direction.

5.7.2 PARALLEL MODE

The modem transfers channel data via the host processor bus in the parallel mode. The mode is defined by PDM bit located at [W:3:1].

5.7.3 HDLC MODE

The modem performs framing and deframing by HDLC format in the HDLC mode. This mode is included by parallel mode. The mode is defined by HDLC bit located at [W:3:3].

6 ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
SUPPLY VOLTAGE	VDD	-0.5 to 7.0	V
INPUT VOLTAGE	VIN	-0.5 to 7.0	V
OUTPUT VOLTAGE	VOUT	-0.5 to 7.0	V
INPUT CURRENT	IIN	+20	mA
OUTPUT CURRENT	IOUT	+20	mA
POWER DISSIPATION	Pd	1.3	W
STORAGE TEMPERATURE	Tstg	-55 to 150	°C
SOLDERING TEMPERATURE (10 seconds)	Tsol	260	°C

RECOMMENDED OPERATIONAL CONDITION

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
SUPPLY VOLTAGE	VDD		4.75	5.0	5.25	V
INPUT VOLTAGE	VIN		0		VDD	V
SYSTEM CLOCK FREQUENCY DEFLECTION (Group 2 facsimile mode)	f	VDD = 5.0V + 5% fclk = 6.2208MHz	-5	0	+5	ppm
SYSTEM CLOCK FREQUENCY DEFLECTION (Except Group 2)	f	VDD = 5.0V + 5% fclk = 6.2208MHz	-100	0	+100	ppm
OPERATING TEMPERATURE	Topr		0		70	°C

6.2 DC CHARACTERISTICS

ITEM	SYMBOL	PIN NAME	CONDITION	MIN.	TYP.	MAX	UNIT
CONSUMPTION CURRENT	IDD	VDD	VDD = 5.25V CLK = 6.3MHz			120	mA
TYPE 1 TERMINALS HIGH LEVEL INPUT VOLTAGE	VIH(1)	DB0 - DB7, A0 - A3 -CE, -RD, -RTS TXD, ST1		2.4			V
TYPE 1 TERMINALS LOW LEVEL INPUT VOLTAGE	VIL(1)	DB0 - DB7, A0 - A3 -CE, -RD, -RTS TXD, ST1				0.8	V
TYPE 2 TERMINALS HIGH LEVEL INPUT VOLTAGE	VIH(2)	ALL THE INPUT TERMINALS EXCEPT TYPE 1		0.7 VDD			V
TYPE 2 TERMINALS LOW LEVEL INPUT VOLTAGE	VIL(2)	ALL THE INPUT TERMINALS EXCEPT TYPE 1				0.3 VDD	V
LOW LEVEL INPUT CURRENT(1)	IIL(1)	GD0 - GDD	VIN = GND	-750	-500	-365	uA
HIGH LEVEL INPUT CURRENT(1)	IIH(1)	GD0 - GDD	VIN = VDD			10	uA
LOW LEVEL INPUT CURRENT(2)	IIL(2)	DB0 - DB7	VIN - GND	-250	-165	-120	uA
HIGH LEVEL INPUT CURRENT(2)	IIH(2)	DB0 - DB7	VIN - VDD			10	uA
LOW LEVEL INPUT CURRENT(3)	IIL(3)	ALL THE INPUT TERMINAL OTHER THAN THE ABOVE	VIN = GND	-1.0			uA
HIGH LEVEL INPUT CURRENT(3)	IIH(3)	ALL THE INPUT TERMINAL OTHER THAN THE ABOVE	VIN = VDD			1.0	uA

ITEM	SYMBOL	PIN NAME	CONDITION	MIN.	TYP.	MAX.	UNIT
LOW LEVEL OUTPUT CURRENT (1)	IOL(1)	DB0 - DB7 DTCK, RXD -CDC, -CTS	VOL = 0.4V	3.2			mA
HIGH LEVEL OUTPUT CURRENT (1)	IOH(1)	DB0 - DB7 DTCK, RXD -CDC, -CTS	VOH = 2.4V			-3.0	mA
LOW LEVEL OUTPUT CURRENT (2)	IOL(2)	ALL THE INPUT TERMINALS EXCEPT MENTIONED ABOVE AND EYESYC	VOL = 0.4V	2.0			mA
HIGH LEVEL OUTPUT CURRENT (2)	IOH(2)	ALL THE INPUT TERMINALS EXCEPT MENTIONED ABOVE AND EYESYC	VOH = 2.4			-100	mA
LOW LEVEL OUTPUT CURRENT (3)	IOL(3)	EYESYC	VOL = 0.4	2.0			mA
HIGH LEVEL OUTPUT VOLTAGE	VOH	ALL THE INPUT EXCEPT EYESYC	IOH = -10uA	4.5			V
HIGH LEVEL OUTPUT OFF - LEAK CURRENT	IDH	EYESYC, EYEDAT	VDH = VDD			10	uA
LOW LEVEL OUTPUT OFF - LEAK CURRENT	IDL	EYESYC, EYEDAT	VDL = GND	-10			uA

6.3 AC CHARACTERISTICS

DATA BUS WRITE TIMING

ITEM	SYMBOL	PIN NAME	CONDITION	MIN.	TYP.	MAX	UNIT
DATA BUS WRITE PULSE WIDTH	TWW(2)	- WR	Cin = 10pF	120			nS
ADDRESS SET - UP TIME	Tset(5)	A0, A1, A2, A3	Cin = 10pF	50			nS
ADDRESS HOLD TIME	Thold(5)	A0, A1, A2, A3	Cin = 10pF	30			nS
DATA BUS DATA SET - UP TIME	Tset(2)	DB0 - DB7	Cin = 10pF	60			nS
DATA BUS DATA HOLD TIME	Thold(2)	DB0 - DB7	Cin = 10pF	35			nS

DATA BUS READ TIMING

ITEM	SYMBOL	PIN NAME	CONDITION	MIN.	TYP.	MAX	UNIT
DATA BUS READ PULSE WIDTH	TWR(2)	- RD	Cin = 10pF	120			nS
ADDRESS SET - UP TIME	Tset(6)	A0, A1, A2, A3	Cin = 10pF	50			nS
ADDRESS HOLD TIME	Thold(6)	A0, A1, A2, A3	Cin = 10pF	30			nS
DATA BUS OUTPUIT ENABLE TIME	Tpzh(2) Tpzl(2)	DB0 - DB7	Cin = 100pF RL = 1.5kΩ			150	nS
DATA BUS OUTPUT DISABLE TIME	Tphz(2) Tplz(2)	DB0 - DB7	Cin = 100pF RL = 1.5kΩ			150	nS

OPERATION TIMING

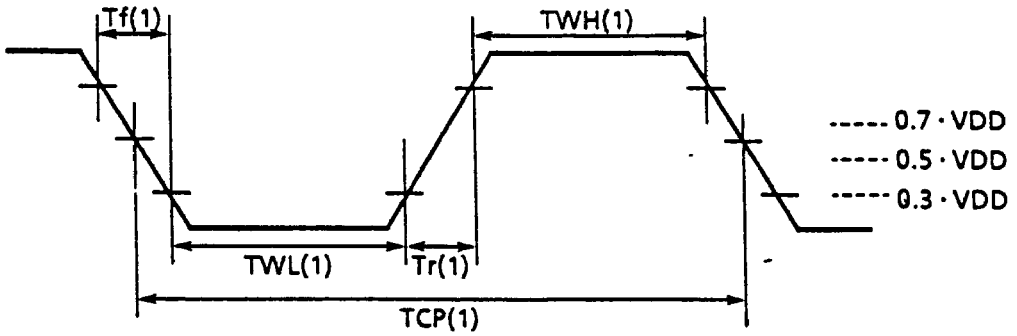
ITEM	SYMBOL	PIN NAME	CONDITION	MIN.	TYP.	MAX	UNIT
CLOCK CYCLE	TCP(1)	CLK	Cin = 10pF	160			nS
CLOCK WIDTH	TWH(1) TWL(1)	CLK	Cin = 10pF	60			nS
CLOCK RISE TIME	Tr(1)	CLK	Cin = 10pF			15	nS
CLOCK FALL TIME	Tf(1)	CLK	Cin = 10pF			10	nS
SYSTEM RESET PULSE WIDTH	TWRST	-RST	Cin = 10pF	450			nS

SERIAL DATA OUTPUT TIMING

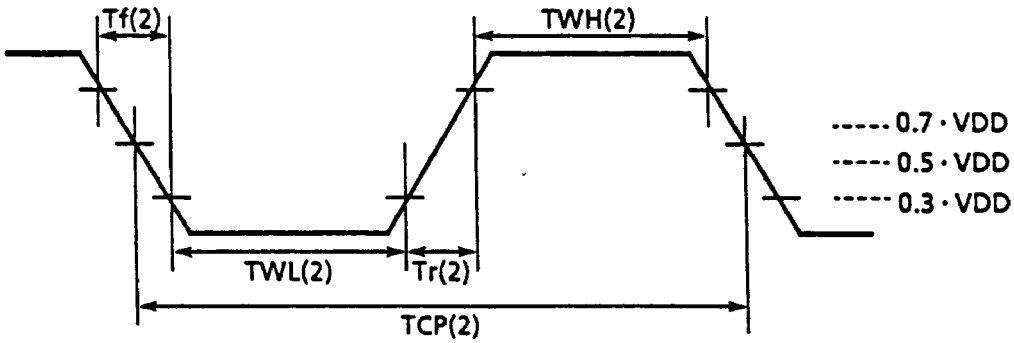
ITEM	SYMBOL	PIN NAME	CONDITION	MIN.	TYP.	MAX	UNIT
SERIAL DATA OUTPUT ENABLE TIME	Tpzh(3) Tpzl(3)	EYEDAT	CL = 100pF RL = 1.5kΩ			170	nS
SERIAL DATA OUTPUT DELAY TIME	Tphl(1) Tplh(1)	EYEDAT	CL = 30pF			170	nS
SERIAL DATA OUTPUT DISABLE TIME	Tphz(3) Tplz(3)	EYEDAT	CL = 100pF RL = 1.5kΩ			500	nS
SERIAL DATA REQUEST OUTPUT ENABLE TIME	Tpzl(4)	EYESYC	CL = 30pF RL = 1.5kΩ			170	nS
SERIAL DATA REQUEST OUTPUT DISABLE TIME	Tplz(4)	EYESYC	CL = 30pF RL = 1.5kΩ			170	nS

CONTROL SIGNAL WAVE FORM

CLK

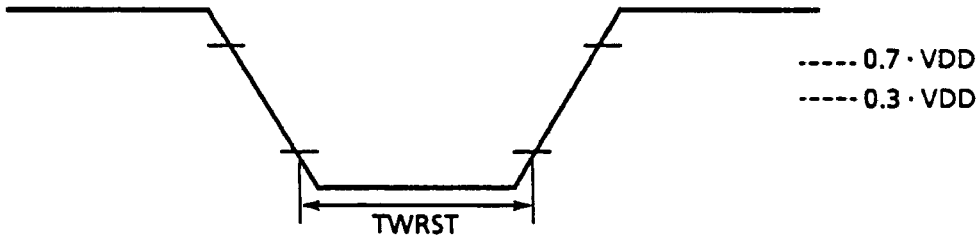


EYECLK

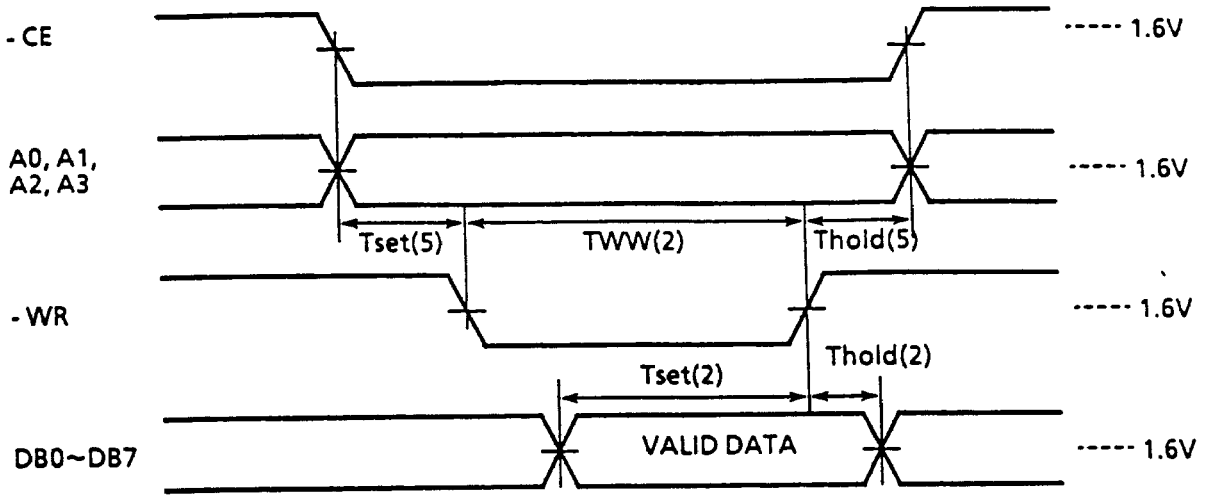


INPUT CLOCK WAVE FORM

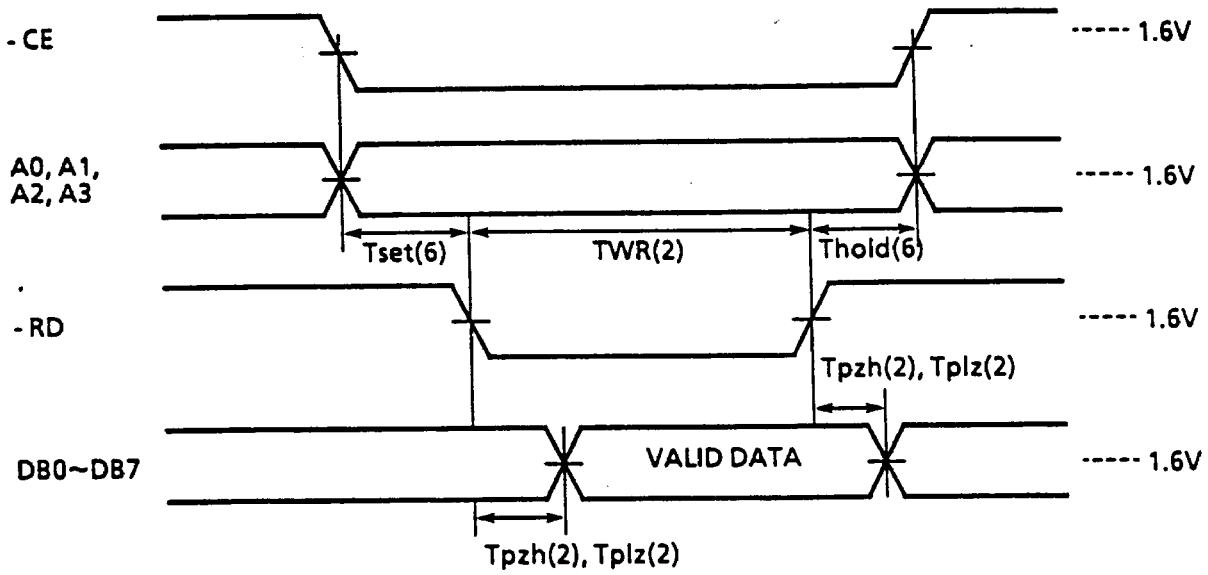
- RST



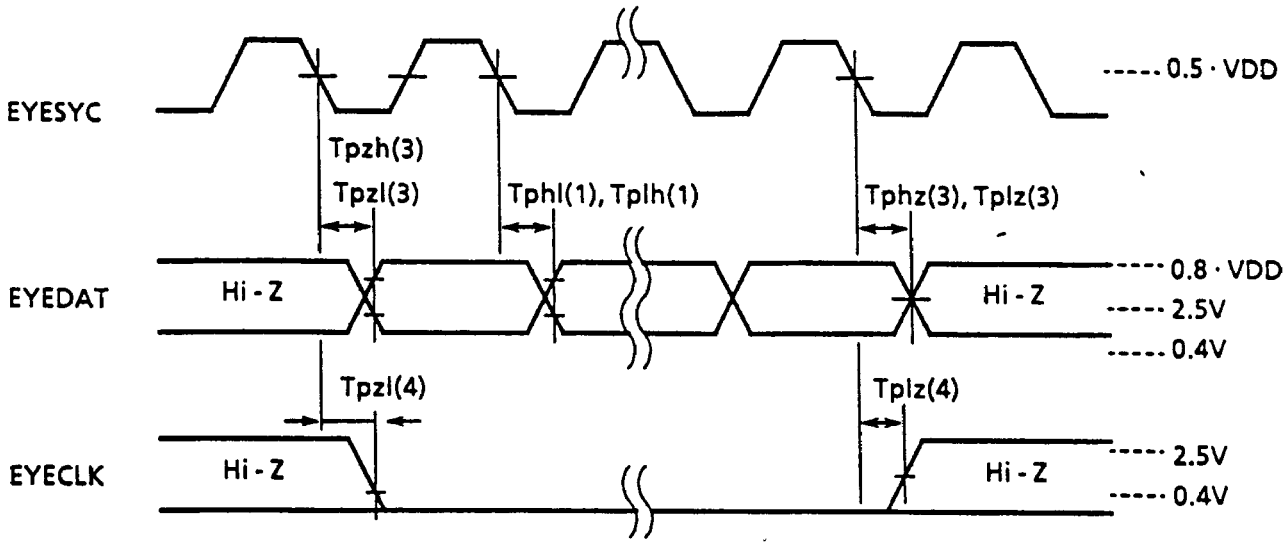
SYSTEM RESET PULSE WAVE FORM



DATA BUS WRITE TIMING



DATA BUS READ TIMING



SERIAL DATA OUTPUT TIMING

APPLICATION CIRCUIT DIAGRAM

9600BPS ECM FACSIMILE MODEM