TC35102F
CMOS INTEGRATED CIRCUIT
SILICON MONOLITHIC

# TC35102F

# MODEM ANALOG FRONT END

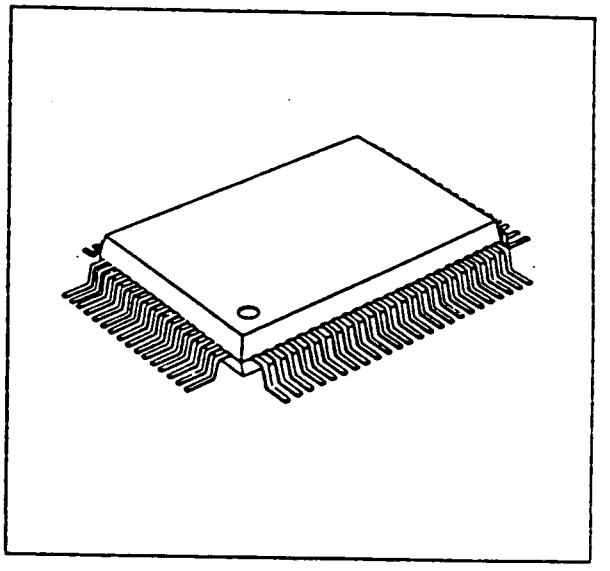
'89 - 8 - 7

## GENERAL DESCRIPTION

The TC35102F is the Modem Analog Front-end LSI to compose a 2-wire half-duplex modem and a 4-wire full-duplex modem, which satisfy CCITT Recommendation V29(9600bps), V27ter ( 4800bps ), V26bis ( 2400bps ), V21 (300bps,chan.2), T4 and T3. The TC35102F includes receiving and transmitting SCF filters, A/D and D/A converters, a digital controlled programable gain amplifier, and a transmitting attenuator etc.

User selectable features using parallel interface allow the change of an attenuation ratio, and the response of Cable Equalizer.

The TC35102F is designed for use in G3, G2, and G1 Facsimile machines and data modems using with TOSHIBA Modem Processor LSIs.



## FEATURES

- o MODEM PROCESSOR
  1) TC35107F for 9600bps G3/G2/G1 FACSIMILE MODEM
  2) TC35100P/F,TC35101P/F for 4800bps G3 FACSIMILE MODEM and V.26bis DATA MODEM
- o FULL-DUPLEX STRUCTURE
- o RECEIVING BAND-PASS FILTER
- o TRANSMITTING LOW-PASS FILTER
- o TRANSMITTING and RECEIVING CABLE EQUALIZERS ( 4 STEPS CHARACTERISTIC SELECTABLE)
- o JAPAN 1 LINK COMPROMISED GROUP DELAY EQUALIZER
- o TRANSMITTING ATTENUATOR (FROM 0 to -15dB 1dB STEP)
- o DIGITAL CONTROL PROGRAMABLE GAIN AMPLIFIER
- o A/D and D/A CONVERTERS
- o MINIMUM EXTERNAL PARTS
- o 2 POWER SUPPLY OF +5V and -5V OPERATIONS
- o CMOS LOW POWER CONSUMPTION 75mW Typ.
- o 80 PIN FLAT PACKAGE

## STRUCTURE 1

TC35107F, TC35102F
- o Clock Frequency 6.2208MHz
- o G3: CCITT Recommendation V29 (9600/7200/4800bps)
  V27ter (4800/2400bps)
- o G2
- o G1: for Transmitting Function only
- o V21 (ch2) T30 Binary Procedure
- o DTMF Dialing
- o Tone Transmission
- o Tone Detection
- o Serial Interface (RS-232C)
- o Parallel Interface

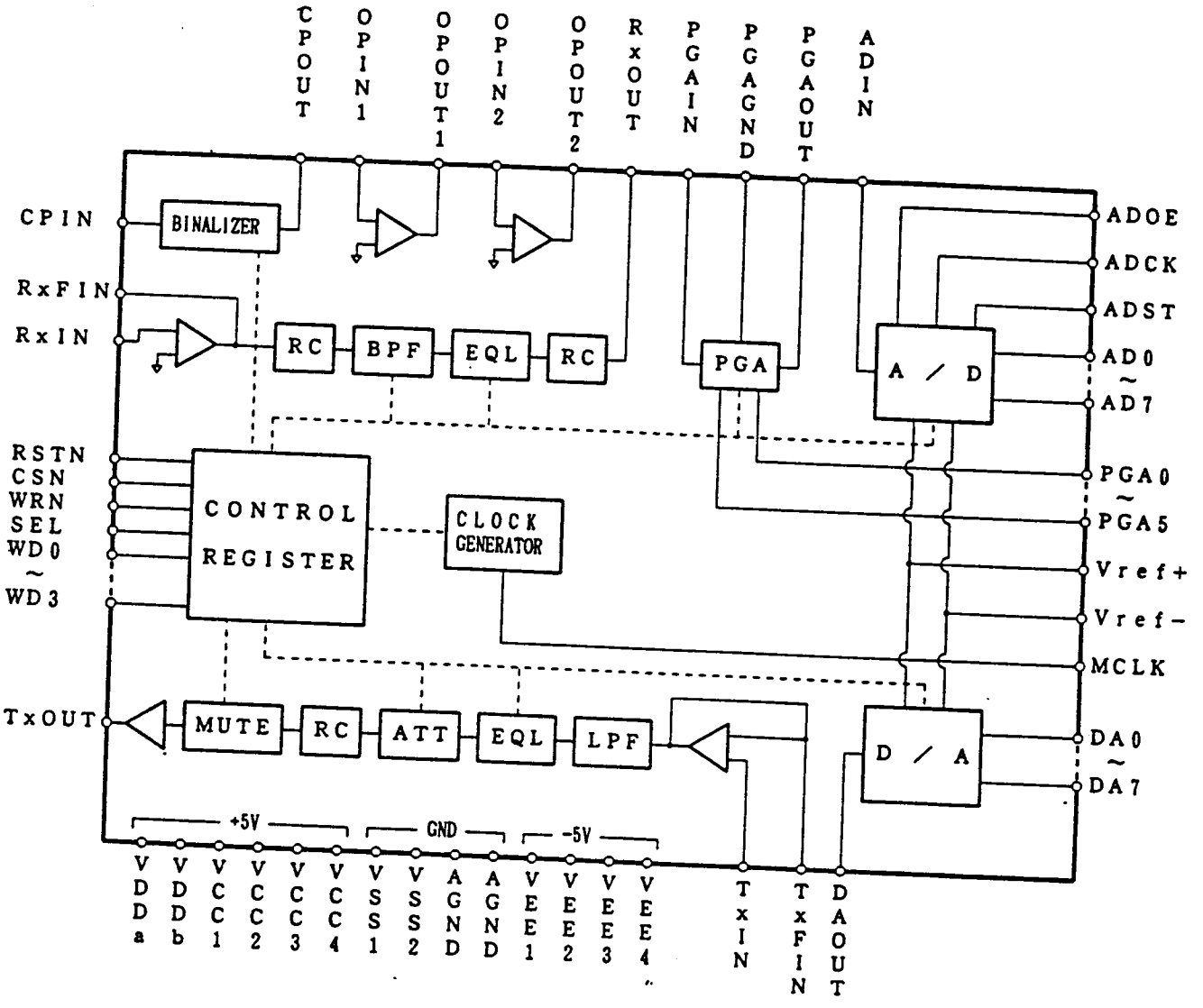
## STRUCTURE 2

TC35100P/F,TC35101P/F, TC35102F
- o Clock Frequency 4.8384MHz
- o CCITT Recommendation V27ter (4800/2400bps)
  V26bis (2400/1200bps)
- o V21 (ch2) T30 Binary Procedure
- o DTMF Dialing
- o Tone Transmission
- o Tone Detection
- o Serial Interface (RS-232C)
- o Parallel Interface

## APPLICATION

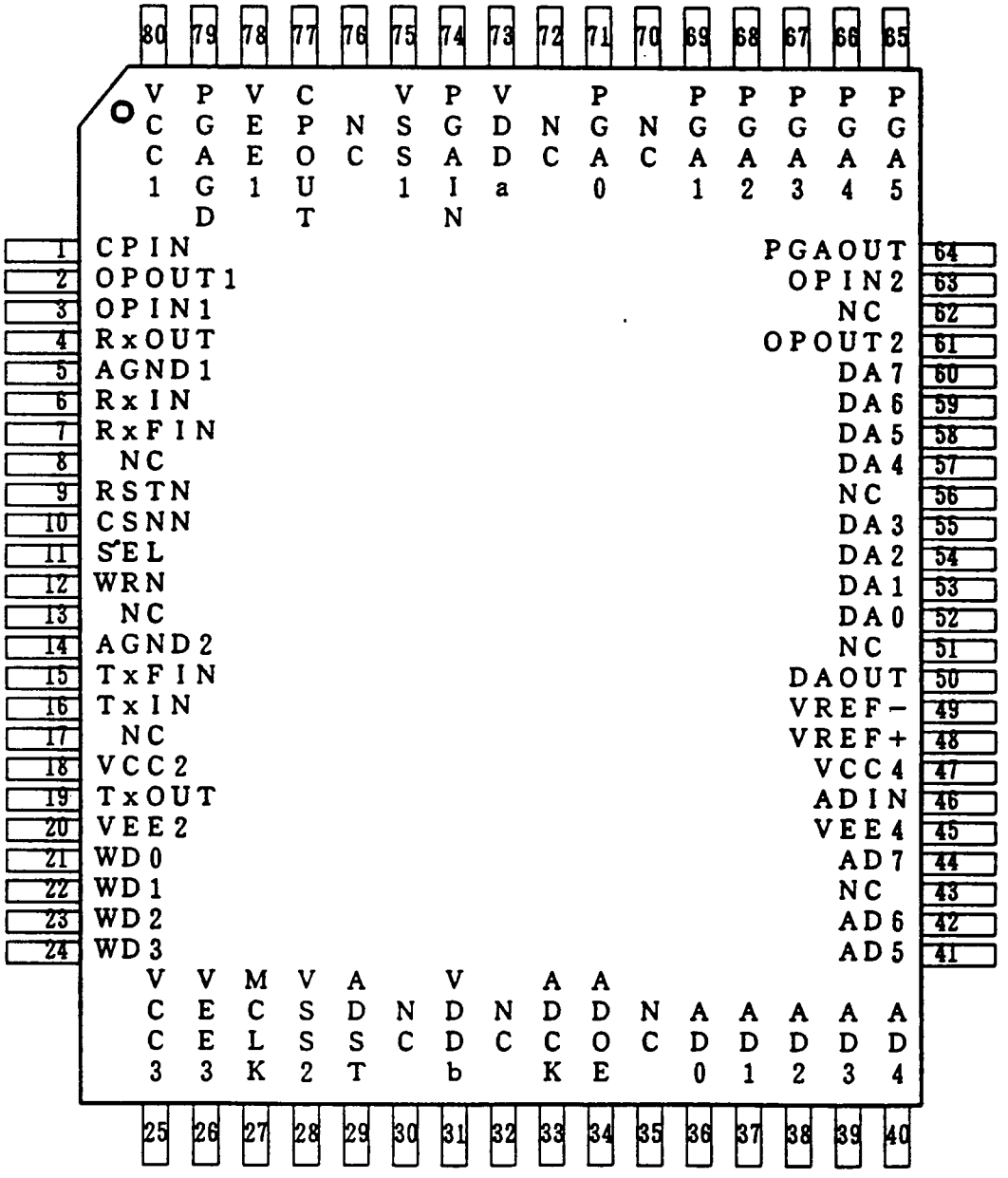
- o G3 FACSIMILE MACHINE
- o DATA COMMUNICATION TERMINALS

## 1. SYSTEM BLOCK




RC1 : Anti-alias Filter
RC2 : Smoothing Filter
EQL : 4-Selectable Cable Equalizer (0.4.8.12dB)
PGA : Programable Gain Amplifier
BPF : Receiving Band Pass Filter
LPF : transmitting Low Pass Filter
ATT : Transmitting attenuator (0 to -15dB)

## 2. PIN ASSIGNMENT



3. PIN FUNCTION

| Pin No. | Pin Name | A/D | I/O | Function |
|---|---|---|---|---|
| 1 | CPIN | A | I | Input terminal for binarized circuit |
| 2 | OPOUT1 | A | O | Input terminal for opamp1 |
| 3 | OPIN1 | A | I | Opamp1 signal output terminal |
| 4 | RxOUT | A | O | input terminal for Receiving BPF |
| 5 | AGND1 | - | - | Analog ground |
| 7 | RxFIN | A | O | Output terminal of buffer opAmp of Rx side |
| 6 | RxIN | A | I | Input terminal of receiving BPF |
| 11 | SEL | D | I | Input select terminal for MODE setting |
| 9 | RSTN | D | I | Clear signal input ("L"level active) |
| 10 | CSN | D | I | Input terminal of chip select signal |
| 12 | WRN | D | I | Input terminal for MODE setting at the rising edge of the WRN pulse when "CSN" is "L" |
| 14 | AGND2 | - | - | Analog ground |
| 15 | TxFIN | A | O | Output buffer opamp of Tx side |
| 16 | TxIN | A | I | Input terminal for transmitting LPF |
| 18 | VCC2 | - | - | +5V Power supply |
| 19 | TxOUT | A | O | Transmitting LPF signal output |
| 20 | VEE2 | - | - | -5V Power supply |
| 21 | WD0 | D | I | Data input for setting mode register (LSB) |
| 22 | WD1 | D | I | |
| 23 | WD2 | D | I | |
| 24 | WD3 | D | I | (MSB) |
| 25 | VCC3 | - | - | +5V Power supply |
| 26 | VEE3 | - | - | -5V Power supply |
| 27 | MCLK | D | I | Input terminal of master clock |
| 28 | VSS2 | - | - | Analog ground |
| 29 | ADST | D | I | A/D converter starting signal input terminal |
| 31 | VDDb | - | - | +5V Power supply |
| 33 | ADCK | D | I | Clock input terminal for AD converter |
| 34 | ADOE | D | I | Enable signal input terminal for A/D converter |

| Pin No. | Pin Name | A/D | I/O | Function |
|---|---|---|---|---|
| 36 | AD0 | D | O | A/D converter signal output (LSB) |
| 37 | AD1 | D | O | terminal |
| 38 | AD2 | D | O | |
| 39 | AD3 | D | O | |
| 40 | AD4 | D | O | |
| 41 | AD5 | D | O | |
| 42 | AD6 | D | O | |
| 44 | AD7 | D | O | (MSB) |
| 45 | VEE4 | - | - | -5V Power supply |
| 46 | ADIN | A | I | Analog input terminal ,input voltage range is VRef-/2~VRef+/2 |
| 47 | VCC4 | - | - | +5V Power supply |
| 48 | VRef+ | A | I | Reference voltage supplying terminal, which performs as full-scale voltage |
| 49 | VRef- | A | I | Reference voltage supplying terminal, which performs as zero-scale voltage |
| 50 | DAOUT | A | O | D/A converter signal output terminal |
| 52 | DA0 | D | I | Data input terminal for D/A (LSB) |
| 53 | DA1 | D | I | converter |
| 54 | DA2 | D | I | |
| 55 | DA3 | D | I | |
| 57 | DA4 | D | I | |
| 58 | DA5 | D | I | |
| 59 | DA6 | D | I | |
| 60 | DA7 | D | I | (MSB) |
| 61 | OPOUT2 | A | O | OpAmp2 signal output terminal |
| 63 | OPIN2 | A | I | Input terminal of opamp2 |
| 64 | PGAOUT | A | O | Programable Gain Amp signal output terminal |
| 65 | PGA5 | D | I | Data input terminal for PGA (MSB) |
| 66 | PGA4 | D | I | |
| 67 | PGA3 | D | I | |
| 68 | PGA2 | D | I | |
| 69 | PGA1 | D | I | |
| 71 | PGA0 | D | I | (LSB) |
| 73 | VDDa | - | - | +5V Power supply |
| 74 | PGAIN | A | I | Analog input terminal of PGA |
| 75 | VSS1 | - | - | Analog ground |
| 77 | CPOUT | D | O | Binarized data output terminal |
| 78 | VEE1 | - | - | -5V Power supply |
| 79 | PGAGD | A | I | Standard voltage supplying terminal for PGA |
| 80 | VCC1 | - | - | +5V Power supply |

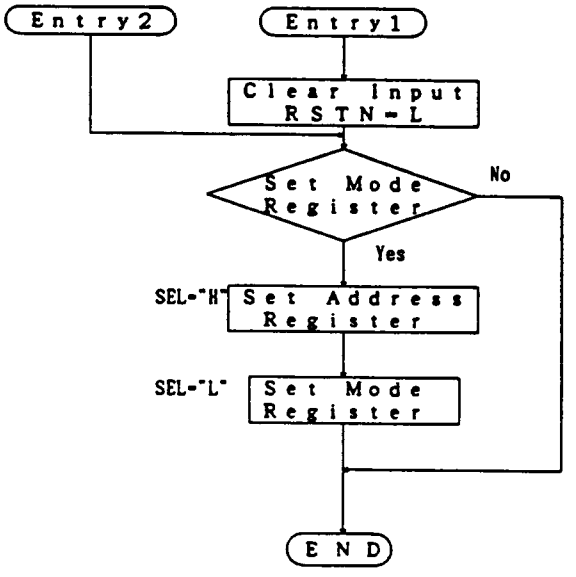
| Pin No. | Pin Name | A/D | I/O | Function |
|---|---|---|---|---|
| 8 | NC | - | - | Non-Connected pin |
| 13 | | - | - | |
| 17 | | - | - | |
| 30 | | - | - | |
| 32 | | - | - | |
| 35 | | - | - | |
| 43 | | - | - | |
| 51 | | - | - | |
| 56 | | - | - | |
| 62 | | - | - | |
| 70 | | - | - | |
| 72 | | - | - | |
| 76 | | - | - | |

## MODE SETTING

TC35102F has feature of selectable 4 kind of cable equalizing response for both transmitter and receiving system, transmitting attenuation ratio from 0dB to -15dB by 1dB step, clock frequency in order to interface two different Modem Processor LSI facsimiles of the 9600bps system (composition 1,2) and the 4800bps system (composition 3).

TC35102 has 4 port (4bit, WD3 to 0) of mode register which is selected by setting address data (001,010,011,100) to the address register.

Setting sequences is described as follows:
After supplying power, TC35102F should be clear (RSTN: L).
Address data corresponding to required mode register should be set (SEL=H), before Mode data is set to the mode register.
The flow chart and the timing chart of mode setting are presented as follows.




Entry1. Initial setting after supplying power.
Entry2. Setting mode register during operation.

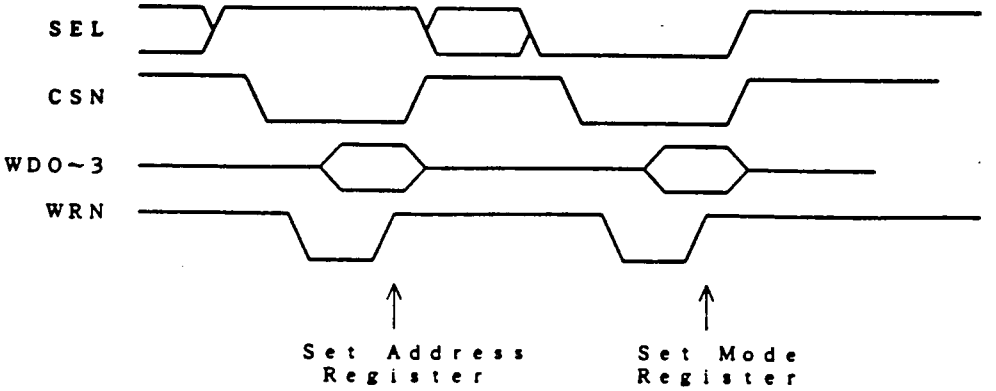



Fig. 4-2

## SETTING PROCEDURE OF ADDRESS REGISTER AND MODE REGISTER

(1) Address Register

| X | 0 | 0 | 1 |
|---|---|---|---|

Mode Register

| 0 | Lo/Hi | 0 | 0 |
|---|---|---|---|

0: Master Clock 6.2208MHz
1: Master Clock 4.8384MHz

At resetting, the master clock shall be set at 6.2208MHz.

(2) Address Register

| X | 0 | 1 | 0 |
|---|---|---|---|

Mode Register

| AT8 | AT4 | AT2 | AT1 |
|---|---|---|---|

| MSB | | | | LSB | | Atten.Ratio |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | | - | 0dB |
| 0 | 0 | 0 | 1 | | - | 1dB |
| 0 | 0 | 1 | 0 | | - | 2dB |
| 0 | 1 | 0 | 0 | | - | 4dB |
| 1 | 0 | 0 | 0 | | - | 8dB |

The attenuation ratio of transmitting attenuater shall be set by 1dB step. It is weighted in binary, which achieves the attenuation ratio 0dB for 0(H) and 15dB for F(H). At resetting, F(H) value is set.

(3) Address Register

| X | 0 | 1 | 1 |
|---|---|---|---|

Mode Register

| TCEQ2 | TCEQ1 | RCEQ2 | RCEQ1 |
|---|---|---|---|

The characteristic of the receiving cable equalizer can be selected at RCEQ1 and 2, and similarly that of the transmitting cable equalizer can be done at TCEQ1 and 2 in four steps as listed below.

| TCEQ2 | TCEQ1 | FOR TRANSMITTING |
|---|---|---|
| RECQ2 | RCEQ1 | FOR RECEIVING |
| 0 | 0 | Non-equalizing ratio |
| 0 | 1 | 4dB equivalent equalizing ratio |
| 1 | 0 | 8dB equivalent equalizing ratio |
| 1 | 1 | 12dB equivalent equalizing ratio |

At resetting, 0(H) shall be set, when receiving and transmitting equalizer reaches the non-equalizing ratio state.

(4) Address Register

| X | 1 | 0 | 0 |
|---|---|---|---|

Mode Register

| GD2 | GD1 | 2VAL | MUTE |
|---|---|---|---|

MUTE:
0: Mute Switch OFF(transmissible)
1: Mute Switch ON (untransmissible)

2VAL:
0: Binary Coded Circuit Enable
1: Binary Coded Circuit Disable

GD2 GD1:
0: 0 Group Delay Non-equalized
0: 1 Group Delay Non-equalized
1: 0 Reciving Filter Group Delay Distortion Equalized.
1: 1 1 Link Equivalent Group Delay Distortion Equalized

To prevent the filter noise of transmitting system from interfering with receiving system, the mute switch must be controlled with MUTE. The 2VAL does disable when the binary coded converter is not used.
The group delay distortion equalized filter of the receiving filter and NTT 1 link equivalent group delay equalized filter can be selected by CD1 and 2. At resetting, 0(H) shall set.

## MAXIMUM RATINGS

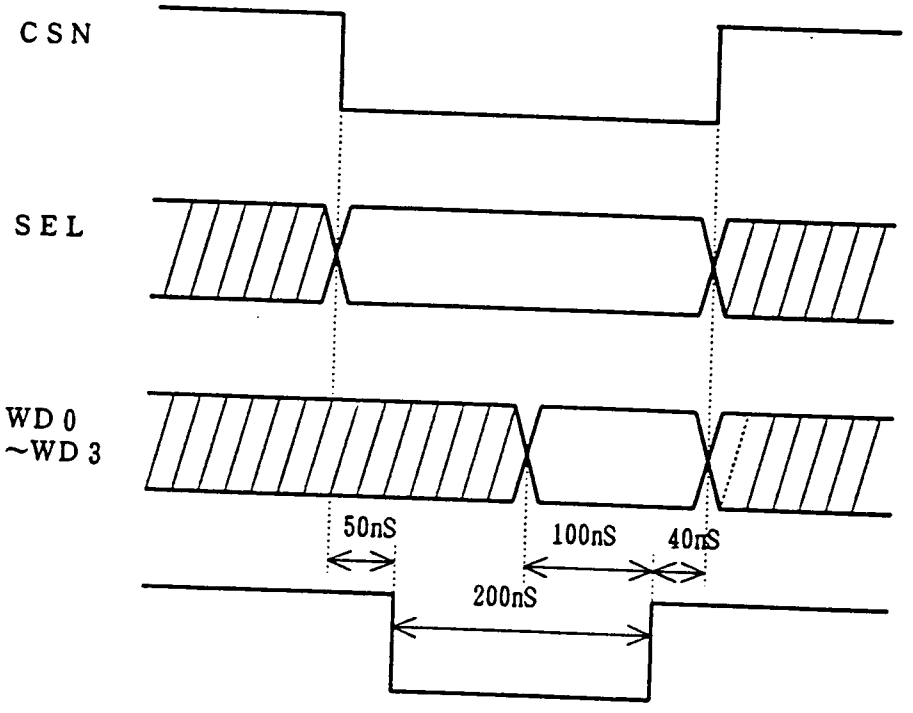
| ITEM | SYMBOL | RATINGS | | UNIT |
|---|---|---|---|---|
| | | MIN. | MAX. | |
| Supply Voltage | VDD | -0.5 | 7.0 | V |
| | VCC | -0.5 | 7.0 | V |
| | VEE | -7.0 | 0.5 | V |
| Analog Input Voltage | VIN | VEE-0.5 | VDD+0.5 | V |
| digital Input Voltage | VIN | -0.5 | VDD+0.5 | V |
| Analog Output Voltage | VOUT | VEE-0.5 | VDD+0.5 | V |
| Digital Output Voltage | VOUT | -0.5 | VDD+0.5 | V |
| Input Current | VIN | -20 | +20 | mA |
| Operation Temperature | Topr | -10 | +70 | ℃ |
| Storage Temperature | Tstg | -55 | +125 | ℃ |
| Power Dissipation | PD | | 600 | mW |
| Lead Temperature/Time | Tsol | 260 ℃ . 10sec | | |

## 7. DC AC CHARACTERISTICS

(Ta = -10 ~ 70 ℃ VSS=AGND=0V)

| Item | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Operation Voltage | VDD | fck=6.2208 or 4.8384MHz | 4.5 | 5.0 | 5.5 | V |
| 〃 | VCC | 〃 | 4.5 | 5.0 | 5.5 | V |
| 〃 | VEE | 〃 | -5.5 | -5.0 | -4.5 | V |
| Operation Current | IDD | | | 12 | 30 | mA |
| 〃 | IEE | | | 12 | 30 | mA |
| Clock Frequency | Fck | fck=4.8384MHz | 4.8379 | 4.8384 | 4.8389 | MHz |
| | | fck=6.2208MHz | 6.2201 | 6.2208 | 6.2214 | MHz |
| H level output current | IOH | ADO~7 | | | 0.1 | mA |
| | | CPout | | | 0.1 | mA |
| L level output current | IOL | ADO~7 | | | 0.4 | mA |
| | | CPout | | | 0.4 | mA |
| H level input current | IIH | Except PGAIN.CPIN | -10 | | 10 | uA |
| | | PGAIN.CPIN | 25 | | 120 | uA |
| L level input current | IIL | Except PGAIN.CPIN | -10 | | 10 | uA |
| | | PGAIN.CPIN | -120 | | -25 | uA |
| Enable Time | tPZL | ADO~7<br>RL=10 kΩ, CL=30PF | | | 200 | nS |
| Disable Time | tPLZ | ADO~7 | | | 200 | nS |
| Setup Time | tsetup | CSN, SEL→WRN | | | 50 | nS |
| | | WDO~3→WRN | | | 100 | nS |
| Hold Time | thold | WRN→WDO~3, SEL | | | 40 | nS |

TIMING CHART




| | | |
|---|---|---|
| t setup (1) | CSN、SEL−WRN | 50nS |
| t setup (2) | WD0～3−WRN | 100nS |
| t hold | WRN−CSN, SEL, WD0～3 | 40nS |
| t w0 | WRN | 200nS |

RECEIVING FILTER (Lo/Hibit=0 : Fck=6.2208MHz)

| ITEM | CONDITION | | MIN. | TYP. | MAX. | 単位 |
|---|---|---|---|---|---|---|
| GAIN CHAR. | VDD=4.5V<br>VEE=-4.5V<br>Rxout<br>Rxin=0dBm | fin=60Hz | | -33 | -30 | dB |
| | | fin=300Hz | | -2.5 | -2 | dB |
| | | fin=1000Hz | -0.3 | 0 | 0.7 | dB |
| | | fin=3200Hz | -0.7 | 0 | 0.7 | dB |
| | | fin=5000Hz | | -25 | -22 | dB |
| | | fin=8000Hz | | -60 | -57 | dB |
| GROUP DELAY DIST. DIFF. | VDD=4.5, VEE=-4.5V Rxin=0dBm<br>Rxout, NO EQUALIZING | fin=800 ~3000Hz DIFF. | | 120 | | μs |
| | VDD=4.5, VEE=-4.5V Rxin=0dBm<br>Rxout JAPAN ILINK COMP. EQUALIZING | 600-2000Hz DIFF. | 166 | 266 | 366 | μs |
| | | 3200-2000Hz DIFF. | 366 | 466 | 566 | μs |
| INPUT LEVEL | VDD=4.5V VEE=-4.5V Rxin.Opin1.OPin2 | | -48 | | 0 | dBm |
| OFFSET VOLTAGE | VDD=5.5V.VEE=-5.5V Rxout.Opout1.2 | | -200 | | +200 | mV |
| DISTORTION | VDD=4.5V. VEE=-4.5V.RL=30KΩ.CL=80PF<br>fin=1000Hz | Rxout (10dBm) | | -47 | -35 | dB |
| | | Opout1.2 (0dBm) | | -85 | -55 | dB |
| OUTPUT IMPEDANCE | VDD=4.5V. VEE=-4.5V.<br>fin=1000Hz. RL=10KΩ | Rxout | | | 600 | Ω |
| | | Rxfin.Opout1.2 | | | 150 | Ω |

TRANSMITTING FILTER (Lo/Hibit=0 : Fck=6.2208MHz)

| ITEM | CONDITION | | | | | | MIN. | TYP. | MAX. | 単位 |
|---|---|---|---|---|---|---|---|---|---|---|
| GAIN CHAR. | AT3.AT4.AT2.AT1 = 0.0.0.0<br>VDD=4.5V<br>VEE=-4.5V<br>Txout<br>Txin=0dBm | fin=300Hz | | | | | 3.8 | 4.3 | 4.8 | dB |
| | | fin=1000Hz | | | | | 3.8 | 4.3 | 4.8 | dB |
| | | fin=3200Hz | | | | | 3.5 | 4.3 | 4.9 | dB |
| | | fin=5000Hz | | | | | | -29 | -24 | dB |
| | | fin=7000Hz | | | | | | -64 | -54 | dB |
| | | fin=9000Hz | | | | | | -64 | -54 | dB |
| | | fin=20000Hz | | | | | | -60 | -50 | dB |
| GROUP DELAY DIST. | VDD=4.5, VEE=-4.5V Txin=0dBm.Txout | fin=300 ~3000Hz | | | | | | 70 | | μs |
| INPUT LEVEL | VDD=4.5V. VEE=-4.5V TXin | | | | | | | | 0 | dBm |
| OFFSET VOLTAGE | VDD=5.5V. VEE=-5.5V TXout | | | | | | -300 | | 300 | mV |
| DISTORTION | VDD=4.5V. VEE=-4.5VMAX GAIN TXout.fin=1000Hz | | | | | | | -47 | -40 | dB |
| ATT. RATIO | VDD=4.5V<br>VEE=-4.5V Txout<br>1dB STEP | AT3 | AT4 | AT2 | AT1 | | | | | |
| | | 0 | 0 | 0 | 0 | | 3.8 | 4.3 | 4.8 | dB |
| | | 0 | 0 | 0 | 1 | | 2.8 | 3.3 | 3.8 | dB |
| | | 0 | 0 | 1 | 0 | | 1.8 | 2.3 | 2.8 | dB |
| | | 0 | 1 | 0 | 0 | | -0.2 | 0.3 | 0.8 | dB |
| | | 1 | 0 | 0 | 0 | | -4.2 | -3.7 | -3.2 | dB |
| | | 1 | 1 | 1 | 1 | | -11.2 | -10.7 | -10.2 | dB |
| ATT. STEP | VDD=4.5V. VEE=-4.5V Txout.fin=1000Hz | | | | | | -0.75 | 1.0 | 1.25 | dB |
| OUTPUT IMPEDANCE | VDD=4.5V. VEE=-4.5V.fin=1KHz. RL=10KΩ.Txout | | | | | | | | 600 | Ω |

RECEIVING FILTER (Lo/Hibit=1 ; Fck=4.8384MHz)

| ITEM | CONDITION | | MIN. | TYP. | MAX. | 単位 |
|---|---|---|---|---|---|---|
| GAIN CHAR. | VDD=4.5V<br>VEE=-4.5V<br>Rxout<br>Rxin=0dBm | fin=60Hz | | -35 | -30 | dB |
| | | fin=300Hz | | -2.5 | -2 | dB |
| | | fin=1000Hz | -0.3 | 0 | 0.7 | dB |
| | | fin=3200Hz | -0.7 | 0 | 0.7 | dB |
| | | fin=5000Hz | | -25 | -22 | dB |
| | | fin=8000Hz | | -60 | -57 | dB |
| GROUP DELAY DIST. DIFF. | VDD=4.5, VEE=-4.5V Rxin=0dBm<br>Rxout , NO EQUALIZING | fin=800 ~3000Hz DIFF. | | 120 | | μs |
| | VDD=4.5, VEE=-4.5V Rxin=0dBm<br>Rxout JAPAN ilink comp. equalizing | 600-2000Hz DIFF. | 166 | 266 | 366 | μs |
| | | 3200-2000Hz DIFF. | 368 | 468 | 568 | μs |
| INPUT LEVEL | VDD=4.5V VEE=-4.5V Rxin.Opin1.OPin2 | | -48 | | 6 | dBm |
| OFFSET VOLTAGE | VDD=5.5V.VEE=-5.5V Rxout.Opout1.2 | | -200 | | +200 | mV |
| DISTORTION | VDD=4.5V, VEE=-4.5V.RL=30KΩ.CL=30PF<br>fin=1000Hz | Rxout (10dBm) | | -47 | -35 | dB |
| | | Opout1.2 (0dBm) | | -35 | -55 | dB |
| output impedance | VDD=4.5V, VEE=-4.5V,<br>fin=1000Hz, RL=10KΩ | Rxout | | | 600 | Ω |
| | | Rxfin.Opout1.2 | | | 150 | Ω |

TRANSMITTING FILTER (Lo/Hibit=1 ; Fck=4.8384MHz)

| ITEM | CONDITION | | | | | MIN. | TYP. | MAX. | 単位 |
|---|---|---|---|---|---|---|---|---|---|
| GAIN CHAR. | AT8.AT4.AT2.AT1 = 0.0.0.0<br>VDD=4.5V<br>VEE=-4.5V<br>Txout<br>Txin=0dBm | fin=300Hz | | | | -3.0 | -2.5 | -2.0 | dB |
| | | fin=1000Hz | | | | -3.0 | -2.5 | -2.0 | dB |
| | | fin=3200Hz | | | | -3.3 | -2.5 | -1.9 | dB |
| | | fin=5000Hz | | | | | -38 | -30 | dB |
| | | fin=7000Hz | | | | | -70 | -60 | dB |
| | | fin=9000Hz | | | | | -70 | -60 | dB |
| | | fin=20000Hz | | | | | -65 | -55 | dB |
| GROUP DELAY DIST. | VDD=4.5, VEE=-4.5V Txin=0dBm.Txout | fin=300 ~3000Hz | | | | | 70 | | μs |
| INPUT LEVEL | VDD=4.5V, VEE=-4.5V TXin | | | | | | | 6 | dBm |
| OFFSET VOLTAGE | VDD=5.5V, VEE=-5.5V TXout | | | | | -300 | | 300 | mV |
| DISTORTION | VDD=4.5V, VEE=-4.5V MAX GAIN TXout.fin=1000Hz | | | | | | -47 | -40 | dB |
| ATT. ratio | VDD=4.5V<br>VEE=-4.5V Txout<br>1dB STEP | AT8 | AT4 | AT2 | AT1 | | | | |
| | | 0 | 0 | 0 | 0 | -3.0 | -2.5 | -3.0 | dB |
| | | 0 | 0 | 0 | 1 | -4.0 | -3.5 | -3.0 | dB |
| | | 0 | 0 | 1 | 0 | -5.0 | -4.5 | -4.0 | dB |
| | | 0 | 1 | 0 | 0 | -7.0 | -6.5 | -6.0 | dB |
| | | 1 | 0 | 0 | 0 | -11.0 | -10.5 | -10.0 | dB |
| | | 1 | 1 | 1 | 1 | -18.0 | -17.5 | -17.0 | dB |
| ATT. STEP | VDD=4.5V, VEE=-4.5V Txout.fin=1000Hz | | | | | -0.75 | 1.0 | 1.25 | dB |
| OUTPUT IMPEDANCE | VDD=4.5V, VEE=-4.5V.fin=1KHz, RL=10KΩ.Txout | | | | | | | 600 | Ω |

AGC (Programable Gain Amp.)

| ITEM | CONDITION | | | | | | fck=6.2208MHz Lo/Hi=0 | | | fck=4.8384MHz Lo/Hi=1 | | | 単 位 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| GAIN CHAR. | PGA1 | PGA4 | PGA3 | PGA2 | PGA1 | PGA0 | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | |
| VDD=4.5V | 0 | 0 | 0 | 0 | 0 | 0 | -8.05 | -7.8 | -7.55 | -5.25 | -5.0 | -4.75 | dB |
| VEE=-4.5V | 0 | 0 | 0 | 0 | 0 | 1 | -7.3 | -7.05 | -6.8 | -4.5 | -4.25 | -4.0 | dB |
| 0.75dB STEP | 0 | 0 | 0 | 0 | 1 | 0 | -6.55 | -6.3 | -6.05 | -3.75 | -3.5 | -3.25 | dB |
| Gain=-7.8 | 0 | 0 | 0 | 1 | 0 | 0 | -5.05 | -4.8 | -4.55 | -2.25 | -2.0 | -1.75 | dB |
| +0.75$I | 0 | 0 | 1 | 0 | 0 | 0 | -2.05 | -1.8 | -1.55 | 0.75 | 1.0 | 1.25 | dB |
| (I=0.1,…,83) | 0 | 1 | 0 | 0 | 0 | 0 | 3.95 | 4.2 | 4.45 | 6.75 | 7.0 | 7.25 | dB |
| GAIN DIFF. | 1 | 0 | 0 | 0 | 0 | 0 | 15.95 | 16.2 | 16.45 | 18.75 | 19.0 | 19.25 | dB |
| ±0.30 | 1 | 1 | 1 | 1 | 1 | 1 | 39.2 | 39.45 | 39.7 | 42.0 | 42.25 | 42.5 | dB |
| STEP DIFF. | | | | | | | 0.5 | 0.75 | 1.0 | 0.5 | 0.75 | 1.0 | dB |

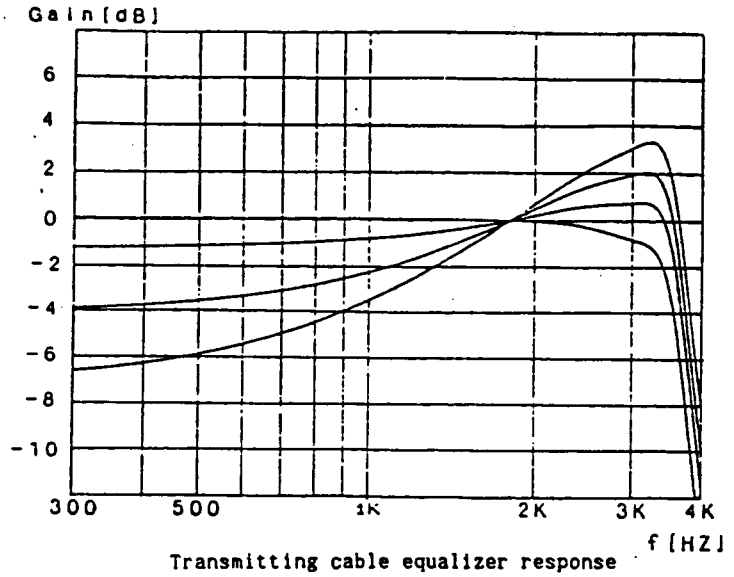
AD CONVERTER

| ITEM | CONDITION | MIN. | TYP. | MAX. | 単 位 |
|---|---|---|---|---|---|
| RESOLUTION | | | 8 | | bit |
| CONVERSION RANGE | VDD=5.0V<br>VRef+ = 5.0V AD7~AD0=00(H)<br>VRef- = -5.0V AD7~AD0=FF(H)<br>$1LSB = \frac{VFF-V00}{255}$ | | -2.5<br>+2.5 | | V |

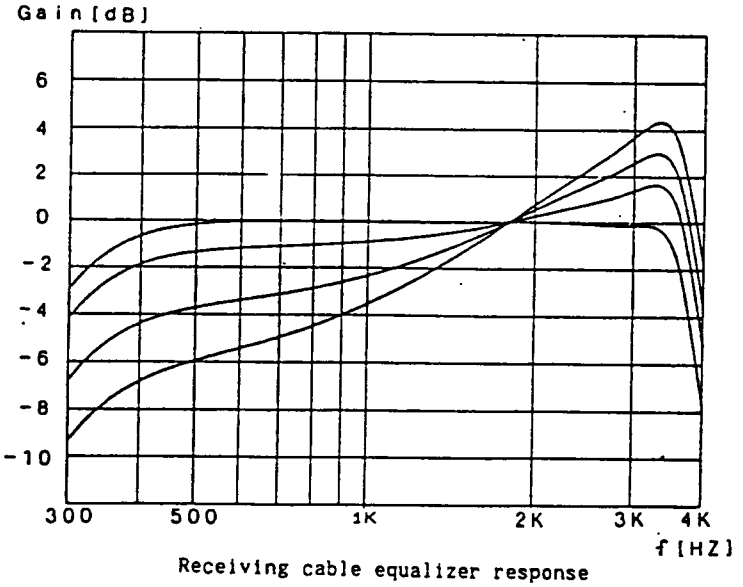
DA CONVERTER

| ITEM | CONDITION | MIN. | TYP. | MAX. | 単 位 |
|---|---|---|---|---|---|
| RESOLUTION | | | 8 | | bit |
| CONVERSION RANGE | VDD=5.0V<br>VRef+ = 5.0V AD7~DA0=00(H)<br>VRef- = -5.0V AD7~DA0=FF(H)<br>$1LSB = \frac{VFF-V00}{255}$ | | -2.5<br>+2.5 | | V |

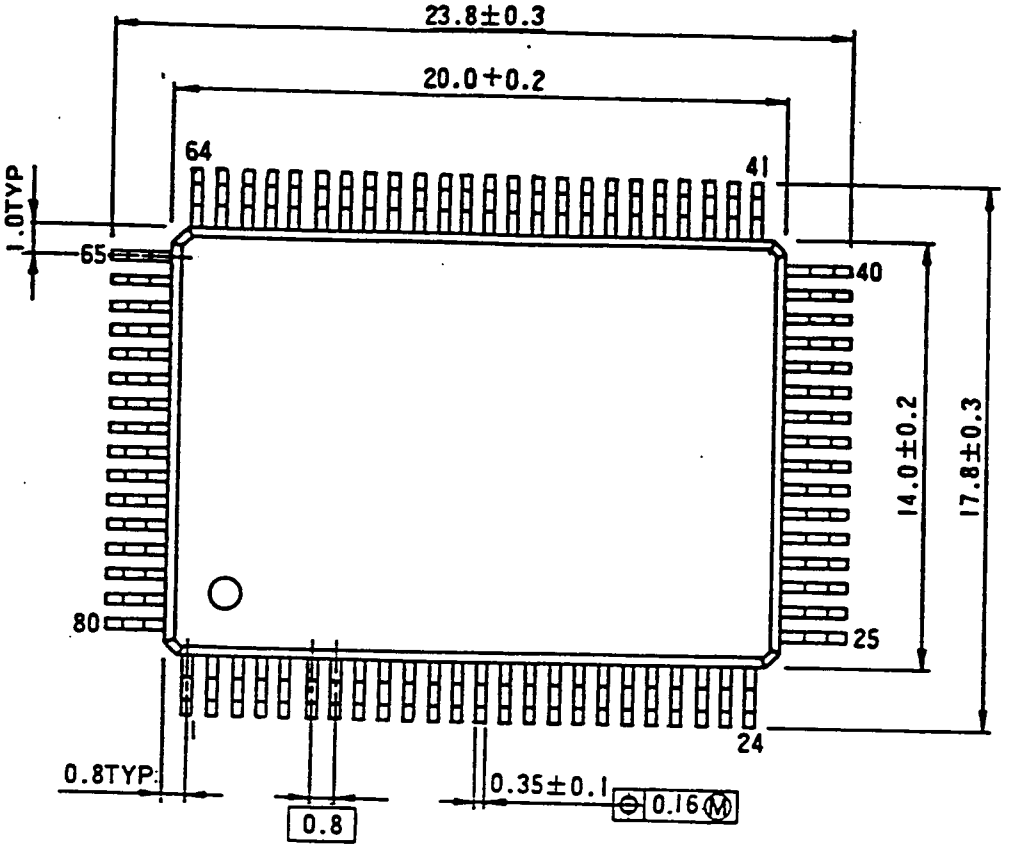
CABLE EQUALIZER RESPONSE

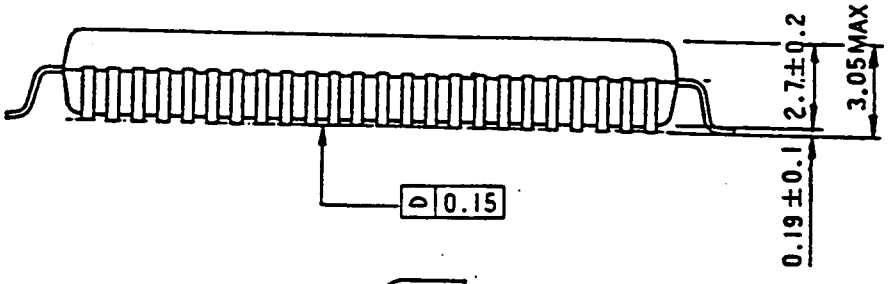


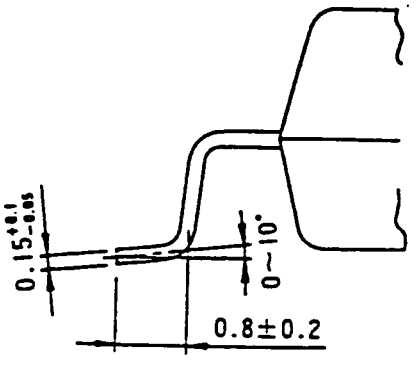

Transmitting cable equalizer response

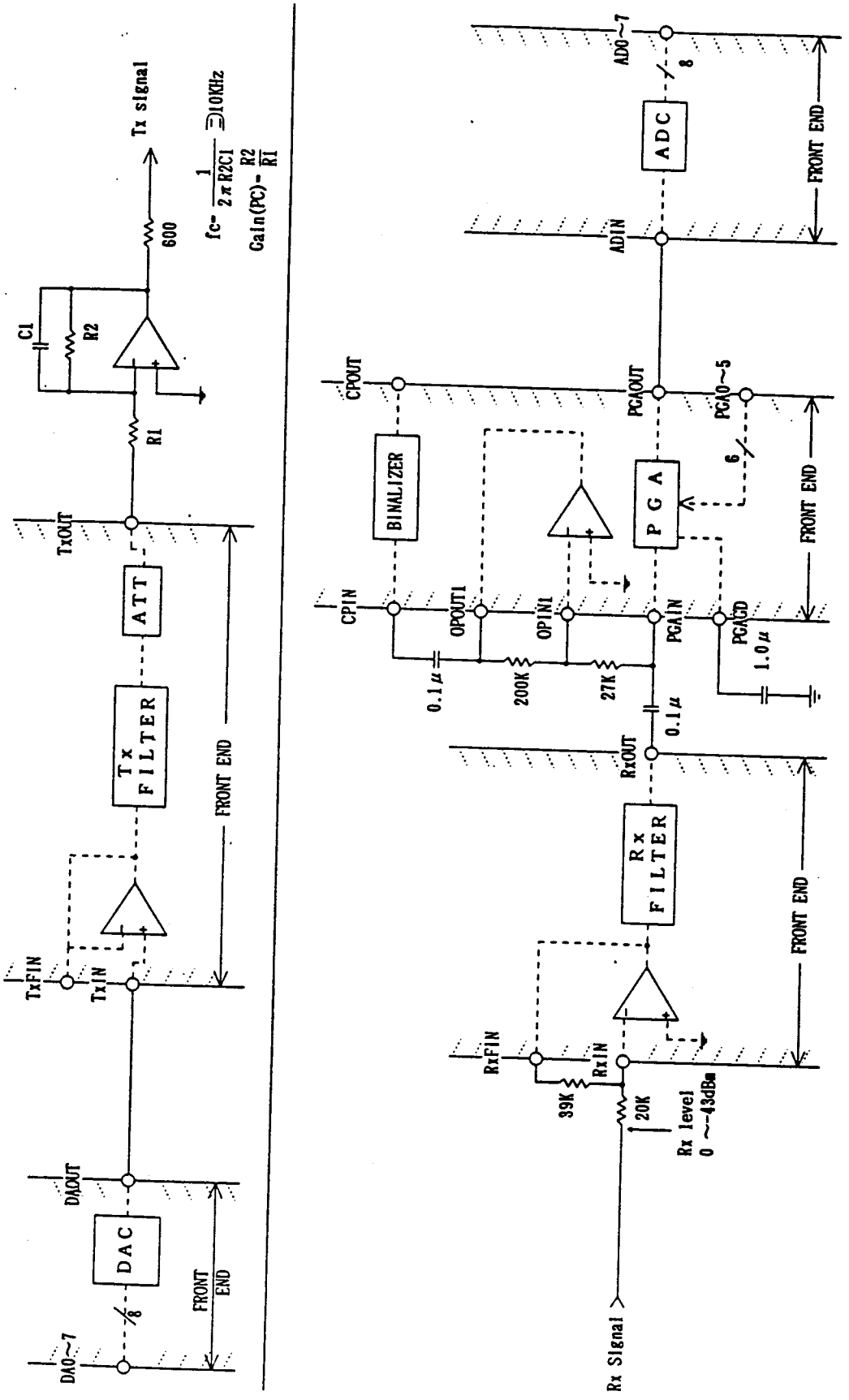



Receiving cable equalizer response


23.8±0.3
20.0±0.2
64
41
1.0TYP
65
40
14.0±0.2
17.8±0.3
80
25
1
24
0.8TYP
0.8
0.35±0.1
0.16 M


2.7±0.2
3.05MAX
0.15
0.19±0.1

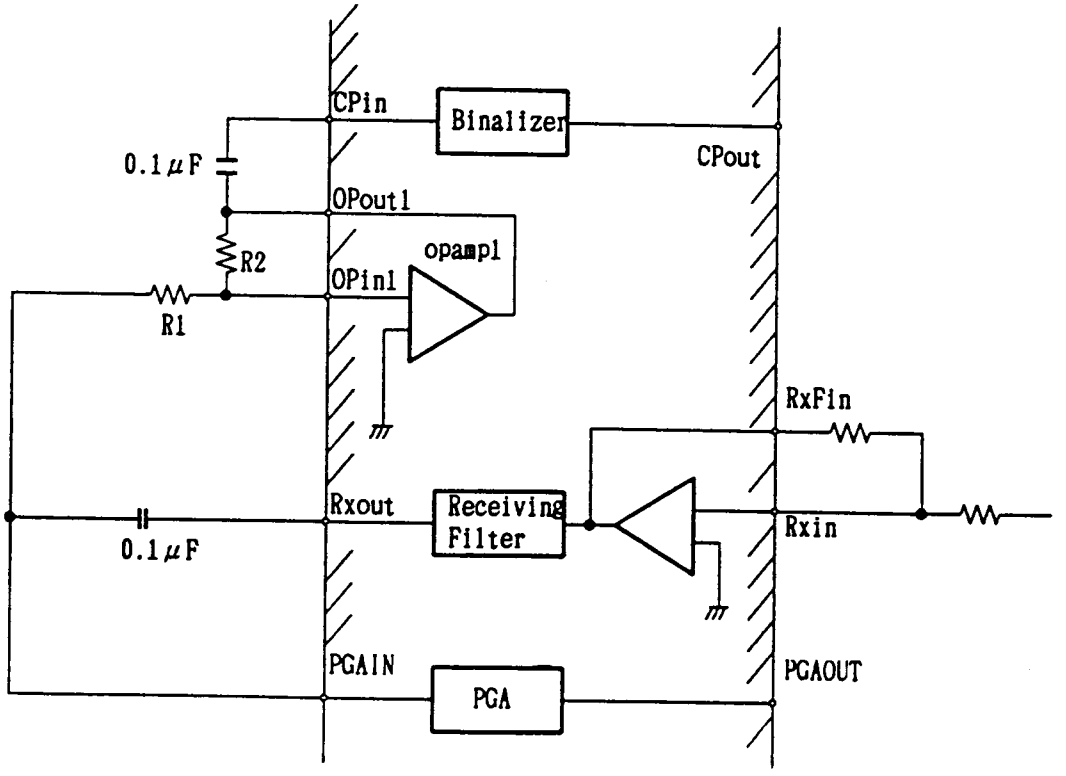

0.15
0~10°
0.8±0.2

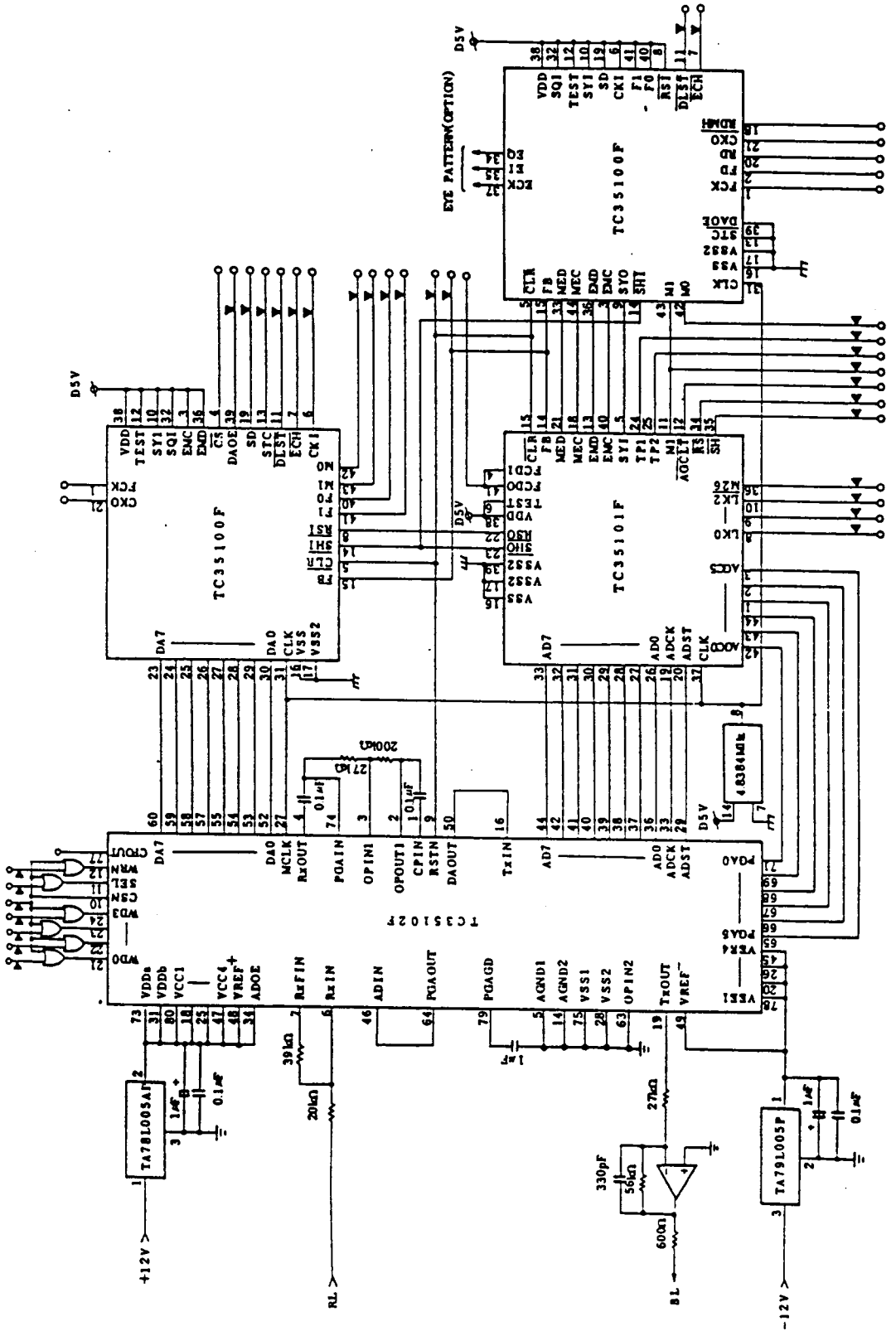

Tx signal
600
fc= 1/2πR2C1 ≒10KHz
Gain(PC)= R2/R1
C1
R2
R1
TxOUT
ATT
Tx FILTER
FRONT END
TxFIN
TxIN
DAOUT
DAC
8
FRONT END
DA0~7
AD0~7
8
ADC
FRONT END
ADIN
CPOUT
PGAOUT
PGA0~5
6
BINALIZER
P G A
FRONT END
CPIN
OPOUT1
OPIN1
PGAIN
PGACD
1.0μ
0.1μ
200K
27K
0.1μ
RxOUT
Rx FILTER
FRONT END
RxFIN
RxIN
39K
20K
Rx level
0 ~-43dBm
Rx Signal

## For setting of binarised detection level

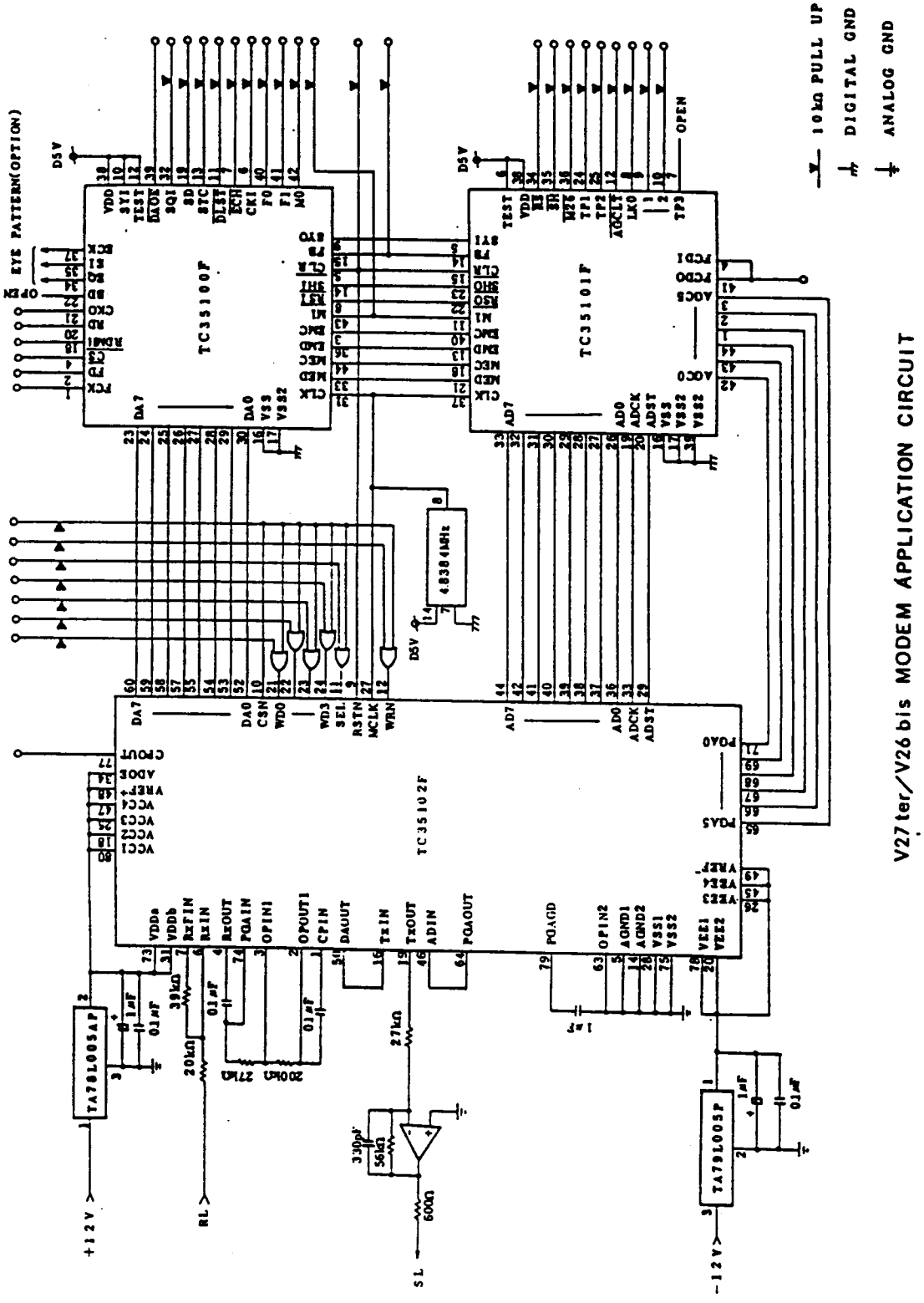
TC35102F converts inputed tone signal from CPin above -20.8±2dBm in range of ±5.0±10% supply voltage to TTL level. Binarized detection level of tone signal is determined by R1 and R2 which is added to binarized circuit and opamp1.

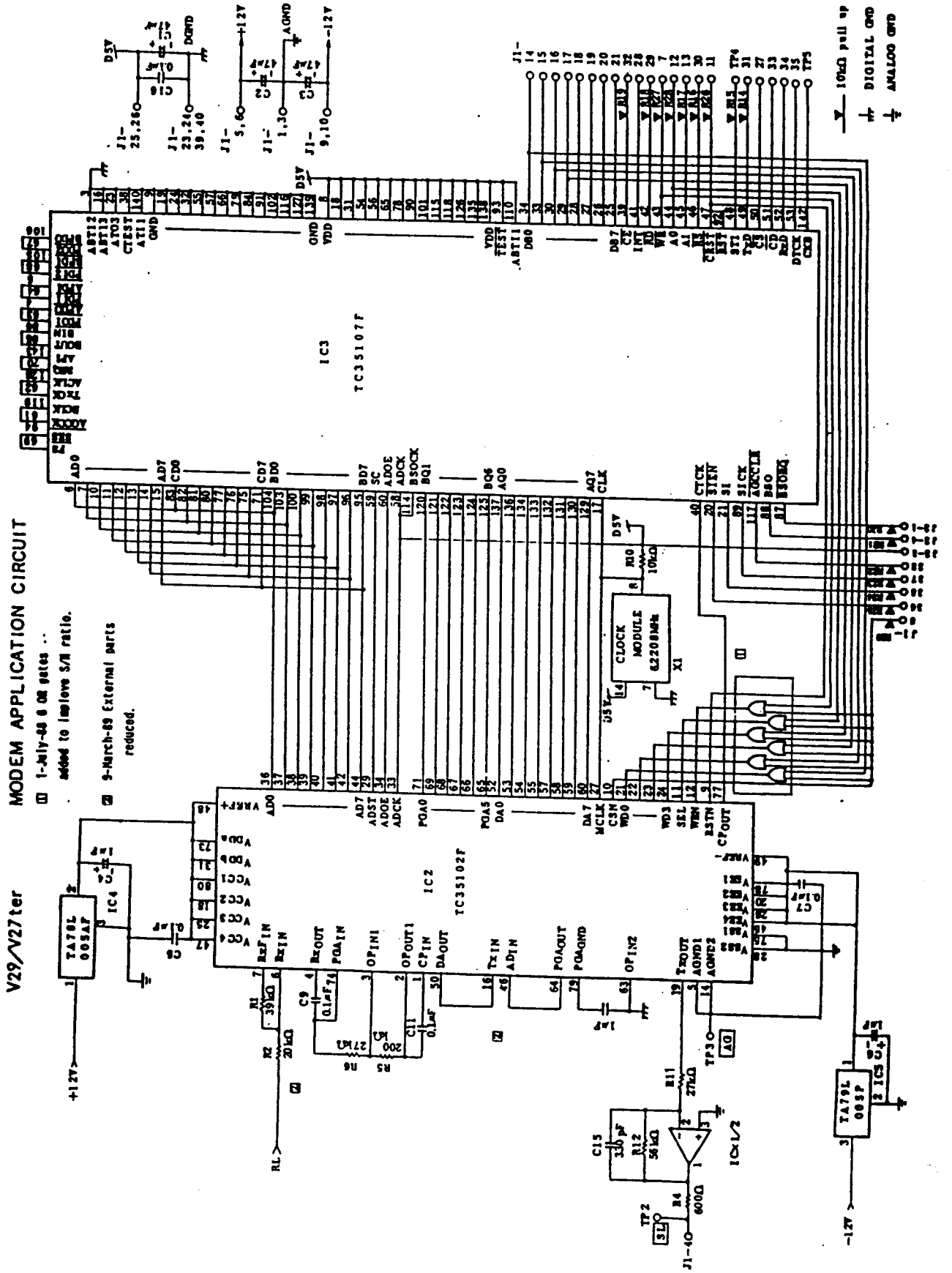
(ex)detection level above -43dBm (supply voltage ±5.0±10%V)
43dBm*18.8dB=24.2dB
R2/R1=17.7(25dB)
R1=27kohm (select R1≧15kohm)
R2=480kohm






V27
V27 bis/V26
V27 ter/V26 bis 4-Wire FULL DUPLEX MODEM
APPLICATION CIRCUIT


10kΩ PULL UP
DIGITAL GND
ANALOG GND
EYE PATTERN(OPTION)
TC35100F
TC35101F
TC35102F
4.8384MHz
TA78L005AP
+12V
-12V
RL
SL
V27 ter/V26 bis MODEM APPLICATION CIRCUIT


MODEM APPLICATION CIRCUIT
V29/V27ter
IC3 TC35107F
IC2 TC35102F
CLOCK MODULE
X1
IC4
IC1×1/2
1-July-88 8 OR gates ..
added to improve S/N ratio.
9-March-89 External parts
reduced.

## Noise Characteristic

| Noise Source | | Neutral | Sensitive | |
|---|---|---|---|---|
| H | L | | H | L |
| 9 : SEL | 10 : RSTN | 5 : AGND1 | 1 : CPIN | 2 : OPOUT2 |
| 12 : WRN | 11 : CSN | 14 : AGND2 | 3 : OPIN1 | 4 : RXOUT |
| 21 : WD0 | 36 : AD0 | 28 : VSS1 | 7 : RXIN | 6 : RXFIN |
| 22 : WD1 | 37 : AD1 | 75 : VSS2 | 16 : TXIN | 15 : TXFIN |
| 23 : WD2 | 38 : AD2 | 18 : VCC2 | 46 : ADIN | 19 : TXOUT |
| 24 : WD3 | 39 : AD3 | 25 : VCC3 | 48 : VREF+ | 50 : DAOUT |
| 27 : MCLK | 40 : AD4 | 31 : VDDb | 49 : VREF− | 61 : OPOUT2 |
| 29 : ADST | 41 : AD5 | 47 : VCC4 | 63 : OPIN2 | 64 : PGAOUT |
| 33 : ADCK | 42 : AD6 | 73 : VDDa | 74 : PGAIN | |
| 34 : ADOE | 44 : AD7 | 80 : VCC1 | 79 : PGAGD | |
| 77 : CPOUT | 52 : DA0 | 20 : VEE2 | | |
| | 53 : DA1 | 26 : VEE3 | | |
| | 54 : DA2 | 45 : VEE4 | | |
| | 55 : DA3 | 78 : VEE1 | | |
| | 57 : DA4 | | | |
| | 58 : DA5 | | | |
| | 59 : DA6 | | | |
| | 60 : DA7 | | | |
| | 65 : PGA5 | | | |
| | 66 : PGA4 | | | |
| | 67 : PGA3 | | | |
| | 68 : PGA2 | | | |
| | 69 : PGA1 | | | |
| | 71 : PGA0 | | | |

1)Voltage source terminals should be connected each and all.
2)NC pins should be open.
3)Analog signal line and voltage source line should be as wide as possible , more than 0.05 inch.
4)Separate analog signal line from degital one.
5)Shield MCLK signal line from other signal lines with AGND .
6)Following signal lines should be short particularly.