

TC35095P 8 BIT 8-CH SERIAL I/O ANALOG TO DIGITAL CONVERTER

GENERAL DESCRIPTION

The TC35095P is a monolithic CMOS 8 bit successive approximation A/D converter with serial I/O and 8 channel multiplex inputs.

Conversion start when $\overline{CS}$ is set low and start bit ("L" level) and channel select bit (three bits) are given to serial input DI.

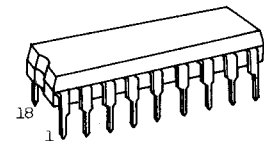
In case that $\overline{SE}$ is high, as soon as the conversion starts a start bit ("L" level) appears at serial output DO and 8 bit conversion data (MSB first) and a stop bit ("H" level) follow continuously.

In case that $\overline{SE}$ is low, after the conversion is completed a start bit, 8 bit conversion data (LSB first) and a stop bit appear at DO.

The TC35095P has features of high speed, high accuracy and microprocessor compatible I/O which make the device well suited to a broad application field such as process and machine control and automotive equipment.

FEATURES

- High accuracy $\pm \frac{3}{4}$ LSB MAX
- High speed conversion 35 μ sec MAX @f_{CP}=400kHz
- Single Power supply 5V $\pm$ 10%
- Low Power consumption 5mW MAX @T_a=25°C
- Serial I/O
- 8 channel analog multiplex input
- Easy interface to all microprocessors
- 3-state output
- Zero or full scale adjustment free

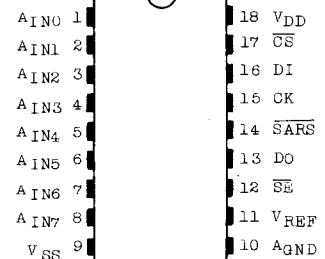


DIP18(3D18A-P)

ABSOLUTE MAXIMUM RATINGS

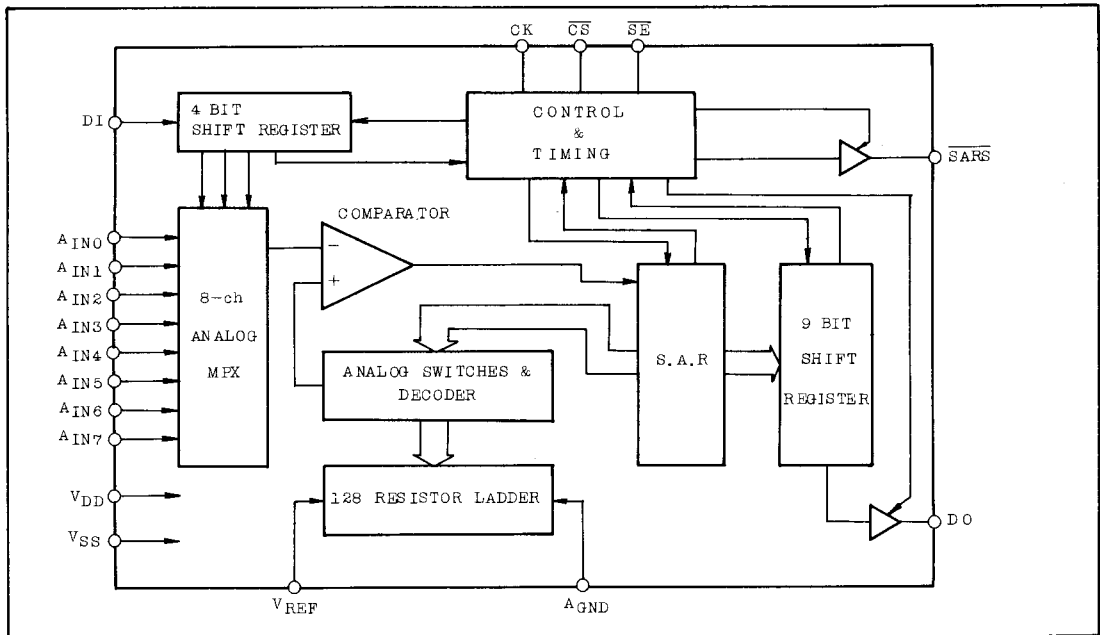
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V _{DD}	V _{SS} -0.5~V _{SS} +7	V
DC Input Voltage	V _{IN}	V _{SS} -0.5~V _{DD} +0.5	V
DC Output Voltage	V _{OUT}	V _{SS} -0.5~V _{DD} +0.5	V
Reference Voltage	V _{REF}	V _{SS} -0.5~V _{DD} +0.5	V
Analog Ground Voltage	A _{GND}	V _{SS} -0.5~V _{DD} +0.5	V
DC Input Current	I _{IN}	±10	mA
Power Dissipation	P _D	300	mW
Storage Temperature	T _{stg}	-65 ~ 150	°C
Lead Temperature 10sec.	T _L	300	°C

PIN ASSIGNMENT

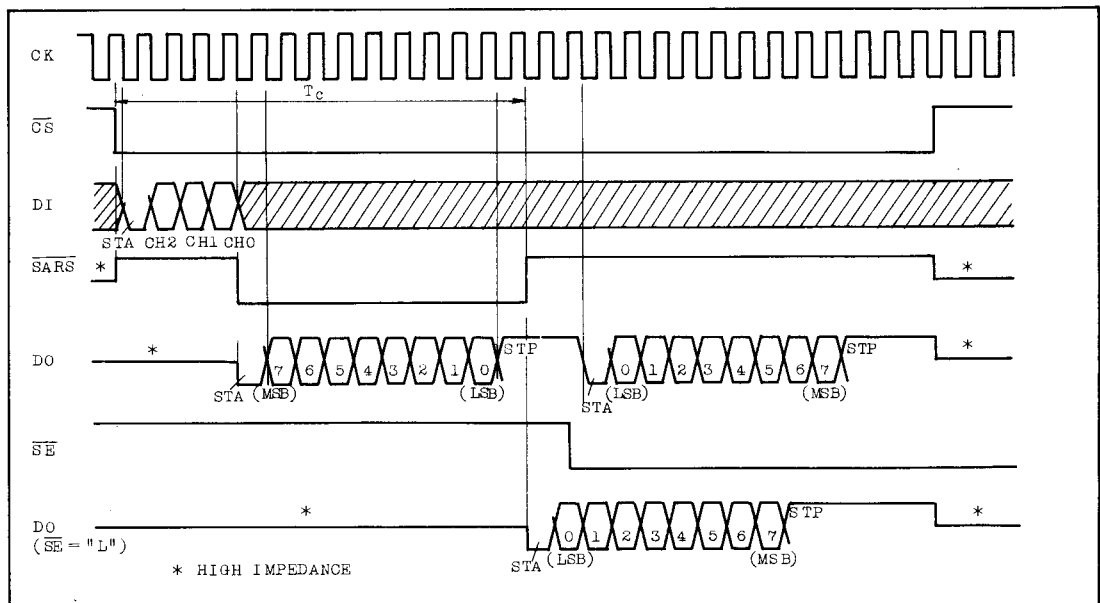


(TOP VIEW)

BLOCK DIAGRAM



TIMING CHART



PIN & FUNCTION

PIN NO.	SYMBOL	PIN NAME & FUNCTION	PIN NO.	SYMBOL	PIN NAME & FUNCTION																																							
1	A _{IN0}	[ANALOG INPUT] One of A_{IN0} ~ A_{IN7} is selected according to the serial channel select bit applied on DI input. Full range of input signal is to be from A_{GND} to V_{REF}. <table><tr><th rowspan="2">ON Channel</th><th colspan="3">DI Serial Data</th></tr><tr><th>CH2</th><th>CH1</th><th>CH0</th></tr><tr><td>A_{IN0}</td><td>L</td><td>L</td><td>L</td></tr><tr><td>A_{IN1}</td><td>L</td><td>L</td><td>H</td></tr><tr><td>A_{IN2}</td><td>L</td><td>H</td><td>L</td></tr><tr><td>A_{IN3}</td><td>L</td><td>H</td><td>H</td></tr><tr><td>A_{IN4}</td><td>H</td><td>L</td><td>L</td></tr><tr><td>A_{IN5}</td><td>H</td><td>L</td><td>H</td></tr><tr><td>A_{IN6}</td><td>H</td><td>H</td><td>L</td></tr><tr><td>A_{IN7}</td><td>H</td><td>H</td><td>H</td></tr></table>	ON Channel	DI Serial Data			CH2	CH1	CH0	A _{IN0}	L	L	L	A _{IN1}	L	L	H	A _{IN2}	L	H	L	A _{IN3}	L	H	H	A _{IN4}	H	L	L	A _{IN5}	H	L	H	A _{IN6}	H	H	L	A _{IN7}	H	H	H	10	A _{GND}	[ANALOG GROUND] A _{GND} defines the zero level of A _{IN} .
ON Channel	DI Serial Data																																											
	CH2		CH1	CH0																																								
A _{IN0}	L		L	L																																								
A _{IN1}	L		L	H																																								
A _{IN2}	L		H	L																																								
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A _{IN4}	H		L	L																																								
A _{IN5}	H	L	H																																									
A _{IN6}	H	H	L																																									
A _{IN7}	H	H	H																																									
2	A _{IN1}	11	V _{REF}	[REFERENCE VOLTAGE] V _{REF} defines the full scale of A _{IN} .																																								
3	A _{IN2}	12	$\overline{SE}$	[SELECT INPUT] $\overline{SE}$ determines the order of output data. $\overline{SE}$ ="L" LSB first $\overline{SE}$ ="H" MSB first																																								
4	A _{IN3}	13	DO	[DATA OUTPUT] Output data is sent out in series.																																								
5	A _{IN4}	14	$\overline{SARS}$	[SAR STATUS] When a start bit ("L" level) is detected at DI input, $\overline{SARS}$ is set "L" level and conversion starts. When conversion is completed $\overline{SARS}$ returns to "H" level.																																								
6	A _{IN5}	15	CK	[CLOCK INPUT] Basic system clock. Duty cycle is to be 50%.																																								
7	A _{IN6}	16	DI	[DATA INPUT] For starting the conversion a start bit ("L" level) and channel select bit (from CH2 to CH0 in order) are to be applied.																																								
8	A _{IN7}	17	$\overline{CS}$	[CHIP SELECT] At the falling edge of $\overline{CS}$, the device is set stand-by for conversion. When $\overline{CS}$ is "H" the device is reset and all outputs become high impedance.																																								
9	V _{SS}	[DIGITAL GROUND]	18	V _{DD}	[Power Supply] 5V ± 10%																																							

RECOMMENDED OPERATING CONDITIONS ($V_{SS}=0V$)

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Reference Voltage	V_{REE}	$V_{DD}=5V$, $AGND=0V$	2.0	V_{DD}	V_{DD}	V
Analog Ground Voltage	$AGND$	$V_{DD}=5V$, $V_{REF}=5V$	0.0	0.0	3.0	V
Voltage Between V_{REF} and $AGND$		$V_{DD}=5V \pm 10\%$	2.0	V_{DD}	V_{DD}	V
Clock Frequency	f_{cp}	$V_{DD}=5V \pm 10\%$	-	-	400	kHz
Clock Pulse Width	$t_w(H)$ $t_w(L)$	$V_{DD}=5V \pm 10\%$	0.63	1.25	-	μS
Operating Temperature	T_{opr}		-40	-	+85	$^{\circ}C$

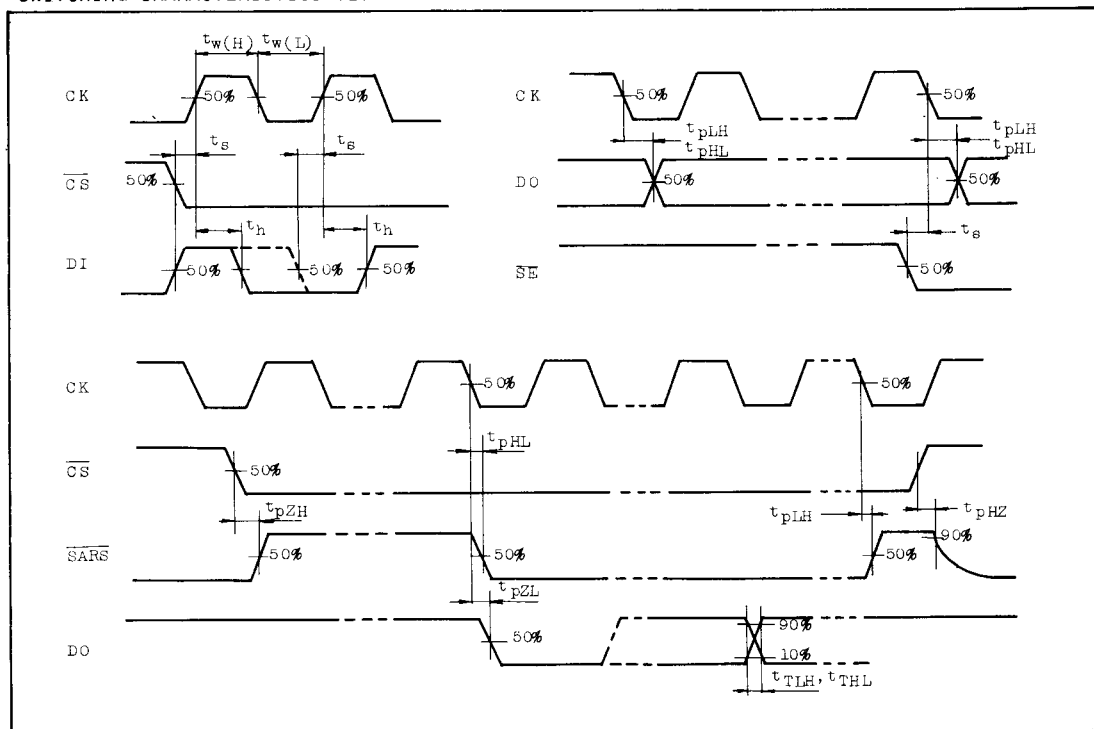
DC ELECTRICAL CHARACTERISTICS ($V_{DD}=5V \pm 10\%$, $V_{SS}=0V$)

PARAMETER	SYMBOL	TEST CONDITION	25 $^{\circ}C$			-40 ~ 85 $^{\circ}C$		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage	V_{OH}	$ I_{OUT} < 1\mu A$ $V_{IN}=V_{SS}, V_{DD}$	$V_{DD}-0.05$	V_{DD}	-	$V_{DD}-0.05$	-	V
Low Level Output Voltage	V_{OL}	$ I_{OUT} < 1\mu A$ $V_{IN}=V_{SS}, V_{DD}$	-	0.00	0.05	-	0.05	V
High Level Output Current	I_{OH}	$V_{OH}=V_{DD}-0.4V$ $V_{IN}=V_{SS}, V_{DD}$	-0.44	-	-	-0.36	-	mA
Low Level Output Current	I_{OL}	$V_{OL}=0.4V$ $V_{IN}=V_{SS}, V_{DD}$	2.0	-	-	1.6	-	mA
High Level Input Voltage	V_{IH}	$ I_{OUT} < 1\mu A$ $V_{OUT}=0.5V$, $V_{DD}-0.5V$	$0.7 \times V_{DD}$	-	-	$0.7 \times V_{DD}$	-	V
Low Level Input Voltage	V_{IL}	$ I_{OUT} < 1\mu A$ $V_{OUT}=0.5V$, $V_{DD}-0.5V$		-	$0.3 \times V_{DD}$	-	$0.3 \times V_{DD}$	V
3-State Output Disable Current	I_{DH} I_{DL}	$V_{OH}=V_{DD}$ or $V_{OL}=0.0V$		-	± 0.5	-	± 1	μA
Digital Input Current	I_{IH} I_{IL}	$V_{IH}=V_{DD}$ or $V_{IL}=0.0V$		-	± 0.3	-	± 1	μA
ON Channel Input Current	I_{ON}	$V_{IH}=V_{REF}$ or $V_{IL}=0.0V$ $f_{cp}=400kHz$	-	-	± 2	-	± 5	μA
OFF Channel Input Current	I_{OFF}	$V_{IH}=V_{DD}$ or $V_{IL}=0.0V$	-	-	± 0.2	-	± 1	μA
Operating Current	I_{DD}	$f_{cp}=400kHz$	-	-	1.1	-	1.4	mA
Reference Resistance	R_{REF}		1.4	2.6	3.8	1.2	4.2	k Ω

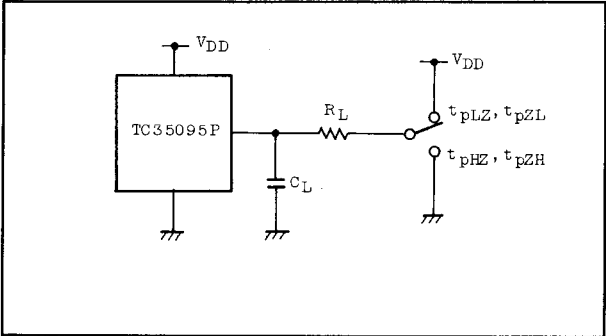
SWITCHING CHARACTERISTICS ($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, $T_a=25^\circ C$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}	$C_L=50pF$	-		100	nS
Propagation Delay Time (CK-Data)	t_{PLH} t_{PHL}	$C_L=50pF$	-		250	
Propagation Delay Time (CK- $\overline{SARS}$)	t_{PLH} t_{PHL}	$C_L=50pF$	-		250	
3-State Output Enable Time ($\overline{CS}-\overline{SARS}$, $\overline{SARS}$ -Data)	t_{pZH} t_{pZL}	$C_L=50pF$ $R_L=1k$	-		200	
3-State Output Disable Time ($\overline{CS}-\overline{SARS}$, Data)	t_{pHZ} t_{pLZ}		-		200	
Minimum Pulse Width ($\overline{CS}$)	$t_{w(H)}$	$C_L=50pF$	-		100	
Minimum Set-up Time ($\overline{CS}$, $\overline{SE}$, DI)	t_s	$C_L=50pF$	-		150	
Minimum Hold Time (DI)	t_h	$C_L=50pF$	-		50	
Input Capacitance	C_{IN1}	Digital Input	-	5	-	pF
Input Capacitance	C_{IN2}	Analog In(ON)	-	5	-	
Input Capacitance	C_{IN3}	Analog In(OFF)	-	5	-	
Output Capacitance	C_{OUT}	3-State Out	-	10	-	

SWITCHING CHARACTERISTICS TEST WAVEFORM



3-STATE OUTPUT TEST CIRCUIT



SYSTEM CHARACTERISTICS (T_a=−40 ~ 85°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Zero Point Error	E _{ZR}	V _{DD} =5.0V V _{REF} =5.000V f _{CP} =400kHz Duty=50%	−	±1/4	±1/2	LSB
Full Scale Error	E _{FS}		−	±1/4	±1/2	
Nonlinearity Error	E _{LI}		−	±1/4	−	
Total Error	E _T		−	±1/4	±3/4	
Conversion Time	T _C	f _{CP} =400kHz	−	35	36.5	μS

APPLICATION CIRCUIT (EXAMPLE)

$$T_c = \frac{14}{f_{cp}} \pm \alpha \quad 0 < \alpha < \frac{1}{2f_{cp}}$$

