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TSC332/333/334/335
Hex Inverter Gates

- 4-Inverter, 2-NAND (Open Collector)
- 4-Inverter, 2-NAND (Passive Pullup)
- Strobed Hex NAND (Open Collector)
- Strobed Hex NAND (Passive Pullup)

Features

332/333/334/335

- FOUR INVERTERS AND TWO GATES IN 332/333
- COLLECTOR OR'ABLE
- 332 SINKS UP TO 16 mA AT 12V and 20 mA AT 15V
- 332/334 OUTPUT LEVELS ADJUSTABLE TO DTL, TTL OR MOS LEVELS
- 333/335 HAS PULLUP RESISTORS ON CHIP

General Description

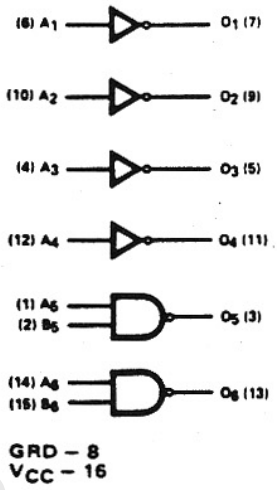
332/333/334/335

The 332 and 333 provide four inverters and two 2-input NAND gates for applications such as "wire-OR" logic systems and interfaces with other logic families. The 332 is used with an external pullup resistor while the 333 has pullup resistors on the chip.

The 334 and 335 contain six 2-input NAND gates connected such that two gates share one strobe input and four gates share another strobe input. The configuration is ideal for applications such as transferring data in parallel from one register to another. The devices may also be used in "wire-OR" logic systems and for the interfaces with other logic families.

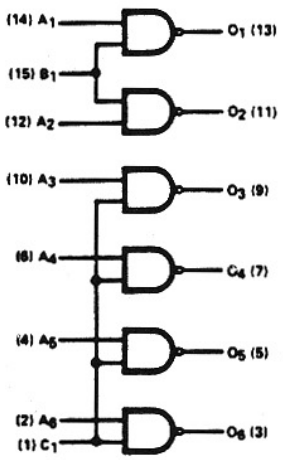
Logic Diagram

332/333



GRD – 8
V_{CC} – 16

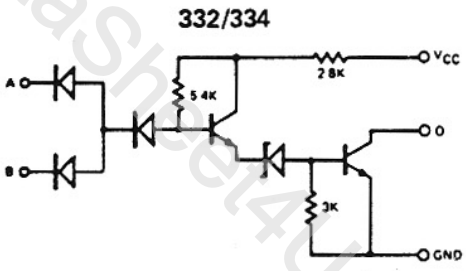
334/335



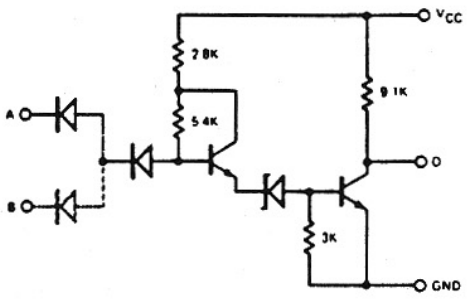
GRD – 8
V_{CC} – 16

Equivalent Circuits

332/334



333/335



Specifications

332/334

I_{CC} (WORST-CASE)	28 mA @ 13V, 42 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	140 ns A+O−	350 ns A−O+

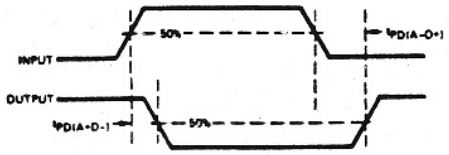
333/335

I_{CC} (WORST-CASE)	42 mA @ 13V, 60 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	140 ns A+O−	350 ns A−O−

NOTE:
I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range. t_{PD} is guaranteed at V_{CC} ±1V and across the applicable temp rage with the output loaded with 5 unit loads.

See page 12 for electrical summary data.

Switching Time Waveforms



Loading Tables

332/333

PINS	FUNCTION	LOADING
A,B	Inputs	1 UL
0	Outputs	5 UL (333) 7 UL (332 with 5 KΩ pullup resistor) 7 UL (333 with 10 KΩ supplemental pullup resistor)

332 also handles 4 TTL loads at 400 mV

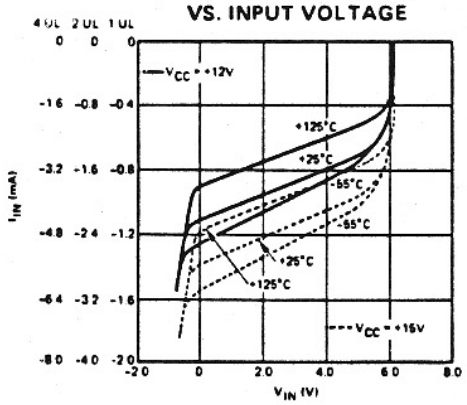
334/335

PINS	FUNCTION	LOADING
A	Data Inputs	1 UL
B	Strobe Input	2 UL
C	Strobe Input	4 UL
O	Outputs	5 UL (335) 7 UL (334 with 5 KΩ pullup resistor) 7 UL (335 with 10 KΩ supplemental pullup resistor)

334 also handles 4 TTL loads at 400 mV

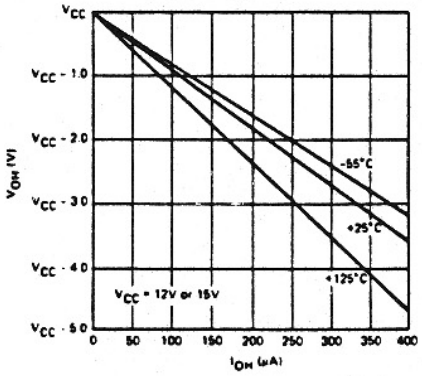
Typical Performance Characteristics

INPUT CURRENT VS. INPUT VOLTAGE

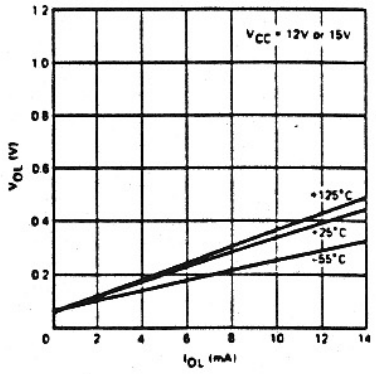


OUTPUT CURRENT VS OUTPUT VOLTAGE

OUTPUT HIGH*



OUTPUT LOW



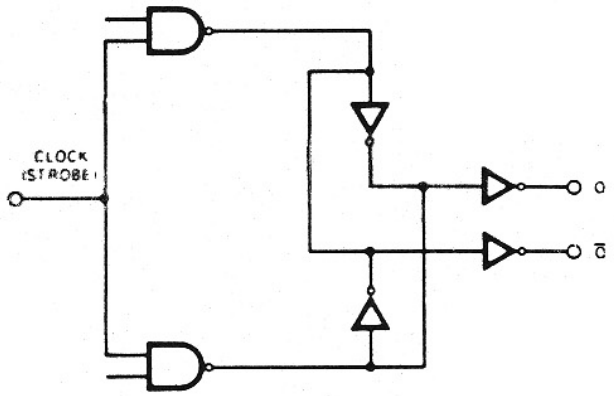
*333, 335 only

Typical Applications

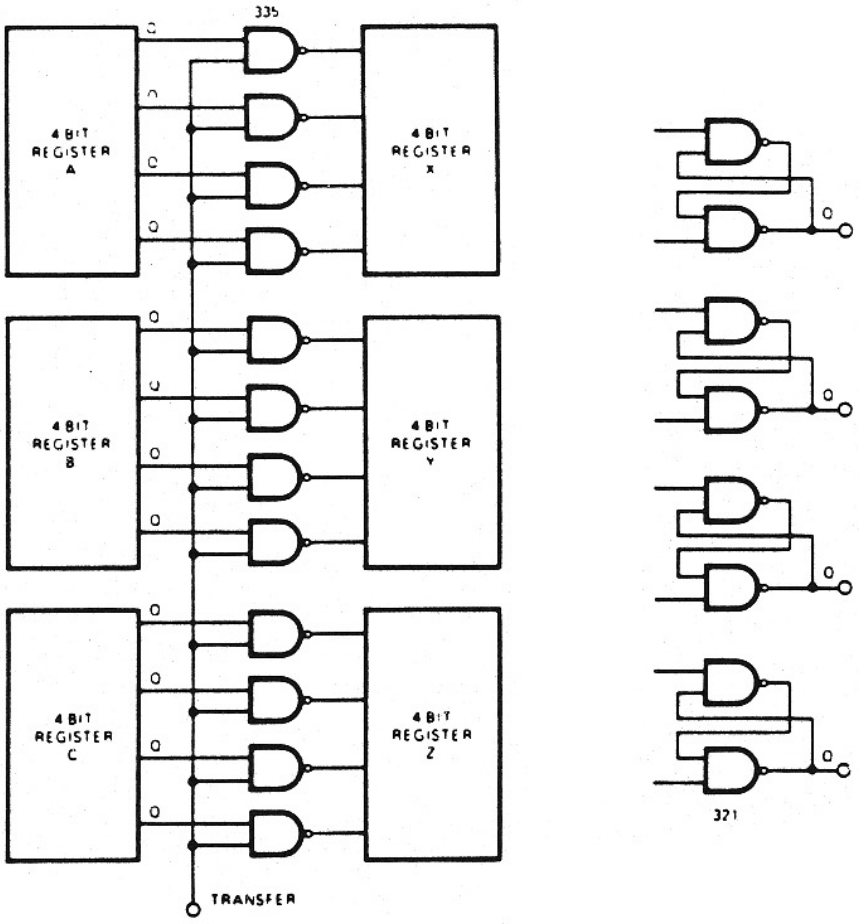
Rules for selecting external resistors and calculating fanout with collectors OR'd are given in the applications notes. The external resistor of the 332 or 334 may be connected to a voltage other than V_{CC} to adjust the output voltage level. To use the NAND gates as inverters, the A and B inputs may both be connected to the same input data line, or one input may be connected to V_{CC}.

For transfer of data, the strobe input is held high. Data on the A inputs of those gates will appear inverted on the outputs. When the strobe input is low, the outputs remain high. If the two strobe inputs are connected, six lines of data may be transferred with one strobe control (presenting 6 unit loads).

CLOCKED S-R FLIP-FLOP WITH BUFFERED OUTPUTS



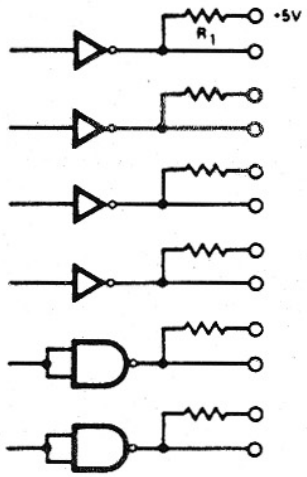
PARALLEL TRANSFER OF DATA



Two 335 strobed hex inverters transfer 12 lines in parallel from register A, B and C to register X, Y and Z when the strobe input (transfer line is momentarily taken high. The data inversion during transfer is circumvented by using the $\overline{Q}$ outputs of registers A, B and C. Each of these registers may be made with a pair of 321 quad NAND gates.

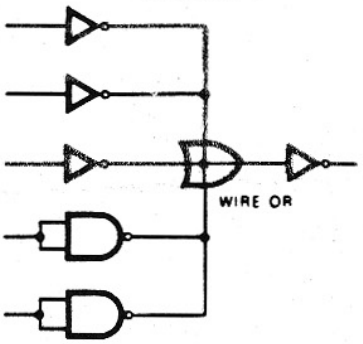
Typical Applications (contd.)

TTL INTERFACE
332

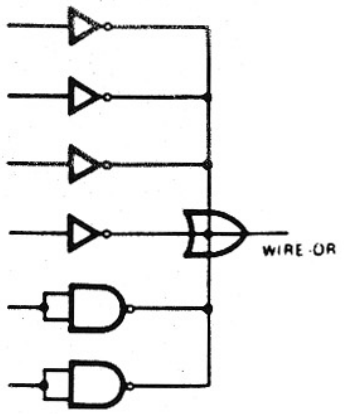


This type of interface will protect TTL data processing systems from electromechanical noise generated in peripherals. The value of R is selected by the rules given in the applications notes, except that pullup is to 5V rather than 12V or 15V V_{CC}.

FIVE-INPUT OR GATE
332/333



SIX-INPUT OR GATE
332/333



BIDIRECTIONAL BUSING (MEMORY SYSTEM EXAMPLE)