TOSHIBA

ASIC
DATA BOOK

TC200G/E SERIES

MACROCELLS
(Non-liner Delay Models)

1997

ASIC Data Book

TC200G/E SERIES MACROCELLS (Non-linear Delay Models)

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Preface

This databook was written for logic and system designers who wish to use the TC200G/E Series Gate Array From Toshiba Corporation.

TC200G/E Series Gate Array databook consist of the volumes listed below.

This databook contains the specifications for each cell in the Verilog-HDL sign-off libraries (for use with Verilog-XL, VCS, etc.) and VHDL sign-off libraries (for use with VITAL), including the number of grids used, load and drive characteristics, function, schematic symbol, and parameters used to compute propagation delay.

TC200/E SERIES Data Book Set

<table>
<tr><td>Delay Model</td><td>Non-linear Delay Model</td><td>Linear Delay Model</td><td rowspan="2">Cataloged Cell Type</td></tr>
<tr><td>Sign-Off</td><td>Customer</td><td>Toshiba VLCAD</td></tr>
<tr><td rowspan="3">Title</td><td>TC200G/E SERIES MACROCELLS
(Non-linear Delay Model)</td><td>TC200G/E SERIES MACROCELLS</td><td>• Internal Macrocells
• I/O Macrocells</td></tr>
<tr><td colspan="2">GATE ARRAY/EMBEDDED ARRAY MACROFUNCTIONS</td><td>• Macrofunctions
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<tr><td>TC200G/E • TC203G/ESERIE
MEGACELLS
MEGAFUNCTIONS
(Non-linear Delay Model)</td><td>TC200G/E • TC203G/E SERIE
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Chapter 2 Internal Macrocells

Chapter 3 I/O Macrocells

Manual Organization

This manual is organized as follows:

Chapter 1: Fundamentals

- **Master Line-up**

  This section describes part numbers of TC200G/E Series usable gates, and the number of I/O slots.

- **Functional Index**

  All the cells available, both internal and I/O macrocells, are arranged by their functions for quick reference.

- **Drive Options for Internal Macrocells**

  This section describes types of macrocells that are typical macrocells, clock drivers.

- **Drive Options for I/O Macrocells**

  This section describes types of I/O macrocells that are input buffers, output buffers and bidirectional buffers.

- **How to Find Target Input Buffer**
- **How to Find Target Output Buffer**
- **How to Find Target Bidirectional buffer**

  Every macrocell has a type name that denotes its generic function.This section describes the macrocell naming conventions so that you can find target macrocells quickly.

- **Oscillator Cell**

  This section describes the notation for configuring crystal oscillator circuit using oscillator cells.

- **DC Characteristics**

  This section describes the characteristics for currents of output buffers and threshold voltage of input buffers, and pull-up, pull-down transistor DC characteristics.

- **Input Capacitance Values for I/O Buffers**

- **Power and Ground Lines**

  This section describes power and ground lines.

- **Delay Estimation**

  This section describes how to calculate propagation delays, capacitance loading with estimated wire length, factors in variation of propagation delay, and characteristics with the temperature, supply voltage and processing tolerance.

- **Reading Data Sheets**

  This section gives a brief description about how to read the cell catalog in chapter 2 and 3.

Chapter 2: Internal Macrocells

This section is primarily a catalog of the internal macrocells, together with an alphabetical index.

Chapter 3: I/O Macrocells

This section is primarily a catalog of the I/O macrocells, together with an alphabetical index.

Chapter 1

Fundamentals

Master Line-up

This section describes part numbers of TC200G/E Series usable gates and the number of I/O slots.

TC200G GATE ARRAY

Double-Layer Metal		Triple-Layer Metal		Raw Gates	Max I/O Pads[2]			Maximum I/O Slots[4]
						TAB		
Part number	Usable Gate[1]	Part number	Usable Gate[1]		Wire Bonding	QTP • QFP-P [TAB]	QFP-P [TAB]	
TC200G42	404,000	TC200G92	704,000	1,154,200	512[3]	776[3]	—	1,036
TC200G40	288,000	TC200G90	503,000	824,180	432[3]	656[3]	—	876
TC200G36	228,000	TC200G86	398,000	652,256	384[3]	584[3]	—	780
TC200G32	175,000	TC200G82	306,000	501,184	336[3]	512[3]	—	684
TC200G24	125,000	TC200G74	218,000	329,840	272[3]	416[3]	556[3]	556
TC200G20	98,000	TC200G70	170,000	257,560	240	368[3]	492[3]	492
TC200G16	82,000	TC200G66	142,000	194,684	208	320[3]	428[3]	428
TC200G14	67,000	TC200G64	117,000	159,840	192	292[3]	388[3]	388
TC200G12	56,000	TC200G62	98,000	134,244	176	268[3]	356[3]	356
TC200G10	47,000	TC200G60	81,000	110,880	160	244	324[3]	324
TC200G08	39,000	TC200G58	67,000	92,168	144	220	296[3]	296
TC200G06	31,000	TC200G56	53,000	68,526	128	192	256	256
TC200G04	22,000	TC200G54	38,000	44,916	104	156	208	208
TC200G02	13,000	TC200G52	22,000	26,100	80	120	160	160

Notes
1. Actual usable gates depend on cell types used and circuit configuration on the system.
2. Additional I/O pads may be configured as VDD/VSS.
3. I/O signals presently limited to 256 by tester capability.
4. Actual usable I/O slots depend on I/O macrocell types and locations used.

TC200E EMBEDDED ARRAY

Double-Layer Metal		Triple-Layer Metal		Raw Gates	Max I/O Pads[2]			Maximum I/O Slots[4]
						TAB		
Part number	Usable Gate[1]	Part number	Usable Gate[1]		Wire Bonding	QTP • QFP-P [TAB]	QFP-P [TAB	
TC200E020	13,000			26,100	80	120	160	160
TC200E040	22,000			44,916	104	156	208	208
TC200E060	31,000			68,526	128	192	256[3]	256
TC200E080	39,000	TC200E580	67,000	92,168	144	220	296[3]	296
TC200E100	47,000	TC200E600	81,000	110,880	160	244	324[3]	324
TC200E120	56,000	TC200E620	98,000	134,244	176	268[3]	356[3]	356
TC200E140	67,000	TC200E640	117,000	159,840	192	292[3]	388[3]	388
TC200E160	82,000	TC200E660	142,000	194,648	208	320[3]	428[3]	428
TC200E180	86,000	TC200E680	149,000	225,280	224	344[3]	460[3]	460
TC200E200	98,000	TC200E700	170,000	257,560	240	368[3]	492[3]	492
TC200E220	111,000	TC200E720	193,000	292,584	256[3]	392[3]	524[3]	524
TC200E240	125,000	TC200E740	218,000	329,840	272[3]	416[3]	556[3]	556
TC200E260	140,000	TC200E760	244,000	369,328	288[3]	440[3]	—	588
TC200E280	144,000	TC200E780	251,000	411,048	304[3]	464[3]	—	620
TC200E300	159,000	TC200E800	278,000	455,000	320[3]	488[3]	—	652
TC200E320	175,000	TC200E820	306,000	501,184	336[3]	512[3]	—	684
TC200E340	201,000	TC200E840	350,000	574,236	360[3]	548[3]	—	732
TC200E360	228,000	TC200E860	398,000	652,256	384[3]	584[3]	—	780
TC200E380	257,000	TC200E880	448,000	735,244	408[3]	620[3]	—	828
TC200E400	288,000	TC200E900	503,000	824,180	432[3]	656[3]	—	876
TC200E420*	404,000	TC200E920*	704,000	1,154,200	512[3]	776[3]	—	1,036

Notes
1. Actual usable gates depend on cell types used and circuit configuration on the system.
2. Additional I/O pads may be configured as VDD/VSS.
3. I/O signals presently limited to 256 by tester capability.
4. Actual usable I/O slots depend on I/O macrocell types and locations used.

* : Under development

Functional Index

TC200G/E SERIES MACROCELL FUNCTIONAL INDEX

Note: ***'x' can be substituted by characteristics, for example, input type, pull-up and pull-down, etc. on I/O. Please see "How to Find Target Input Buffer" on page 1-17, "How to Find Target Output Buffer" on page 1-20 and "How to Find Target Bidirectional Buffer" on page 1-23".***

Drive Options for Internal Macrocells

This section describes types of macrocells that are typical macrocells, clock drivers.

Typical Macrocells

The complete set of internal macrocells available for our previous gate array series is usable in the TC200G/E designs. Like our previous series, the TC200G/E macrocells are available with two drive options: standard drive and power (double) drive.

The form for internal macrocell type names is:

<base_name> <drive>

Where:

<base_name>=denotes the generic function of a macrocell.
<drive> =Null (i.e, no letter) for standard drive types; “P” for power-drive types.

Example:

ND2	Standard-drive 2-input NAND gate
ND2P	Power-drive 2-input NAND gate

Use power drive types with heavy output load. However, be sure not to overuse power drive cells because they require a greater load drive capability of standard drive type cell.

Clock Driver

Four types of internal buffers are available to buffer heavily loaded internal signals — IDRV4, IDRV8, IDRV16, and IDRV24. These buffers use large-geometry transistors in I/O slot regions to provide high fan-out on-chip drive capability. Use the appropriate one consistent with your needs.

Drive Options for I/O Macrocells

I/O buffer lines include input, output, and bidirectional types. The paragraphs that follow discuss drive options available for I/O buffers.

Input Buffer

- Standard type: This type is effective in reducing noise.
- High-speed type: Use high-speed (or high-drive) input buffers to accommodate your critical path needs. High-speed options are available for part of the input buffers. Cell names have a suffix of “H”.
- Example:

  IBUFN (Standard type)
  IBUFNH (High-speed type)

Output Buffer

- Standard type: Standard drive types offer a drive capability that stands between comparable high-speed and slew-rate-control types.
- High-speed type: Use high-speed(or high-drive)types to accommodate your critical path needs. High-speed options are available for output buffers with drive capability of no less than 4 mA. The cell name has a qualifier of “H” in it.
- Slew rate type: Use output buffers with internal slew rate control circuit to minimize unwanted voltage transients. Slew rate control options are available for output buffers with drive capability of no less than 4 mA. The cell name has a qualifier of “R” in it.
- Example:

  B4 (Standard type)
  B4H (High-speed type)
  B4R (Slew rate type)

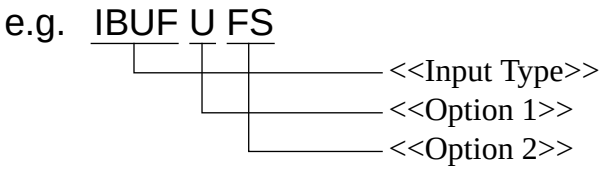
Bidirectional Buffer

Bidirectional buffers contain various type which combine input buffers and output buffers described above.

How to Find Target Input Buffer

This section decsribes the input buffer naming conventions so that you can find target input buffers quickly.

Naming standard Drive Input Buffer



<<Input Type>>

IBUF:	CMOS level
IBUFN:	CMOS level inverted
IBUFNH:	CMOS level inverted high speed
TLCHTH:	LVTTL level high speed
TLCHN:	LVTTL level inverted
TLCHNH:	LVTTL level inverted high speed
SMTC:	SCHMITT TRIGGER CMOS level
SMTT:	SCHMITT TRIGGER LVTTL level
IPCI:	PCI local bus output buffer

<<Option 1>>

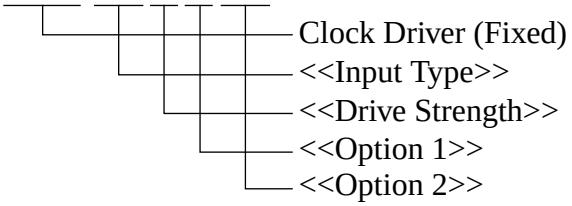
null:	no option
D:	pull-down resistor
U:	pull-up resistor

<<Option 2>>

null:	normal
FS:	failsafe input

Naming High Drive Input Buffers

e.g. DRV SC 4 U FS



<<Input Type>>

T:	LVTTL Level
C:	CMOS Level
SC:	SCHMITT TRIGGER CMOS level

<<Drive Strength>>

4:	equal ‘IDRV4’
8:	equal ‘IDRV8’
16:	equal ‘IDRV16’

<<Option 1>>

null:	without pull resistance
D:	pull-down resistor
U:	pull-up resistor

<<Option 2>>

null:	normal
FS:	failsafe input

Usable Input Buffer Configuration

Table 1-1 Usable Input Buffer Configuration

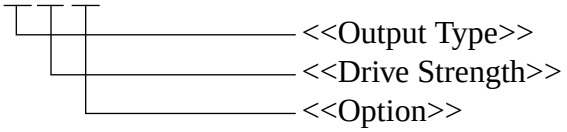
Without Pull Resistance	With Pull-down	With Pull-up	Page
IBUF	IBUFD	IBUFU	3 - 258
IBUFFS	IBUFDFS	—	3 - 261
IBUFN	IBUFND	IBUFNU	3 - 264
IBUFNFS	IBUFNDFS	—	3 - 267
IBUFNH	IBUFNHD	IBUFNHU	3 - 270
IBUFNHFS	IBUFNHDFS	—	3 - 273
SMTC	SMTCD	SMTCU	3 - 278
SMTCFS	SMTCDFS	—	3 - 281
TLCHTH	TLCHTHD	TLCHTHU	3 - 302
TLCHTHFS	TLCHTHDFS	—	3 - 305
TLCHN	TLCHND	TLCHNU	3 - 290
TLCHNFS	TLCHNDFS	—	3 - 293
TLCHNH	TLCHNHD	TLCHNHU	3 - 296
TLCHNHFS	TLCHNHDFS	—	3 - 299
SMTT	SMTTD	SMTTU	3 - 284
SMTTFS	SMTTDFS	—	3 - 287
IPCI	IPCID	IPCIU	3 - 276
DRVC4	DRVC4D	DRVC4U	3 - 213
DRVC4FS	DRVC4DFS	—	3 - 216
DRVC8	DRVC8D	DRVC8U	3 - 219
DRVC8FS	DRVC8DFS	—	3 - 222
DRVC16	DRVC16D	DRVC16U	3 - 225
DRVC16FS	DRVC16DFS	—	3 - 228
DRVSC4	DRVSC4D	DRVSC4U	3 - 231
DRVSC8	DRVSC8D	DRVSC8U	3 - 234
DRVSC16	DRVSC16D	DRVSC16U	3 - 237
DRVT4	DRVT4D	DRVT4U	3 - 240
DRVT4FS	DRVT4DFS	—	3 - 243
DRVT8	DRVT8D	DRVT8U	3 - 246
DRVT8FS	DRVT8DFS	—	3 - 249
DRVT16	DRVT16D	DRVT16U	3 - 252
DRVT16FS	DRVT16DFS	—	3 - 255

How to Find Target Output Buffer

This section describes the output buffer naming conventions so that you can find target output buffers quickly.

Naming Two-state Output Buffer

e.g. B 4 R



<<Output Type>>

B:	unidirectional output buffer (Fixed)

<<Drive Strength>>

2:	2 mA drive
4:	4 mA drive
8:	8 mA drive
16:	16mA drive
24:	24mA drive
PCI:	PCI local bus output buffer

<<Option>>

null:	no option
H:	high-speed type
R:	slew rate type

Usable Two-state Output Configuration

Table 1-2 Usable Output Buffer Configuration

Standard Type	High-speed Type	Slew Rate Type	Drive(mA)	Page
B2	—	—	2	3 - 185
B4	B4H	B4R	4	3 - 187
B8	B8H	B8R	8	3 - 193
B16	B16H	B16R	16	3 - 199
B24	B24H	B24R	24	3 - 205
BPCI	—	—	—	3 - 211

Naming Tri-state Output Buffer

e.g. BT 4 ODFS

<<Tri-state Output Type>>
<<Drive Strength>>
<<Option>>

<<Tri-state Output Type>>

BT:	tri-state output buffer (Fixed)

<<Drive Strength>>

2:	2 mA drive
4:	4 mA drive
8:	8 mA drive
16:	16 mA drive
24:	24 mA drive
PCI:	PCI local bus output buffer

<<Option>>

null:	no option
H:	high-speed type
R:	slew rate type
ODFS:	open drain, failsafe

Usable Tri-State Output Buffer Configuration

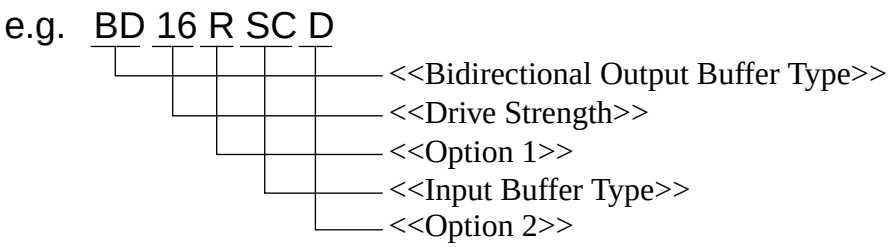
Table 1-3 Usable Tri-State Output Buffer Configuration

Standard	High-speed	Slew Rate	Open Drain Failsafe	Page
BT2	—	—	BT2ODFS	3 - 89 ~ 94
BT4	BT4H	BT4R	BT4ODFS	3 - 95 ~ 118
BT8	BT8H	BT8R	BT8ODFS	3 - 119 ~ 139
BT16	BT16H	BT16R	BT16ODFS	3 - 140 ~ 160
BT24	BT24H	BT24R	BT24ODFS	3 - 161 ~ 181
BTPCI	—	—	—	3 - 182

How to Find Target Bidirectional Buffer

This section describes the bidirectional buffer naming conventions so that you can find target bidirectional buffers quickly.

Naming Bidirectional Output Buffer



<<Bidirectional Output Buffer Type>>

BD:	bidirectional output buffer (Fixed)

<<Drive Strength>>

2:	2 mA drive
4:	4 mA drive
8:	8 mA drive
16:	16 mA drive
24:	24 mA drive
PCI:	PCI local bus input output buffer

<<Input Buffer Type>>

C:	CMOS level
CN:	CMOS level inverted
CNH:	CMOS level inverted high-speed
TH:	LVTTL level high speed
TN:	LVTTL level inverted
TNH:	LVTTL level inverted high-speed
SC:	schmitt trigger CMOS level
ST:	schmitt trigger LVTTL level

<<Option 1>>

null:	no option
H:	high-speed type
R:	slew rate control type

<<Option 2>>

null:	no option
U:	with pull-up
D:	with pull-down
ODFS:	open drain, failsafe

Usable Bidirectional Output Buffer Configuration

Table 1-4 CMOS Input Type

	C	C D	C U	C ODFS	H C	H C D	H C U	R C	R C D	R C U	Drive (mA)	Page
BD2	●	●	●	●	—	—	—	—	—	—	2	3 - 1 ~ 9
BD4	●	●	●	●	●	●	●	●	●	●	4	3 - 10 ~ 28
BD8	●	●	●	●	●	●	●	●	●	●	8	3 - 29 ~ 47
BD16	●	●	●	●	●	●	●	●	●	●	16	3 - 48 ~ 66
BD24	●	●	●	●	●	●	●	●	●	●	24	3 - 67 ~ 85

Table 1-5 CMOS Input with Inverted Type

	CN	CN D	CN U	CN ODFS	H CN	H CN D	H CN U	R CN	R CN D	R CN U	Drive (mA)	Page
BD2	●	●	●	●	—	—	—	—	—	—	2	3 - 1 ~ 9
BD4	●	●	●	●	●	●	●	●	●	●	4	3 - 10 ~ 28
BD8	●	●	●	●	●	●	●	●	●	●	8	3 - 29 ~ 47
BD16	●	●	●	●	●	●	●	●	●	●	16	3 - 48 ~ 66
BD24	●	●	●	●	●	●	●	●	●	●	24	3 - 67 ~ 85

	CNH	CNH D	CNH U	CNH ODFS	H CNH	H CNH D	H CNH U	R CNH	R CNH D	R CNH U	Drive (mA)	Page
BD2	●	●	●	●	—	—	—	—	—	—	2	3 - 1 ~ 9
BD4	●	●	●	●	●	●	●	●	●	●	4	3 - 10 ~ 28
BD8	●	●	●	●	●	●	●	●	●	●	8	3 - 29 ~ 47
BD16	●	●	●	●	●	●	●	●	●	●	16	3 - 48 ~ 66
BD24	●	●	●	●	●	●	●	●	●	●	24	3 - 67 ~ 85

Table 1-6 CMOS SCHMITT TRIGGER Input Type

	SC	SC D	SC U	SC ODFS	H SC	H SC D	H SC U	R SC	R SC D	R SC U	Drive (mA)	Page
BD2	●	●	●	●	—	—	—	—	—	—	2	3 - 1 ~ 9
BD4	●	●	●	●	●	●	●	●	●	●	4	3 - 10 ~ 28
BD8	●	●	●	●	●	●	●	●	●	●	8	3 - 29 ~ 47
BD16	●	●	●	●	●	●	●	●	●	●	16	3 - 48 ~ 66
BD24	●	●	●	●	●	●	●	●	●	●	24	3 - 67 ~ 85

Table 1-7 LVTTL Input Type

	TH	TH D	TH U	TH ODFS	H TH	H TH D	H TH U	R TH	R TH D	R TH U	Drive (mA)	Page
BD2	●	●	●	●	—	—	—	—	—	—	2	3 - 1 ~ 9
BD4	●	●	●	●	●	●	●	●	●	●	4	3 - 10 ~ 28
BD8	●	●	●	●	●	●	●	●	●	●	8	3 - 29 ~ 47
BD16	●	●	●	●	●	●	●	●	●	●	16	3 - 48 ~ 66
BD24	●	●	●	●	●	●	●	●	●	●	24	3 - 67 ~ 85

Table 1-8 LVTTL Input with Inverted Type

	TN	TN D	TN U	TN ODFS	H TN	H TN D	H TN U	R TN	R TN D	R TN U	Drive (mA)	Page
BD2	●	●	●	●	—	—	—	—	—	—	2	3 - 1 ~ 9
BD4	●	●	●	●	●	●	●	●	●	●	4	3 - 10 ~ 28
BD8	●	●	●	●	●	●	●	●	●	●	8	3 - 29 ~ 47
BD16	●	●	●	●	●	●	●	●	●	●	16	3 - 48 ~ 66
BD24	●	●	●	●	●	●	●	●	●	●	24	3 - 67 ~ 85

	TNH	TNH D	TNH U	TNH ODFS	H TNH	H TNH D	H TNH U	R TNH	R TNH D	R TNH U	Drive (mA)	Page
BD2	●	●	●	●	—	—	—	—	—	—	2	3 - 1 ~ 9
BD4	●	●	●	●	●	●	●	●	●	●	4	3 - 10 ~ 28
BD8	●	●	●	●	●	●	●	●	●	●	8	3 - 29 ~ 47
BD16	●	●	●	●	●	●	●	●	●	●	16	3 - 48 ~ 66
BD24	●	●	●	●	●	●	●	●	●	●	24	3 - 67 ~ 85

Table 1-9 LVTTL SCHMITT TRIGGER Input Type

	ST	ST D	ST U	ST ODFS	H ST	H ST D	H ST U	R ST	R ST D	R ST U	Drive (mA)	Page
BD2	●	●	●	●	—	—	—	—	—	—	2	3 - 1 ~ 9
BD4	●	●	●	●	●	●	●	●	●	●	4	3 - 10 ~ 28
BD8	●	●	●	●	●	●	●	●	●	●	8	3 - 29 ~ 47
BD16	●	●	●	●	●	●	●	●	●	●	16	3 - 48 ~ 66
BD24	●	●	●	●	●	●	●	●	●	●	24	3 - 67 ~ 85

Table 1-10 **Special Type**

Standard	with Pull-down	with Pull-up	Page
BDPCI	BDPCID	BDPCIU	3 - 86

Oscillator Cells

This section describes the notation for configuring crystal oscillator circuit using oscillator cells.

Naming Oscillator Cell

- Standard Type

OSC4D	(oscillator with stop control)
OSC6D	(oscillator with stop control)

- Cornered Type

OSCX05	(corner oscillator with feedback resistor)
OSCX30	(corner oscillator with feedback resistor)

How to Find Target Oscillator Cells

The following table shows the availability of the oscillator cells. Use the appropriate oscillator cells with your need. When appropriate oscillator cells are not used, power dissipation may increase, and the oscillator cells might not behave.

Table 1-11 **Oscillator Specifications**

	Frequency (MHz)	Stop Control	Feedback Resistor	I/O counts	Page
OSC4D		●	—		
OSC6D		●	—		
OSCX05		●	●	*	
OSCX30		●	●	*	

* : Restricted to pre-determined I/O Slot locations

Notes on Crystal Oscillator

- When designing a system using a crystal oscillator, the unstable period which is found on oscillation starting time or oscillation stopping time should be taken into account.
- During logic simulation, specify the CMOS level to the Z output of the oscillator cell.
- Since the Z output of the oscillator cell is to drive the load on the LSI tester prove head, be a wore of the propagation delays for the Z to ZI path.
- Since the oscillator cell is susceptible to current noise from another signal, its input and output pin should be placed between VDD and VSS pins as shown on Figure 1-1 on page 1-30 and Figure 1-2 on page 1-32
- Make the lengths of the wires between parts as short as possible, and do not allow the wires to cross.

Oscillator Application Note

Figure 1-1 and Figure 1-2 show examples of application circuits with OSC4D and OSCX05, respectively. Table 1-12 ,Table 1-13, Table 1-14 and Table 1-15 give the recommended circuit parameters and electrical characteristics for each of those oscillator cells. The external CR and electric characteristics depend on the type of a crystal oscillator used and the soldering states of the devices on the PC board. Contact the crystal oscillator supplier for details.

Figure 1-1 **An example of application circuit (OSC4D)**

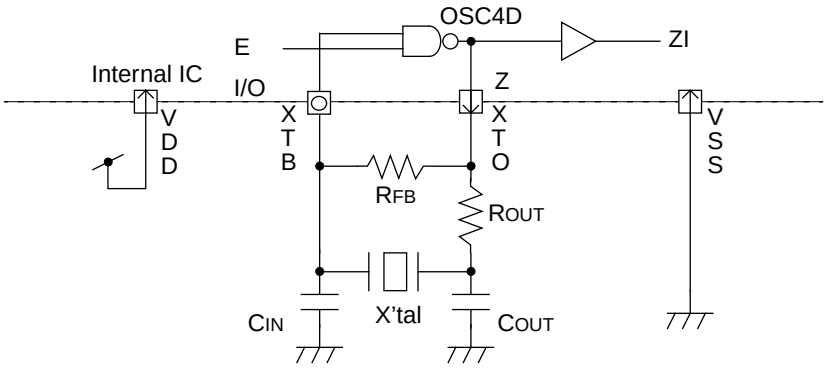


Table 1-12 Recommended Oscillation Condition

Cell Name	Parameter	Symbol	Recommended value		Unit
OSC4D	<crystal oscillator> frequency crystal impedance	 f CI			
	feedback resistor	RFB			
	output resistor	ROUT			
	external condenser	CIN, COUT			
OSC6D	<crystal oscillator> frequency crystal impedance	 f CI			
	feedback resistor	RFB			
	output resistor	ROUT			
	external condenser	CIN, COUT			

Table 1-13 Electrical specification (VSS=0V, VDD=3.3V, Typ.)

Cell Name	Parameter	Symbol	Condition	Typ.	Unit
OSC4D	oscillation starting voltage	VSTA	f =		
			f =		
	oscillation holding voltage	VHOLD	f =		
			f =		
	supply current	IDD	f =		
			f =		
	oscillation starting time	TSTA			
OSC6D	oscillation starting voltage	VSTA	f =		
			f =		
	oscillation holding voltage	VHOLD	f =		
			f =		
	supply current	IDD	f =		
			f =		
	oscillation starting time	TSTA			

Please contact Toshiba DesignCenter for the values in shadowed columns.

Figure 1-2 An example of application circuit (OSCX05)

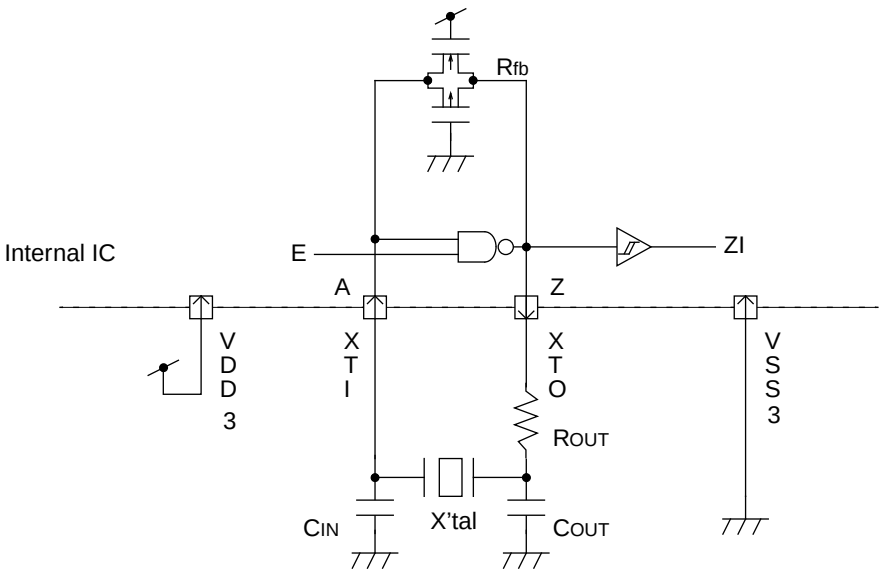


Table 1-14 Recommended Oscillation Condition

Cell Name	Parameter	Symbol	Recommended value		Unit
OSCX05	<crystal oscillator> frequency crystal impedance	 f CI			
	output resistor	ROUT			
	external condenser	CIN, COUT			
OSCX30	<crystal oscillator> frequency crystal impedance	 f CI			
	output resistor	ROUT			
	external condenser	CIN, COUT			

Table 1-15 Electrical specification (VSS=0V, VDD=3.3V, Typ.)

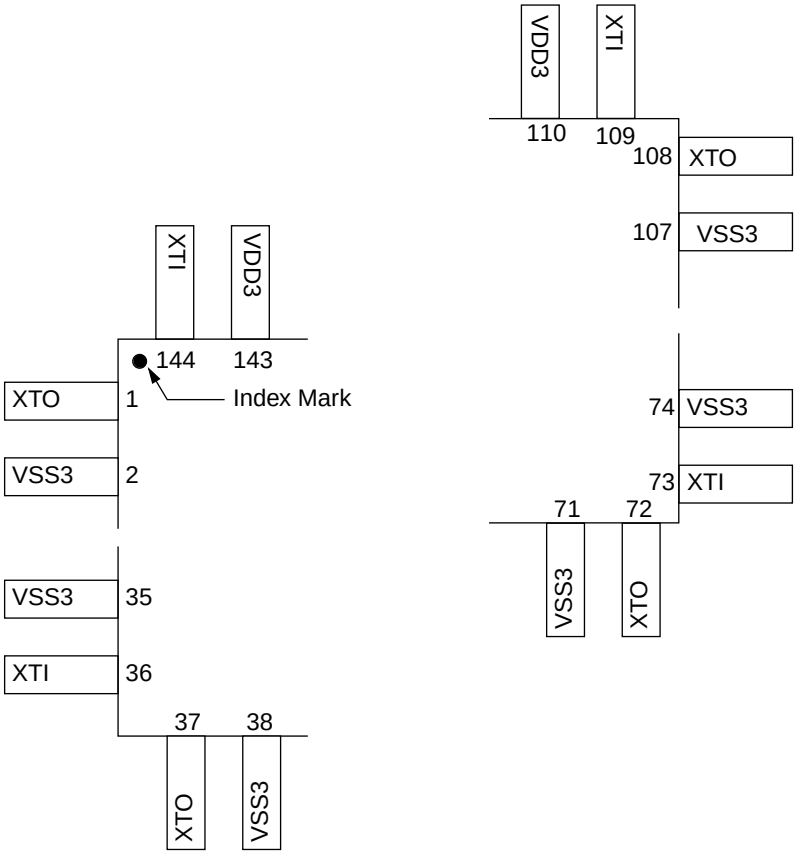
Cell Name	Parameter	Symbol	Condition	Typ.	Unit
OSCX05	oscillation starting voltage	VSTA	f =32kHz		
	oscillation holding voltage	VHOLD			
	supply current	IDD			
	oscillation starting time	TSTA			
OSC6D	oscillation starting voltage	VSTA	f =10MHz		
	oscillation holding voltage	VHOLD			
	supply current	IDD			
	oscillation starting time	TSTA			

Please contact Toshiba DesignCenter for the values in shadowed columns.

Corner Oscillator Cell

The pin locations of OSCX05 and OSCX30 which are the corner oscillator cells are fixed at the corner of the package. Some packages may allow no package lead for the corner oscillator. Contact your Design Center for package leads allowed for the corner oscillator. Figure 1-3 shows the pins on the 144-pin flat package (LFP144) reserved for these cornered oscillator cells.

Figure 1-3 Pin Assignment Example of a Cornered Oscillator (LFP144 face up)



DC Characteristics

This section describes the characteristics for currents of output buffers and threshold voltage of input buffers, and pull-up, pull-down transistor DC characteristics.

Output Characteristics

Figure 1-4 shows V_{OH}-I_{OH} characteristics. Figure 1-5 shows V_{OL}-I_{OL} characteristics.

Figure 1-4 V_{OH}-I_{OH} CHARACTERISTICS (V_{DD}=3.3V, Ta=25°C, typ.)

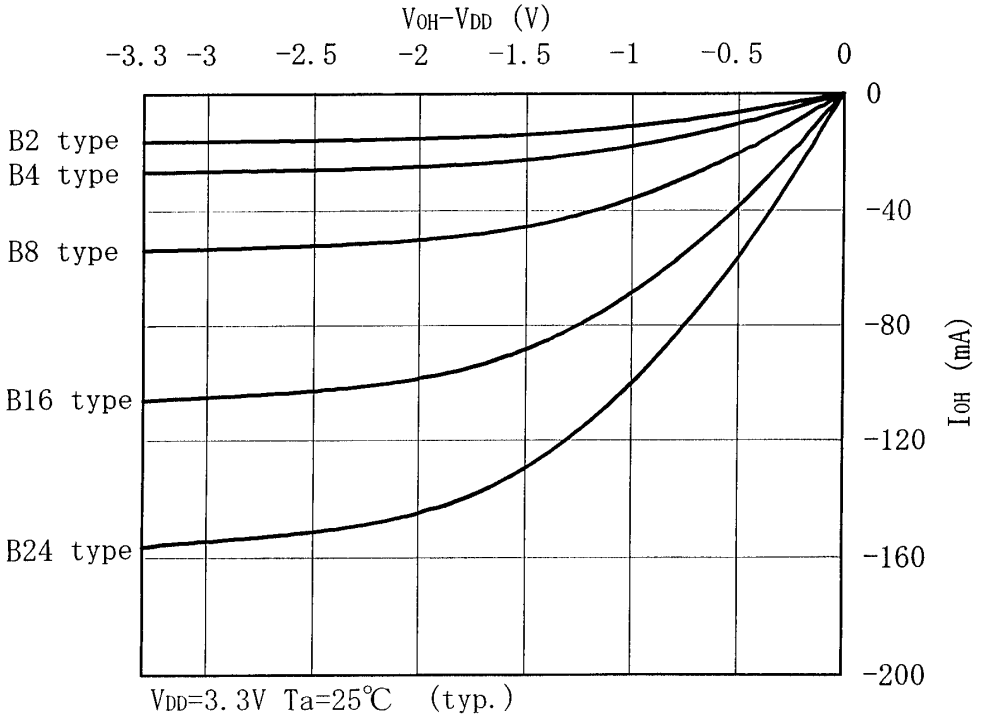
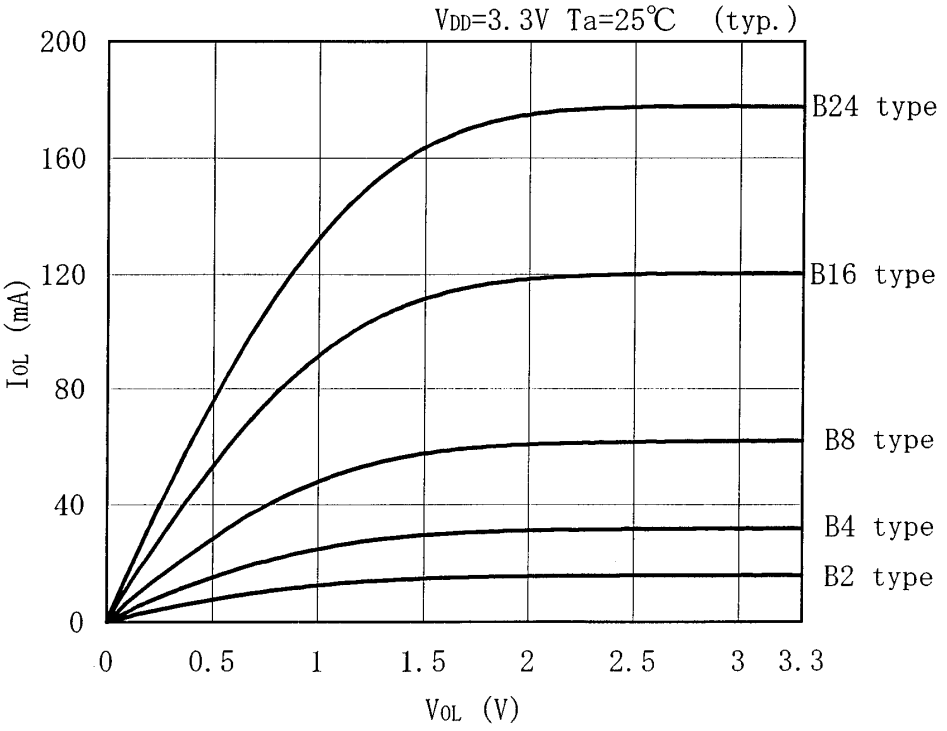


Figure 1-5 V_{OL}-I_{OL} CHARACTERISTICS (V_{DD}=3.3V, Ta=25°C, typ.)



Threshold Characteristics

Figure 1-6 and Figure 1-7 show CMOS level threshold characteristics.
Figure 1-8 and Figure 1-9 show LVTTL level threshold characteristics.

Figure 1-6 **CMOS level threshold characteristics**

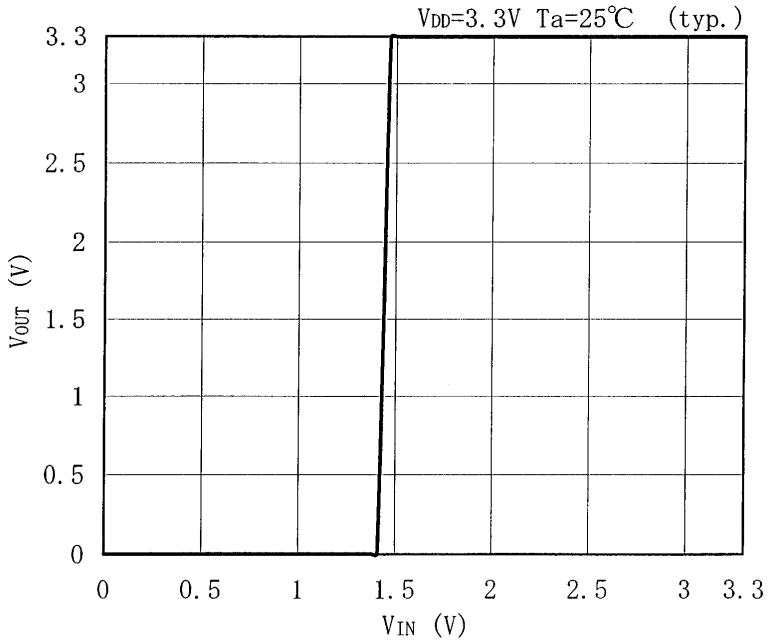


Figure 1-7 **SCHMITT TRIGGER CMOS level threshold characteristics**

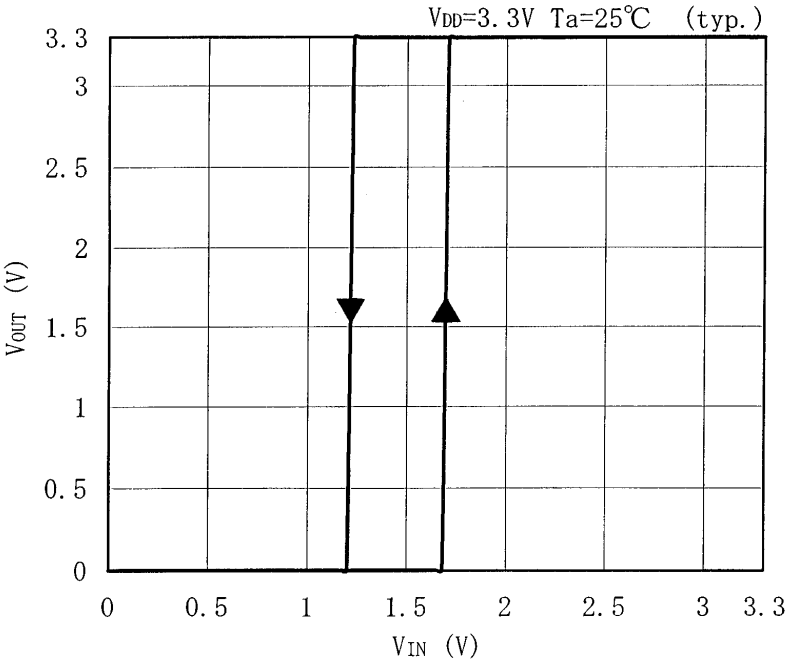


Figure 1-8 **LVTTL level threshold characteristics**

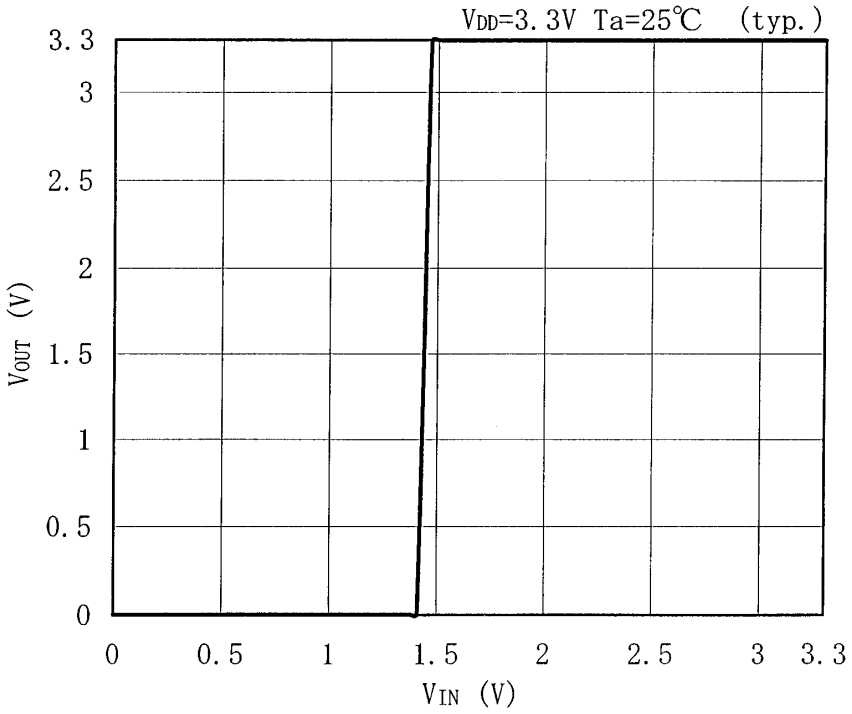
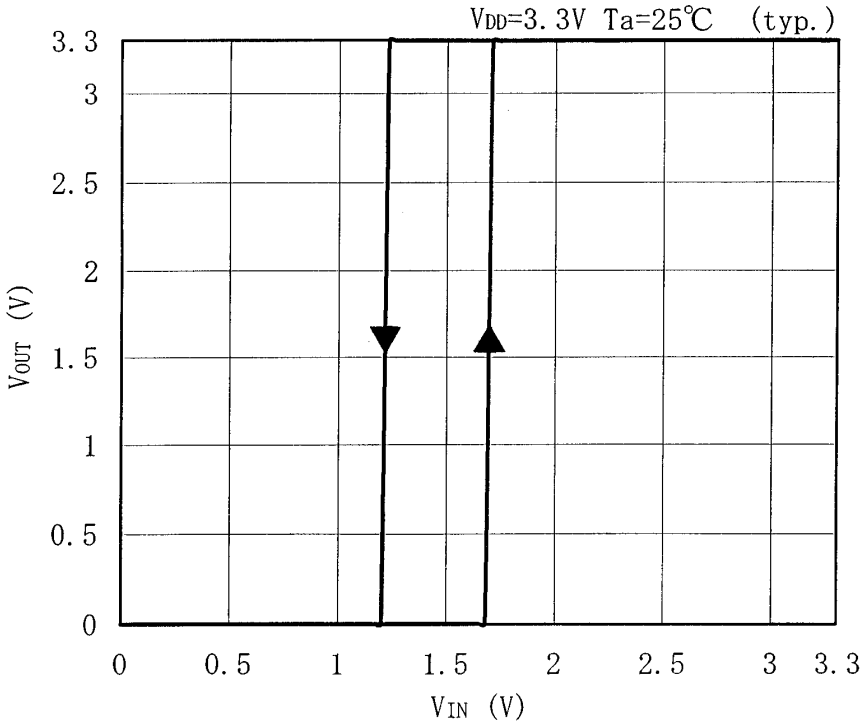


Figure 1-9 **SCHMITT TRIGGER LVTTL level threshold characteristics**



Pull-Up, Pull- Down Characteristics

Figure 1-10 shows pull-up transistor DC characteristics. Figure 1-11 shows pull-down transistor DC characteristics.

Figure 1-10 **Pull-up transistor DC characteristics (VDD=3.3V, Ta=25°C, typ.)**

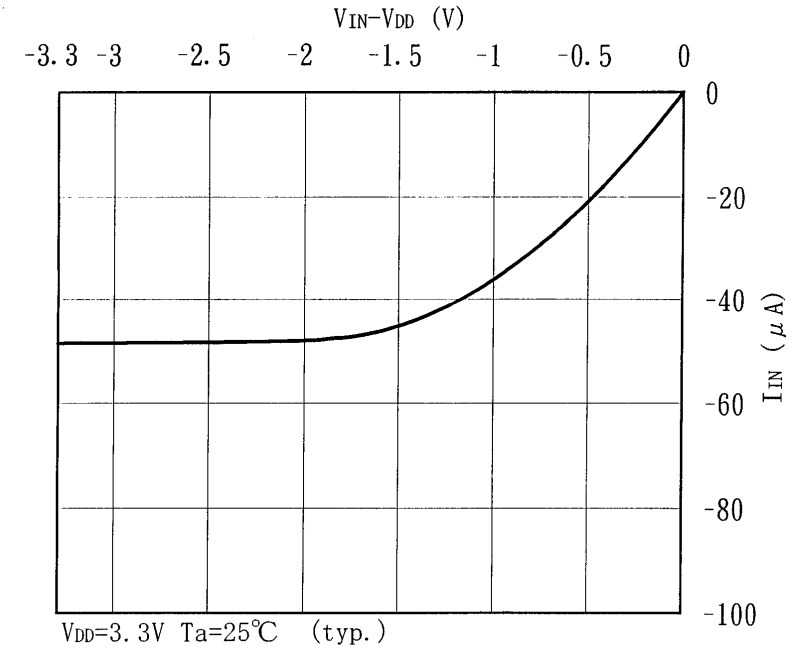
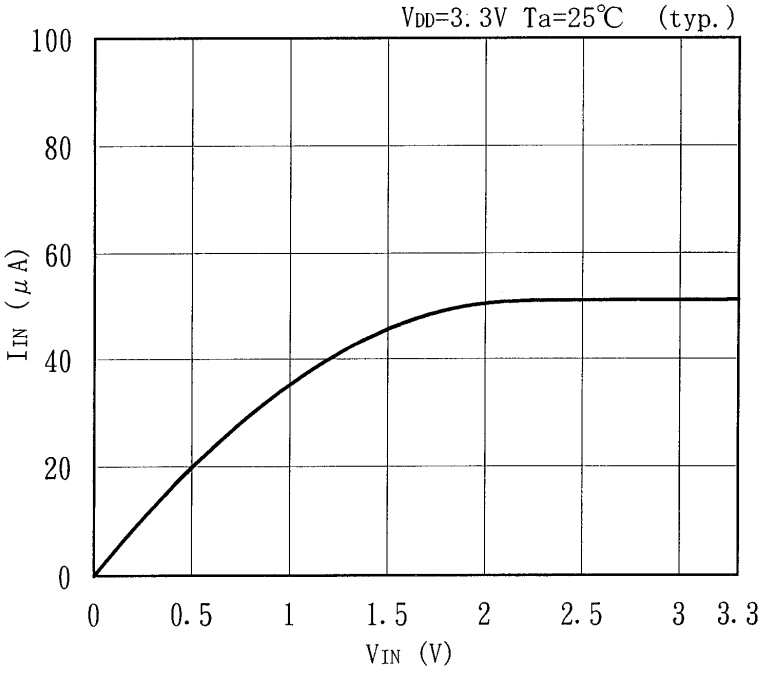


Figure 1-11 **Pull-down transistor DC characteristics (VDD=3.3V, Ta=25°C, typ.)**



Input Capacitance Values for I/O Buffers

This section gives the input capacitances associated with the input pins of input buffers and the output pins of tri-state output buffers in the high-impedance state. Input capacitance values are used to calculate I/O delays

.

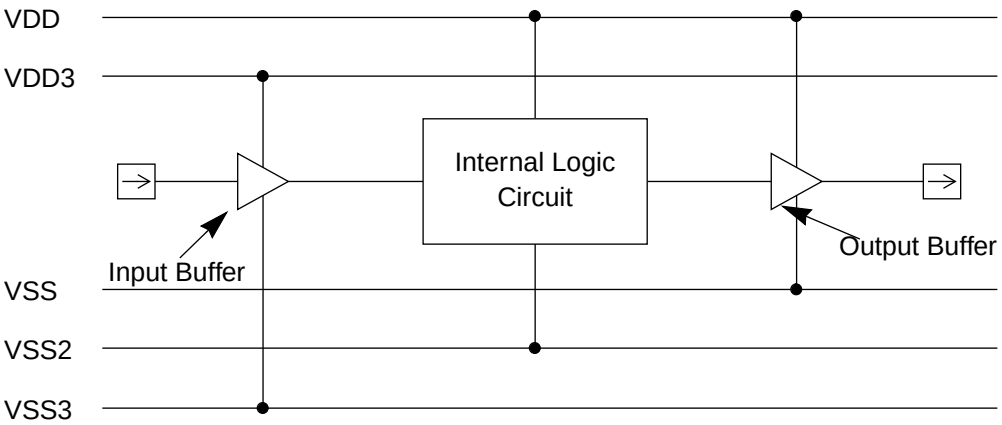
Table 1-16 Input Capacitance Values for I/O Buffers

Type	Cell Name	Pin Name	Capacitance (pF)
Input buffers	DRVC4x, DRVC8x, DRVC16x DRVSC4x, DRVSC8x, DRVSC16x DRVT4x, DRCT8x, DRVT16x IBUFx, IBUFNx, IBUFNHx SMTCx, SMTTx TLCHNx, TLCHNHx, TLCHTHx IPCIx	A	5.56
	DRVC4xFS, DRVC8xFS, DRVC16xFS DRVT4xFS, DRVT8xFS, DRVT16xFS IBUFxFS, IBUFNxFS, IBUFNHxFS SMTCxFS, SMTTxFS TLCHNxFS, TLCHNHxFS, TLCHTHxFS	A	2.78
Tri-state output Buffers	BT2, BT4, BT4H, BT4R, BT8, BT8H, BT8R, BT16, BT16H, BT16R, BTPCI	Z	5.56
	BT24, BT24H, BT24R	Z	9.13
	BT2ODFS, BT4ODFS, BT8ODFS, BT16ODFS	Z	2.78
	BT24ODFS	Z	3.56
Bidirectional Biffers	BD2x, BD4x, BD4Hx, BD4Rx, BD8x, BD8Hx, BD8Rx, BD16x, BD16Hx, BD16Rx, BDPCIx	IO	5.56
	BD24x, BD24Hx, BD24Rx	IO	9.13
	BD2xODFS, BD4xODFS, BD8xODFS, BD16xODFS	IO	2.78
	BD24xODFS	IO	3.56

The Power and Ground Lines

The TC200G/E series has three types of VSS buses and two types of VDD buses. The positions of standard power of these power lines are fixed depending on combination of a package and master chip. Some additional power pins are required under the condition of input buffers, output buffers or simultaneous switchings. Please contact Toshiba Design Center for the details.

Figure 1-12 **Power Supply Lines**



VDD : a power bus for external output buffers and internal macrocells
VDD3 : a power bus for external input buffers
VSS : a ground bus for external output buffers
VSS2 : a ground bus for internal macrocells
VSS3 : a ground bus for external input buffers

Delay Estimation

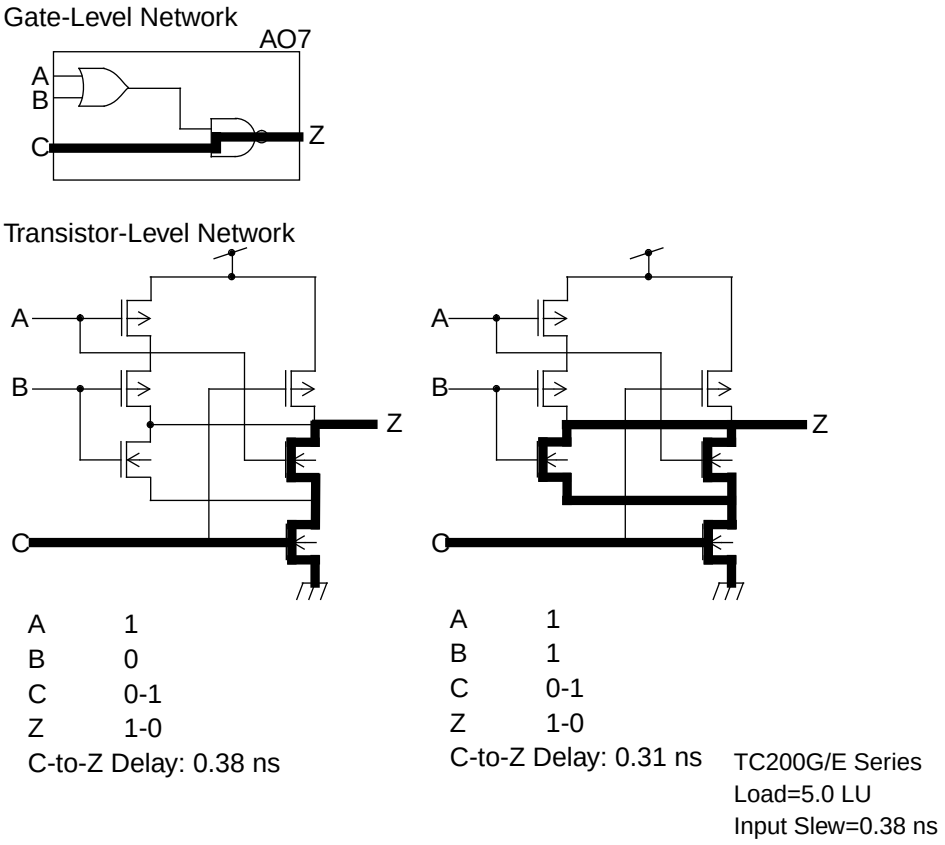
As feature sizes shrink, timing accuracy plays a more critical role in the success of deep-submicron ASIC technologies. You must use as accurate timing estimations as possible in the early stage of the design to minimize design iterations involved in complex designs. To this end, the accuracy of the libraries and the delay equation was enhanced for the release of our sign-off verification systems, Verilog-XL Sign-off (VSO) System and VITAL Sign-off System. The advanced technical features for delay prediction include Non-linear Delay Models (NLDMs) and State-Dependent Path Delays (SDPDs).

The NLDMs and SDPDs combine to realize sign-off-accuracy simulation that is “very close” to Spice results and representative of actual silicon.

State-Dependent Path Delays (SDPDs)

The new modeling methodology uses state-dependent path delays (SDPDs), which describe pin-to-pin delays whose validity is conditioned by other pins. This feature is illustrated below in Figure 1-13, where input A is at logic 1, and when input C makes a 0-to-1 transition, output Z goes low. The signal flows indicated by bold paths show that the C-to-Z timing arc is conditioned by the state at input B.

Figure 1-13 **State-Dependent Path Delays (SDPDs)**

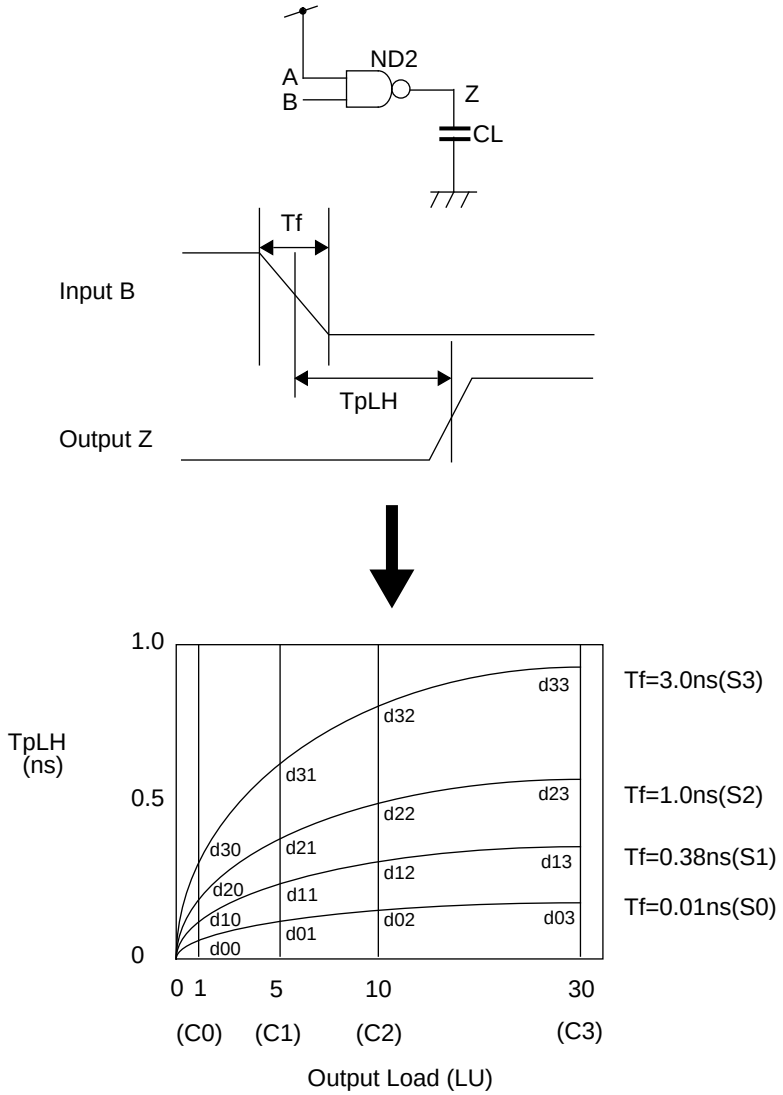


Non-linear Delay Model

In the deep-submicron world, the traditional linear scaling of the fanout time estimates are not accurate enough. Wire delays are beginning to dominate designs, and the traditional method can not accurately model interconnect wires.

The new delay estimation method interprets the input wave as a slope, based on table lookup and interpolation. Figure 1-14 illustrates the procedures Toshiba uses to extract delay table data. This example shows the steps for creating a lookup table for the rise delay of a 2-input NAND gate.

Figure 1-14 Extracting Delay Table Data for an 2-input NAND Gate



Delay extraction is performed with the input transition time of input B and the output load of CL set at four different points each.

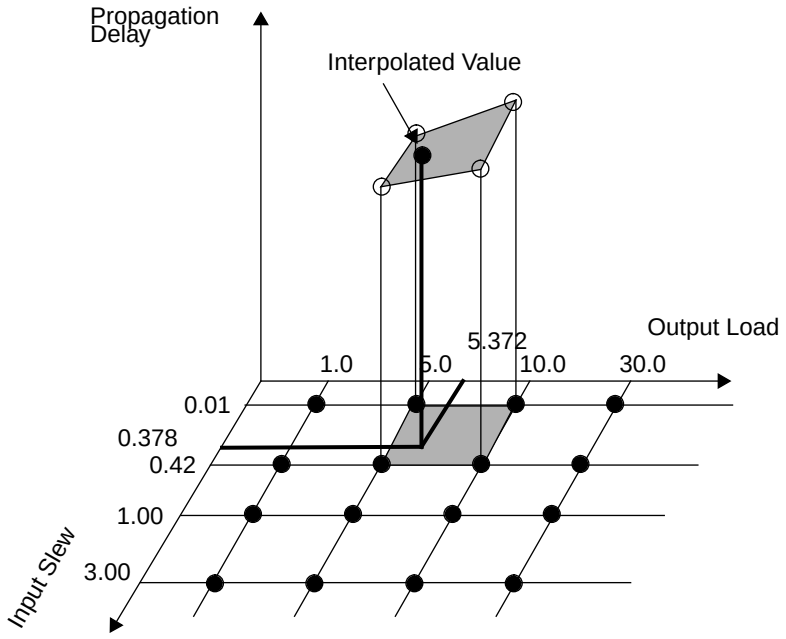
Tf: input transition time

	C0	C1	C2	C3
S0	d00	d01	d02	d03
S1	d10	d11	d12	d13
S2	d20	d21	d22	d23
S3	d30	d31	d32	d33

Four-by-four points of the delay curves are translated into a look-up table.

Figure 1-15 illustrates by example how the macrocell propagation delay is computed using the new delay modeling method.

Figure 1-15 Table Lookup and Interpolation

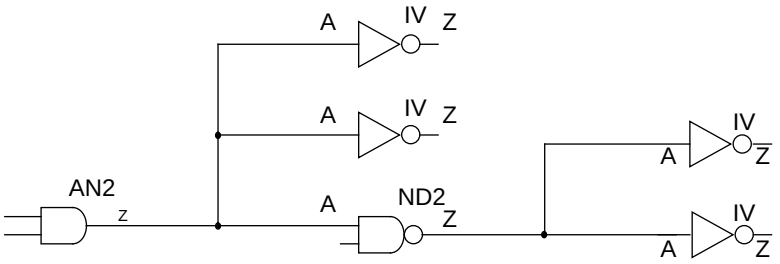


This technique uses a two-dimensional table indexed by output load and input slew rate. The output load is either estimated using library-defined wire load models or back-annotated from the physical layout of a design. The slew rate (or the transition time) of a gate's input pin is computed by evaluating the output delay of the previous gate. Assuming the output load is 5.372 LU, and the input slew rate is 0.378 ns, four bounding-table values (or corner values in the figure) are found by examining the index values. The delay value is then determined by "interpolating" between these four points. In Figure 1-15, the black dots represent points that are defined in the lookup table in the technology library.

Non-linear Delay Calculation Example

The following example illustrates the process to determine the fall delay across the A-to-Z timing arc of the NAND cell (ND2) in Figure 1-16.

Figure 1-16 Non-linear Delay Calculation Example



If you have a need to calculate a macrocell's propagation delay manually, use the following steps.

1. Calculate the total capacitive load on the ND2's output pin.

a. Determine the total fanout load. It represents the sum of loading units of the driven macrocell input pins. Input loading unit numbers are listed in the "INPUT LOAD" section of each macrocell data sheet. Fanout load associated with the ND2's output pin is calculated as:

$$\text{Fanout} = 1.0 + 1.0 = 2.0(\text{LU})$$

* Remember to include the INPUT CAPACITANCE value for tri-state drivers.

b. Determine the estimated wire load (EWL), referring to an appropriate equation in Table 1-17, Table 1-18, Table 1-19 and Table 1-20. If a design is implemented using array TC200G10, it is calculated as:

$$\begin{aligned}\text{EWL} &= 1.349 \times 2 + 0.674 \\ &= 3.372\ (\text{LU})\end{aligned}$$

Therefore, the total capacitive load (C_{total}) on the ND2's output pin is:

$$C_{total(ND2)} = 2.0 + 3.372 = 5.372\ (\text{LU})$$

2. Calculate the slew rate (or transition time) of the ND2's A input.

a. Calculate the capacitive load on the AN2's output pin, using the sequence shown at step 1.

$$C_{total(AN2)} = \text{fanout} + EWL$$
$$= (1.0 + 1.0 + 1.03) + (1.349 \times 3 + 0.674)$$
$$= 7.751 \text{ (LU)}$$

b. The equation for calculating the input slew rate (Slew) is:

$$Slew_{(ND2)} = FACTOR_{(AN2)} \times C_{total(AN2)} + CONSTANT_{(AN2)}$$

FACTOR and CONSTANT parameters are defined, for each timing arc and transition, in the SLEW FACTOR sections in each library cell data sheet. When the ND2's output rises, the driving output of the previous-stage AN2 falls. Obtain the FACTOR and CONSTANT parameters, taking care to use the figures of corresponding output conditions(s). Referring to the AN2 page, $Slew_{(ND2)}$ is calculated as:

$$Slew_{(ND2)} = 0.0397 \times 7.751 + 0.07$$
$$= 0.378 \text{ (ns)}$$

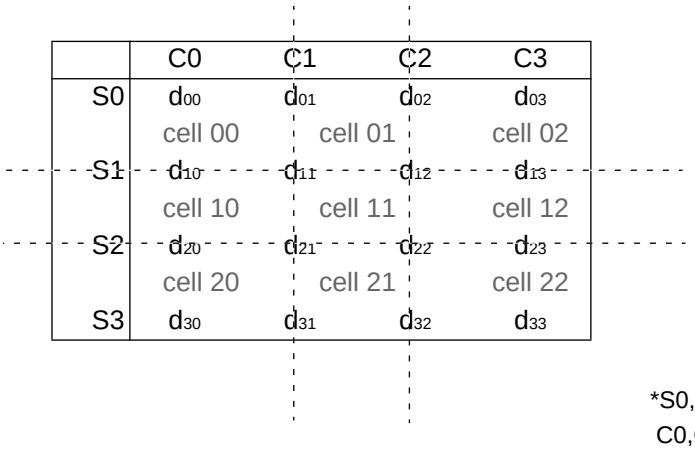
3. Referring to the PATH DELAY section of the ND2 page, choose four neighboring points for interpolation.

The new delay estimation method uses a 4×4 lookup table indexed by output load and input slew rate. Use these two values to index into ND2's rise path delay table. Four bounding-table values (or corner values in Figure 1-15) used for interpolation are found by examining the index values.

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.09
0.38	0.11	0.26	0.43	1.12
1.00	0.13	0.30	0.49	1.17
3.00	0.15	0.37	0.60	1.35

4. Interpolate the bounding-table values.

Use the capacitive-load and slew-rate values computed at step 1 and step 2 to choose a table cell from the following interpolation matrix, where C0 to C3 are the capacitance index values in the x-axis, and S0 to S3 are the slew-rate index values in the y-axis in the PATH DELAY table.



*S0,S1,S2,S3: Input Slew
C0,C1,C2,C3: Output Load

Cell Selection

cell 00 (s≤S1, c≤C1)	cell 01 (s≤S1, C1<c≤C2)	cell 02 (s≤S1, C2<c)
cell 10 (S1<s≤S2, c≤C1)	cell 11 (S1<s≤S2, C1<c≤C2)	cell 12 (S1<s≤S2, C2<c)
cell 20 (S2<s, c≤C1)	cell 21 (S2<s C1<c≤C2)	cell 22 (S2<s, C2<c)

s=Slew, c=C total

The interpolation equation for $cell_{(ij)}$ is:

$$\text{Propagation Delay } d=(X_{ij} \times s \times c + Y_{ij} \times s + Z_{ij} \times c + W_{ij}) / V_{ij}$$

where:

$X_{ij}=$	$+ d_{ij}$	$- d_{i\,j+1}$	$- d_{i+1\,j}$	$+ d_{i+1\,j+1}$
$Y_{ij}=$	$-C_{j+1} \times d_{ij}$	$+ C_j \times d_{i\,j+1}$	$+ C_{j+1} \times d_{i+1\,j}$	$- C_j \times d_{i+1\,j+1}$
$Z_{ij}=$	$-S_{i+1} \times d_{ij}$	$+ S_{i+1} \times d_{i\,j+1}$	$+ S_i \times d_{i+1\,j}$	$- S_i \times d_{i+1\,j+1}$
$W_{ij}=$	$+ S_{i+1} \times C_{j+1} \times d_{ij}$	$-S_{i+1} \times C_j \times d_{i\,j+1}$	$-S_i \times C_{j+1} \times d_{i+1\,j}$	$+ S_i \times C_j \times d_{i+1\,j+1}$

$V_{ij}=(S_{i+1}-S_i)(C_{j+1}-C_j)$

The output-load/input-slew condition in our example rises into $cell_{(01)}$. Using the above equation, the rise delay (TpLH) across the A-to-Z timing arc of the ND2 in Figure 1-16 is computed as follows:

$$X_{01} = d_{01} - d_{02} - d_{11} + d_{12}$$
$$= 0.23 - 0.40 - 0.26 + 0.43 = 0$$

$$Y_{01} = -(C2 \times d_{01}) + (C1 \times d_{02}) + (C2 \times d_{11}) - (C1 \times d_{12})$$
$$= -(10.00 \times 0.23) + (5.00 \times 0.40) + (10.00 \times 0.26) - (5.00 \times 0.43)$$
$$= 0.15$$

$$Z_{01} = -(S1 \times d_{01}) + (S1 \times d_{02}) + (S0 \times d_{11}) - (S0 \times d_{12})$$
$$= -(0.38 \times 0.23) + (0.38 \times 0.40) + (0.01 \times 0.26) - (0.01 \times 0.43)$$
$$= 0.063$$

$$W_{01} = (S1 \times C2 \times d_{01}) - (S1 \times C1 \times d_{02}) - (S0 \times C2 \times d_{11}) + (S0 \times C1 \times d_{12})$$
$$= (0.38 \times 10.00 \times 0.23) - (0.38 \times 5.00 \times 0.40) - (0.01 \times 10.00 \times 0.26) + (0.01 \times 5.00 \times 0.43)$$
$$= 0.11$$

$$V_{01} = (S1 - S0)(C2 - C1)$$
$$= (0.38 - 0.01) \times (10.00 - 5.00)$$
$$= 1.85$$

Therefore,

$$d = \{(X_{01} \times s \times c) + (Y_{01} \times s) + (Z_{01} \times c) + W_{01}\} \div V_{01}$$
$$= \{(0 \times 0.378 \times 5.372) + (0.15 \times 0.378) + (0.063 \times 5.372) + 0.11\} \div 1.85$$
$$= 0.27 \text{ (ns)}$$

Figure 1-17 ND2 Data Sheet

TC200G SERIES

DATA SHEET

ND2 ND2 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0997	0.16

PATH DELAY (ns)

LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.09
0.38	0.11	0.26	0.43	1.12
1.00	0.13	0.30	0.49	1.17
3.00	0.15	0.37	0.60	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0654	0.10

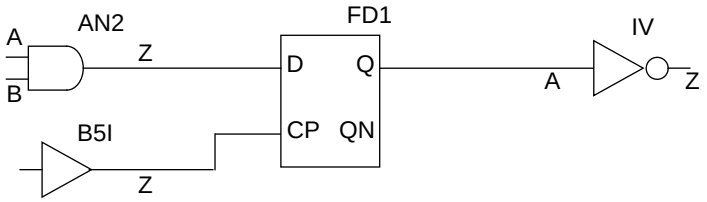
PATH DELAY (ns)

LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.79

Non-linear Setup/Hold Time Calculation Example

The following example illustrates the process to determine the setup time on the D input of the FD1 flip-flop in Figure 1-18.

Figure 1-18 **Non-linear Setup/Hold Time Calculation Example**



1. **Calculate the input slew rates (or transition times) of the data (D) and clock (CP) pins of the FD1, using the steps discussed in the previous section.**

   CP input: $Slew_{up}$ = 0.185 (ns)
   D input: $Slew_{up}$ = 0.383 (ns)
   D input: $Slew_{dn}$ = 0.190 (ns)

2. **Referring to the SETUP section of the FD1 page, choose four neighboring points for interpolation.**

   The setup/hold estimation method uses a 4 × 4 lookup table indexed by clock and data slew rates. There are two lookup tables, depending on the data values. Use the clock and data slew rate values to index into the FD1's setup time tables. Four bounding-table values used for interpolation are found by examining the index values.

3. **Interpolate the bounding-table values for these two cases, D=High and D=Low, using the equation shown in the previous section.**

   In our example, setup(H) and setup(L) are calculated to be as follows:

   setup(H) = 0.38 (ns)
   setup(L) = 0.37 (ns)

4. **Use the larger value of the two as the setup time.**

Figure 1-19 **FD1 Data Sheet**

TC200G SERIES

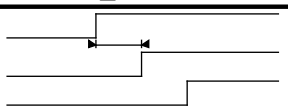
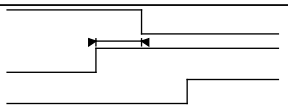
DATA SHEET

FD1 FD1 3/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	---

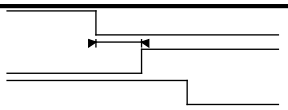
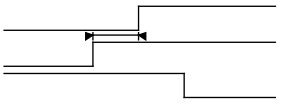
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.352	0.334	0.305	0.209
0.38	0.388	0.370	0.339	0.241
1.00	0.448	0.429	0.397	0.295
3.00	0.641	0.620	0.584	0.468

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.291	0.323	0.377	0.551
0.38	0.257	0.289	0.343	0.517
1.00	0.200	0.232	0.286	0.460
3.00	0.016	0.048	0.102	0.276

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.368	0.336	0.282	0.107
0.38	0.402	0.369	0.315	0.141
1.00	0.458	0.426	0.372	0.198
3.00	0.641	0.609	0.555	0.382

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.305	0.322	0.352	0.447
0.38	0.269	0.287	0.318	0.416
1.00	0.209	0.228	0.260	0.362
3.00	0.016	0.038	0.074	0.190

Estimated Wiring Load Table

Table 1-17 **TC200G Series (Double-layer Metal)**

Double-layer metal	
Part Number	EWL (LU)
TC200G42	2.056×WAY+1.028
TC200G40	1.935×WAY+0.968
TC200G36	1.855×WAY+0.928
TC200G32	1.769×WAY+0.885
TC200G24	1.641×WAY+0.821
TC200G20	1.570×WAY+0.785
TC200G16	1.493×WAY+0.746
TC200G14	1.440×WAY+0.720
TC200G12	1.396×WAY+0.698
TC200G10	1.349×WAY+0.674
TC200G08	1.305×WAY+0.652
TC200G06	1.237×WAY+0.618
TC200G04	1.146×WAY+0.573
TC200G02	1.040×WAY+0.520

Note: "WAY" stands for the number of branches into which the output pin forks.

Table 1-18 **TC200G Series (Triple-layer Metal)**

Triple-layer metal	
Part Number	EWL (LU)
TC200G92	1.966×WAY+0.983
TC200G90	1.851×WAY+0.925
TC200G86	1.774×WAY+0.887
TC200G82	1.692×WAY+0.846
TC200G74	1.570×WAY+0.785
TC200G70	1.501×WAY+0.751
TC200G66	1.427×WAY+0.714
TC200G64	1.378×WAY+0.689
TC200G62	1.335×WAY+0.668
TC200G60	1.290×WAY+0.645
TC200G58	1.248×WAY+0.624
TC200G56	1.183×WAY+0.591
TC200G54	1.096×WAY+0.548
TC200G52	0.994×WAY+0.497

Note: "WAY" stands for the number of branches into which the output pin forks.

Table 1-19 **TC200E Series (Double-layer Metal)**

Double-layer metal	
Part Number	EWL (LU)
TC200E020	1.040×WAY+0.520
TC200E040	1.146×WAY+0.573
TC200E060	1.237×WAY+0.618
TC200E080	1.305×WAY+0.652
TC200E100	1.349×WAY+0.674
TC200E120	1.396×WAY+0.698
TC200E140	1.440×WAY+0.720
TC200E160	1.493×WAY+0.746
TC200E180	1.532×WAY+0.766
TC200E200	1.570×WAY+0.785
TC200E220	1.606×WAY+0.803
TC200E240	1.641×WAY+0.821
TC200E260	1.675×WAY+0.837
TC200E280	1.707×WAY+0.854
TC200E300	1.739×WAY+0.869
TC200E320	1.769×WAY+0.885
TC200E340	1.813×WAY+0.907
TC200E360	1.855×WAY+0.928
TC200E380	1.896×WAY+0.948
TC200E400	1.935×WAY+0.968
*TC200E420	2.056×WAY+1.028

* : Under development

Note: "WAY" stands for the number of branches into which the output pin forks.

Table 1-20 **TC200E Series (Triple-layer Metal)**

Triple-layer metal	
Part Number	EWL (LU)
TC200E580	1.248×WAY+0.624
TC200E600	1.290×WAY+0.645
TC200E620	1.335×WAY+0.668
TC200E640	1.378×WAY+0.689
TC200E660	1.427×WAY+0.714
TC200E680	1.465×WAY+0.733
TC200E700	1.501×WAY+0.751
TC200E720	1.536×WAY+0.768
TC200E740	1.570×WAY+0.785
TC200E760	1.602×WAY+0.801
TC200E780	1.633×WAY+0.816
TC200E800	1.663×WAY+0.832
TC200E820	1.692×WAY+0.846
TC200E840	1.734×WAY+0.867
TC200E860	1.774×WAY+0.887
TC200E880	1.813×WAY+0.907
TC200E900	1.851×WAY+0.925
*TC200E920	1.966×WAY+0.983

* : Under development

Note: "WAY" stands for the number of branches into which the output pin forks.

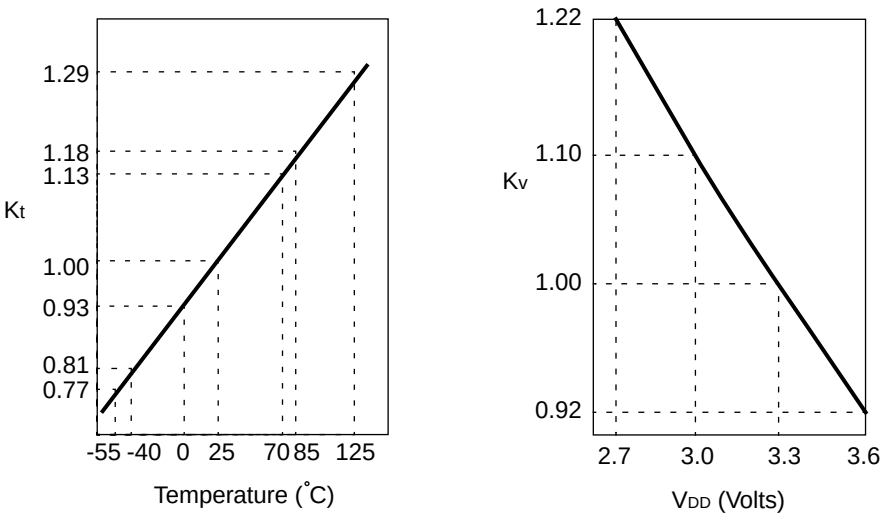
Variations in Propagation Delays

The previous subsections explained how to determine propagation delays under the “nominal” (typical) condition. The nominal condition represents a 3.3V power supply, 25 temperature, and nominal process model.

Once the nominal delay is calculated, the best- and worst-case analyses should be made. the best- and worst-case propagation delays of a macrocell are determined by multiplying its nominal delay by appropriate factors called K-factors(Kf).

Process variation could decrease or increase delays. Thus, a multiplier factor called Kp is used to estimate the effect of best- and worst-case processing. Junction Multipliers for Kt and Kv are shown in Figure 1-20.

Figure 1-20 **Propagation Delay as a Function of Temperature and as a Function on Supply Voltage**



The formula for calculating the overall K-factor (Kf) is:

$$Kp \times Kt \times Kv$$

The typical-case, best-case, and worst-case Kf factors are shown in Table 1-21 and Table 1-22.

The “commercial” operating conditions are defined below:

Worst-case commercial: 70 °C, 2.7V
Best-case commercial: 0 °C, 3.6V

It is probable that the supply voltage and junction temperature differ from these standards. The user can calculate K-factors for operating conditions other than the standard ones in a similar manner.

Table 1-21 TC200G Series Maximum Delay Factor (Kf)

VDD	Kf (Ta=0 °C~70°C)		
	Best-case	Typical-case	Worst-case
3.3V±0.3V	0.51	1.00	1.68
3.0V±0.3V	0.56	(1.10)	1.86

Table 1-22 TC200E Series Maximum Delay Factor (Kf)

VDD	Kf (Ta=0 °C~70°C)		
	Best-case	Typical-case	Worst-case
3.3V±0.3V	0.51	1.00	1.74
3.0V±0.3V	0.56	(1.10)	1.93

Reading Data Sheets

Macrocell “ND2” is given as an example.

(1) CELL NAME:

Macrocell name.
‘x’ can be substituted by characteristics, for example, pull-up, pull-down, open-drain, high-speed and slew-rate, etc. on I/O macrocells. Please see “CELL NAME” of data sheet for more details.

(2) FUNCTION:

Function of macrocells.

(3) CELL COUNT:

Numbers of gates and I/O slots used by the macrocell.

(4) LOGIC SYMBOL:

Logic symbol of macrocell.

(5) TRUTH TABLE

Truth table which shows the state of I/O. X indicates the state of “Do not care” and Hz is “High impedance”.

(6) Verilog-HDL DESCRIPTION

(7) VHDL DESCRIPTION

(8) ELECTROMIGRATION:

To avoid potential electromigration problems, the maximum load that an macrocell output can drive is specified, based on its switching speed. The “ELECTROMIGRATION” table lists the maximum values of the load (in LU) times the switching frequency (in MHz). The following examples illustrate the way to calculate the maximum output drive using the switching frequency (f) as a basis:

When f=10 MHz: 6880÷ 10 = 688

When f=100 MHz: 6880÷ 100 = 69

Notes: ***The maximum load a macrocell output can drive is determined as the smaller of this result and the OUTPUT DRIVE value.***

(9) INPUT LOAD:

Load capacitance of macrocell input in LU unit. It is also a factor of delay calculation.

(10) OUTPUT DRIVE:

Load drive capability of macrocell output in units of LU.

(11) PATH CONDITION

This table shows the conditions when the validity of pin-to-pin delays are conditioned by other pins.

PATH: shows a module path. Since more than one source may have a module path to the same destination, each source (or input) pin is listed for each destination (or output) pin.

CONDITION: shows the Boolean equation when the validity of the path delay is state-dependent. Examples of Boolean equations are given below:

~B

~A|B&~C

A&~B

The tilde character (~) denotes negation or NOT.

FUNCTION: There may be delay values independently for each of the four output transitions.

IO LEVEL: Output buffer propagation delay is a function of buffer type, capacitive load, and type of device being driven. When driving CMOS chips, output buffer propagation delays are measured from their inception to the time at which the signal achieves the CMOS threshold of 1.5 volts. When driving LVTTL chips, the delays are measured from their inception to the time at which the signal achieves the LVTTL threshold of 1.5 volts.

(12) SLEW FACTOR

This table shows parameters used to calculate the input slew rate (or transition time). Input slew rate is determined by the following equation:

(Input slew rate) = FACTOR x output_load + CONSTANT

(13) PATH DELAY

This is a lookup table indexed by output loads and input slew rates. The total propagation delay is computed by interpolating table values.

Notes: ***(1) For I/O macrocells, following values are shown in chapter "DC Characteristics" table on page 1-34: output current, threshold voltage, and pull-up/pull-down transistor characteristic.***

(2)Pad capacitance is shown in 'INPUT CAPACITANCE' table on input buffer and a state of output buffer is 'Hz'.

(3) 'TRUTH TABLE' and 'AC CHARACTERISTICS' of input buffer are not included in Data Sheet of bidirectional buffer. Please see Data Sheet of same type macrocell.

Figure 1-21 **Example of Macrocell Data Sheet**

Chapter 2

Internal Macrocells

Alphanumeric Index

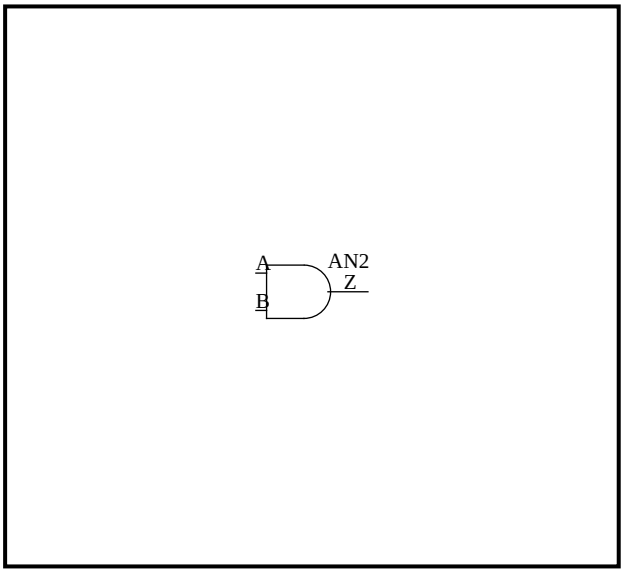
Internal Macrocell Data Sheets

ver. 1.10.5

AN2	AN2	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
AN2	2-INPUT AND	2	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
A	B	Z
L	L	L
L	H	L
H	L	L
H	H	H

Verilog-HDL DESCRIPTION

```
AN2  inst(Z,A,B);
```

VHDL DESCRIPTION

```
inst:AN2
   port   map(Z,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.08
B	1.09

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	45.6

Rev.1.01.10

AN2 AN2 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0939	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.31	0.48	1.12
0.38	0.24	0.38	0.54	1.18
1.00	0.31	0.45	0.61	1.26
3.00	0.46	0.61	0.77	1.42

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0397	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.28	0.39	0.85
0.38	0.20	0.30	0.42	0.88
1.00	0.24	0.35	0.47	0.93
3.00	0.31	0.43	0.55	1.02

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0939	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.33	0.49	1.13
0.38	0.24	0.38	0.54	1.18
1.00	0.29	0.43	0.60	1.24
3.00	0.40	0.54	0.71	1.36

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0397	0.07

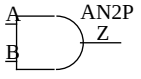
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.31	0.43	0.89
0.38	0.23	0.34	0.46	0.91
1.00	0.29	0.40	0.52	0.98
3.00	0.40	0.53	0.65	1.12

Rev.1.01.10

AN2P	AN2P	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
AN2P	2-INPUT AND	2	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
A	B	Z
L	L	L
L	H	L
H	L	L
H	H	H

Verilog-HDL DESCRIPTION

```
AN2P  inst(Z,A,B);
```

VHDL DESCRIPTION

```
inst:AN2P
   port   map(Z,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.01
B	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	82.1

Rev.1.01.10

AN2P | AN2P | 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0546	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.27	0.37	0.74
0.38	0.26	0.35	0.45	0.82
1.00	0.35	0.43	0.53	0.90
3.00	0.54	0.62	0.72	1.09

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0203	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.26	0.33	0.58
0.38	0.22	0.28	0.36	0.61
1.00	0.27	0.34	0.41	0.67
3.00	0.36	0.44	0.51	0.78

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0546	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.29	0.38	0.76
0.38	0.25	0.34	0.44	0.81
1.00	0.32	0.41	0.50	0.88
3.00	0.45	0.54	0.64	1.02

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

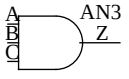
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0203	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.29	0.36	0.62
0.38	0.24	0.32	0.39	0.64
1.00	0.31	0.38	0.45	0.71
3.00	0.44	0.52	0.60	0.87

AN3	AN3	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
AN3	3-INPUT AND	2	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
A	B	C	Z
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

Verilog-HDL DESCRIPTION

```
AN3  inst(Z,A,B,C);
```

VHDL DESCRIPTION

```
inst:AN3
   port   map(Z,A,B,C);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.06
B	1.02
C	0.98

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	46.0

Rev.1.01.10

AN3 AN3 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0957	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.38	0.55	1.22
0.38	0.31	0.45	0.63	1.29
1.00	0.40	0.55	0.72	1.39
3.00	0.64	0.79	0.97	1.64

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0362	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.28	0.40	0.82
0.38	0.21	0.31	0.43	0.85
1.00	0.24	0.35	0.46	0.89
3.00	0.26	0.38	0.50	0.93

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0957	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.40	0.58	1.24
0.38	0.31	0.46	0.63	1.30
1.00	0.40	0.55	0.72	1.39
3.00	0.61	0.76	0.93	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0362	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.32	0.43	0.86
0.38	0.24	0.35	0.46	0.89
1.00	0.28	0.39	0.51	0.94
3.00	0.35	0.47	0.59	1.02

AN3 AN3 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0957	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.42	0.59	1.25
0.38	0.31	0.45	0.62	1.29
1.00	0.35	0.50	0.67	1.34
3.00	0.45	0.61	0.78	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

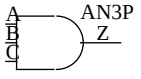
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0362	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.35	0.46	0.90
0.38	0.26	0.37	0.49	0.92
1.00	0.32	0.44	0.55	0.99
3.00	0.45	0.58	0.70	1.13

AN3P	AN3P	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
AN3P	3-INPUT AND	3	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
A	B	C	Z
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

Verilog-HDL DESCRIPTION

```
AN3P  inst(Z,A,B,C);
```

VHDL DESCRIPTION

```
inst:AN3P
   port   map(Z,A,B,C);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.07
B	1.08
C	0.99

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	78.5

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AN3P AN3P 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0541	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.35	0.45	0.83
0.38	0.34	0.43	0.53	0.91
1.00	0.45	0.54	0.64	1.02
3.00	0.72	0.81	0.91	1.29

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0238	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.28	0.36	0.64
0.38	0.23	0.31	0.39	0.67
1.00	0.28	0.35	0.43	0.72
3.00	0.32	0.41	0.49	0.79

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0541	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.38	0.48	0.86
0.38	0.34	0.43	0.53	0.91
1.00	0.44	0.53	0.63	1.01
3.00	0.67	0.76	0.86	1.25

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0238	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.31	0.39	0.68
0.38	0.26	0.34	0.42	0.71
1.00	0.31	0.39	0.47	0.76
3.00	0.39	0.48	0.57	0.87

AN3P | AN3P | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0541	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.39	0.49	0.87
0.38	0.34	0.43	0.53	0.91
1.00	0.39	0.48	0.58	0.96
3.00	0.52	0.61	0.72	1.11

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

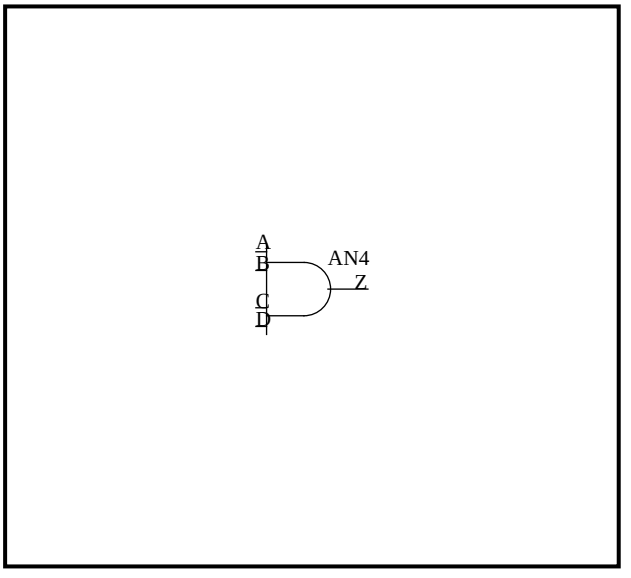
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0238	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.33	0.41	0.71
0.38	0.27	0.36	0.44	0.73
1.00	0.34	0.42	0.51	0.80
3.00	0.46	0.56	0.65	0.95

AN4	AN4	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
AN4	4-INPUT AND	3	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT
A	B	C	D	Z
H	H	H	H	H
ALL OTHER COMBINATIONS				L

Verilog-HDL DESCRIPTION

```
AN4  inst(Z,A,B,C,D);
```

VHDL DESCRIPTION

```
inst:AN4
   port   map(Z,A,B,C,D);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A,B	1.04
C	0.98
D	1.08

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	46.4

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AN4 AN4 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0928	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.43	0.60	1.25
0.38	0.35	0.50	0.67	1.32
1.00	0.45	0.60	0.78	1.43
3.00	0.74	0.89	1.06	1.72

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0370	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.29	0.40	0.84
0.38	0.22	0.32	0.44	0.87
1.00	0.24	0.35	0.47	0.90
3.00	0.23	0.35	0.47	0.92

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0928	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.46	0.63	1.28
0.38	0.37	0.52	0.69	1.34
1.00	0.46	0.61	0.79	1.44
3.00	0.73	0.88	1.05	1.71

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0370	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.33	0.44	0.88
0.38	0.25	0.35	0.47	0.91
1.00	0.28	0.40	0.51	0.95
3.00	0.31	0.43	0.56	1.01

AN4 AN4 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0928	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.49	0.67	1.32
0.38	0.38	0.53	0.70	1.35
1.00	0.45	0.60	0.77	1.42
3.00	0.64	0.80	0.97	1.63

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0370	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.37	0.49	0.93
0.38	0.28	0.39	0.51	0.95
1.00	0.33	0.45	0.57	1.01
3.00	0.41	0.55	0.67	1.12

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0928	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.51	0.68	1.33
0.38	0.39	0.54	0.71	1.36
1.00	0.43	0.58	0.76	1.41
3.00	0.56	0.72	0.90	1.56

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	FALL

SLEW FACTOR

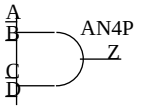
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0370	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.39	0.52	0.96
0.38	0.30	0.41	0.54	0.98
1.00	0.36	0.48	0.60	1.04
3.00	0.47	0.60	0.73	1.19

AN4P	AN4P	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
AN4P	4-INPUT AND	3	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT
A	B	C	D	Z
H	H	H	H	H
ALL OTHER COMBINATIONS				L

Verilog-HDL DESCRIPTION

```
AN4P  inst(Z,A,B,C,D);
```

VHDL DESCRIPTION

```
inst:AN4P
   port   map(Z,A,B,C,D);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A,D	1.06
B,C	1.01

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	78.4

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AN4P | AN4P | 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0539	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.39	0.50	0.89
0.38	0.38	0.47	0.58	0.96
1.00	0.50	0.59	0.69	1.08
3.00	0.81	0.90	1.00	1.39

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0237	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.27	0.35	0.64
0.38	0.23	0.31	0.39	0.67
1.00	0.27	0.35	0.43	0.72
3.00	0.28	0.37	0.46	0.76

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0539	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.43	0.54	0.92
0.38	0.39	0.49	0.59	0.98
1.00	0.50	0.59	0.69	1.08
3.00	0.78	0.87	0.97	1.36

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0237	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.31	0.39	0.67
0.38	0.26	0.34	0.42	0.70
1.00	0.30	0.39	0.47	0.76
3.00	0.35	0.44	0.53	0.83

AN4P | AN4P | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0539	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.46	0.57	0.95
0.38	0.41	0.50	0.60	0.99
1.00	0.47	0.56	0.67	1.06
3.00	0.67	0.76	0.87	1.26

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0237	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.35	0.43	0.72
0.38	0.29	0.37	0.45	0.75
1.00	0.35	0.43	0.52	0.81
3.00	0.45	0.54	0.63	0.94

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0539	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.38	0.47	0.58	0.96
0.38	0.41	0.50	0.61	0.99
1.00	0.45	0.54	0.65	1.04
3.00	0.59	0.68	0.79	1.19

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	FALL

SLEW FACTOR

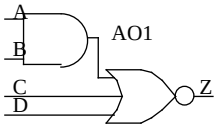
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0237	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.34	0.43	0.72
0.38	0.28	0.37	0.45	0.75
1.00	0.34	0.43	0.51	0.81
3.00	0.46	0.55	0.65	0.95

AO1	AO1	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
AO1	2-INPUT AND into 3-INPUT NOR	2	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT
A	B	C	D	Z
L	L	L	L	H
L	H	L	L	H
H	L	L	L	H
ALL OTHER COMBINATIONS				L

Verilog-HDL DESCRIPTION

```
AO1  inst(Z,A,B,C,D);
```

VHDL DESCRIPTION

```
inst:AO1
   port   map(Z,A,B,C,D);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.08
B	1.05
C	0.98
D	1.00

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	14.5

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AO1 AO1 2/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.2784	0.46

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.74	1.23	3.17
0.38	0.36	0.75	1.23	3.18
1.00	0.44	0.81	1.29	3.21
3.00	0.69	1.08	1.54	3.40

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0656	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.27	0.46	1.20
0.38	0.18	0.33	0.52	1.26
1.00	0.21	0.40	0.60	1.35
3.00	0.20	0.48	0.76	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.2784	0.46

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.67	1.16	3.11
0.38	0.30	0.68	1.17	3.12
1.00	0.37	0.75	1.22	3.15
3.00	0.58	0.99	1.46	3.34

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0656	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.26	0.44	1.18
0.38	0.18	0.34	0.53	1.27
1.00	0.23	0.44	0.65	1.41
3.00	0.24	0.57	0.88	1.79

AO1 AO1 3/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&~B&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.2784	0.46

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.38	0.77	1.26	3.21
0.38	0.36	0.76	1.25	3.20
1.00	0.39	0.77	1.25	3.19
3.00	0.56	0.94	1.40	3.27

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&~B&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0656	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.19	0.31	0.79
0.38	0.16	0.27	0.40	0.88
1.00	0.20	0.36	0.51	1.02
3.00	0.20	0.46	0.70	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&B&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.2784	0.46

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.85	1.34	3.28
0.38	0.44	0.84	1.33	3.28
1.00	0.46	0.85	1.33	3.27
3.00	0.64	1.01	1.47	3.34

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&B&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0656	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.20	0.32	0.81
0.38	0.17	0.28	0.41	0.89
1.00	0.22	0.37	0.52	1.04
3.00	0.23	0.48	0.72	1.39

AO1 AO1 4/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&~B&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.2784	0.46

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.67	1.08	2.70
0.38	0.33	0.66	1.07	2.70
1.00	0.37	0.69	1.09	2.71
3.00	0.55	0.88	1.27	2.84

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&~B&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0656	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.20	0.32	0.80
0.38	0.17	0.28	0.41	0.89
1.00	0.22	0.37	0.52	1.03
3.00	0.24	0.49	0.72	1.39

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	A&~B&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.2784	0.46

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.40	0.80	1.28	3.23
0.38	0.38	0.78	1.27	3.22
1.00	0.37	0.76	1.24	3.18
3.00	0.49	0.86	1.31	3.17

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	A&~B&~C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0656	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.20	0.32	0.80
0.38	0.16	0.28	0.40	0.89
1.00	0.20	0.37	0.52	1.03
3.00	0.22	0.48	0.71	1.39

AO1 AO1 5/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~A&B&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.2784	0.46

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.87	1.36	3.30
0.38	0.45	0.85	1.34	3.30
1.00	0.44	0.83	1.32	3.26
3.00	0.56	0.93	1.38	3.24

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~A&B&~C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0656	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.21	0.33	0.82
0.38	0.17	0.29	0.42	0.90
1.00	0.23	0.38	0.53	1.05
3.00	0.26	0.50	0.73	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~A&~B&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.2784	0.46

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.69	1.10	2.72
0.38	0.34	0.67	1.09	2.71
1.00	0.34	0.66	1.07	2.68
3.00	0.45	0.77	1.15	2.70

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~A&~B&~C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0656	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.21	0.33	0.81
0.38	0.17	0.29	0.41	0.90
1.00	0.23	0.38	0.53	1.04
3.00	0.27	0.51	0.74	1.40

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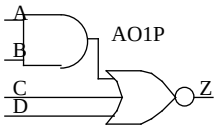
AO1P	AO1P	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
AO1P	2-INPUT AND into 3-INPUT NOR	4	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT
A	B	C	D	Z
L	L	L	L	H
L	H	L	L	H
H	L	L	L	H
ALL OTHER COMBINATIONS				L

Verilog-HDL DESCRIPTION

```
AO1P  inst(Z,A,B,C,D);
```

VHDL DESCRIPTION

```
inst:AO1P
   port   map(Z,A,B,C,D);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A,C	2.08
B	2.16
D	1.98

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	27.9

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AO1P | AO1P | 2/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1458	0.49

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.45	0.71	1.72
0.38	0.26	0.46	0.72	1.74
1.00	0.34	0.54	0.78	1.78
3.00	0.55	0.78	1.03	2.01

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0305	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.16	0.25	0.61
0.38	0.16	0.24	0.34	0.70
1.00	0.19	0.31	0.43	0.83
3.00	0.18	0.38	0.57	1.12

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1458	0.49

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.53	0.78	1.80
0.38	0.33	0.53	0.78	1.80
1.00	0.41	0.61	0.85	1.84
3.00	0.66	0.87	1.12	2.09

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0305	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.18	0.27	0.62
0.38	0.15	0.23	0.32	0.69
1.00	0.18	0.29	0.39	0.77
3.00	0.15	0.31	0.48	0.97

AO1P | AO1P | 3/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&~B&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1458	0.49

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.43	0.64	0.89	1.91
0.38	0.41	0.62	0.88	1.90
1.00	0.43	0.63	0.88	1.89
3.00	0.60	0.80	1.04	2.00

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&~B&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0305	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.14	0.20	0.43
0.38	0.15	0.21	0.28	0.52
1.00	0.19	0.28	0.37	0.65
3.00	0.19	0.34	0.48	0.90

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&B&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1458	0.49

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.56	0.82	1.83
0.38	0.33	0.54	0.80	1.82
1.00	0.35	0.55	0.81	1.81
3.00	0.52	0.73	0.97	1.93

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&B&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0305	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.07	0.12	0.18	0.42
0.38	0.14	0.20	0.27	0.51
1.00	0.17	0.27	0.36	0.63
3.00	0.15	0.31	0.46	0.89

AO1P | AO1P | 4/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&~B&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1458	0.49

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.49	0.70	1.54
0.38	0.30	0.47	0.69	1.54
1.00	0.34	0.50	0.71	1.55
3.00	0.51	0.69	0.90	1.71

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&~B&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0305	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.08	0.13	0.19	0.43
0.38	0.15	0.21	0.28	0.52
1.00	0.20	0.28	0.37	0.65
3.00	0.20	0.34	0.49	0.91

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	A&~B&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1458	0.49

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.66	0.91	1.93
0.38	0.42	0.63	0.89	1.91
1.00	0.41	0.62	0.87	1.88
3.00	0.54	0.73	0.97	1.92

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	A&~B&~C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0305	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.14	0.20	0.44
0.38	0.16	0.22	0.28	0.53
1.00	0.20	0.29	0.38	0.65
3.00	0.21	0.36	0.50	0.92

AO1P | AO1P | 5/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~A&B&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1458	0.49

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.58	0.84	1.85
0.38	0.34	0.55	0.81	1.84
1.00	0.34	0.54	0.79	1.80
3.00	0.46	0.67	0.90	1.85

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~A&B&~C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0305	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.08	0.13	0.19	0.43
0.38	0.14	0.20	0.27	0.52
1.00	0.18	0.27	0.36	0.64
3.00	0.17	0.33	0.47	0.90

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~A&~B&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1458	0.49

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.51	0.72	1.56
0.38	0.31	0.49	0.70	1.55
1.00	0.31	0.48	0.69	1.52
3.00	0.42	0.60	0.80	1.59

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~A&~B&~C	FALL

SLEW FACTOR

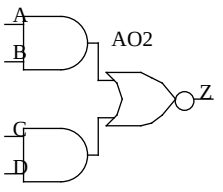
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0305	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.14	0.20	0.44
0.38	0.16	0.22	0.28	0.52
1.00	0.20	0.29	0.38	0.65
3.00	0.23	0.37	0.51	0.92

AO2	AO2	1/7

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
AO2	2-WIDE 2-INPUT AND into 2-INPUT NOR	2	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT
A	B	C	D	Z
L	L	H	H	L
L	H	H	H	L
H	L	H	H	L
H	H	L	L	L
H	H	L	H	L
H	H	H	L	L
H	H	H	H	L
ALL OTHER COMBINATIONS				H

Verilog-HDL DESCRIPTION

```
AO2  inst(Z,A,B,C,D);
```

VHDL DESCRIPTION

```
inst:AO2
   port   map(Z,A,B,C,D);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.04
B	1.08
C	1.00
D	0.99

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	19.5

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AO2 AO2 2/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&C&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.2017	0.43

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.50	0.85	2.25
0.38	0.23	0.51	0.86	2.27
1.00	0.29	0.57	0.92	2.31
3.00	0.45	0.77	1.13	2.50

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&C&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.26	0.44	1.18
0.38	0.18	0.34	0.53	1.27
1.00	0.23	0.44	0.65	1.41
3.00	0.27	0.59	0.89	1.79

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~C&D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.2017	0.43

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.53	0.86	2.21
0.38	0.27	0.54	0.88	2.23
1.00	0.33	0.61	0.93	2.27
3.00	0.49	0.80	1.14	2.46

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~C&D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.28	0.46	1.20
0.38	0.20	0.36	0.55	1.29
1.00	0.25	0.46	0.67	1.43
3.00	0.32	0.62	0.91	1.81

AO2 AO2 3/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~C&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.2017	0.43

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.39	0.65	1.73
0.38	0.19	0.41	0.67	1.75
1.00	0.24	0.46	0.73	1.79
3.00	0.34	0.62	0.91	2.00

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~C&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.26	0.44	1.18
0.38	0.18	0.34	0.53	1.27
1.00	0.23	0.44	0.65	1.41
3.00	0.30	0.61	0.90	1.79

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&C&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.2017	0.43

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.55	0.90	2.30
0.38	0.28	0.56	0.91	2.31
1.00	0.35	0.62	0.96	2.35
3.00	0.54	0.84	1.19	2.55

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&C&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.27	0.46	1.20
0.38	0.17	0.33	0.52	1.26
1.00	0.21	0.40	0.60	1.35
3.00	0.22	0.50	0.76	1.61

AO2 AO2 4/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~C&D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.2017	0.43

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.58	0.92	2.26
0.38	0.32	0.59	0.93	2.27
1.00	0.39	0.65	0.98	2.31
3.00	0.58	0.87	1.20	2.51

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~C&D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.29	0.48	1.22
0.38	0.19	0.35	0.54	1.28
1.00	0.24	0.42	0.62	1.37
3.00	0.26	0.53	0.79	1.63

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~C&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.2017	0.43

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.43	0.69	1.77
0.38	0.23	0.44	0.71	1.78
1.00	0.28	0.50	0.77	1.83
3.00	0.43	0.69	0.97	2.04

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~C&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.27	0.46	1.20
0.38	0.17	0.33	0.52	1.26
1.00	0.21	0.40	0.60	1.35
3.00	0.24	0.51	0.77	1.61

AO2 AO2 5/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.2017	0.43

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.62	0.96	2.30
0.38	0.34	0.62	0.96	2.30
1.00	0.35	0.62	0.95	2.29
3.00	0.43	0.70	1.02	2.31

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.32	0.51	1.25
0.38	0.22	0.38	0.57	1.31
1.00	0.27	0.45	0.65	1.40
3.00	0.33	0.58	0.83	1.66

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.2017	0.43

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.57	0.91	2.25
0.38	0.29	0.57	0.90	2.25
1.00	0.30	0.57	0.90	2.23
3.00	0.38	0.65	0.97	2.26

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.30	0.49	1.23
0.38	0.20	0.36	0.55	1.29
1.00	0.25	0.43	0.63	1.38
3.00	0.30	0.56	0.81	1.64

AO2 AO2 6/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&~A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.2017	0.43

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.45	0.71	1.72
0.38	0.25	0.46	0.71	1.73
1.00	0.26	0.47	0.73	1.74
3.00	0.34	0.56	0.82	1.83

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&~A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.32	0.50	1.24
0.38	0.21	0.37	0.56	1.30
1.00	0.27	0.45	0.64	1.39
3.00	0.34	0.59	0.84	1.66

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.2017	0.43

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.60	0.95	2.35
0.38	0.31	0.60	0.96	2.36
1.00	0.32	0.60	0.95	2.34
3.00	0.37	0.67	1.01	2.37

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.31	0.50	1.24
0.38	0.23	0.39	0.58	1.32
1.00	0.30	0.49	0.70	1.46
3.00	0.40	0.68	0.96	1.85

AO2 AO2 7/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.2017	0.43

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.55	0.90	2.30
0.38	0.26	0.55	0.90	2.31
1.00	0.27	0.55	0.90	2.29
3.00	0.32	0.61	0.96	2.32

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.29	0.48	1.22
0.38	0.21	0.37	0.56	1.30
1.00	0.27	0.47	0.68	1.44
3.00	0.36	0.65	0.94	1.83

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&~A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.2017	0.43

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.44	0.71	1.78
0.38	0.22	0.45	0.72	1.80
1.00	0.24	0.46	0.74	1.81
3.00	0.29	0.54	0.82	1.89

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&~A&~B	FALL

SLEW FACTOR

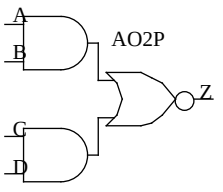
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.30	0.49	1.23
0.38	0.22	0.38	0.57	1.31
1.00	0.30	0.49	0.70	1.45
3.00	0.41	0.69	0.97	1.85

AO2P	AO2P	1/7

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
AO2P	2-WIDE 2-INPUT AND into 2-INPUT NOR	4	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT
A	B	C	D	Z
L	L	H	H	L
L	H	H	H	L
H	L	H	H	L
H	H	L	L	L
H	H	L	H	L
H	H	H	L	L
H	H	H	H	L
ALL OTHER COMBINATIONS				H

Verilog-HDL DESCRIPTION

```
AO2P  inst(Z,A,B,C,D);
```

VHDL DESCRIPTION

```
inst:AO2P
   port   map(Z,A,B,C,D);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	2.00
B,D	2.15
C	2.16

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	37.8

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AO2P | AO2P | 2/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&C&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1014	0.31

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.33	0.51	1.21
0.38	0.20	0.34	0.52	1.23
1.00	0.26	0.41	0.58	1.28
3.00	0.41	0.59	0.79	1.50

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&C&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0319	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.17	0.26	0.63
0.38	0.16	0.24	0.34	0.72
1.00	0.19	0.32	0.44	0.85
3.00	0.22	0.41	0.59	1.14

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~C&D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1014	0.31

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.38	0.56	1.27
0.38	0.26	0.40	0.58	1.29
1.00	0.32	0.46	0.64	1.33
3.00	0.48	0.65	0.84	1.55

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~C&D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0319	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.19	0.28	0.65
0.38	0.18	0.26	0.36	0.74
1.00	0.23	0.34	0.46	0.87
3.00	0.27	0.45	0.62	1.16

AO2P | AO2P | 3/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~C&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1014	0.31

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.27	0.41	0.98
0.38	0.17	0.29	0.43	1.00
1.00	0.22	0.34	0.49	1.05
3.00	0.33	0.49	0.66	1.25

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~C&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0319	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.17	0.26	0.63
0.38	0.15	0.24	0.34	0.71
1.00	0.20	0.32	0.44	0.85
3.00	0.24	0.43	0.61	1.15

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&C&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1014	0.31

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.38	0.56	1.27
0.38	0.25	0.39	0.57	1.28
1.00	0.32	0.46	0.64	1.33
3.00	0.51	0.68	0.86	1.56

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&C&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0319	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.18	0.27	0.65
0.38	0.16	0.24	0.33	0.71
1.00	0.19	0.29	0.40	0.79
3.00	0.18	0.34	0.50	1.00

AO2P | AO2P | 4/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~C&D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1014	0.31

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.44	0.62	1.33
0.38	0.31	0.45	0.63	1.34
1.00	0.37	0.52	0.69	1.38
3.00	0.58	0.74	0.91	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~C&D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0319	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.20	0.30	0.67
0.38	0.18	0.26	0.35	0.73
1.00	0.21	0.31	0.42	0.81
3.00	0.22	0.37	0.53	1.02

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~C&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1014	0.31

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.31	0.46	1.02
0.38	0.21	0.33	0.47	1.04
1.00	0.27	0.39	0.53	1.09
3.00	0.43	0.57	0.73	1.30

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~C&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0319	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.18	0.27	0.65
0.38	0.15	0.24	0.33	0.71
1.00	0.19	0.29	0.40	0.79
3.00	0.20	0.35	0.51	1.01

AO2P | AO2P | 5/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1014	0.31

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.49	0.66	1.37
0.38	0.33	0.48	0.66	1.37
1.00	0.34	0.48	0.65	1.35
3.00	0.41	0.56	0.73	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0319	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.23	0.33	0.70
0.38	0.20	0.28	0.38	0.76
1.00	0.25	0.35	0.45	0.84
3.00	0.30	0.44	0.59	1.06

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1014	0.31

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.43	0.61	1.32
0.38	0.28	0.42	0.60	1.31
1.00	0.28	0.42	0.60	1.30
3.00	0.36	0.50	0.68	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0319	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.21	0.31	0.68
0.38	0.18	0.26	0.36	0.74
1.00	0.22	0.32	0.43	0.82
3.00	0.26	0.41	0.56	1.04

AO2P | AO2P | 6/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&~A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1014	0.31

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.34	0.48	1.01
0.38	0.23	0.34	0.48	1.01
1.00	0.25	0.36	0.49	1.02
3.00	0.32	0.44	0.58	1.11

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&~A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0319	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.23	0.32	0.69
0.38	0.20	0.28	0.37	0.75
1.00	0.25	0.34	0.45	0.84
3.00	0.31	0.45	0.59	1.06

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1014	0.31

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.43	0.61	1.32
0.38	0.28	0.43	0.61	1.32
1.00	0.28	0.43	0.60	1.31
3.00	0.33	0.48	0.66	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0319	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.22	0.31	0.69
0.38	0.21	0.29	0.39	0.77
1.00	0.27	0.38	0.50	0.90
3.00	0.37	0.52	0.69	1.21

AO2P | AO2P | 7/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1014	0.31

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.38	0.56	1.26
0.38	0.23	0.37	0.55	1.27
1.00	0.23	0.37	0.55	1.25
3.00	0.27	0.42	0.60	1.29

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0319	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.20	0.29	0.67
0.38	0.19	0.27	0.37	0.75
1.00	0.24	0.36	0.48	0.88
3.00	0.32	0.49	0.66	1.19

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&~A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1014	0.31

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.31	0.44	0.97
0.38	0.19	0.31	0.44	0.98
1.00	0.20	0.32	0.45	0.99
3.00	0.24	0.37	0.52	1.06

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&~A&~B	FALL

SLEW FACTOR

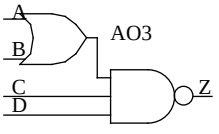
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0319	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.21	0.31	0.68
0.38	0.21	0.29	0.39	0.76
1.00	0.27	0.38	0.50	0.89
3.00	0.38	0.54	0.70	1.22

AO3	AO3	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
AO3	2-INPUT OR into 3-INPUT NAND	2	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT
A	B	C	D	Z
L	H	H	H	L
H	L	H	H	L
H	H	H	H	L
ALL OTHER COMBINATIONS				H

Verilog-HDL DESCRIPTION

```
AO3  inst(Z,A,B,C,D);
```

VHDL DESCRIPTION

```
inst:AO3
   port   map(Z,A,B,C,D);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.05
B	1.08
C	0.98
D	1.00

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	19.4

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AO3 AO3 2/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1783	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.44	0.75	1.98
0.38	0.21	0.46	0.77	2.01
1.00	0.24	0.51	0.82	2.05
3.00	0.31	0.63	0.97	2.22

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1000	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.38	0.66	1.77
0.38	0.23	0.46	0.74	1.86
1.00	0.30	0.58	0.87	2.00
3.00	0.43	0.81	1.19	2.42

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1783	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.46	0.77	2.01
0.38	0.21	0.47	0.78	2.02
1.00	0.21	0.47	0.78	2.02
3.00	0.20	0.49	0.81	2.05

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1000	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.41	0.68	1.80
0.38	0.26	0.49	0.77	1.88
1.00	0.34	0.61	0.90	2.02
3.00	0.51	0.86	1.23	2.45

AO3 AO3 3/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1783	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.31	0.48	1.16
0.38	0.19	0.33	0.51	1.19
1.00	0.22	0.38	0.56	1.24
3.00	0.25	0.45	0.67	1.42

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1000	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.37	0.61	1.54
0.38	0.24	0.44	0.67	1.60
1.00	0.32	0.53	0.78	1.71
3.00	0.47	0.75	1.04	2.05

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1783	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.29	0.47	1.15
0.38	0.18	0.32	0.49	1.18
1.00	0.20	0.36	0.55	1.23
3.00	0.21	0.42	0.64	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1000	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.43	0.71	1.82
0.38	0.25	0.48	0.76	1.88
1.00	0.32	0.56	0.84	1.96
3.00	0.47	0.76	1.08	2.23

AO3 AO3 4/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1783	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.30	0.48	1.16
0.38	0.19	0.33	0.50	1.19
1.00	0.21	0.37	0.56	1.24
3.00	0.22	0.43	0.65	1.41

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1000	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.46	0.74	1.85
0.38	0.28	0.51	0.79	1.91
1.00	0.35	0.59	0.87	1.99
3.00	0.51	0.80	1.11	2.26

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1783	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.33	0.50	1.19
0.38	0.21	0.35	0.52	1.21
1.00	0.25	0.40	0.58	1.26
3.00	0.30	0.50	0.71	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1000	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.39	0.62	1.55
0.38	0.24	0.43	0.67	1.60
1.00	0.29	0.50	0.73	1.67
3.00	0.40	0.65	0.92	1.89

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AO3 AO3 5/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1783	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.31	0.49	1.17
0.38	0.19	0.34	0.51	1.20
1.00	0.22	0.38	0.57	1.25
3.00	0.25	0.46	0.68	1.43

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1000	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.44	0.72	1.83
0.38	0.25	0.48	0.76	1.88
1.00	0.30	0.53	0.81	1.93
3.00	0.40	0.67	0.97	2.10

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1783	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.32	0.50	1.19
0.38	0.20	0.35	0.52	1.21
1.00	0.23	0.39	0.58	1.26
3.00	0.26	0.47	0.69	1.44

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1000	0.19

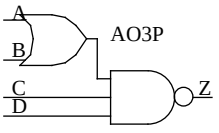
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.47	0.75	1.86
0.38	0.28	0.51	0.79	1.91
1.00	0.33	0.56	0.84	1.96
3.00	0.44	0.71	1.00	2.13

Rev.1.01.10

AO3P	AO3P	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
AO3P	2-INPUT OR into 3-INPUT NAND	4	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT
A	B	C	D	Z
L	H	H	H	L
H	L	H	H	L
H	H	H	H	L
ALL OTHER COMBINATIONS				H

Verilog-HDL DESCRIPTION

```
AO3P  inst(Z,A,B,C,D);
```

VHDL DESCRIPTION

```
inst:AO3P
   port   map(Z,A,B,C,D);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A,B	2.17
C	2.05
D	1.98

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	38.0

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AO3P | AO3P | 2/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0890	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.29	0.44	1.06
0.38	0.18	0.31	0.46	1.09
1.00	0.20	0.34	0.51	1.13
3.00	0.25	0.42	0.62	1.28

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0537	0.21

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.26	0.41	1.01
0.38	0.21	0.34	0.50	1.10
1.00	0.27	0.44	0.62	1.24
3.00	0.40	0.64	0.87	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0890	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.31	0.46	1.08
0.38	0.18	0.31	0.47	1.09
1.00	0.18	0.31	0.47	1.09
3.00	0.14	0.30	0.48	1.12

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0537	0.21

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.29	0.44	1.04
0.38	0.24	0.37	0.52	1.12
1.00	0.32	0.48	0.65	1.26
3.00	0.49	0.70	0.92	1.65

AO3P | AO3P | 3/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0890	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.22	0.31	0.65
0.38	0.17	0.25	0.33	0.68
1.00	0.20	0.28	0.38	0.74
3.00	0.22	0.33	0.45	0.86

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0537	0.21

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.27	0.40	0.89
0.38	0.23	0.33	0.46	0.96
1.00	0.29	0.41	0.55	1.06
3.00	0.44	0.60	0.76	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0890	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.21	0.29	0.64
0.38	0.16	0.23	0.32	0.66
1.00	0.17	0.26	0.36	0.72
3.00	0.16	0.28	0.41	0.84

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0537	0.21

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.31	0.46	1.06
0.38	0.23	0.36	0.51	1.11
1.00	0.29	0.43	0.58	1.19
3.00	0.43	0.60	0.78	1.43

AO3P | AO3P | 4/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0890	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.22	0.31	0.65
0.38	0.17	0.24	0.33	0.67
1.00	0.18	0.27	0.37	0.73
3.00	0.18	0.29	0.42	0.85

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0537	0.21

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.34	0.49	1.10
0.38	0.26	0.39	0.54	1.15
1.00	0.33	0.46	0.62	1.22
3.00	0.48	0.64	0.82	1.46

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0890	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.24	0.33	0.67
0.38	0.19	0.26	0.35	0.70
1.00	0.22	0.31	0.40	0.76
3.00	0.26	0.37	0.49	0.90

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0537	0.21

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.29	0.41	0.91
0.38	0.23	0.33	0.46	0.95
1.00	0.27	0.39	0.52	1.02
3.00	0.37	0.51	0.67	1.21

AO3P | AO3P | 5/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0890	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.22	0.31	0.66
0.38	0.17	0.25	0.34	0.68
1.00	0.19	0.28	0.38	0.74
3.00	0.20	0.31	0.44	0.87

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0537	0.21

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.32	0.47	1.08
0.38	0.24	0.36	0.51	1.12
1.00	0.28	0.41	0.56	1.16
3.00	0.37	0.53	0.70	1.32

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0890	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.23	0.32	0.67
0.38	0.18	0.26	0.35	0.69
1.00	0.20	0.29	0.39	0.75
3.00	0.22	0.33	0.45	0.88

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0537	0.21

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.35	0.50	1.11
0.38	0.27	0.39	0.55	1.15
1.00	0.31	0.44	0.59	1.20
3.00	0.41	0.56	0.73	1.35

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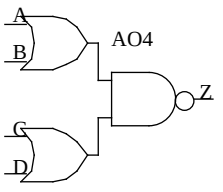
AO4	AO4	1/7

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
AO4	2-WIDE 2-INPUT OR into 2-INPUT NAND	2	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT
A	B	C	D	Z
L	L	L	L	H
L	L	L	H	H
L	L	H	L	H
L	L	H	H	H
L	H	L	L	H
H	L	L	L	H
H	H	L	L	H
ALL OTHER COMBINATIONS				L

Verilog-HDL DESCRIPTION

```
AO4  inst(Z,A,B,C,D);
```

VHDL DESCRIPTION

```
inst:AO4
   port   map(Z,A,B,C,D);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.04
B	1.08
C	1.00
D	0.99

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	20.2

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AO4 AO4 2/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&C&D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1783	0.34

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.44	0.74	1.98
0.38	0.20	0.45	0.76	2.00
1.00	0.25	0.51	0.81	2.04
3.00	0.38	0.68	1.01	2.24

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&C&D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0775	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.24	0.41	1.10
0.38	0.17	0.32	0.50	1.19
1.00	0.22	0.42	0.62	1.33
3.00	0.27	0.58	0.87	1.73

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&C&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1783	0.34

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.46	0.77	2.00
0.38	0.22	0.47	0.78	2.02
1.00	0.27	0.53	0.83	2.06
3.00	0.38	0.68	1.01	2.25

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&C&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0775	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.30	0.51	1.33
0.38	0.21	0.39	0.60	1.42
1.00	0.28	0.50	0.72	1.56
3.00	0.38	0.70	1.00	1.97

Rev.1.01.10

AO4 AO4 3/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&~C&D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1783	0.34

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.44	0.75	1.98
0.38	0.20	0.45	0.76	2.00
1.00	0.25	0.51	0.81	2.04
3.00	0.35	0.66	0.99	2.23

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&~C&D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0775	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.30	0.51	1.38
0.38	0.19	0.38	0.60	1.47
1.00	0.25	0.49	0.73	1.61
3.00	0.34	0.69	1.01	2.02

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&C&D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1783	0.34

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.46	0.77	2.00
0.38	0.20	0.46	0.77	2.01
1.00	0.22	0.47	0.78	2.01
3.00	0.28	0.55	0.86	2.07

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&C&D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0775	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.43	1.12
0.38	0.19	0.34	0.51	1.20
1.00	0.24	0.44	0.64	1.35
3.00	0.33	0.62	0.90	1.75

AO4 AO4 4/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&C&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1783	0.34

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.48	0.79	2.03
0.38	0.23	0.48	0.79	2.03
1.00	0.24	0.49	0.80	2.03
3.00	0.27	0.55	0.86	2.08

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&C&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0775	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.32	0.53	1.35
0.38	0.23	0.41	0.61	1.44
1.00	0.31	0.52	0.74	1.58
3.00	0.44	0.74	1.04	1.99

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&~C&D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1783	0.34

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.46	0.77	2.01
0.38	0.21	0.46	0.77	2.01
1.00	0.21	0.47	0.78	2.01
3.00	0.24	0.52	0.84	2.06

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&~C&D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0775	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.32	0.54	1.40
0.38	0.21	0.40	0.62	1.49
1.00	0.28	0.51	0.75	1.63
3.00	0.41	0.73	1.04	2.05

AO4 AO4 5/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~D&A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1783	0.34

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.57	0.88	2.12
0.38	0.31	0.56	0.88	2.11
1.00	0.34	0.58	0.89	2.11
3.00	0.44	0.69	0.99	2.18

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~D&A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0775	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.26	0.42	1.05
0.38	0.19	0.33	0.49	1.12
1.00	0.24	0.40	0.58	1.22
3.00	0.29	0.53	0.76	1.51

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~D&A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1783	0.34

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.55	0.86	2.09
0.38	0.29	0.54	0.85	2.09
1.00	0.31	0.55	0.86	2.09
3.00	0.40	0.65	0.95	2.15

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~D&A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0775	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.33	0.53	1.36
0.38	0.21	0.38	0.58	1.41
1.00	0.25	0.44	0.65	1.48
3.00	0.29	0.55	0.81	1.69

AO4 AO4 6/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~D&~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1783	0.34

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.57	0.88	2.11
0.38	0.31	0.56	0.87	2.11
1.00	0.33	0.57	0.88	2.11
3.00	0.42	0.67	0.97	2.17

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~D&~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0775	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.35	0.56	1.38
0.38	0.23	0.40	0.61	1.43
1.00	0.28	0.46	0.67	1.50
3.00	0.33	0.58	0.83	1.71

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~C&A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1783	0.34

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.55	0.86	2.10
0.38	0.31	0.56	0.87	2.11
1.00	0.37	0.62	0.92	2.15
3.00	0.56	0.82	1.13	2.35

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~C&A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0775	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.27	0.44	1.11
0.38	0.19	0.33	0.51	1.18
1.00	0.24	0.41	0.60	1.29
3.00	0.28	0.53	0.79	1.58

AO4 AO4 7/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~C&A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1783	0.34

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.53	0.84	2.07
0.38	0.28	0.54	0.85	2.08
1.00	0.34	0.59	0.90	2.12
3.00	0.51	0.79	1.10	2.32

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~C&A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0775	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.33	0.54	1.41
0.38	0.20	0.38	0.60	1.47
1.00	0.24	0.44	0.67	1.54
3.00	0.27	0.55	0.83	1.76

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~C&~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1783	0.34

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.55	0.86	2.10
0.38	0.30	0.56	0.87	2.10
1.00	0.36	0.61	0.92	2.14
3.00	0.54	0.81	1.12	2.33

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~C&~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0775	0.17

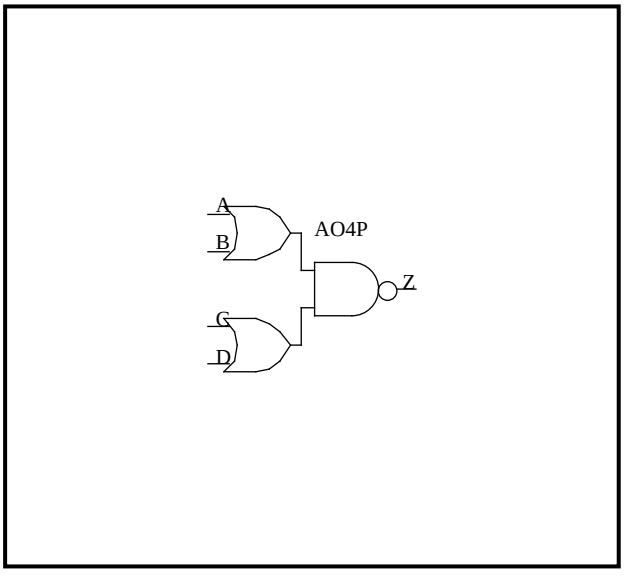
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.35	0.57	1.44
0.38	0.23	0.40	0.62	1.49
1.00	0.27	0.47	0.69	1.57
3.00	0.32	0.58	0.86	1.79

Rev.1.01.10

AO4P	AO4P	1/7

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
AO4P	2-WIDE 2-INPUT OR into 2-INPUT NAND	4	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT
A	B	C	D	Z
L	L	L	L	H
L	L	L	H	H
L	L	H	L	H
L	L	H	H	H
L	H	L	L	H
H	L	L	L	H
H	H	L	L	H
ALL OTHER COMBINATIONS				L

Verilog-HDL DESCRIPTION

```
AO4P  inst(Z,A,B,C,D);
```

VHDL DESCRIPTION

```
inst:AO4P
   port   map(Z,A,B,C,D);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A,B	2.17
C	1.98
D	2.06

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	39.1

Rev.1.01.10

AO4P | AO4P | 2/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&C&D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0890	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.28	0.44	1.06
0.38	0.17	0.30	0.46	1.08
1.00	0.21	0.35	0.51	1.12
3.00	0.32	0.48	0.67	1.31

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&C&D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0420	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.17	0.27	0.66
0.38	0.16	0.25	0.36	0.75
1.00	0.21	0.34	0.47	0.89
3.00	0.26	0.46	0.65	1.22

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&C&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0890	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.30	0.46	1.08
0.38	0.19	0.32	0.48	1.10
1.00	0.23	0.37	0.53	1.14
3.00	0.31	0.48	0.66	1.32

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&C&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0420	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.23	0.35	0.83
0.38	0.21	0.32	0.44	0.91
1.00	0.28	0.41	0.56	1.06
3.00	0.39	0.58	0.78	1.41

Rev.1.01.10

AO4P | AO4P | 3/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&~C&D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0890	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.28	0.44	1.06
0.38	0.17	0.30	0.46	1.08
1.00	0.21	0.35	0.51	1.12
3.00	0.28	0.46	0.64	1.30

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&~C&D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0420	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.21	0.33	0.80
0.38	0.18	0.29	0.41	0.89
1.00	0.23	0.38	0.53	1.03
3.00	0.32	0.53	0.74	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&C&D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0890	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.31	0.46	1.08
0.38	0.17	0.30	0.46	1.09
1.00	0.18	0.31	0.47	1.09
3.00	0.21	0.36	0.53	1.15

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&C&D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0420	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.19	0.29	0.68
0.38	0.18	0.27	0.37	0.77
1.00	0.24	0.36	0.49	0.91
3.00	0.33	0.51	0.69	1.25

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&C&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0890	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.33	0.48	1.10
0.38	0.19	0.33	0.49	1.11
1.00	0.20	0.33	0.49	1.11
3.00	0.20	0.35	0.53	1.16

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&C&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0420	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.25	0.37	0.85
0.38	0.23	0.34	0.46	0.93
1.00	0.31	0.44	0.58	1.08
3.00	0.46	0.64	0.83	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&~C&D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0890	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.31	0.46	1.08
0.38	0.17	0.31	0.46	1.09
1.00	0.18	0.31	0.47	1.09
3.00	0.18	0.33	0.50	1.14

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&~C&D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0420	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.23	0.35	0.83
0.38	0.20	0.31	0.43	0.91
1.00	0.27	0.41	0.55	1.05
3.00	0.40	0.59	0.79	1.41

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~D&A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0890	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.42	0.57	1.19
0.38	0.28	0.41	0.57	1.19
1.00	0.30	0.43	0.58	1.19
3.00	0.39	0.52	0.68	1.28

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~D&A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0420	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.22	0.31	0.67
0.38	0.19	0.27	0.37	0.74
1.00	0.24	0.34	0.44	0.83
3.00	0.30	0.43	0.58	1.06

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~D&A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0890	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.39	0.55	1.17
0.38	0.26	0.39	0.54	1.17
1.00	0.27	0.40	0.55	1.17
3.00	0.34	0.47	0.63	1.24

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~D&A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0420	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.26	0.38	0.86
0.38	0.21	0.31	0.43	0.90
1.00	0.25	0.36	0.48	0.97
3.00	0.29	0.45	0.61	1.15

AO4P | AO4P | 6/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~D&~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0890	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.41	0.57	1.19
0.38	0.28	0.41	0.56	1.19
1.00	0.29	0.42	0.57	1.19
3.00	0.36	0.50	0.65	1.26

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~D&~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0420	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.29	0.41	0.88
0.38	0.23	0.33	0.45	0.93
1.00	0.28	0.38	0.51	0.99
3.00	0.34	0.48	0.64	1.18

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~C&A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0890	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.40	0.55	1.17
0.38	0.28	0.41	0.56	1.18
1.00	0.34	0.47	0.62	1.23
3.00	0.52	0.66	0.82	1.44

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~C&A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0420	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.20	0.29	0.66
0.38	0.18	0.26	0.35	0.72
1.00	0.22	0.32	0.43	0.81
3.00	0.24	0.39	0.55	1.03

AO4P | AO4P | 7/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~C&A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0890	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.37	0.53	1.15
0.38	0.26	0.38	0.54	1.16
1.00	0.31	0.44	0.60	1.20
3.00	0.47	0.62	0.78	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~C&A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0420	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.24	0.36	0.83
0.38	0.19	0.29	0.41	0.89
1.00	0.22	0.34	0.46	0.95
3.00	0.24	0.40	0.57	1.12

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~C&~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0890	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.39	0.55	1.17
0.38	0.28	0.40	0.56	1.18
1.00	0.33	0.46	0.62	1.22
3.00	0.49	0.64	0.80	1.42

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~C&~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0420	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.26	0.38	0.86
0.38	0.21	0.31	0.43	0.91
1.00	0.25	0.36	0.49	0.97
3.00	0.29	0.44	0.60	1.15

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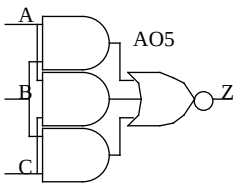
AO5	AO5	1/4

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
AO5	INVERTING 2 of 3 MAJORITY GATE	3	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
A	B	C	Z
L	L	L	H
L	L	H	H
L	H	L	H
H	L	L	H
ALL OTHER COMBINATIONS			L

Verilog-HDL DESCRIPTION

```
AO5  inst(Z,A,B,C);
```

VHDL DESCRIPTION

```
inst:AO5
   port   map(Z,A,B,C);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.98
B	1.97
C	0.99

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	18.0

Rev.1.01.10

AO5 AO5 2/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1896	0.78

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.61	0.91	2.09
0.38	0.37	0.62	0.92	2.10
1.00	0.42	0.67	0.96	2.14
3.00	0.58	0.84	1.15	2.32

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0739	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.35	0.54	1.28
0.38	0.29	0.44	0.63	1.37
1.00	0.37	0.56	0.76	1.51
3.00	0.49	0.76	1.03	1.90

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1896	0.78

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.60	0.91	2.15
0.38	0.36	0.61	0.93	2.18
1.00	0.41	0.66	0.97	2.21
3.00	0.57	0.84	1.16	2.39

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0739	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.33	0.51	1.20
0.38	0.27	0.42	0.59	1.29
1.00	0.35	0.53	0.72	1.43
3.00	0.45	0.71	0.98	1.81

AO5 AO5 3/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1896	0.78

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.73	1.06	2.37
0.38	0.45	0.72	1.05	2.37
1.00	0.50	0.77	1.09	2.41
3.00	0.70	0.97	1.30	2.59

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0739	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.36	0.54	1.28
0.38	0.26	0.42	0.60	1.34
1.00	0.32	0.49	0.69	1.44
3.00	0.37	0.61	0.87	1.70

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1896	0.78

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.60	0.90	2.14
0.38	0.34	0.59	0.90	2.14
1.00	0.34	0.60	0.91	2.14
3.00	0.39	0.65	0.97	2.18

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0739	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.40	0.61	1.44
0.38	0.31	0.49	0.69	1.52
1.00	0.41	0.61	0.83	1.66
3.00	0.58	0.85	1.14	2.08

AO5 AO5 4/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1896	0.78

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.43	0.70	1.02	2.34
0.38	0.42	0.69	1.02	2.33
1.00	0.43	0.69	1.02	2.32
3.00	0.53	0.78	1.10	2.36

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0739	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.34	0.51	1.21
0.38	0.25	0.40	0.57	1.27
1.00	0.31	0.47	0.65	1.36
3.00	0.38	0.60	0.83	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1896	0.78

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.60	0.89	2.07
0.38	0.36	0.60	0.89	2.07
1.00	0.37	0.61	0.90	2.07
3.00	0.45	0.69	0.98	2.12

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0739	0.29

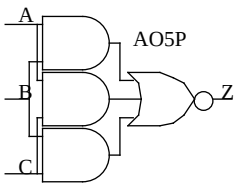
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.40	0.61	1.43
0.38	0.28	0.45	0.66	1.48
1.00	0.33	0.51	0.72	1.55
3.00	0.41	0.64	0.89	1.77

Rev.1.01.10

AO5P	AO5P	1/4

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
AO5P	INVERTING 2 of 3 MAJORITY GATE	5	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
A	B	C	Z
L	L	L	H
L	L	H	H
L	H	L	H
H	L	L	H
ALL OTHER COMBINATIONS			L

Verilog-HDL DESCRIPTION

```
AO5P  inst(Z,A,B,C);
```

VHDL DESCRIPTION

```
inst:AO5P
   port   map(Z,A,B,C);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	4.14
B	3.97
C	2.19

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	30.2

Rev.1.01.10

AO5P | AO5P | 2/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1114	0.85

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.47	0.63	1.25
0.38	0.34	0.47	0.63	1.26
1.00	0.39	0.52	0.68	1.30
3.00	0.55	0.69	0.86	1.49

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0432	0.33

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.24	0.34	0.70
0.38	0.25	0.33	0.42	0.79
1.00	0.33	0.43	0.54	0.92
3.00	0.42	0.57	0.73	1.24

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1114	0.85

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.43	0.59	1.21
0.38	0.31	0.44	0.60	1.23
1.00	0.36	0.49	0.65	1.27
3.00	0.50	0.65	0.82	1.46

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0432	0.33

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.24	0.34	0.70
0.38	0.25	0.33	0.42	0.78
1.00	0.32	0.43	0.54	0.92
3.00	0.41	0.57	0.73	1.24

Rev.1.01.10

AO5P | AO5P | 3/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1114	0.85

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.47	0.62	0.82	1.58
0.38	0.45	0.61	0.80	1.57
1.00	0.50	0.66	0.85	1.61
3.00	0.72	0.88	1.07	1.82

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0432	0.33

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.24	0.33	0.69
0.38	0.23	0.30	0.39	0.76
1.00	0.27	0.37	0.47	0.84
3.00	0.29	0.43	0.58	1.06

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1114	0.85

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.42	0.58	1.19
0.38	0.29	0.41	0.57	1.20
1.00	0.29	0.42	0.58	1.20
3.00	0.30	0.44	0.61	1.24

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0432	0.33

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.33	0.46	0.94
0.38	0.32	0.42	0.54	1.03
1.00	0.41	0.53	0.67	1.17
3.00	0.59	0.76	0.94	1.54

Rev.1.01.10

AO5P | AO5P | 4/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1114	0.85

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.44	0.60	0.79	1.55
0.38	0.43	0.58	0.78	1.54
1.00	0.43	0.58	0.77	1.53
3.00	0.53	0.68	0.86	1.58

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0432	0.33

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.25	0.34	0.71
0.38	0.23	0.31	0.40	0.77
1.00	0.29	0.38	0.48	0.85
3.00	0.35	0.47	0.61	1.07

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1114	0.85

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.46	0.62	1.24
0.38	0.33	0.46	0.62	1.24
1.00	0.34	0.47	0.62	1.24
3.00	0.41	0.54	0.70	1.30

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&B	FALL

SLEW FACTOR

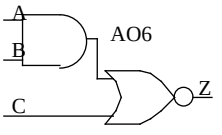
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0432	0.33

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.34	0.46	0.94
0.38	0.28	0.38	0.50	0.99
1.00	0.33	0.43	0.56	1.05
3.00	0.40	0.54	0.69	1.23

AO6	AO6	1/4

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
AO6	2-INPUT AND into 2-INPUT NOR	2	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
A	B	C	Z
L	L	L	H
L	H	L	H
H	L	L	H
ALL OTHER COMBINATIONS			L

Verilog-HDL DESCRIPTION

```
AO6  inst(Z,A,B,C);
```

VHDL DESCRIPTION

```
inst:AO6
   port   map(Z,A,B,C);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.07
B	1.03
C	0.99

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	20.1

Rev.1.01.10

AO6 AO6 2/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1953	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.53	0.87	2.22
0.38	0.27	0.54	0.88	2.24
1.00	0.34	0.61	0.94	2.28
3.00	0.53	0.82	1.16	2.48

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.27	0.46	1.20
0.38	0.17	0.33	0.52	1.26
1.00	0.21	0.40	0.60	1.35
3.00	0.22	0.50	0.76	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1953	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.48	0.82	2.17
0.38	0.23	0.50	0.84	2.19
1.00	0.28	0.56	0.89	2.24
3.00	0.43	0.75	1.10	2.43

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.26	0.44	1.18
0.38	0.18	0.34	0.53	1.27
1.00	0.23	0.44	0.65	1.41
3.00	0.27	0.59	0.89	1.79

AO6 AO6 3/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1953	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.52	0.86	2.22
0.38	0.24	0.52	0.86	2.22
1.00	0.26	0.53	0.86	2.20
3.00	0.37	0.64	0.97	2.26

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.08	0.18	0.29	0.74
0.38	0.14	0.25	0.37	0.83
1.00	0.19	0.34	0.49	0.97
3.00	0.21	0.45	0.67	1.32

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1953	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.57	0.91	2.27
0.38	0.29	0.57	0.91	2.27
1.00	0.31	0.58	0.91	2.26
3.00	0.42	0.69	1.01	2.31

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.19	0.30	0.76
0.38	0.16	0.27	0.39	0.84
1.00	0.21	0.35	0.50	0.98
3.00	0.24	0.47	0.69	1.33

AO6 AO6 4/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1953	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.42	0.67	1.70
0.38	0.21	0.42	0.68	1.71
1.00	0.24	0.44	0.70	1.72
3.00	0.33	0.56	0.82	1.83

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&~B	FALL

SLEW FACTOR

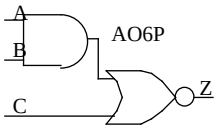
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.18	0.30	0.75
0.38	0.16	0.26	0.38	0.84
1.00	0.21	0.35	0.50	0.98
3.00	0.25	0.48	0.70	1.33

AO6P	AO6P	1/4

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
AO6P	2-INPUT AND into 2-INPUT NOR	3	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
A	B	C	Z
L	L	L	H
L	H	L	H
H	L	L	H
ALL OTHER COMBINATIONS			L

Verilog-HDL DESCRIPTION

```
AO6P  inst(Z,A,B,C);
```

VHDL DESCRIPTION

```
inst:AO6P
   port   map(Z,A,B,C);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	2.11
B	2.03
C	1.96

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	39.3

Rev.1.01.10

AO6P | AO6P | 2/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1001	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.37	0.54	1.24
0.38	0.24	0.38	0.55	1.25
1.00	0.31	0.45	0.62	1.30
3.00	0.50	0.66	0.84	1.52

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0318	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.18	0.27	0.64
0.38	0.15	0.23	0.33	0.70
1.00	0.18	0.29	0.40	0.79
3.00	0.17	0.33	0.50	0.99

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1001	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.32	0.49	1.19
0.38	0.19	0.33	0.51	1.21
1.00	0.25	0.39	0.57	1.25
3.00	0.40	0.57	0.77	1.47

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0318	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.16	0.26	0.63
0.38	0.15	0.24	0.34	0.71
1.00	0.19	0.31	0.44	0.84
3.00	0.21	0.40	0.59	1.14

Rev.1.01.10

AO6P | AO6P | 3/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1001	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.37	0.54	1.24
0.38	0.21	0.36	0.54	1.24
1.00	0.23	0.37	0.54	1.23
3.00	0.31	0.46	0.63	1.30

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0318	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.15	0.22	0.50
0.38	0.15	0.22	0.30	0.58
1.00	0.19	0.29	0.39	0.71
3.00	0.23	0.38	0.54	0.99

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1001	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.42	0.60	1.29
0.38	0.27	0.41	0.59	1.29
1.00	0.28	0.42	0.59	1.28
3.00	0.37	0.51	0.69	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0318	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.16	0.23	0.51
0.38	0.17	0.24	0.31	0.60
1.00	0.22	0.31	0.41	0.73
3.00	0.27	0.41	0.56	1.01

Rev.1.01.10

AO6P | AO6P | 4/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1001	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.30	0.44	0.97
0.38	0.19	0.30	0.44	0.97
1.00	0.21	0.32	0.46	0.99
3.00	0.29	0.41	0.56	1.10

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0318	0.14

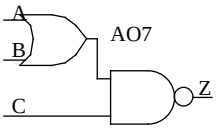
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.15	0.23	0.50
0.38	0.17	0.23	0.31	0.59
1.00	0.22	0.31	0.41	0.72
3.00	0.28	0.42	0.57	1.01

Rev.1.01.10

AO7	AO7	1/4

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
AO7	2-INPUT OR into 2-INPUT NAND	2	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
A	B	C	Z
L	H	H	L
H	L	H	L
H	H	H	L
ALL OTHER COMBINATIONS			H

Verilog-HDL DESCRIPTION

```
AO7  inst(Z,A,B,C);
```

VHDL DESCRIPTION

```
inst:AO7
   port   map(Z,A,B,C);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.08
B	1.03
C	0.99

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	21.6

Rev.1.01.10

AO7	AO7	2/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1783	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.46	0.77	2.01
0.38	0.21	0.46	0.77	2.01
1.00	0.22	0.47	0.78	2.01
3.00	0.25	0.53	0.84	2.06

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0726	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.30	0.50	1.32
0.38	0.21	0.38	0.59	1.40
1.00	0.27	0.49	0.72	1.55
3.00	0.39	0.70	1.00	1.96

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1783	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.44	0.75	1.98
0.38	0.20	0.45	0.76	2.00
1.00	0.25	0.51	0.82	2.04
3.00	0.36	0.66	0.99	2.23

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0726	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.28	0.48	1.30
0.38	0.19	0.36	0.57	1.39
1.00	0.24	0.47	0.70	1.53
3.00	0.32	0.66	0.97	1.94

AO7 AO7 3/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1783	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.28	0.44	1.08
0.38	0.18	0.31	0.47	1.11
1.00	0.22	0.36	0.53	1.17
3.00	0.30	0.47	0.67	1.36

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0726	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.25	0.40	1.02
0.38	0.18	0.31	0.47	1.09
1.00	0.23	0.39	0.56	1.19
3.00	0.30	0.53	0.75	1.48

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1783	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.28	0.44	1.08
0.38	0.17	0.31	0.47	1.11
1.00	0.20	0.35	0.52	1.16
3.00	0.26	0.45	0.65	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0726	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.33	0.53	1.35
0.38	0.21	0.37	0.58	1.40
1.00	0.26	0.44	0.65	1.47
3.00	0.34	0.58	0.82	1.69

AO7 AO7 4/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1783	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.28	0.44	1.08
0.38	0.17	0.31	0.47	1.11
1.00	0.20	0.35	0.52	1.16
3.00	0.26	0.45	0.65	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&B	FALL

SLEW FACTOR

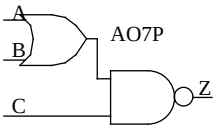
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0726	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.33	0.53	1.35
0.38	0.21	0.37	0.58	1.40
1.00	0.26	0.44	0.65	1.47
3.00	0.34	0.58	0.82	1.69

AO7P	AO7P	1/4

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
AO7P	2-INPUT OR into 2-INPUT NAND	3	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
A	B	C	Z
L	H	H	L
H	L	H	L
H	H	H	L
ALL OTHER COMBINATIONS			H

Verilog-HDL DESCRIPTION

```
AO7P  inst(Z,A,B,C);
```

VHDL DESCRIPTION

```
inst:AO7P
   port   map(Z,A,B,C);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	2.11
B	2.03
C	1.96

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	42.7

Rev.1.01.10

AO7P | AO7P | 2/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0890	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.30	0.46	1.08
0.38	0.17	0.30	0.46	1.08
1.00	0.18	0.31	0.47	1.09
3.00	0.20	0.35	0.52	1.14

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0376	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.21	0.31	0.74
0.38	0.19	0.28	0.40	0.83
1.00	0.25	0.37	0.51	0.97
3.00	0.35	0.54	0.73	1.31

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0890	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.28	0.44	1.05
0.38	0.17	0.30	0.45	1.07
1.00	0.21	0.35	0.51	1.12
3.00	0.30	0.47	0.66	1.30

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0376	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.18	0.29	0.72
0.38	0.17	0.26	0.38	0.81
1.00	0.21	0.35	0.49	0.95
3.00	0.28	0.48	0.68	1.28

AO7P | AO7P | 3/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0890	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.25	0.34	0.74
0.38	0.19	0.27	0.37	0.76
1.00	0.23	0.32	0.42	0.82
3.00	0.33	0.44	0.56	0.99

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0376	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.18	0.26	0.60
0.38	0.17	0.24	0.33	0.66
1.00	0.21	0.31	0.41	0.76
3.00	0.27	0.41	0.55	1.00

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0890	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.24	0.34	0.73
0.38	0.18	0.27	0.36	0.76
1.00	0.22	0.31	0.42	0.81
3.00	0.30	0.41	0.54	0.98

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0376	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.24	0.34	0.77
0.38	0.20	0.28	0.39	0.83
1.00	0.24	0.34	0.46	0.90
3.00	0.31	0.45	0.60	1.10

Rev.1.01.10

AO7P | AO7P | 4/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0890	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.23	0.33	0.72
0.38	0.17	0.25	0.35	0.74
1.00	0.21	0.30	0.40	0.80
3.00	0.29	0.40	0.53	0.96

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0376	0.18

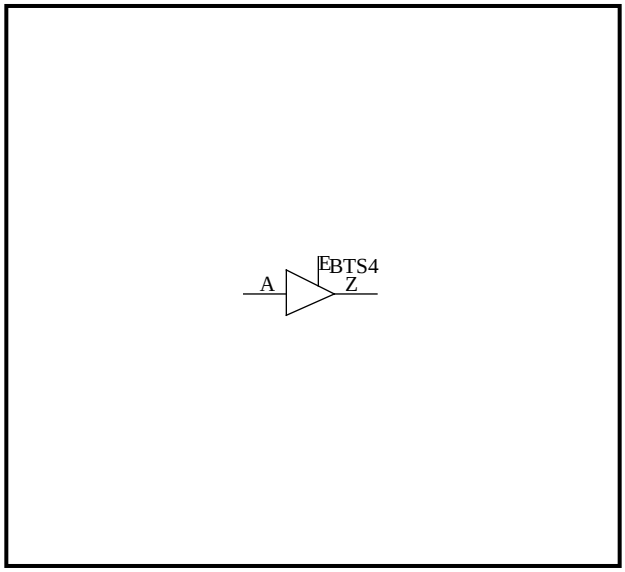
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.21	0.32	0.75
0.38	0.17	0.26	0.37	0.80
1.00	0.21	0.32	0.44	0.87
3.00	0.27	0.41	0.57	1.07

Rev.1.01.10

BTS4	BTS4	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BTS4	TRI-STATE INTERNAL BUFFER (HIGH ENABLE)	3	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
E	A	Z
H	L	L
H	H	H
L	X	HZ

Verilog-HDL DESCRIPTION

```
BTS4  inst(Z,A,E);
```

VHDL DESCRIPTION

```
inst:BTS4
   port   map(Z,A,E);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT CAPACITANCE (LU)

PIN NAME	Z
Cin	0.79

INPUT LOAD (LU)

PIN NAME	TYPICAL
A	2.17
E	2.04

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	45.2

Rev.1.01.11

BTS4 BTS4 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0944	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.79	5.79	10.79	30.79
0.01	0.17	0.31	0.47	1.13
0.38	0.21	0.35	0.52	1.17
1.00	0.25	0.40	0.56	1.23
3.00	0.32	0.48	0.66	1.33

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0399	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.79	5.79	10.79	30.79
0.01	0.23	0.34	0.47	0.94
0.38	0.23	0.34	0.46	0.93
1.00	0.27	0.38	0.51	0.98
3.00	0.38	0.51	0.65	1.13

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	1-Z

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0399	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.79	5.79	10.79	30.79
0.01	0.12	0.12	0.12	0.12
0.38	0.16	0.16	0.16	0.16
1.00	0.21	0.21	0.21	0.21
3.00	0.31	0.31	0.31	0.31

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	0-Z

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0944	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.79	5.79	10.79	30.79
0.01	0.19	0.19	0.19	0.19
0.38	0.22	0.22	0.22	0.22
1.00	0.27	0.27	0.27	0.27
3.00	0.40	0.40	0.40	0.40

BTS4 BTS4 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	Z-1

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0944	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.79	5.79	10.79	30.79
0.01	0.14	0.28	0.44	1.10
0.38	0.20	0.34	0.50	1.16
1.00	0.26	0.40	0.57	1.22
3.00	0.37	0.53	0.71	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	Z-0

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0399	0.08

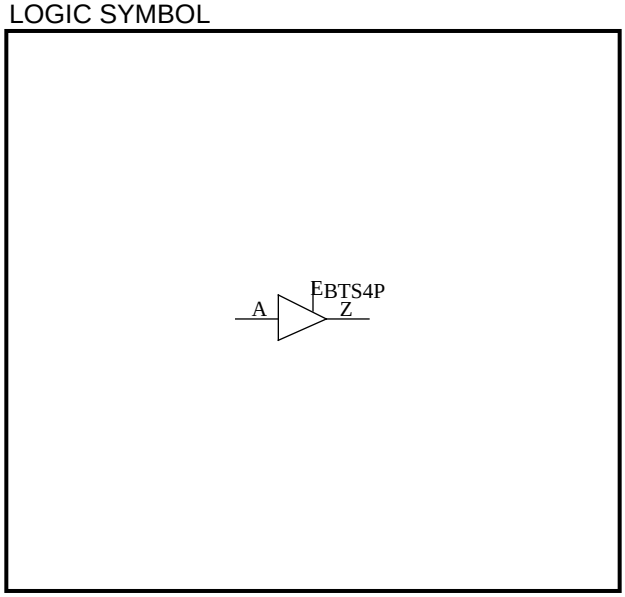
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.79	5.79	10.79	30.79
0.01	0.26	0.37	0.50	0.97
0.38	0.31	0.43	0.55	1.02
1.00	0.37	0.48	0.61	1.08
3.00	0.46	0.57	0.70	1.17

Rev.1.01.11

BTS4P	BTS4P	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BTS4P	TRI-STATE INTERNAL BUFFER (HIGH ENABLE)	4	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
E	A	Z
H	L	L
H	H	H
L	X	HZ

Verilog-HDL DESCRIPTION

```
BTS4P  inst(Z,A,E);
```

VHDL DESCRIPTION

```
inst:BTS4P
   port   map(Z,A,E);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT CAPACITANCE (LU)

PIN NAME	Z
Cin	0.79

INPUT LOAD (LU)

PIN NAME	TYPICAL
A	2.14
E	2.05

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	85.4

Rev.1.01.11

BTS4P | BTS4P | 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0462	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.79	5.79	10.79	30.79
0.01	0.16	0.24	0.33	0.65
0.38	0.22	0.29	0.38	0.70
1.00	0.27	0.35	0.43	0.76
3.00	0.37	0.45	0.55	0.89

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0244	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.79	5.79	10.79	30.79
0.01	0.24	0.32	0.40	0.70
0.38	0.24	0.32	0.40	0.69
1.00	0.28	0.36	0.44	0.74
3.00	0.39	0.48	0.57	0.87

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	1-Z

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0244	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.79	5.79	10.79	30.79
0.01	0.16	0.16	0.16	0.16
0.38	0.19	0.19	0.19	0.19
1.00	0.25	0.25	0.25	0.25
3.00	0.37	0.37	0.37	0.37

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	0-Z

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0462	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.79	5.79	10.79	30.79
0.01	0.21	0.21	0.21	0.21
0.38	0.24	0.24	0.24	0.24
1.00	0.29	0.29	0.29	0.29
3.00	0.41	0.41	0.41	0.41

Rev.1.01.11

BTS4P | BTS4P | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	Z-1

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0462	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.79	5.79	10.79	30.79
0.01	0.14	0.22	0.30	0.63
0.38	0.20	0.28	0.37	0.69
1.00	0.27	0.35	0.44	0.77
3.00	0.39	0.49	0.59	0.93

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	Z-0

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0244	0.10

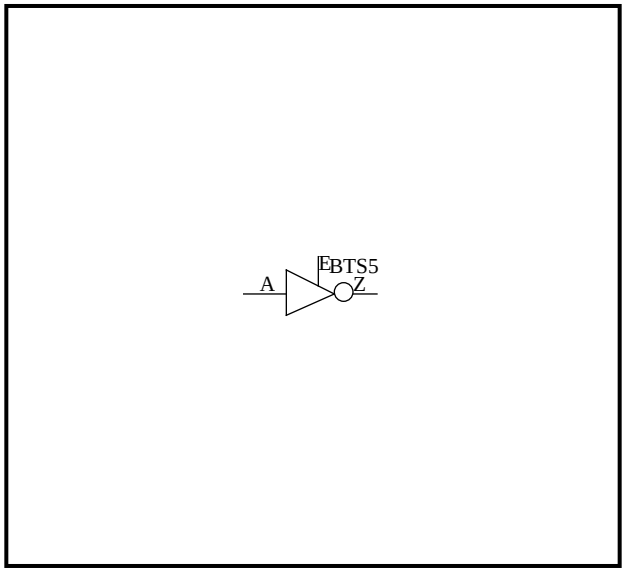
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.79	5.79	10.79	30.79
0.01	0.27	0.34	0.43	0.72
0.38	0.32	0.40	0.48	0.78
1.00	0.37	0.45	0.53	0.83
3.00	0.45	0.53	0.62	0.91

Rev.1.01.11

BTS5	BTS5	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BTS5	TRI-STATE INTERNAL INVERTING BUFFER (HIGH ENABLE)	3	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
E	A	Z
H	L	H
H	H	L
L	X	HZ

Verilog-HDL DESCRIPTION

```
BTS5  inst(Z,A,E);
```

VHDL DESCRIPTION

```
inst:BTS5
   port   map(Z,A,E);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT CAPACITANCE (LU)

PIN NAME	Z
Cin	0.79

INPUT LOAD (LU)

PIN NAME	TYPICAL
A	0.99
E	1.48

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	39.0

Rev.1.01.11

BTS5 BTS5 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0901	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.79	5.79	10.79	30.79
0.01	0.31	0.45	0.60	1.21
0.38	0.34	0.48	0.63	1.25
1.00	0.41	0.54	0.70	1.31
3.00	0.54	0.68	0.83	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0662	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.79	5.79	10.79	30.79
0.01	0.26	0.41	0.60	1.34
0.38	0.33	0.49	0.67	1.41
1.00	0.40	0.55	0.74	1.48
3.00	0.52	0.67	0.86	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	1-Z

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0662	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.79	5.79	10.79	30.79
0.01	0.12	0.12	0.12	0.12
0.38	0.16	0.16	0.16	0.16
1.00	0.21	0.21	0.21	0.21
3.00	0.31	0.31	0.31	0.31

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	0-Z

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0901	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.79	5.79	10.79	30.79
0.01	0.00	0.00	0.00	0.00
0.38	0.05	0.05	0.05	0.05
1.00	0.14	0.14	0.14	0.14
3.00	0.41	0.41	0.41	0.41

BTS5 BTS5 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	Z-1

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0901	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.79	5.79	10.79	30.79
0.01	0.14	0.27	0.43	1.04
0.38	0.21	0.34	0.49	1.10
1.00	0.26	0.40	0.56	1.17
3.00	0.38	0.54	0.70	1.33

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	Z-0

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0662	0.08

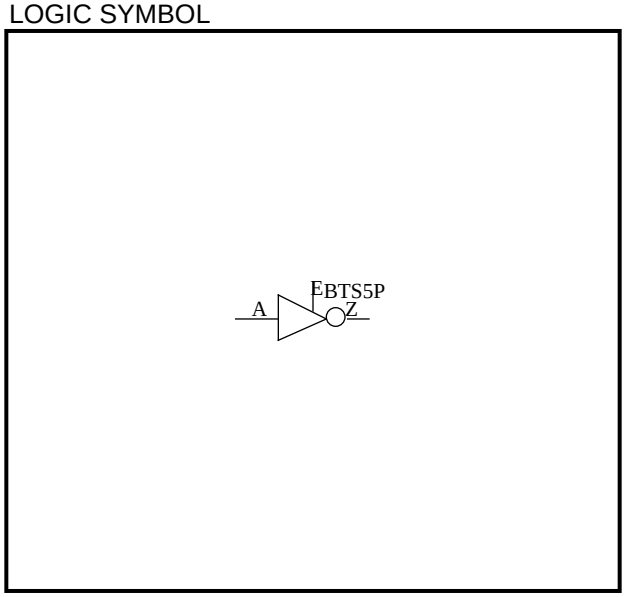
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.79	5.79	10.79	30.79
0.01	0.10	0.25	0.44	1.18
0.38	0.14	0.30	0.49	1.23
1.00	0.14	0.35	0.56	1.32
3.00	0.01	0.35	0.65	1.54

Rev.1.01.11

BTS5P	BTS5P	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BTS5P	TRI-STATE INTERNAL INVERTING BUFFER (HIGH ENABLE)	4	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
E	A	Z
H	L	H
H	H	L
L	X	HZ

Verilog-HDL DESCRIPTION

```
BTS5P  inst(Z,A,E);
```

VHDL DESCRIPTION

```
inst:BTS5P
   port   map(Z,A,E);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT CAPACITANCE (LU)

PIN NAME	Z
Cin	0.79

INPUT LOAD (LU)

PIN NAME	TYPICAL
A	0.99
E	1.95

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	67.8

Rev.1.01.11

BTS5P | BTS5P | 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0451	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.79	5.79	10.79	30.79
0.01	0.29	0.37	0.46	0.77
0.38	0.33	0.41	0.49	0.81
1.00	0.39	0.47	0.55	0.87
3.00	0.52	0.60	0.69	1.00

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0448	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.79	5.79	10.79	30.79
0.01	0.26	0.37	0.50	0.99
0.38	0.34	0.44	0.57	1.07
1.00	0.40	0.51	0.64	1.14
3.00	0.52	0.63	0.76	1.26

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	1-Z

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0448	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.79	5.79	10.79	30.79
0.01	0.16	0.16	0.16	0.16
0.38	0.19	0.19	0.19	0.19
1.00	0.25	0.25	0.25	0.25
3.00	0.37	0.37	0.37	0.37

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	0-Z

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0451	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.79	5.79	10.79	30.79
0.01	0.00	0.00	0.00	0.00
0.38	0.05	0.05	0.05	0.05
1.00	0.14	0.14	0.14	0.14
3.00	0.41	0.41	0.41	0.41

Rev.1.01.11

BTS5P | BTS5P | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	Z-1

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0451	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.79	5.79	10.79	30.79
0.01	0.13	0.20	0.28	0.60
0.38	0.19	0.27	0.35	0.67
1.00	0.25	0.34	0.42	0.74
3.00	0.37	0.48	0.57	0.91

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	Z-0

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0448	0.09

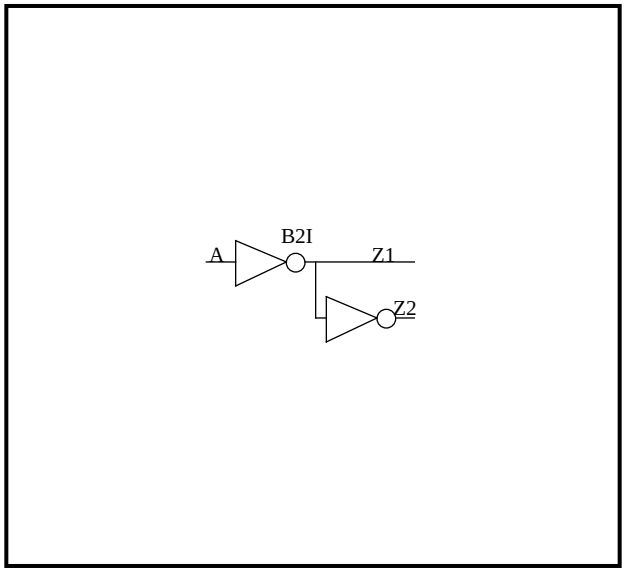
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.79	5.79	10.79	30.79
0.01	0.08	0.19	0.32	0.82
0.38	0.11	0.22	0.35	0.85
1.00	0.09	0.24	0.39	0.90
3.00	-0.08	0.15	0.36	1.01

Rev.1.01.11

B2I	B2I	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
B2I	INVERTER into 3 PARALLEL INVERTERS	2	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT	
A	Z1	Z2
L	H	L
H	L	H

Verilog-HDL DESCRIPTION

```
B2I  inst(Z1,Z2,A);
```

VHDL DESCRIPTION

```
inst:B2I
   port   map(Z1,Z2,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z1	Z2
ELECTRO MIGRATION DRIVE	6880.0	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.00

OUTPUT DRIVE (LU)

PIN NAME	Z1	Z2
DRIVE	36.9	95.5

Rev.1.01.10

B2I | B2I | 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0976	0.47

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.34	0.51	1.17
0.38	0.23	0.37	0.53	1.20
1.00	0.28	0.42	0.60	1.26
3.00	0.39	0.57	0.76	1.47

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0397	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.24	0.35	0.81
0.38	0.21	0.32	0.44	0.90
1.00	0.30	0.43	0.56	1.04
3.00	0.43	0.62	0.81	1.42

PATH CONDITION

PATH	CONDITION	FUNCTION
Z1->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0341	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.05	0.10	0.16	0.38
0.38	0.07	0.12	0.18	0.41
1.00	0.08	0.14	0.22	0.46
3.00	0.09	0.18	0.27	0.57

PATH CONDITION

PATH	CONDITION	FUNCTION
Z1->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0151	0.10

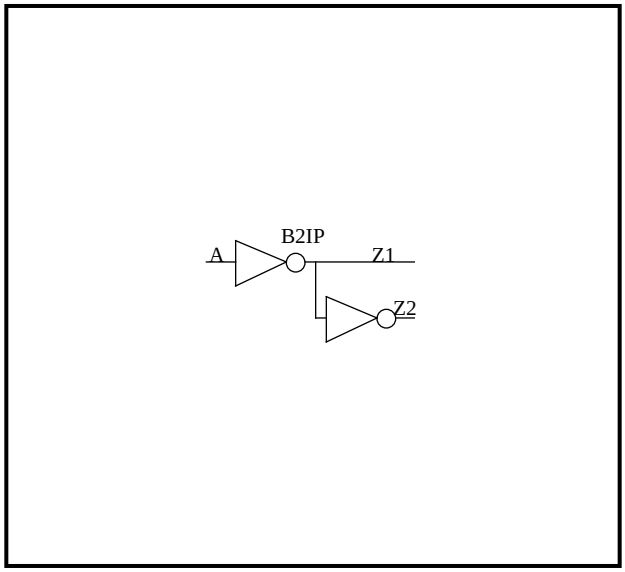
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.04	0.08	0.12	0.31
0.38	0.09	0.14	0.20	0.40
1.00	0.12	0.20	0.28	0.52
3.00	0.16	0.29	0.41	0.76

Rev.1.01.10

B2IP	B2IP	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
B2IP	INVERTER into 3 PARALLEL INVERTERS	4	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT	
A	Z1	Z2
L	H	L
H	L	H

Verilog-HDL DESCRIPTION

```
B2IP  inst(Z1,Z2,A);
```

VHDL DESCRIPTION

```
inst:B2IP
   port   map(Z1,Z2,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z1	Z2
ELECTRO MIGRATION DRIVE	6880.0	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	2.15

OUTPUT DRIVE (LU)

PIN NAME	Z1	Z2
DRIVE	75.0	169.6

Rev.1.01.10

B2IP B2IP 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0450	0.42

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.22	0.30	0.61
0.38	0.19	0.25	0.33	0.64
1.00	0.23	0.30	0.38	0.70
3.00	0.31	0.40	0.50	0.86

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0230	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.20	0.27	0.54
0.38	0.22	0.28	0.35	0.62
1.00	0.29	0.37	0.45	0.75
3.00	0.41	0.52	0.64	1.03

PATH CONDITION

PATH	CONDITION	FUNCTION
Z1->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0169	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.04	0.07	0.10	0.23
0.38	0.06	0.09	0.12	0.25
1.00	0.08	0.12	0.16	0.30
3.00	0.12	0.17	0.23	0.40

PATH CONDITION

PATH	CONDITION	FUNCTION
Z1->Z2	---	FALL

SLEW FACTOR

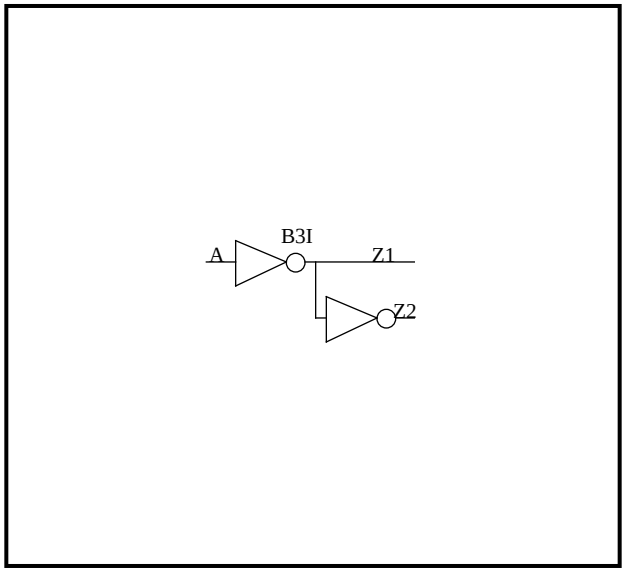
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0072	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.03	0.05	0.07	0.16
0.38	0.06	0.10	0.13	0.24
1.00	0.07	0.12	0.17	0.31
3.00	0.07	0.14	0.22	0.44

B3I	B3I	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
B3I	2 PARALLEL INVERTERS into 2 PARALLEL INVERTERS	2	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT	
A	Z1	Z2
L	H	L
H	L	H

Verilog-HDL DESCRIPTION

```
B3I  inst(Z1,Z2,A);
```

VHDL DESCRIPTION

```
inst:B3I
   port   map(Z1,Z2,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z1,Z2
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	2.06

OUTPUT DRIVE (LU)

PIN NAME	Z1	Z2
DRIVE	77.4	68.5

Rev.1.01.10

B3I | B3I | 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0444	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.15	0.23	0.54
0.38	0.11	0.18	0.26	0.57
1.00	0.14	0.22	0.31	0.63
3.00	0.19	0.30	0.41	0.78

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0231	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.07	0.13	0.20	0.47
0.38	0.13	0.20	0.27	0.55
1.00	0.17	0.27	0.36	0.68
3.00	0.25	0.38	0.52	0.94

PATH CONDITION

PATH	CONDITION	FUNCTION
Z1->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0541	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.06	0.13	0.23	0.59
0.38	0.08	0.16	0.25	0.62
1.00	0.10	0.20	0.30	0.68
3.00	0.15	0.28	0.40	0.83

PATH CONDITION

PATH	CONDITION	FUNCTION
Z1->Z2	---	FALL

SLEW FACTOR

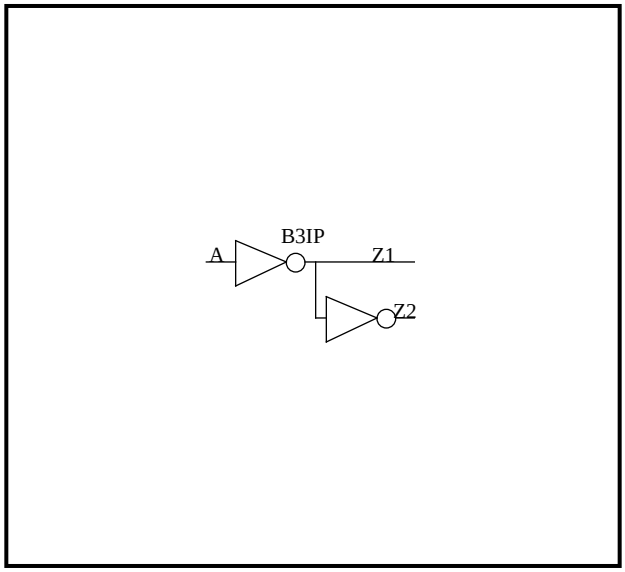
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0225	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.04	0.09	0.16	0.43
0.38	0.08	0.16	0.24	0.52
1.00	0.10	0.21	0.31	0.64
3.00	0.11	0.28	0.43	0.88

B3IP	B3IP	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
B3IP	2 PARALLEL INVERTERS into 2 PARALLEL INVERTERS	4	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT	
A	Z1	Z2
L	H	L
H	L	H

Verilog-HDL DESCRIPTION

```
B3IP  inst(Z1,Z2,A);
```

VHDL DESCRIPTION

```
inst:B3IP
  port  map(Z1,Z2,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z1,Z2
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	4.12

OUTPUT DRIVE (LU)

PIN NAME	Z1	Z2
DRIVE	142.6	122.6

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B3IP B3IP 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0213	0.21

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.08	0.11	0.15	0.31
0.38	0.10	0.14	0.18	0.34
1.00	0.13	0.17	0.22	0.39
3.00	0.18	0.23	0.30	0.51

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0113	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.06	0.09	0.13	0.27
0.38	0.12	0.16	0.20	0.35
1.00	0.16	0.21	0.27	0.45
3.00	0.23	0.30	0.38	0.64

PATH CONDITION

PATH	CONDITION	FUNCTION
Z1->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0262	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.05	0.09	0.13	0.32
0.38	0.06	0.11	0.16	0.34
1.00	0.08	0.14	0.20	0.40
3.00	0.13	0.20	0.28	0.52

PATH CONDITION

PATH	CONDITION	FUNCTION
Z1->Z2	---	FALL

SLEW FACTOR

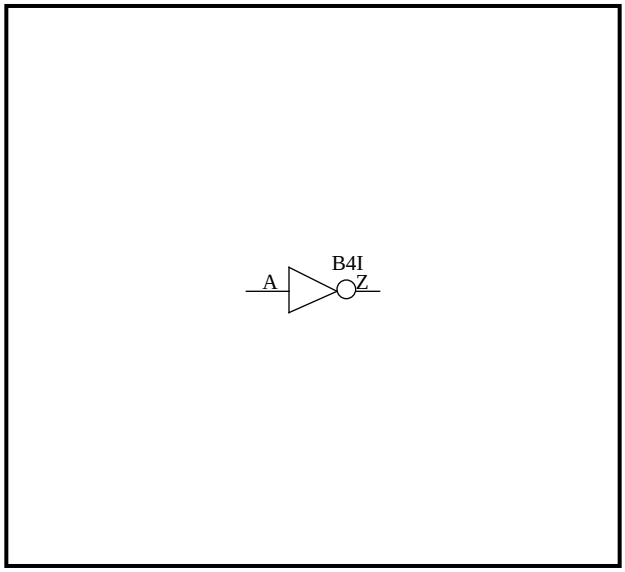
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0108	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.03	0.06	0.09	0.23
0.38	0.07	0.11	0.16	0.31
1.00	0.08	0.15	0.21	0.40
3.00	0.08	0.18	0.28	0.57

B4I	B4I	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
B4I	4 PARALLEL INVERTERS	2	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	H
H	L

Verilog-HDL DESCRIPTION

```
B4I  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:B4I
  port  map(Z,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	4.03

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	132.2

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B4I B4I 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0211	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.04	0.08	0.12	0.27
0.38	0.06	0.10	0.14	0.30
1.00	0.07	0.12	0.17	0.35
3.00	0.10	0.17	0.24	0.46

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

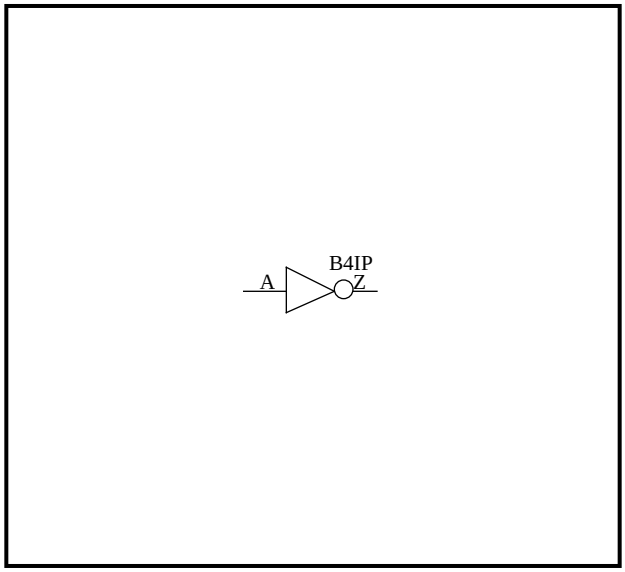
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0109	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.03	0.06	0.10	0.23
0.38	0.07	0.11	0.16	0.31
1.00	0.09	0.15	0.22	0.41
3.00	0.11	0.20	0.30	0.58

B4IP	B4IP	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
B4IP	4 PARALLEL INVERTERS	4	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	H
H	L

Verilog-HDL DESCRIPTION

```
B4IP  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:B4IP
  port  map(Z,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	8.05

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	219.1

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B4IP B4IP 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0100	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.03	0.05	0.08	0.15
0.38	0.05	0.07	0.10	0.18
1.00	0.06	0.09	0.12	0.22
3.00	0.09	0.13	0.17	0.30

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0056	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.03	0.04	0.06	0.13
0.38	0.06	0.09	0.11	0.20
1.00	0.08	0.11	0.15	0.27
3.00	0.09	0.15	0.20	0.38

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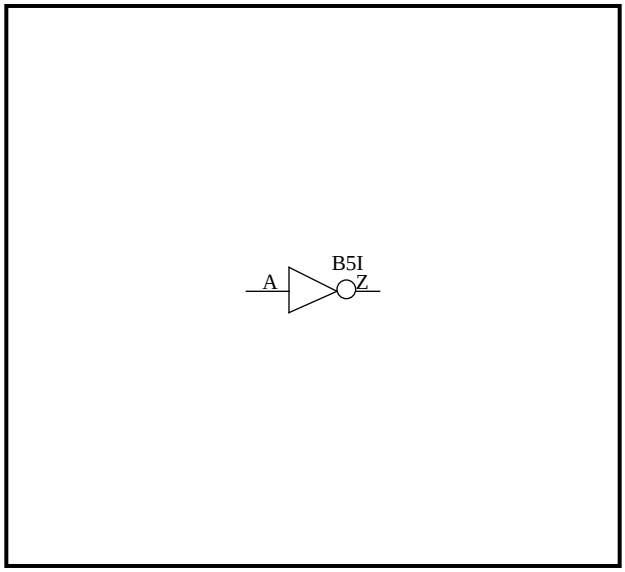
B5I	B5I	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
B5I	3 PARALLEL INVERTERS	2	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	H
H	L

Verilog-HDL DESCRIPTION

```
B5I  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:B5I
  port  map(Z,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	3.03

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	109.3

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B5I | B5I | 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0282	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.05	0.09	0.14	0.35
0.38	0.07	0.11	0.17	0.38
1.00	0.09	0.15	0.21	0.43
3.00	0.12	0.21	0.29	0.57

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0136	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.04	0.07	0.11	0.28
0.38	0.08	0.13	0.19	0.37
1.00	0.10	0.18	0.25	0.48
3.00	0.12	0.24	0.35	0.68

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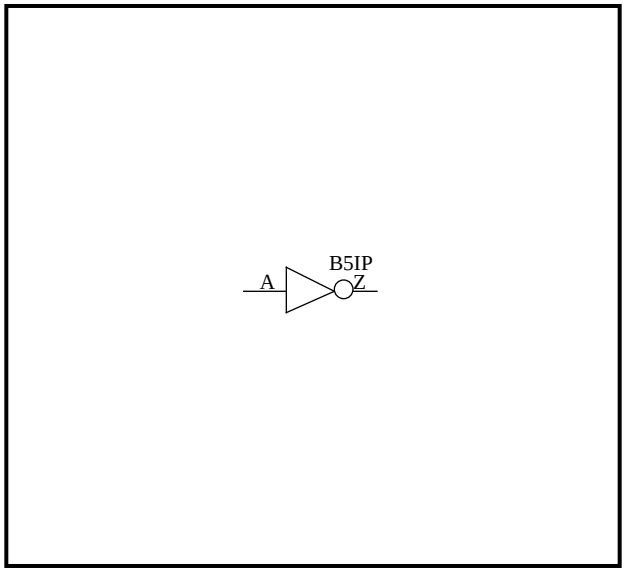
B5IP	B5IP	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
B5IP	3 PARALLEL INVERTERS	3	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	H
H	L

Verilog-HDL DESCRIPTION

```
B5IP  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:B5IP
  port  map(Z,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	6.04

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	178.8

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B5IP B5IP 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0136	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.04	0.06	0.09	0.19
0.38	0.05	0.08	0.11	0.22
1.00	0.07	0.10	0.14	0.27
3.00	0.09	0.14	0.19	0.36

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0073	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.03	0.05	0.07	0.16
0.38	0.06	0.10	0.13	0.24
1.00	0.08	0.13	0.17	0.32
3.00	0.10	0.17	0.24	0.45

Rev.1.01.10

D24GL	D24GL	1/7

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
D24GL	2 TO 4 DECODER (GATED OUTPUTS ACTIVE LOW)	7	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL

TRUTH TABLE

INPUT			OUTPUT			
G	A	B	Z0	Z1	Z2	Z3
L	X	X	H	H	H	H
H	L	L	L	H	H	H
H	H	L	H	L	H	H
H	L	H	H	H	L	H
H	H	H	H	H	H	L

Verilog-HDL DESCRIPTION

```
D24GL  inst(Z0,Z1,Z2,Z3,A,B,G);
```

VHDL DESCRIPTION

```
inst:D24GL
   port   map(Z0,Z1,Z2,Z3,A,B,G);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z0,Z1,Z2,Z3
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	3.42
B	3.47
G	4.21

OUTPUT DRIVE (LU)

PIN NAME	Z0,Z1	Z2	Z3
DRIVE	28.0	28.4	29.5

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D24GL D24GL 2/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z0	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.1001	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.36	0.53	1.21
0.38	0.29	0.43	0.60	1.29
1.00	0.35	0.49	0.67	1.35
3.00	0.44	0.59	0.77	1.46

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z0	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.1115	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.62	0.94	2.18
0.38	0.39	0.65	0.97	2.21
1.00	0.46	0.72	1.04	2.28
3.00	0.61	0.87	1.19	2.43

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.1001	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.27	0.44	1.12
0.38	0.15	0.30	0.47	1.15
1.00	0.16	0.33	0.52	1.21
3.00	0.13	0.35	0.59	1.36

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.1115	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.44	0.75	1.99
0.38	0.26	0.50	0.81	2.05
1.00	0.33	0.61	0.92	2.16
3.00	0.53	0.86	1.22	2.51

D24GL D24GL 3/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.1000	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.36	0.53	1.22
0.38	0.29	0.43	0.61	1.29
1.00	0.35	0.50	0.67	1.36
3.00	0.45	0.60	0.78	1.47

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.1062	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.60	0.90	2.09
0.38	0.39	0.63	0.93	2.12
1.00	0.45	0.70	1.00	2.19
3.00	0.61	0.85	1.15	2.34

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0999	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.27	0.44	1.12
0.38	0.15	0.30	0.47	1.15
1.00	0.17	0.34	0.52	1.21
3.00	0.18	0.39	0.62	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z3	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0909	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.37	0.63	1.66
0.38	0.22	0.43	0.69	1.72
1.00	0.29	0.53	0.79	1.82
3.00	0.45	0.75	1.06	2.15

D24GL | D24GL | 4/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z0	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.1001	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.33	0.50	1.19
0.38	0.26	0.40	0.58	1.26
1.00	0.32	0.46	0.64	1.32
3.00	0.40	0.56	0.74	1.43

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z0	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.1115	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.60	0.91	2.15
0.38	0.36	0.63	0.94	2.18
1.00	0.43	0.69	1.01	2.25
3.00	0.58	0.85	1.16	2.41

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.1001	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.33	0.50	1.19
0.38	0.26	0.40	0.58	1.26
1.00	0.32	0.46	0.64	1.32
3.00	0.40	0.56	0.74	1.43

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.1115	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.60	0.91	2.15
0.38	0.37	0.63	0.94	2.18
1.00	0.43	0.70	1.01	2.25
3.00	0.59	0.85	1.17	2.41

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D24GL D24GL 5/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.1000	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.10
0.38	0.13	0.28	0.45	1.13
1.00	0.13	0.31	0.50	1.19
3.00	0.08	0.32	0.56	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.1062	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.40	0.69	1.88
0.38	0.23	0.48	0.78	1.96
1.00	0.32	0.60	0.91	2.10
3.00	0.53	0.89	1.26	2.53

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0999	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.24	0.42	1.10
0.38	0.13	0.27	0.45	1.13
1.00	0.14	0.31	0.50	1.19
3.00	0.11	0.34	0.58	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z3	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0909	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.35	0.60	1.63
0.38	0.21	0.43	0.68	1.71
1.00	0.29	0.55	0.82	1.85
3.00	0.48	0.81	1.15	2.27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Z0	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.1001	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.30	0.47	1.15
0.38	0.18	0.32	0.49	1.17
1.00	0.20	0.36	0.55	1.22
3.00	0.20	0.42	0.64	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Z0	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.1115	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.48	0.80	2.04
0.38	0.26	0.52	0.83	2.07
1.00	0.30	0.56	0.87	2.11
3.00	0.39	0.68	1.01	2.25

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.1001	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.30	0.47	1.15
0.38	0.18	0.32	0.50	1.17
1.00	0.20	0.37	0.55	1.23
3.00	0.21	0.42	0.64	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.1115	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.48	0.79	2.03
0.38	0.26	0.52	0.83	2.07
1.00	0.30	0.56	0.87	2.11
3.00	0.40	0.69	1.01	2.25

D24GL | D24GL | 7/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.1000	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.30	0.47	1.15
0.38	0.18	0.32	0.49	1.17
1.00	0.20	0.37	0.55	1.23
3.00	0.22	0.43	0.65	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.1062	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.46	0.75	1.94
0.38	0.24	0.49	0.79	1.97
1.00	0.28	0.52	0.82	2.01
3.00	0.36	0.64	0.95	2.13

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0999	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.30	0.47	1.15
0.38	0.18	0.32	0.49	1.17
1.00	0.21	0.37	0.55	1.23
3.00	0.26	0.46	0.67	1.41

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Z3	---	FALL

SLEW FACTOR

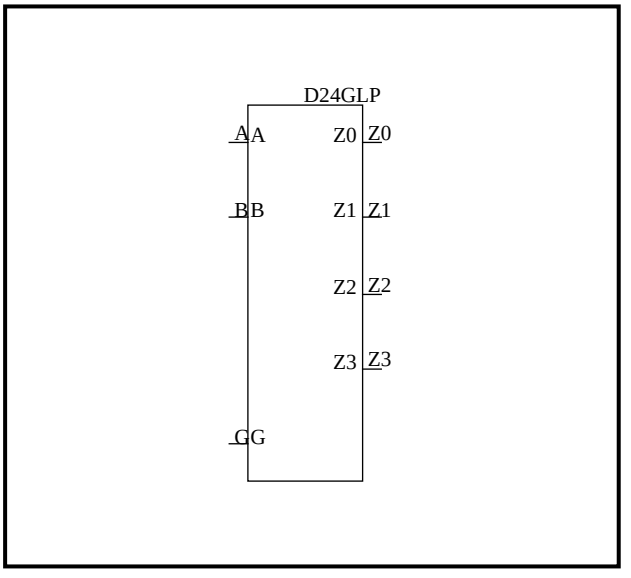
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0909	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.39	0.65	1.68
0.38	0.22	0.43	0.69	1.72
1.00	0.26	0.48	0.74	1.76
3.00	0.33	0.60	0.88	1.92

D24GLP	D24GLP	1/7

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
D24GLP	2 TO 4 DECODER (GATED OUTPUTS ACTIVE LOW)	13	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT			
G	A	B	Z0	Z1	Z2	Z3
L	X	X	H	H	H	H
H	L	L	L	H	H	H
H	H	L	H	L	H	H
H	L	H	H	H	L	H
H	H	H	H	H	H	L

Verilog-HDL DESCRIPTION

```
D24GLP  inst(Z0,Z1,Z2,Z3,A,B,G);
```

VHDL DESCRIPTION

```
inst:D24GLP
   port   map(Z0,Z1,Z2,Z3,A,B,G);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z0,Z1,Z2,Z3
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	5.77
B	5.59
G	8.76

OUTPUT DRIVE (LU)

PIN NAME	Z0	Z1	Z2	Z3
DRIVE	52.4	53.2	53.1	50.6

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z0	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0566	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.33	0.42	0.76
0.38	0.33	0.41	0.50	0.85
1.00	0.42	0.50	0.59	0.93
3.00	0.55	0.64	0.73	1.09

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z0	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0572	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.40	0.54	0.71	1.35
0.38	0.43	0.57	0.73	1.38
1.00	0.50	0.64	0.81	1.45
3.00	0.68	0.82	0.99	1.63

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0551	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.17	0.25	0.58
0.38	0.12	0.20	0.28	0.60
1.00	0.13	0.22	0.31	0.66
3.00	0.08	0.20	0.33	0.76

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0572	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.29	0.45	1.07
0.38	0.21	0.34	0.49	1.11
1.00	0.26	0.41	0.57	1.19
3.00	0.41	0.58	0.76	1.44

D24GLP D24GLP 3/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0547	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.32	0.40	0.73
0.38	0.32	0.40	0.48	0.81
1.00	0.41	0.49	0.57	0.90
3.00	0.55	0.63	0.72	1.06

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0553	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.40	0.54	0.69	1.31
0.38	0.43	0.56	0.72	1.34
1.00	0.51	0.64	0.80	1.41
3.00	0.69	0.82	0.98	1.59

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0547	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.17	0.26	0.58
0.38	0.12	0.20	0.28	0.60
1.00	0.13	0.22	0.32	0.66
3.00	0.09	0.21	0.35	0.77

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z3	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0543	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.28	0.43	1.03
0.38	0.20	0.32	0.48	1.08
1.00	0.25	0.39	0.55	1.15
3.00	0.38	0.55	0.73	1.38

D24GLP D24GLP 4/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z0	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0566	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.30	0.40	0.79
0.38	0.29	0.38	0.48	0.87
1.00	0.37	0.46	0.56	0.96
3.00	0.50	0.59	0.70	1.10

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z0	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0572	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.52	0.69	1.33
0.38	0.40	0.55	0.72	1.36
1.00	0.48	0.63	0.79	1.44
3.00	0.65	0.81	0.98	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0551	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.29	0.39	0.78
0.38	0.29	0.37	0.48	0.86
1.00	0.37	0.46	0.56	0.95
3.00	0.50	0.59	0.69	1.09

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0572	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.52	0.69	1.33
0.38	0.40	0.55	0.72	1.36
1.00	0.48	0.63	0.80	1.44
3.00	0.66	0.81	0.98	1.62

D24GLP D24GLP 5/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0547	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.17	0.26	0.65
0.38	0.11	0.19	0.29	0.68
1.00	0.11	0.22	0.33	0.73
3.00	0.05	0.20	0.35	0.84

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0553	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.25	0.40	1.02
0.38	0.20	0.33	0.48	1.10
1.00	0.27	0.43	0.61	1.24
3.00	0.45	0.67	0.89	1.63

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0547	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.17	0.26	0.65
0.38	0.11	0.19	0.29	0.68
1.00	0.11	0.22	0.33	0.73
3.00	0.05	0.20	0.35	0.84

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z3	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0543	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.25	0.40	1.00
0.38	0.19	0.32	0.48	1.08
1.00	0.26	0.43	0.60	1.22
3.00	0.44	0.66	0.87	1.60

D24GLP D24GLP 6/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Z0	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0566	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.20	0.29	0.64
0.38	0.15	0.23	0.32	0.66
1.00	0.16	0.25	0.36	0.72
3.00	0.14	0.26	0.40	0.83

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Z0	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0572	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.32	0.48	1.12
0.38	0.21	0.35	0.51	1.15
1.00	0.25	0.39	0.56	1.19
3.00	0.34	0.51	0.69	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0551	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.19	0.27	0.60
0.38	0.14	0.21	0.30	0.62
1.00	0.15	0.24	0.34	0.68
3.00	0.12	0.24	0.37	0.79

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0572	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.31	0.47	1.11
0.38	0.21	0.35	0.51	1.14
1.00	0.25	0.39	0.55	1.19
3.00	0.35	0.51	0.69	1.34

D24GLP D24GLP 7/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0547	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.18	0.27	0.59
0.38	0.13	0.21	0.29	0.61
1.00	0.14	0.23	0.33	0.67
3.00	0.12	0.24	0.36	0.78

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0553	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.30	0.46	1.07
0.38	0.21	0.33	0.49	1.11
1.00	0.24	0.38	0.53	1.15
3.00	0.34	0.49	0.67	1.30

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0547	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.19	0.27	0.60
0.38	0.14	0.21	0.30	0.62
1.00	0.15	0.24	0.34	0.68
3.00	0.13	0.25	0.38	0.80

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Z3	---	FALL

SLEW FACTOR

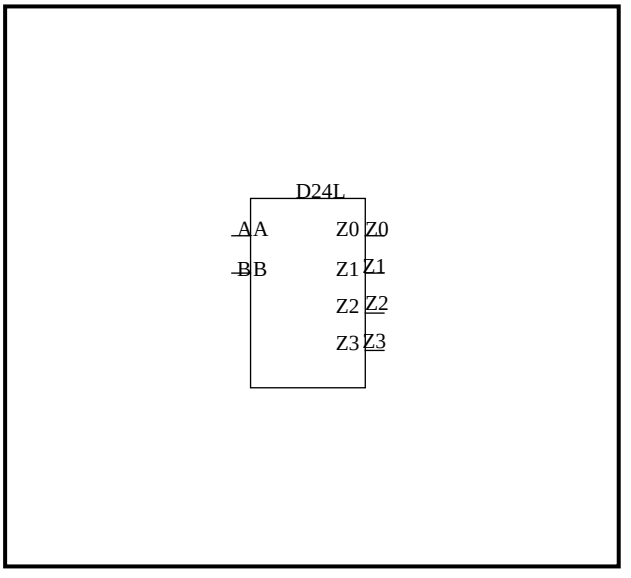
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0543	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.29	0.44	1.04
0.38	0.20	0.32	0.48	1.08
1.00	0.24	0.37	0.52	1.12
3.00	0.32	0.48	0.65	1.26

D24L	D24L	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
D24L	2 TO 4 DECODER (OUTPUT ACTIVE LOW)	5	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT			
A	B	Z0	Z1	Z2	Z3
L	L	L	H	H	H
H	L	H	L	H	H
L	H	H	H	L	H
H	H	H	H	H	L

Verilog-HDL DESCRIPTION

```
D24L  inst(Z0,Z1,Z2,Z3,A,B);
```

VHDL DESCRIPTION

```
inst:D24L
   port   map(Z0,Z1,Z2,Z3,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z0,Z1,Z2,Z3
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	3.08
B	3.17

OUTPUT DRIVE (LU)

PIN NAME	Z0	Z1	Z2	Z3
DRIVE	39.3	42.3	39.0	36.4

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D24L D24L 2/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z0	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0971	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.32	0.49	1.16
0.38	0.24	0.39	0.56	1.23
1.00	0.31	0.45	0.62	1.30
3.00	0.41	0.56	0.73	1.41

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z0	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0577	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.38	0.56	1.22
0.38	0.27	0.42	0.59	1.25
1.00	0.33	0.48	0.65	1.32
3.00	0.46	0.62	0.80	1.46

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0862	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.08	0.21	0.36	0.96
0.38	0.10	0.24	0.39	0.99
1.00	0.12	0.28	0.44	1.05
3.00	0.14	0.35	0.55	1.23

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0587	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.08	0.22	0.39	1.06
0.38	0.15	0.30	0.47	1.14
1.00	0.20	0.40	0.59	1.28
3.00	0.31	0.60	0.86	1.68

D24L D24L 3/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0971	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.32	0.49	1.16
0.38	0.24	0.39	0.56	1.23
1.00	0.31	0.45	0.62	1.30
3.00	0.41	0.56	0.73	1.41

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0588	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.39	0.56	1.24
0.38	0.27	0.42	0.60	1.27
1.00	0.33	0.49	0.66	1.34
3.00	0.46	0.63	0.81	1.48

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0967	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.07
0.38	0.11	0.26	0.43	1.10
1.00	0.14	0.30	0.48	1.15
3.00	0.17	0.39	0.61	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z3	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0584	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.22	0.39	1.06
0.38	0.15	0.30	0.47	1.14
1.00	0.20	0.40	0.59	1.29
3.00	0.30	0.59	0.86	1.68

D24L D24L 4/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z0	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0971	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.32	0.47	1.07
0.38	0.27	0.39	0.55	1.14
1.00	0.33	0.46	0.61	1.21
3.00	0.45	0.58	0.74	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z0	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0577	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.39	0.56	1.22
0.38	0.27	0.42	0.59	1.25
1.00	0.33	0.48	0.65	1.31
3.00	0.46	0.62	0.79	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0862	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.32	0.47	1.05
0.38	0.27	0.39	0.54	1.13
1.00	0.33	0.46	0.61	1.20
3.00	0.45	0.58	0.74	1.33

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0587	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.39	0.56	1.23
0.38	0.28	0.42	0.59	1.26
1.00	0.34	0.48	0.65	1.33
3.00	0.47	0.62	0.79	1.47

D24L | D24L | 5/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0971	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.23	0.39	1.00
0.38	0.13	0.26	0.41	1.02
1.00	0.16	0.31	0.47	1.08
3.00	0.22	0.41	0.61	1.27

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0588	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.23	0.40	1.06
0.38	0.14	0.29	0.45	1.12
1.00	0.18	0.36	0.54	1.21
3.00	0.24	0.49	0.73	1.49

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0967	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.23	0.38	1.00
0.38	0.13	0.26	0.41	1.02
1.00	0.16	0.31	0.47	1.08
3.00	0.22	0.41	0.61	1.27

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z3	---	FALL

SLEW FACTOR

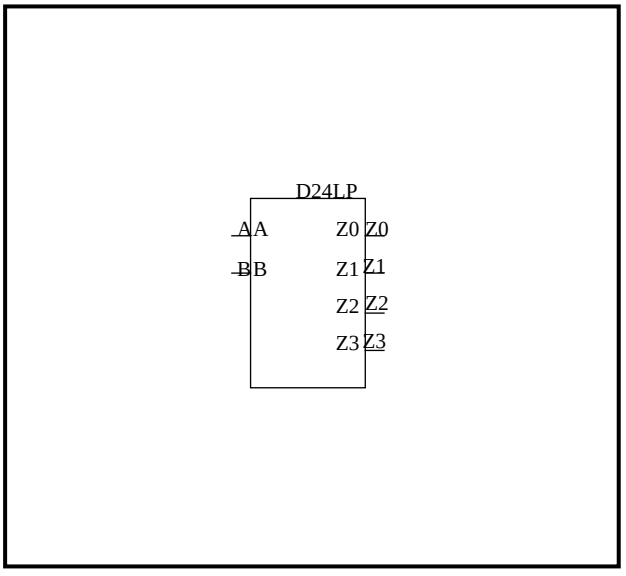
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0584	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.23	0.40	1.07
0.38	0.14	0.29	0.46	1.13
1.00	0.18	0.36	0.54	1.22
3.00	0.24	0.49	0.73	1.49

D24LP	D24LP	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
D24LP	2 TO 4 DECODER (OUTPUT ACTIVE LOW)	9	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT			
A	B	Z0	Z1	Z2	Z3
L	L	L	H	H	H
H	L	H	L	H	H
L	H	H	H	L	H
H	H	H	H	H	L

Verilog-HDL DESCRIPTION

```
D24LP  inst(Z0,Z1,Z2,Z3,A,B);
```

VHDL DESCRIPTION

```
inst:D24LP
   port   map(Z0,Z1,Z2,Z3,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z0,Z1,Z2,Z3
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	5.10
B	5.36

OUTPUT DRIVE (LU)

PIN NAME	Z0	Z1	Z2	Z3
DRIVE	77.1	74.1	79.1	75.6

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z0	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0480	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.29	0.38	0.72
0.38	0.30	0.38	0.46	0.81
1.00	0.39	0.47	0.56	0.90
3.00	0.55	0.63	0.72	1.07

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z0	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0309	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.38	0.48	0.85
0.38	0.32	0.41	0.51	0.88
1.00	0.39	0.48	0.58	0.96
3.00	0.54	0.64	0.74	1.12

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0450	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.08	0.15	0.23	0.54
0.38	0.10	0.17	0.25	0.57
1.00	0.12	0.21	0.30	0.63
3.00	0.14	0.26	0.38	0.77

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0306	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.08	0.15	0.24	0.60
0.38	0.13	0.22	0.31	0.67
1.00	0.17	0.28	0.40	0.78
3.00	0.25	0.42	0.57	1.06

D24LP D24LP 3/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0423	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.27	0.35	0.65
0.38	0.29	0.36	0.44	0.73
1.00	0.38	0.45	0.53	0.83
3.00	0.54	0.61	0.70	1.00

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0295	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.37	0.47	0.83
0.38	0.32	0.40	0.50	0.86
1.00	0.39	0.48	0.57	0.93
3.00	0.54	0.63	0.73	1.10

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0424	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.08	0.14	0.21	0.51
0.38	0.10	0.16	0.24	0.53
1.00	0.12	0.20	0.28	0.60
3.00	0.14	0.25	0.36	0.74

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z3	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0287	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.08	0.15	0.23	0.58
0.38	0.12	0.21	0.30	0.64
1.00	0.17	0.27	0.38	0.75
3.00	0.24	0.40	0.55	1.02

D24LP | D24LP | 4/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z0	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0480	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.29	0.37	0.68
0.38	0.30	0.37	0.45	0.77
1.00	0.38	0.46	0.54	0.86
3.00	0.54	0.62	0.71	1.03

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z0	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0309	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.37	0.47	0.85
0.38	0.31	0.40	0.50	0.88
1.00	0.38	0.47	0.58	0.95
3.00	0.53	0.63	0.73	1.11

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0450	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.29	0.38	0.70
0.38	0.30	0.37	0.46	0.78
1.00	0.39	0.46	0.55	0.87
3.00	0.55	0.63	0.71	1.04

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0306	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.37	0.47	0.85
0.38	0.32	0.41	0.51	0.88
1.00	0.39	0.48	0.58	0.95
3.00	0.54	0.63	0.73	1.11

D24LP | D24LP | 5/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0423	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.08	0.14	0.22	0.52
0.38	0.10	0.17	0.25	0.55
1.00	0.12	0.20	0.29	0.61
3.00	0.14	0.25	0.37	0.75

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0295	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.08	0.15	0.24	0.58
0.38	0.13	0.21	0.30	0.65
1.00	0.17	0.28	0.39	0.76
3.00	0.25	0.41	0.56	1.04

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0424	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.08	0.14	0.22	0.52
0.38	0.10	0.17	0.25	0.55
1.00	0.12	0.20	0.29	0.61
3.00	0.14	0.26	0.37	0.75

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z3	---	FALL

SLEW FACTOR

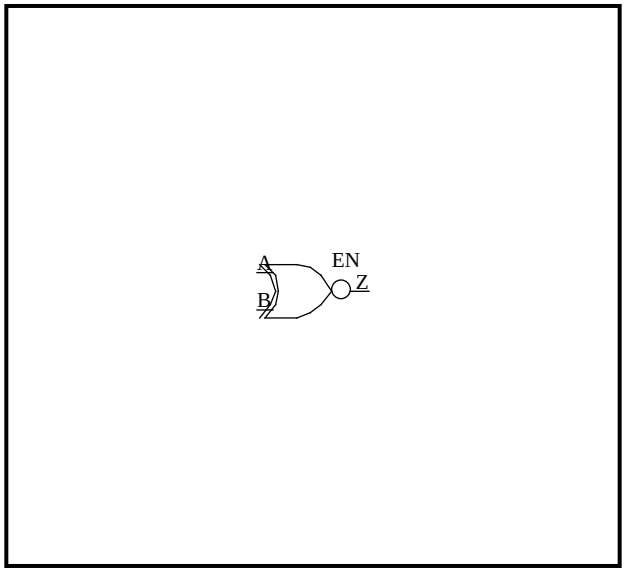
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0287	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.08	0.15	0.23	0.58
0.38	0.13	0.21	0.30	0.65
1.00	0.17	0.28	0.39	0.76
3.00	0.25	0.41	0.56	1.03

EN	EN	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
EN	2-INPUT EXCLUSIVE NOR	3	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
A	B	Z
L	L	H
L	H	L
H	L	L
H	H	H

Verilog-HDL DESCRIPTION

```
EN  inst(Z,A,B);
```

VHDL DESCRIPTION

```
inst:EN
   port   map(Z,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	0.98
B	2.11

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	44.6

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0961	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.42	0.59	1.26
0.38	0.34	0.50	0.67	1.34
1.00	0.43	0.58	0.76	1.43
3.00	0.59	0.74	0.92	1.59

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0389	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.47	0.61	1.09
0.38	0.36	0.50	0.64	1.12
1.00	0.43	0.58	0.72	1.20
3.00	0.59	0.75	0.89	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0961	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.38	0.53	0.70	1.37
0.38	0.42	0.56	0.73	1.40
1.00	0.48	0.62	0.80	1.47
3.00	0.61	0.75	0.92	1.59

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0389	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.47	0.61	1.08
0.38	0.42	0.55	0.68	1.15
1.00	0.48	0.61	0.74	1.22
3.00	0.58	0.71	0.85	1.32

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0961	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.33	0.49	1.16
0.38	0.26	0.40	0.57	1.24
1.00	0.32	0.46	0.63	1.30
3.00	0.41	0.56	0.73	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0389	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.35	0.48	0.95
0.38	0.26	0.38	0.51	0.98
1.00	0.32	0.45	0.58	1.05
3.00	0.46	0.59	0.73	1.20

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0961	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.44	0.61	1.28
0.38	0.33	0.47	0.65	1.32
1.00	0.39	0.54	0.71	1.37
3.00	0.51	0.66	0.83	1.49

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A	FALL

SLEW FACTOR

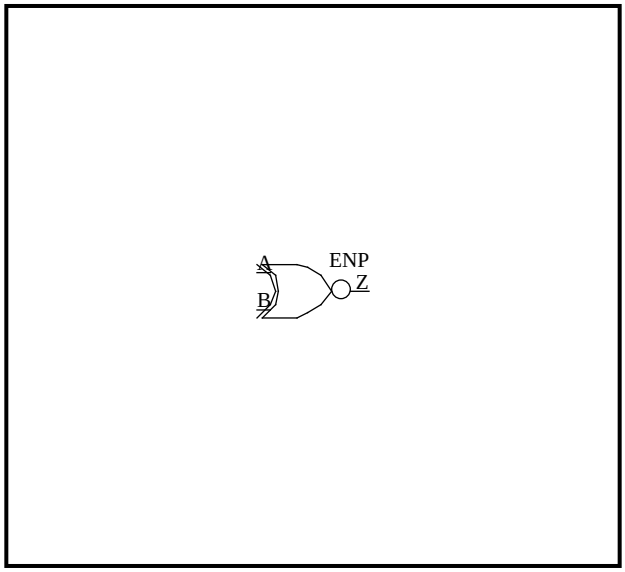
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0389	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.35	0.48	0.96
0.38	0.30	0.43	0.56	1.04
1.00	0.41	0.53	0.66	1.14
3.00	0.52	0.64	0.78	1.25

ENP	ENP	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
ENP	2-INPUT EXCLUSIVE NOR	4	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
A	B	Z
L	L	H
L	H	L
H	L	L
H	H	H

Verilog-HDL DESCRIPTION

```
ENP  inst(Z,A,B);
```

VHDL DESCRIPTION

```
inst:ENP
  port  map(Z,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	0.98
B	2.06

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	89.9

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ENP ENP 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0466	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.34	0.43	0.77
0.38	0.34	0.42	0.51	0.85
1.00	0.44	0.52	0.61	0.95
3.00	0.61	0.70	0.79	1.13

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0210	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.41	0.50	0.78
0.38	0.36	0.45	0.54	0.82
1.00	0.43	0.52	0.61	0.89
3.00	0.60	0.70	0.79	1.08

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0466	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.38	0.46	0.55	0.89
0.38	0.42	0.50	0.59	0.92
1.00	0.48	0.56	0.65	0.98
3.00	0.61	0.69	0.78	1.11

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0210	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.43	0.51	0.79
0.38	0.42	0.50	0.59	0.86
1.00	0.48	0.56	0.65	0.92
3.00	0.59	0.67	0.76	1.03

ENP | ENP | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0466	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.27	0.36	0.70
0.38	0.27	0.35	0.44	0.78
1.00	0.35	0.43	0.52	0.86
3.00	0.49	0.57	0.66	1.00

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0210	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.31	0.39	0.66
0.38	0.26	0.34	0.42	0.69
1.00	0.32	0.41	0.49	0.76
3.00	0.47	0.56	0.65	0.93

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0466	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.36	0.45	0.78
0.38	0.31	0.39	0.48	0.82
1.00	0.37	0.45	0.54	0.88
3.00	0.49	0.57	0.66	1.00

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A	FALL

SLEW FACTOR

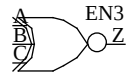
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0210	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.28	0.37	0.64
0.38	0.28	0.37	0.45	0.73
1.00	0.40	0.49	0.57	0.84
3.00	0.52	0.60	0.68	0.95

EN3	EN3	1/7

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
EN3	3-INPUT EXCLUSIVE NOR	7	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
A	B	C	Z
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
EN3  inst(Z,A,B,C);
```

VHDL DESCRIPTION

```
inst:EN3
  port  map(Z,A,B,C);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.04
B	3.30
C	2.00

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	48.8

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0842	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.71	0.85	1.01	1.62
0.38	0.74	0.88	1.04	1.65
1.00	0.81	0.96	1.12	1.72
3.00	0.99	1.13	1.30	1.90

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0375	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.61	0.77	0.92	1.41
0.38	0.70	0.85	1.01	1.49
1.00	0.80	0.96	1.11	1.60
3.00	0.99	1.14	1.30	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0842	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.57	0.73	1.34
0.38	0.51	0.65	0.81	1.42
1.00	0.61	0.76	0.92	1.53
3.00	0.82	0.97	1.13	1.74

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0375	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.50	0.66	0.82	1.31
0.38	0.53	0.69	0.85	1.34
1.00	0.60	0.77	0.92	1.42
3.00	0.79	0.96	1.12	1.63

EN3 EN3 3/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0842	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.56	0.73	1.33
0.38	0.50	0.65	0.81	1.41
1.00	0.61	0.75	0.91	1.52
3.00	0.82	0.96	1.12	1.73

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0375	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.65	0.81	1.30
0.38	0.52	0.68	0.84	1.33
1.00	0.60	0.76	0.92	1.41
3.00	0.78	0.95	1.12	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0842	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.72	0.86	1.02	1.63
0.38	0.75	0.89	1.05	1.66
1.00	0.82	0.97	1.13	1.74
3.00	1.00	1.15	1.31	1.92

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&~C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0375	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.61	0.77	0.92	1.41
0.38	0.70	0.85	1.01	1.49
1.00	0.80	0.96	1.11	1.60
3.00	0.99	1.15	1.30	1.79

EN3 EN3 4/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0842	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.43	0.57	0.73	1.34
0.38	0.46	0.60	0.76	1.37
1.00	0.52	0.67	0.83	1.43
3.00	0.66	0.80	0.96	1.57

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0375	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.48	0.63	1.12
0.38	0.40	0.56	0.71	1.20
1.00	0.54	0.69	0.85	1.33
3.00	0.69	0.85	1.00	1.48

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0842	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.47	0.64	1.24
0.38	0.41	0.55	0.72	1.32
1.00	0.49	0.64	0.80	1.41
3.00	0.62	0.76	0.92	1.52

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0375	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.57	0.72	1.21
0.38	0.44	0.59	0.74	1.23
1.00	0.51	0.66	0.81	1.30
3.00	0.68	0.84	0.99	1.49

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0842	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.50	0.66	1.27
0.38	0.43	0.58	0.74	1.35
1.00	0.52	0.67	0.83	1.44
3.00	0.67	0.82	0.98	1.59

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0375	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.39	0.54	0.69	1.17
0.38	0.41	0.56	0.71	1.19
1.00	0.48	0.63	0.78	1.26
3.00	0.64	0.80	0.95	1.44

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0842	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.61	0.77	1.38
0.38	0.49	0.63	0.80	1.41
1.00	0.55	0.70	0.86	1.47
3.00	0.69	0.83	0.99	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&~C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0375	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.45	0.60	1.09
0.38	0.39	0.54	0.69	1.18
1.00	0.53	0.68	0.83	1.31
3.00	0.67	0.82	0.97	1.45

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0842	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.45	0.62	1.22
0.38	0.34	0.49	0.65	1.25
1.00	0.40	0.54	0.71	1.31
3.00	0.52	0.66	0.82	1.42

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0375	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.35	0.49	0.97
0.38	0.30	0.44	0.58	1.06
1.00	0.43	0.57	0.71	1.17
3.00	0.55	0.69	0.82	1.29

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0842	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.34	0.50	1.10
0.38	0.27	0.42	0.58	1.18
1.00	0.34	0.49	0.65	1.25
3.00	0.46	0.59	0.75	1.37

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0375	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.36	0.49	0.96
0.38	0.26	0.39	0.53	1.00
1.00	0.32	0.46	0.60	1.07
3.00	0.47	0.62	0.76	1.23

EN3 EN3 7/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0842	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.35	0.51	1.12
0.38	0.28	0.43	0.59	1.20
1.00	0.36	0.50	0.66	1.27
3.00	0.49	0.63	0.79	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0375	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.35	0.49	0.95
0.38	0.26	0.39	0.52	0.99
1.00	0.32	0.45	0.59	1.05
3.00	0.47	0.60	0.74	1.21

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0842	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.47	0.63	1.24
0.38	0.35	0.50	0.66	1.27
1.00	0.41	0.56	0.72	1.33
3.00	0.53	0.67	0.83	1.44

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&~B	FALL

SLEW FACTOR

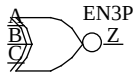
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0375	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.35	0.49	0.96
0.38	0.30	0.43	0.57	1.05
1.00	0.42	0.56	0.69	1.16
3.00	0.54	0.67	0.80	1.27

EN3P	EN3P	1/7

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
EN3P	3-INPUT EXCLUSIVE NOR	7	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
A	B	C	Z
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
EN3P  inst(Z,A,B,C);
```

VHDL DESCRIPTION

```
inst:EN3P
  port  map(Z,A,B,C);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.04
B	3.30
C	2.00

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	84.4

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0465	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.74	0.82	0.92	1.27
0.38	0.77	0.85	0.95	1.30
1.00	0.84	0.93	1.03	1.38
3.00	1.02	1.11	1.21	1.56

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0241	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.63	0.74	0.84	1.17
0.38	0.72	0.82	0.93	1.25
1.00	0.82	0.93	1.03	1.36
3.00	1.00	1.11	1.22	1.54

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0465	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.54	0.64	0.99
0.38	0.54	0.62	0.72	1.08
1.00	0.64	0.73	0.83	1.18
3.00	0.86	0.95	1.05	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0241	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.63	0.74	1.07
0.38	0.55	0.66	0.77	1.10
1.00	0.62	0.73	0.84	1.17
3.00	0.82	0.93	1.04	1.38

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0465	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.53	0.63	0.98
0.38	0.53	0.62	0.71	1.07
1.00	0.63	0.72	0.82	1.17
3.00	0.85	0.94	1.04	1.39

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0241	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.62	0.73	1.06
0.38	0.54	0.65	0.76	1.09
1.00	0.62	0.73	0.83	1.17
3.00	0.81	0.92	1.04	1.37

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0465	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.75	0.84	0.94	1.29
0.38	0.78	0.87	0.97	1.32
1.00	0.86	0.94	1.04	1.40
3.00	1.04	1.12	1.22	1.58

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&~C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0241	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.63	0.74	0.84	1.17
0.38	0.72	0.82	0.93	1.25
1.00	0.82	0.93	1.03	1.36
3.00	1.01	1.12	1.22	1.55

EN3P | EN3P | 4/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0465	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.54	0.64	0.99
0.38	0.49	0.57	0.67	1.02
1.00	0.55	0.64	0.73	1.08
3.00	0.68	0.77	0.87	1.22

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0241	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.45	0.55	0.88
0.38	0.42	0.52	0.63	0.96
1.00	0.56	0.66	0.76	1.09
3.00	0.73	0.83	0.94	1.26

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0465	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.45	0.55	0.90
0.38	0.44	0.53	0.63	0.98
1.00	0.53	0.62	0.72	1.07
3.00	0.68	0.76	0.86	1.21

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0241	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.43	0.54	0.64	0.97
0.38	0.46	0.56	0.67	0.99
1.00	0.53	0.63	0.74	1.06
3.00	0.70	0.81	0.92	1.24

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0465	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.39	0.47	0.57	0.93
0.38	0.47	0.56	0.65	1.01
1.00	0.57	0.65	0.75	1.10
3.00	0.73	0.82	0.92	1.27

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0241	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.40	0.51	0.61	0.93
0.38	0.43	0.53	0.64	0.96
1.00	0.50	0.60	0.70	1.02
3.00	0.67	0.77	0.87	1.20

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0465	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.58	0.68	1.03
0.38	0.52	0.61	0.71	1.06
1.00	0.58	0.67	0.77	1.12
3.00	0.72	0.80	0.90	1.25

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&~C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0241	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.42	0.52	0.85
0.38	0.40	0.51	0.61	0.93
1.00	0.54	0.65	0.75	1.07
3.00	0.70	0.80	0.90	1.22

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0465	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.42	0.52	0.87
0.38	0.37	0.46	0.56	0.91
1.00	0.43	0.51	0.61	0.96
3.00	0.54	0.63	0.73	1.08

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0241	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.32	0.42	0.73
0.38	0.30	0.40	0.50	0.82
1.00	0.45	0.55	0.65	0.96
3.00	0.61	0.71	0.80	1.11

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0465	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.31	0.41	0.76
0.38	0.31	0.39	0.49	0.84
1.00	0.39	0.48	0.58	0.93
3.00	0.55	0.64	0.73	1.08

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0241	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.33	0.43	0.74
0.38	0.27	0.37	0.46	0.77
1.00	0.34	0.43	0.53	0.84
3.00	0.49	0.59	0.69	1.01

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0465	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.32	0.42	0.78
0.38	0.32	0.41	0.51	0.86
1.00	0.41	0.50	0.59	0.95
3.00	0.59	0.67	0.76	1.11

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0241	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.33	0.42	0.73
0.38	0.27	0.36	0.46	0.76
1.00	0.33	0.43	0.52	0.83
3.00	0.48	0.58	0.68	0.99

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0465	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.44	0.54	0.89
0.38	0.39	0.47	0.57	0.93
1.00	0.44	0.53	0.63	0.98
3.00	0.56	0.65	0.75	1.10

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&~B	FALL

SLEW FACTOR

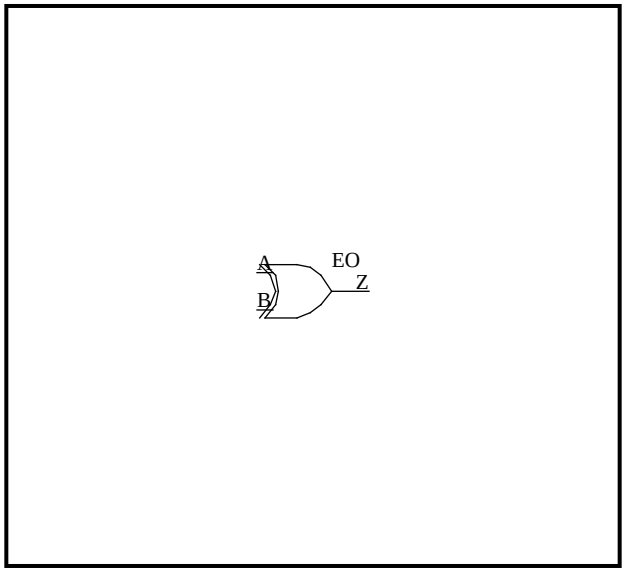
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0241	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.31	0.41	0.73
0.38	0.30	0.40	0.50	0.81
1.00	0.45	0.55	0.64	0.95
3.00	0.60	0.69	0.78	1.08

EO	EO	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
EO	2-INPUT EXCLUSIVE OR	3	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
A	B	Z
L	L	L
L	H	H
H	L	H
H	H	L

Verilog-HDL DESCRIPTION

```
EO  inst(Z,A,B);
```

VHDL DESCRIPTION

```
inst:EO
   port   map(Z,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	0.98
B	2.11

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	45.1

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EO | EO | 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0940	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.38	0.52	0.69	1.35
0.38	0.41	0.56	0.73	1.39
1.00	0.47	0.62	0.79	1.45
3.00	0.60	0.75	0.92	1.58

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0400	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.48	0.62	1.10
0.38	0.42	0.55	0.69	1.17
1.00	0.48	0.62	0.75	1.23
3.00	0.59	0.72	0.86	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0940	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.42	0.59	1.25
0.38	0.35	0.49	0.67	1.33
1.00	0.43	0.58	0.75	1.41
3.00	0.59	0.74	0.91	1.58

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0400	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.47	0.61	1.10
0.38	0.36	0.50	0.64	1.14
1.00	0.44	0.58	0.72	1.21
3.00	0.60	0.75	0.90	1.40

EO | EO | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0940	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.44	0.61	1.27
0.38	0.33	0.47	0.64	1.31
1.00	0.39	0.54	0.71	1.36
3.00	0.52	0.66	0.83	1.48

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0400	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.35	0.49	0.97
0.38	0.30	0.43	0.57	1.05
1.00	0.41	0.53	0.66	1.14
3.00	0.52	0.64	0.77	1.26

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0940	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.32	0.48	1.14
0.38	0.26	0.40	0.56	1.22
1.00	0.32	0.46	0.62	1.28
3.00	0.41	0.55	0.72	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A	FALL

SLEW FACTOR

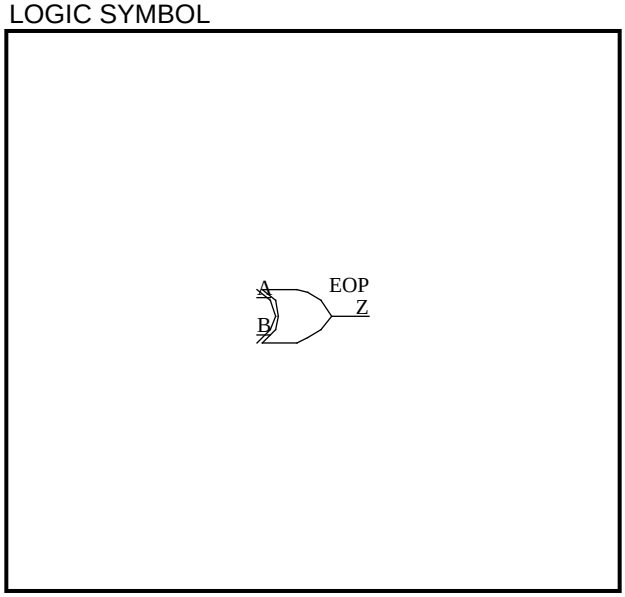
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0400	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.35	0.49	0.97
0.38	0.26	0.39	0.52	1.00
1.00	0.32	0.45	0.58	1.07
3.00	0.47	0.60	0.74	1.22

EOP	EOP	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
EOP	2-INPUT EXCLUSIVE OR	4	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
A	B	Z
L	L	L
L	H	H
H	L	H
H	H	L

Verilog-HDL DESCRIPTION

```
EOP  inst(Z,A,B);
```

VHDL DESCRIPTION

```
inst:EOP
  port  map(Z,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	0.98
B	2.06

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	90.0

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EOP EOP 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0466	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.38	0.46	0.55	0.88
0.38	0.41	0.49	0.58	0.92
1.00	0.47	0.55	0.64	0.98
3.00	0.60	0.68	0.77	1.11

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0210	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.44	0.52	0.79
0.38	0.42	0.51	0.59	0.86
1.00	0.48	0.57	0.65	0.93
3.00	0.59	0.68	0.76	1.03

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0466	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.35	0.44	0.78
0.38	0.35	0.43	0.52	0.86
1.00	0.44	0.52	0.61	0.95
3.00	0.61	0.70	0.79	1.13

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0210	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.41	0.50	0.78
0.38	0.36	0.45	0.53	0.81
1.00	0.43	0.52	0.61	0.89
3.00	0.60	0.70	0.79	1.08

EOP EOP 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0466	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.36	0.45	0.79
0.38	0.31	0.40	0.49	0.82
1.00	0.37	0.45	0.54	0.88
3.00	0.49	0.57	0.66	1.00

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0210	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.29	0.38	0.65
0.38	0.29	0.37	0.45	0.72
1.00	0.41	0.49	0.57	0.84
3.00	0.52	0.60	0.68	0.95

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0466	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.27	0.36	0.69
0.38	0.27	0.35	0.44	0.77
1.00	0.35	0.43	0.52	0.85
3.00	0.49	0.57	0.65	0.99

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A	FALL

SLEW FACTOR

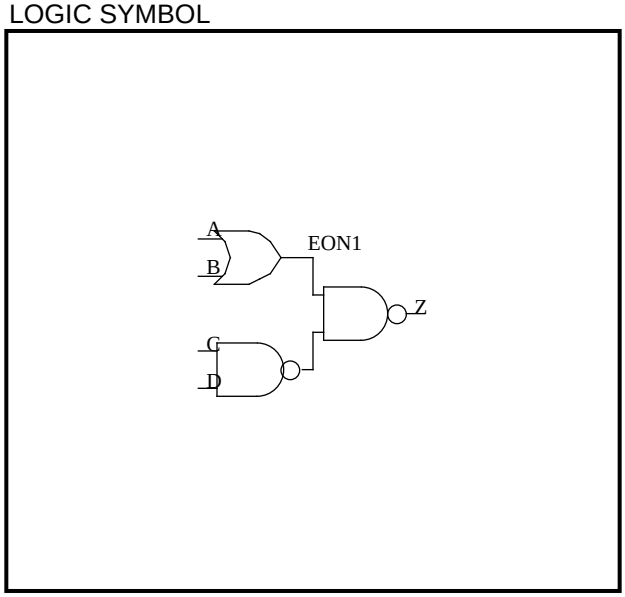
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0210	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.31	0.39	0.66
0.38	0.26	0.34	0.42	0.70
1.00	0.32	0.40	0.49	0.76
3.00	0.47	0.56	0.65	0.93

EON1	EON1	1/7

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
EON1	2-INPUT OR and 2-INPUT NAND into 2-INPUT NAND	3	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT
A	B	C	D	Z
L	L	L	L	H
L	L	L	H	H
L	L	H	L	H
L	L	H	H	H
L	H	H	H	H
H	L	H	H	H
H	H	H	H	H
ALL OTHER COMBINATIONS				L

Verilog-HDL DESCRIPTION

```
EON1  inst(Z,A,B,C,D);
```

VHDL DESCRIPTION

```
inst:EON1
  port  map(Z,A,B,C,D);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.03
B	1.12
C	1.00
D	1.05

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	22.8

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&C&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1782	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.44	0.75	1.98
0.38	0.20	0.45	0.77	2.00
1.00	0.25	0.51	0.82	2.04
3.00	0.36	0.66	0.99	2.23

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&C&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0749	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.29	0.49	1.33
0.38	0.19	0.37	0.58	1.42
1.00	0.25	0.48	0.71	1.56
3.00	0.33	0.67	0.98	1.97

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&~C&D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1782	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.44	0.75	1.98
0.38	0.20	0.45	0.77	2.00
1.00	0.25	0.51	0.82	2.04
3.00	0.36	0.66	0.99	2.23

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&~C&D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0749	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.29	0.49	1.33
0.38	0.19	0.37	0.58	1.42
1.00	0.25	0.48	0.71	1.56
3.00	0.33	0.67	0.98	1.97

EON1 EON1 3/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&~C&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1782	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.44	0.75	1.98
0.38	0.20	0.45	0.77	2.00
1.00	0.25	0.51	0.82	2.04
3.00	0.36	0.66	0.99	2.23

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&~C&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0749	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.29	0.49	1.33
0.38	0.19	0.37	0.58	1.42
1.00	0.25	0.48	0.71	1.56
3.00	0.33	0.67	0.98	1.97

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&C&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1782	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.46	0.77	2.01
0.38	0.21	0.46	0.78	2.02
1.00	0.22	0.47	0.78	2.01
3.00	0.25	0.53	0.84	2.06

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&C&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0749	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.31	0.52	1.35
0.38	0.21	0.39	0.60	1.44
1.00	0.28	0.50	0.73	1.58
3.00	0.40	0.71	1.02	1.99

EON1 EON1 4/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&~C&D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1782	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.46	0.77	2.01
0.38	0.21	0.46	0.78	2.02
1.00	0.22	0.47	0.78	2.01
3.00	0.25	0.53	0.84	2.06

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&~C&D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0749	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.31	0.52	1.35
0.38	0.21	0.39	0.60	1.44
1.00	0.28	0.50	0.73	1.58
3.00	0.40	0.71	1.02	1.99

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&~C&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1782	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.46	0.77	2.01
0.38	0.21	0.46	0.78	2.02
1.00	0.22	0.47	0.78	2.01
3.00	0.25	0.53	0.84	2.06

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&~C&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0749	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.31	0.52	1.35
0.38	0.21	0.39	0.60	1.44
1.00	0.28	0.50	0.73	1.58
3.00	0.40	0.71	1.02	1.99

EON1 EON1 5/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1782	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.38	0.55	1.18
0.38	0.32	0.45	0.62	1.26
1.00	0.39	0.52	0.69	1.33
3.00	0.54	0.68	0.85	1.50

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0749	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.37	0.53	1.18
0.38	0.27	0.40	0.56	1.21
1.00	0.31	0.44	0.61	1.25
3.00	0.38	0.52	0.68	1.33

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1782	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.37	0.53	1.17
0.38	0.30	0.44	0.60	1.24
1.00	0.37	0.51	0.67	1.32
3.00	0.52	0.66	0.83	1.48

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0749	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.42	0.63	1.47
0.38	0.28	0.45	0.66	1.50
1.00	0.32	0.49	0.70	1.54
3.00	0.38	0.56	0.77	1.60

EON1 EON1 6/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1782	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.38	0.54	1.18
0.38	0.32	0.45	0.61	1.25
1.00	0.38	0.52	0.69	1.33
3.00	0.53	0.68	0.84	1.50

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0749	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.45	0.66	1.49
0.38	0.30	0.48	0.69	1.52
1.00	0.34	0.51	0.72	1.56
3.00	0.41	0.58	0.79	1.63

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1782	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.40	0.56	1.20
0.38	0.31	0.45	0.61	1.25
1.00	0.37	0.51	0.67	1.31
3.00	0.48	0.62	0.79	1.44

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0749	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.41	0.57	1.21
0.38	0.30	0.44	0.60	1.24
1.00	0.36	0.49	0.66	1.30
3.00	0.48	0.62	0.79	1.43

EON1 EON1 7/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1782	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.38	0.55	1.19
0.38	0.30	0.44	0.60	1.24
1.00	0.36	0.49	0.66	1.30
3.00	0.46	0.60	0.77	1.43

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0749	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.46	0.67	1.50
0.38	0.31	0.49	0.70	1.53
1.00	0.37	0.54	0.75	1.59
3.00	0.49	0.66	0.87	1.71

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1782	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.40	0.56	1.20
0.38	0.31	0.45	0.61	1.25
1.00	0.37	0.51	0.67	1.31
3.00	0.47	0.62	0.78	1.44

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&~A&B	FALL

SLEW FACTOR

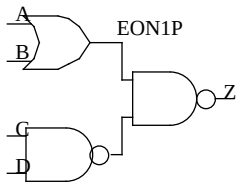
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0749	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.48	0.69	1.53
0.38	0.34	0.51	0.72	1.56
1.00	0.39	0.56	0.77	1.61
3.00	0.51	0.68	0.89	1.73

EON1P	EON1P	1/7

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
EON1P	2-INPUT OR and 2-INPUT NAND into 2-INPUT NAND	4	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT
A	B	C	D	Z
L	L	L	L	H
L	L	L	H	H
L	L	H	L	H
L	L	H	H	H
L	H	H	H	H
H	L	H	H	H
H	H	H	H	H
ALL OTHER COMBINATIONS				L

Verilog-HDL DESCRIPTION

```
EON1P  inst(Z,A,B,C,D);
```

VHDL DESCRIPTION

```
inst:EON1P
   port   map(Z,A,B,C,D);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	2.02
B	1.99
C	1.05
D	1.07

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	39.1

Rev.1.01.10

EON1P | EON1P | 2/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&C&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1051	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.30	0.48	1.20
0.38	0.17	0.32	0.50	1.22
1.00	0.21	0.37	0.55	1.26
3.00	0.31	0.50	0.71	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&C&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0446	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.19	0.32	0.81
0.38	0.16	0.28	0.41	0.90
1.00	0.20	0.36	0.51	1.04
3.00	0.25	0.48	0.70	1.37

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&~C&D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1051	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.30	0.48	1.20
0.38	0.17	0.32	0.50	1.22
1.00	0.21	0.37	0.55	1.26
3.00	0.31	0.50	0.71	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&~C&D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0446	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.19	0.32	0.81
0.38	0.16	0.28	0.41	0.90
1.00	0.20	0.36	0.51	1.04
3.00	0.25	0.48	0.70	1.37

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&~C&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1051	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.30	0.48	1.20
0.38	0.17	0.32	0.50	1.22
1.00	0.21	0.37	0.55	1.26
3.00	0.31	0.50	0.71	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&~C&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0446	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.19	0.32	0.81
0.38	0.16	0.28	0.41	0.90
1.00	0.20	0.36	0.51	1.04
3.00	0.25	0.48	0.70	1.37

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&C&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1051	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.33	0.51	1.22
0.38	0.17	0.32	0.51	1.23
1.00	0.17	0.32	0.50	1.21
3.00	0.16	0.32	0.52	1.23

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&C&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0446	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.22	0.35	0.84
0.38	0.19	0.30	0.43	0.93
1.00	0.24	0.39	0.54	1.07
3.00	0.35	0.55	0.75	1.41

EON1P | EON1P | 4/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&~C&D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1051	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.33	0.51	1.22
0.38	0.17	0.32	0.51	1.23
1.00	0.17	0.32	0.50	1.21
3.00	0.16	0.32	0.52	1.23

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&~C&D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0446	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.22	0.35	0.84
0.38	0.19	0.30	0.43	0.93
1.00	0.24	0.39	0.54	1.07
3.00	0.35	0.55	0.75	1.41

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&~C&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1051	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.33	0.51	1.22
0.38	0.17	0.32	0.51	1.23
1.00	0.17	0.32	0.50	1.21
3.00	0.16	0.32	0.52	1.23

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&~C&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0446	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.22	0.35	0.84
0.38	0.19	0.30	0.43	0.93
1.00	0.24	0.39	0.54	1.07
3.00	0.35	0.55	0.75	1.41

EON1P | EON1P | 5/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1051	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.34	0.44	0.81
0.38	0.34	0.42	0.51	0.88
1.00	0.42	0.50	0.59	0.96
3.00	0.58	0.67	0.76	1.14

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0446	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.34	0.44	0.81
0.38	0.29	0.37	0.47	0.84
1.00	0.34	0.42	0.52	0.89
3.00	0.44	0.53	0.62	1.00

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1051	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.32	0.42	0.79
0.38	0.32	0.40	0.50	0.87
1.00	0.40	0.48	0.58	0.95
3.00	0.56	0.64	0.74	1.12

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0446	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.37	0.50	0.99
0.38	0.30	0.40	0.53	1.02
1.00	0.35	0.45	0.58	1.07
3.00	0.45	0.55	0.68	1.17

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1051	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.34	0.44	0.81
0.38	0.34	0.42	0.51	0.88
1.00	0.42	0.50	0.60	0.97
3.00	0.58	0.66	0.76	1.14

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	D&~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0446	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.40	0.53	1.03
0.38	0.33	0.43	0.56	1.06
1.00	0.38	0.48	0.61	1.11
3.00	0.48	0.58	0.71	1.20

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1051	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.35	0.45	0.82
0.38	0.33	0.41	0.50	0.87
1.00	0.39	0.47	0.56	0.93
3.00	0.50	0.58	0.68	1.06

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0446	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.37	0.47	0.84
0.38	0.32	0.40	0.50	0.87
1.00	0.39	0.47	0.56	0.94
3.00	0.53	0.62	0.72	1.09

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1051	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.34	0.43	0.80
0.38	0.31	0.39	0.49	0.86
1.00	0.37	0.45	0.55	0.92
3.00	0.47	0.56	0.66	1.04

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0446	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.40	0.53	1.03
0.38	0.33	0.43	0.56	1.05
1.00	0.39	0.49	0.62	1.12
3.00	0.54	0.64	0.77	1.26

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1051	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.36	0.45	0.82
0.38	0.33	0.41	0.51	0.87
1.00	0.39	0.47	0.57	0.94
3.00	0.49	0.58	0.68	1.06

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	C&~A&B	FALL

SLEW FACTOR

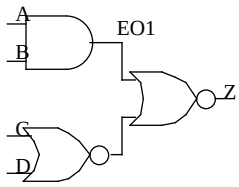
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0446	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.43	0.56	1.06
0.38	0.36	0.46	0.59	1.09
1.00	0.42	0.53	0.65	1.15
3.00	0.57	0.67	0.80	1.29

EO1	EO1	1/7

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
EO1	2-INPUT AND and 2-INPUT NOR into 2-INPUT NOR	3	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT
A	B	C	D	Z
L	L	L	L	L
L	H	L	L	L
H	L	L	L	L
H	H	L	L	L
H	H	L	H	L
H	H	H	L	L
H	H	H	H	L
ALL OTHER COMBINATIONS				H

Verilog-HDL DESCRIPTION

```
EO1  inst(Z,A,B,C,D);
```

VHDL DESCRIPTION

```
inst:EO1
  port   map(Z,A,B,C,D);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.03
B	1.12
C	1.00
D	1.05

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	20.3

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EO1 EO1 2/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&C&D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1953	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.48	0.82	2.18
0.38	0.23	0.50	0.84	2.20
1.00	0.28	0.56	0.89	2.24
3.00	0.44	0.75	1.10	2.43

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&C&D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.26	0.44	1.18
0.38	0.18	0.34	0.53	1.27
1.00	0.23	0.44	0.65	1.41
3.00	0.27	0.59	0.89	1.79

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&C&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1953	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.48	0.82	2.18
0.38	0.23	0.50	0.84	2.20
1.00	0.28	0.56	0.89	2.24
3.00	0.44	0.75	1.10	2.43

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&C&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.26	0.44	1.18
0.38	0.18	0.34	0.53	1.27
1.00	0.23	0.44	0.65	1.41
3.00	0.27	0.59	0.89	1.79

EO1 EO1 3/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~C&D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1953	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.48	0.82	2.18
0.38	0.23	0.50	0.84	2.20
1.00	0.28	0.56	0.89	2.24
3.00	0.44	0.75	1.10	2.43

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~C&D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.26	0.44	1.18
0.38	0.18	0.34	0.53	1.27
1.00	0.23	0.44	0.65	1.41
3.00	0.27	0.59	0.89	1.79

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&C&D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1953	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.53	0.87	2.23
0.38	0.27	0.54	0.88	2.24
1.00	0.34	0.61	0.94	2.28
3.00	0.53	0.82	1.16	2.48

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&C&D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.27	0.46	1.20
0.38	0.17	0.33	0.52	1.26
1.00	0.21	0.40	0.60	1.35
3.00	0.22	0.50	0.77	1.61

EO1 EO1 4/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&C&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1953	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.53	0.87	2.23
0.38	0.27	0.54	0.88	2.24
1.00	0.34	0.61	0.94	2.28
3.00	0.53	0.82	1.16	2.48

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&C&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.27	0.46	1.20
0.38	0.17	0.33	0.52	1.26
1.00	0.21	0.40	0.60	1.35
3.00	0.22	0.50	0.77	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~C&D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1953	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.53	0.87	2.23
0.38	0.27	0.54	0.88	2.24
1.00	0.34	0.61	0.94	2.28
3.00	0.53	0.82	1.16	2.48

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~C&D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.27	0.46	1.20
0.38	0.17	0.33	0.52	1.26
1.00	0.21	0.40	0.60	1.35
3.00	0.22	0.50	0.77	1.61

EO1 EO1 5/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~D&A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1953	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.64	0.98	2.33
0.38	0.42	0.70	1.04	2.39
1.00	0.45	0.72	1.07	2.42
3.00	0.45	0.72	1.07	2.42

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~D&A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.41	0.54	1.00
0.38	0.32	0.43	0.56	1.02
1.00	0.40	0.51	0.64	1.10
3.00	0.60	0.72	0.84	1.32

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~D&~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1953	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.58	0.92	2.28
0.38	0.37	0.64	0.99	2.34
1.00	0.39	0.67	1.01	2.37
3.00	0.40	0.67	1.01	2.37

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~D&~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.40	0.52	0.99
0.38	0.30	0.42	0.55	1.01
1.00	0.38	0.50	0.62	1.09
3.00	0.58	0.70	0.83	1.30

EO1 EO1 6/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~D&~A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1953	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.48	0.74	1.77
0.38	0.33	0.54	0.80	1.83
1.00	0.36	0.57	0.83	1.86
3.00	0.36	0.58	0.84	1.87

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~D&~A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.41	0.53	1.00
0.38	0.32	0.43	0.55	1.02
1.00	0.39	0.51	0.63	1.10
3.00	0.60	0.71	0.84	1.31

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~C&A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1953	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.65	0.99	2.34
0.38	0.43	0.71	1.05	2.41
1.00	0.47	0.75	1.09	2.45
3.00	0.52	0.80	1.14	2.49

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~C&A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.44	0.56	1.03
0.38	0.32	0.43	0.56	1.02
1.00	0.36	0.48	0.60	1.07
3.00	0.50	0.62	0.75	1.22

EO1 EO1 7/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~C&~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1953	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.59	0.94	2.29
0.38	0.38	0.66	1.00	2.36
1.00	0.42	0.70	1.04	2.40
3.00	0.47	0.74	1.08	2.44

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~C&~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.42	0.55	1.01
0.38	0.31	0.42	0.55	1.01
1.00	0.35	0.46	0.59	1.06
3.00	0.48	0.61	0.74	1.21

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~C&~A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1953	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.49	0.75	1.78
0.38	0.34	0.55	0.81	1.84
1.00	0.39	0.60	0.86	1.89
3.00	0.44	0.65	0.91	1.94

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~C&~A&~B	FALL

SLEW FACTOR

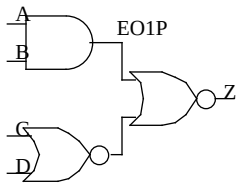
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0655	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.43	0.56	1.02
0.38	0.32	0.43	0.56	1.02
1.00	0.36	0.47	0.60	1.07
3.00	0.49	0.62	0.75	1.22

EO1P	EO1P	1/7

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
EO1P	2-INPUT AND and 2-INPUT NOR into 2-INPUT NOR	4	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT
A	B	C	D	Z
L	L	L	L	L
L	H	L	L	L
H	L	L	L	L
H	H	L	L	L
H	H	L	H	L
H	H	H	L	L
H	H	H	H	L
ALL OTHER COMBINATIONS				H

Verilog-HDL DESCRIPTION

```
EO1P  inst(Z,A,B,C,D);
```

VHDL DESCRIPTION

```
inst:EO1P
  port   map(Z,A,B,C,D);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	2.02
B	1.99
C	1.05
D	1.07

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	35.6

Rev.1.01.10

EO1P | EO1P | 2/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&C&D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1115	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.31	0.50	1.27
0.38	0.17	0.33	0.52	1.29
1.00	0.22	0.38	0.58	1.33
3.00	0.34	0.54	0.75	1.53

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&C&D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0410	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.18	0.30	0.76
0.38	0.15	0.26	0.38	0.85
1.00	0.19	0.34	0.49	0.98
3.00	0.21	0.44	0.66	1.30

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&C&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1115	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.31	0.50	1.27
0.38	0.17	0.33	0.52	1.29
1.00	0.22	0.38	0.58	1.33
3.00	0.34	0.54	0.75	1.53

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&C&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0410	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.18	0.30	0.76
0.38	0.15	0.26	0.38	0.85
1.00	0.19	0.34	0.49	0.98
3.00	0.21	0.44	0.66	1.30

EO1P | EO1P | 3/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~C&D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1115	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.31	0.50	1.27
0.38	0.17	0.33	0.52	1.29
1.00	0.22	0.38	0.58	1.33
3.00	0.34	0.54	0.75	1.53

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~C&D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0410	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.18	0.30	0.76
0.38	0.15	0.26	0.38	0.85
1.00	0.19	0.34	0.49	0.98
3.00	0.21	0.44	0.66	1.30

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&C&D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1115	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.38	0.57	1.33
0.38	0.23	0.39	0.58	1.34
1.00	0.30	0.45	0.64	1.39
3.00	0.49	0.66	0.85	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&C&D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0410	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.20	0.31	0.78
0.38	0.15	0.24	0.36	0.83
1.00	0.17	0.29	0.42	0.89
3.00	0.13	0.31	0.49	1.05

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&C&~D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1115	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.38	0.57	1.33
0.38	0.23	0.39	0.58	1.34
1.00	0.30	0.45	0.64	1.39
3.00	0.49	0.66	0.85	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&C&~D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0410	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.20	0.31	0.78
0.38	0.15	0.24	0.36	0.83
1.00	0.17	0.29	0.42	0.89
3.00	0.13	0.31	0.49	1.05

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~C&D	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1115	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.38	0.57	1.33
0.38	0.23	0.39	0.58	1.34
1.00	0.30	0.45	0.64	1.39
3.00	0.49	0.66	0.85	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~C&D	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0410	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.20	0.31	0.78
0.38	0.15	0.24	0.36	0.83
1.00	0.17	0.29	0.42	0.89
3.00	0.13	0.31	0.49	1.05

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~D&A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1115	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.50	0.70	1.46
0.38	0.41	0.57	0.77	1.53
1.00	0.46	0.62	0.81	1.58
3.00	0.50	0.66	0.85	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~D&A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0410	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.42	0.50	0.80
0.38	0.36	0.44	0.52	0.82
1.00	0.44	0.52	0.60	0.90
3.00	0.65	0.73	0.82	1.12

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~D&~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1115	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.43	0.63	1.39
0.38	0.34	0.50	0.69	1.46
1.00	0.39	0.55	0.74	1.51
3.00	0.43	0.59	0.78	1.54

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~D&~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0410	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.40	0.48	0.78
0.38	0.34	0.42	0.50	0.80
1.00	0.42	0.50	0.58	0.88
3.00	0.62	0.71	0.80	1.10

EO1P | EO1P | 6/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~D&~A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1115	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.37	0.52	1.09
0.38	0.32	0.44	0.59	1.16
1.00	0.36	0.49	0.63	1.21
3.00	0.41	0.53	0.68	1.26

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~D&~A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0410	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.41	0.50	0.79
0.38	0.36	0.43	0.51	0.81
1.00	0.44	0.51	0.60	0.89
3.00	0.65	0.73	0.81	1.11

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~C&A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1115	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.51	0.71	1.47
0.38	0.42	0.58	0.78	1.54
1.00	0.48	0.64	0.84	1.60
3.00	0.57	0.72	0.92	1.68

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~C&A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0410	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.44	0.52	0.82
0.38	0.36	0.44	0.52	0.82
1.00	0.40	0.48	0.56	0.86
3.00	0.53	0.61	0.70	1.01

EO1P | EO1P | 7/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~C&~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1115	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.44	0.64	1.40
0.38	0.35	0.51	0.71	1.47
1.00	0.41	0.57	0.76	1.53
3.00	0.50	0.66	0.84	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~C&~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0410	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.42	0.50	0.80
0.38	0.34	0.42	0.50	0.80
1.00	0.37	0.46	0.54	0.84
3.00	0.50	0.59	0.68	0.99

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~C&~A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1115	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.38	0.53	1.10
0.38	0.33	0.45	0.60	1.18
1.00	0.39	0.51	0.66	1.24
3.00	0.48	0.60	0.75	1.32

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	~C&~A&~B	FALL

SLEW FACTOR

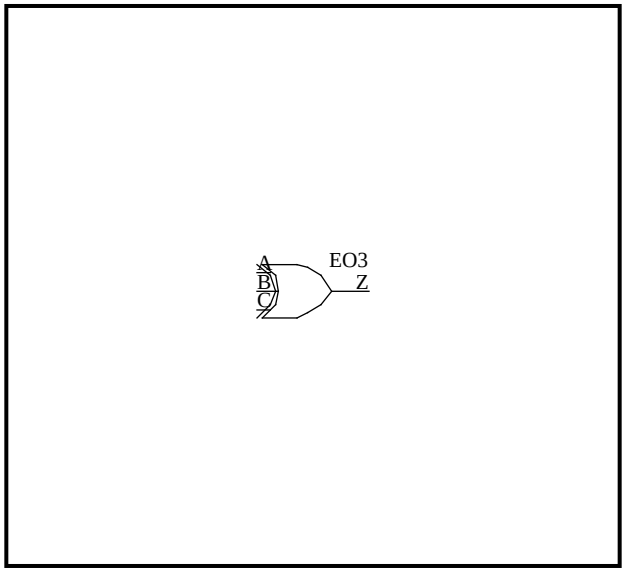
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0410	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.43	0.52	0.81
0.38	0.35	0.43	0.51	0.81
1.00	0.39	0.47	0.55	0.85
3.00	0.53	0.61	0.70	1.00

EO3	EO3	1/7

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
EO3	3-INPUT EXCLUSIVE OR	7	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
A	B	C	Z
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	H

Verilog-HDL DESCRIPTION

```
EO3  inst(Z,A,B,C);
```

VHDL DESCRIPTION

```
inst:EO3
  port  map(Z,A,B,C);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.04
B	3.30
C	2.00

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	48.9

Rev.1.01.10

EO3 EO3 2/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0841	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.57	0.73	1.34
0.38	0.50	0.65	0.81	1.42
1.00	0.61	0.76	0.92	1.53
3.00	0.82	0.97	1.13	1.74

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0375	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.50	0.66	0.82	1.31
0.38	0.53	0.69	0.85	1.34
1.00	0.60	0.77	0.92	1.42
3.00	0.79	0.96	1.12	1.63

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0841	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.71	0.85	1.01	1.62
0.38	0.74	0.88	1.04	1.65
1.00	0.81	0.96	1.12	1.73
3.00	0.99	1.14	1.30	1.91

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0375	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.61	0.76	0.92	1.40
0.38	0.69	0.85	1.00	1.49
1.00	0.80	0.95	1.11	1.59
3.00	0.98	1.14	1.29	1.78

EO3 EO3 3/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0841	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.71	0.86	1.02	1.63
0.38	0.75	0.89	1.05	1.66
1.00	0.82	0.97	1.13	1.74
3.00	1.00	1.15	1.31	1.92

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0375	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.61	0.77	0.92	1.41
0.38	0.70	0.86	1.01	1.50
1.00	0.80	0.96	1.11	1.60
3.00	0.99	1.15	1.30	1.79

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0841	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.57	0.73	1.33
0.38	0.50	0.65	0.81	1.42
1.00	0.61	0.75	0.91	1.52
3.00	0.82	0.96	1.12	1.73

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&~C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0375	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.65	0.81	1.30
0.38	0.52	0.68	0.84	1.33
1.00	0.59	0.76	0.92	1.41
3.00	0.78	0.95	1.12	1.62

EO3 EO3 4/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0841	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.47	0.63	1.24
0.38	0.41	0.55	0.71	1.32
1.00	0.49	0.64	0.80	1.41
3.00	0.62	0.76	0.92	1.53

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0375	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.57	0.72	1.21
0.38	0.44	0.60	0.75	1.23
1.00	0.51	0.67	0.82	1.30
3.00	0.68	0.84	1.00	1.49

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0841	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.43	0.57	0.73	1.34
0.38	0.46	0.60	0.76	1.37
1.00	0.52	0.67	0.83	1.43
3.00	0.66	0.80	0.96	1.57

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0375	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.47	0.63	1.12
0.38	0.40	0.56	0.71	1.20
1.00	0.54	0.69	0.84	1.33
3.00	0.69	0.85	1.00	1.48

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0841	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.60	0.77	1.37
0.38	0.49	0.63	0.80	1.40
1.00	0.55	0.70	0.86	1.47
3.00	0.69	0.83	0.99	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0375	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.45	0.61	1.09
0.38	0.39	0.54	0.70	1.18
1.00	0.53	0.68	0.83	1.31
3.00	0.67	0.82	0.97	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0841	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.50	0.66	1.27
0.38	0.43	0.58	0.74	1.35
1.00	0.52	0.67	0.83	1.44
3.00	0.67	0.81	0.98	1.59

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&~C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0375	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.39	0.54	0.69	1.17
0.38	0.41	0.56	0.71	1.19
1.00	0.48	0.63	0.78	1.26
3.00	0.64	0.80	0.95	1.44

EO3 EO3 6/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0841	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.35	0.51	1.11
0.38	0.28	0.43	0.59	1.19
1.00	0.35	0.50	0.66	1.27
3.00	0.48	0.62	0.78	1.39

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0375	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.35	0.49	0.95
0.38	0.26	0.39	0.52	0.99
1.00	0.32	0.45	0.59	1.06
3.00	0.47	0.61	0.75	1.22

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0841	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.45	0.61	1.21
0.38	0.34	0.48	0.64	1.25
1.00	0.39	0.54	0.70	1.30
3.00	0.51	0.65	0.81	1.41

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0375	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.36	0.51	0.99
0.38	0.30	0.45	0.59	1.07
1.00	0.44	0.58	0.72	1.19
3.00	0.56	0.70	0.84	1.31

EO3 EO3 7/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0841	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.46	0.62	1.23
0.38	0.35	0.49	0.65	1.26
1.00	0.40	0.55	0.71	1.32
3.00	0.52	0.66	0.82	1.43

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0375	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.35	0.49	0.97
0.38	0.30	0.44	0.58	1.05
1.00	0.43	0.57	0.70	1.17
3.00	0.55	0.68	0.82	1.28

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0841	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.36	0.52	1.12
0.38	0.29	0.44	0.60	1.21
1.00	0.37	0.51	0.67	1.28
3.00	0.51	0.65	0.81	1.42

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&~B	FALL

SLEW FACTOR

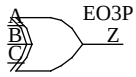
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0375	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.35	0.48	0.94
0.38	0.26	0.38	0.52	0.98
1.00	0.32	0.45	0.58	1.04
3.00	0.46	0.60	0.74	1.20

EO3P	EO3P	1/7

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
EO3P	3-INPUT EXCLUSIVE OR	7	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
A	B	C	Z
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	H

Verilog-HDL DESCRIPTION

```
EO3P  inst(Z,A,B,C);
```

VHDL DESCRIPTION

```
inst:EO3P
   port   map(Z,A,B,C);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.04
B	3.30
C	2.00

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	82.1

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0481	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.54	0.64	0.99
0.38	0.53	0.62	0.72	1.08
1.00	0.64	0.72	0.82	1.18
3.00	0.86	0.95	1.04	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0247	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.63	0.73	1.07
0.38	0.54	0.65	0.76	1.10
1.00	0.62	0.73	0.84	1.17
3.00	0.81	0.93	1.04	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0481	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.73	0.82	0.92	1.28
0.38	0.76	0.85	0.95	1.31
1.00	0.84	0.93	1.03	1.39
3.00	1.02	1.11	1.21	1.57

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0247	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.62	0.73	0.83	1.16
0.38	0.71	0.81	0.92	1.25
1.00	0.81	0.92	1.02	1.35
3.00	1.00	1.10	1.21	1.54

EO3P | EO3P | 3/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0481	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.74	0.83	0.93	1.29
0.38	0.77	0.86	0.96	1.32
1.00	0.85	0.94	1.04	1.40
3.00	1.03	1.12	1.22	1.58

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0247	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.63	0.74	0.84	1.17
0.38	0.72	0.82	0.93	1.26
1.00	0.82	0.93	1.03	1.36
3.00	1.01	1.11	1.22	1.55

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0481	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.53	0.63	0.99
0.38	0.53	0.62	0.71	1.07
1.00	0.63	0.72	0.82	1.18
3.00	0.85	0.94	1.04	1.39

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&~C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0247	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.50	0.62	0.72	1.06
0.38	0.53	0.65	0.75	1.09
1.00	0.61	0.72	0.83	1.16
3.00	0.80	0.92	1.03	1.37

EO3P | EO3P | 4/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0481	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.44	0.54	0.90
0.38	0.44	0.52	0.62	0.98
1.00	0.53	0.62	0.72	1.07
3.00	0.67	0.76	0.86	1.21

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0247	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.43	0.54	0.64	0.97
0.38	0.45	0.56	0.67	1.00
1.00	0.52	0.63	0.73	1.06
3.00	0.70	0.80	0.91	1.24

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0481	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.54	0.64	1.00
0.38	0.48	0.57	0.67	1.03
1.00	0.55	0.63	0.73	1.09
3.00	0.68	0.76	0.86	1.22

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0247	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.44	0.55	0.88
0.38	0.41	0.52	0.62	0.95
1.00	0.55	0.66	0.76	1.09
3.00	0.73	0.84	0.94	1.27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0481	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.58	0.68	1.04
0.38	0.52	0.61	0.70	1.06
1.00	0.58	0.67	0.77	1.12
3.00	0.71	0.79	0.89	1.25

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0247	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.42	0.52	0.85
0.38	0.40	0.51	0.61	0.94
1.00	0.54	0.65	0.75	1.08
3.00	0.70	0.81	0.91	1.24

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&~C	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0481	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.38	0.47	0.57	0.93
0.38	0.47	0.55	0.65	1.01
1.00	0.56	0.65	0.75	1.11
3.00	0.73	0.82	0.92	1.28

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&~C	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0247	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.40	0.50	0.60	0.93
0.38	0.42	0.53	0.63	0.95
1.00	0.49	0.59	0.70	1.02
3.00	0.65	0.76	0.87	1.20

EO3P | EO3P | 6/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0481	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.32	0.42	0.78
0.38	0.31	0.40	0.50	0.86
1.00	0.40	0.49	0.59	0.94
3.00	0.57	0.65	0.75	1.10

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0247	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.32	0.42	0.73
0.38	0.26	0.36	0.45	0.77
1.00	0.33	0.42	0.52	0.83
3.00	0.48	0.58	0.68	1.00

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0481	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.41	0.51	0.87
0.38	0.36	0.45	0.54	0.90
1.00	0.41	0.50	0.60	0.96
3.00	0.53	0.62	0.72	1.07

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0247	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.32	0.43	0.75
0.38	0.31	0.41	0.51	0.83
1.00	0.45	0.56	0.65	0.97
3.00	0.62	0.72	0.82	1.13

EO3P | EO3P | 7/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0481	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.43	0.53	0.89
0.38	0.37	0.46	0.56	0.92
1.00	0.43	0.52	0.62	0.98
3.00	0.54	0.63	0.73	1.09

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0247	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.31	0.41	0.73
0.38	0.30	0.40	0.50	0.82
1.00	0.45	0.55	0.64	0.96
3.00	0.60	0.70	0.79	1.10

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0481	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.33	0.43	0.79
0.38	0.32	0.41	0.51	0.87
1.00	0.42	0.50	0.60	0.96
3.00	0.60	0.68	0.78	1.13

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	~A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0247	0.13

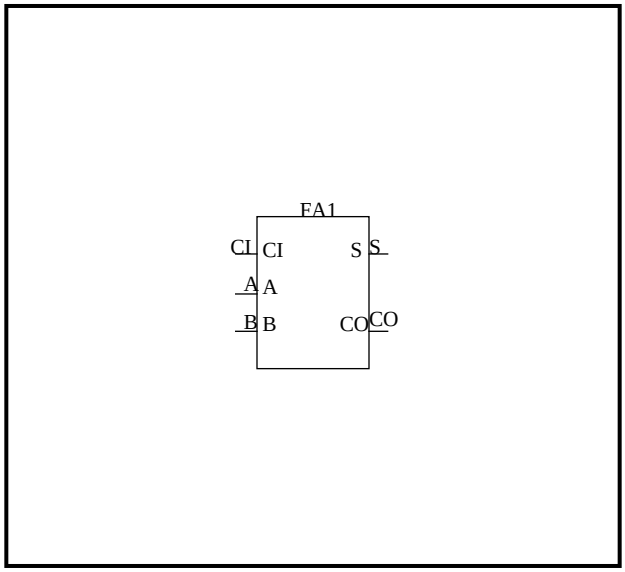
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.32	0.41	0.72
0.38	0.26	0.36	0.45	0.76
1.00	0.33	0.42	0.51	0.82
3.00	0.47	0.57	0.67	0.98

Rev.1.01.10

FA1	FA1	1/10

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FA1	FULL ADDER	9	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT	
CI	A	B	S	CO
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

Verilog-HDL DESCRIPTION

```
FA1  inst(S,CO,CI,A,B);
```

VHDL DESCRIPTION

```
inst:FA1
  port  map(S,CO,CI,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	S,CO
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
CI	4.46
A	3.05
B	4.50

OUTPUT DRIVE (LU)

PIN NAME	S	CO
DRIVE	43.0	46.3

Rev.1.01.10

FA1 FA1 2/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->CO	B&~CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0882	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.41	0.57	1.19
0.38	0.33	0.46	0.62	1.24
1.00	0.40	0.54	0.70	1.31
3.00	0.51	0.65	0.82	1.44

PATH CONDITION

PATH	CONDITION	FUNCTION
A->CO	B&~CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0398	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.61	0.76	1.27
0.38	0.45	0.60	0.75	1.26
1.00	0.48	0.64	0.79	1.30
3.00	0.64	0.80	0.95	1.47

PATH CONDITION

PATH	CONDITION	FUNCTION
A->CO	~B&CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0882	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.43	0.59	1.21
0.38	0.34	0.49	0.65	1.27
1.00	0.42	0.56	0.73	1.35
3.00	0.57	0.71	0.88	1.50

PATH CONDITION

PATH	CONDITION	FUNCTION
A->CO	~B&CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0398	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.64	0.78	1.28
0.38	0.48	0.63	0.77	1.27
1.00	0.50	0.66	0.80	1.30
3.00	0.64	0.79	0.94	1.45

FA1 FA1 3/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	B&CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.1000	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.61	0.76	0.94	1.63
0.38	0.68	0.83	1.01	1.70
1.00	0.74	0.90	1.08	1.77
3.00	0.85	1.00	1.18	1.87

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	B&CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0400	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.64	0.79	0.93	1.43
0.38	0.68	0.83	0.97	1.46
1.00	0.74	0.89	1.03	1.53
3.00	0.87	1.02	1.16	1.66

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	B&~CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.1000	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.70	0.85	1.03	1.72
0.38	0.74	0.89	1.06	1.75
1.00	0.80	0.95	1.13	1.81
3.00	0.93	1.08	1.26	1.94

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	B&~CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0400	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.67	0.81	0.94	1.43
0.38	0.74	0.88	1.01	1.50
1.00	0.81	0.94	1.08	1.56
3.00	0.91	1.05	1.18	1.67

FA1 FA1 4/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	~B&CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.1000	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.59	0.74	0.92	1.61
0.38	0.62	0.77	0.95	1.64
1.00	0.70	0.85	1.03	1.72
3.00	0.87	1.03	1.20	1.89

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	~B&CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0400	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.53	0.68	0.82	1.32
0.38	0.61	0.76	0.90	1.40
1.00	0.70	0.85	0.99	1.49
3.00	0.87	1.01	1.16	1.65

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	~B&~CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.1000	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.59	0.74	0.92	1.60
0.38	0.67	0.82	0.99	1.68
1.00	0.76	0.91	1.08	1.77
3.00	0.92	1.07	1.25	1.93

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	~B&~CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0400	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.65	0.78	0.92	1.40
0.38	0.68	0.81	0.95	1.43
1.00	0.76	0.89	1.03	1.51
3.00	0.93	1.06	1.20	1.68

FA1 FA1 5/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->CO	A&~CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0882	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.40	0.55	1.16
0.38	0.36	0.49	0.64	1.25
1.00	0.46	0.59	0.75	1.35
3.00	0.65	0.79	0.94	1.55

PATH CONDITION

PATH	CONDITION	FUNCTION
B->CO	A&~CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0398	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.38	0.53	0.68	1.19
0.38	0.37	0.52	0.67	1.19
1.00	0.40	0.56	0.71	1.22
3.00	0.51	0.67	0.82	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION
B->CO	~A&CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0882	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.41	0.57	1.19
0.38	0.33	0.47	0.63	1.24
1.00	0.39	0.53	0.69	1.31
3.00	0.49	0.63	0.80	1.42

PATH CONDITION

PATH	CONDITION	FUNCTION
B->CO	~A&CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0398	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.50	0.65	0.79	1.29
0.38	0.50	0.65	0.80	1.29
1.00	0.57	0.72	0.86	1.36
3.00	0.79	0.94	1.09	1.60

FA1 FA1 6/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	A&CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.1000	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.63	0.81	1.50
0.38	0.56	0.71	0.89	1.58
1.00	0.67	0.82	1.00	1.69
3.00	0.80	0.95	1.13	1.82

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	A&CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0400	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.56	0.71	0.85	1.35
0.38	0.60	0.74	0.88	1.38
1.00	0.66	0.80	0.94	1.44
3.00	0.77	0.92	1.06	1.56

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	A&~CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.1000	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.62	0.77	0.94	1.63
0.38	0.65	0.80	0.98	1.66
1.00	0.71	0.86	1.04	1.72
3.00	0.82	0.97	1.15	1.84

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	A&~CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0400	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.54	0.68	0.81	1.30
0.38	0.63	0.76	0.89	1.38
1.00	0.73	0.87	1.00	1.49
3.00	0.86	1.00	1.13	1.62

FA1 FA1 7/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	~A&CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.1000	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.64	0.82	1.51
0.38	0.51	0.67	0.85	1.54
1.00	0.58	0.73	0.91	1.60
3.00	0.74	0.89	1.07	1.76

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	~A&CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0400	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.59	0.74	1.23
0.38	0.52	0.67	0.81	1.31
1.00	0.58	0.73	0.87	1.37
3.00	0.68	0.82	0.97	1.46

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	~A&~CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.1000	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.66	0.83	1.52
0.38	0.58	0.73	0.91	1.59
1.00	0.64	0.79	0.97	1.65
3.00	0.73	0.88	1.06	1.75

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	~A&~CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0400	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.68	0.82	1.30
0.38	0.58	0.71	0.85	1.34
1.00	0.65	0.78	0.92	1.40
3.00	0.80	0.94	1.07	1.56

FA1 FA1 8/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->CO	A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0882	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.42	0.58	1.20
0.38	0.37	0.51	0.67	1.29
1.00	0.46	0.61	0.77	1.39
3.00	0.62	0.77	0.93	1.56

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->CO	A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0398	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.39	0.54	0.69	1.21
0.38	0.40	0.56	0.71	1.22
1.00	0.48	0.63	0.78	1.29
3.00	0.66	0.82	0.97	1.50

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->CO	~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0882	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.42	0.58	1.20
0.38	0.36	0.51	0.67	1.29
1.00	0.45	0.60	0.76	1.39
3.00	0.61	0.75	0.92	1.55

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->CO	~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0398	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.61	0.76	1.27
0.38	0.47	0.63	0.78	1.29
1.00	0.54	0.69	0.84	1.35
3.00	0.74	0.90	1.05	1.57

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.1000	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.33	0.51	1.19
0.38	0.27	0.41	0.59	1.27
1.00	0.33	0.48	0.65	1.33
3.00	0.43	0.58	0.76	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0400	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.36	0.49	0.97
0.38	0.26	0.39	0.52	1.00
1.00	0.33	0.45	0.58	1.06
3.00	0.47	0.60	0.73	1.22

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.1000	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.45	0.63	1.32
0.38	0.34	0.49	0.66	1.35
1.00	0.40	0.55	0.72	1.41
3.00	0.52	0.67	0.85	1.52

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0400	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.35	0.49	0.98
0.38	0.31	0.44	0.58	1.07
1.00	0.42	0.54	0.68	1.16
3.00	0.53	0.66	0.80	1.28

FA1 FA1 10/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.1000	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.45	0.63	1.32
0.38	0.34	0.49	0.66	1.35
1.00	0.40	0.55	0.72	1.41
3.00	0.52	0.67	0.85	1.52

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0400	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.35	0.49	0.98
0.38	0.31	0.44	0.58	1.07
1.00	0.42	0.54	0.68	1.16
3.00	0.53	0.66	0.80	1.28

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	~A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.1000	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.33	0.51	1.19
0.38	0.27	0.41	0.59	1.27
1.00	0.33	0.48	0.65	1.33
3.00	0.43	0.58	0.76	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	~A&~B	FALL

SLEW FACTOR

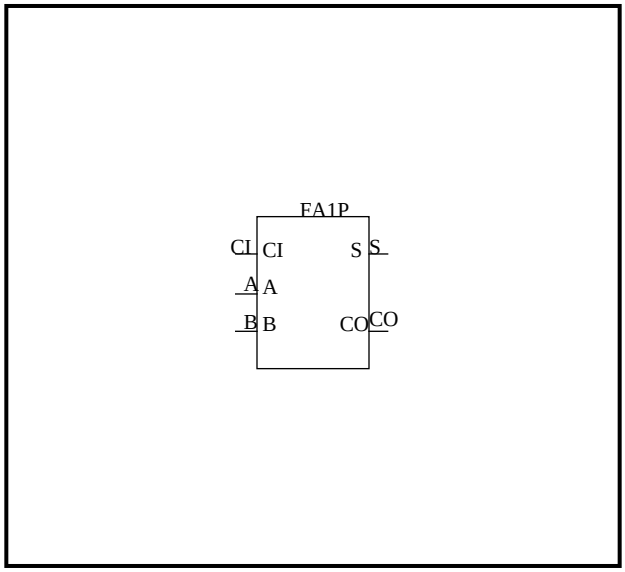
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0400	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.36	0.49	0.97
0.38	0.26	0.39	0.52	1.00
1.00	0.33	0.45	0.58	1.06
3.00	0.47	0.60	0.73	1.22

FA1P	FA1P	1/10

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FA1P	FULL ADDER	10	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT	
CI	A	B	S	CO
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

Verilog-HDL DESCRIPTION

```
FA1P  inst(S,CO,CI,A,B);
```

VHDL DESCRIPTION

```
inst:FA1P
  port  map(S,CO,CI,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	S	CO
ELECTRO MIGRATION DRIVE	6880.0	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
CI	4.46
A	3.04
B	4.54

OUTPUT DRIVE (LU)

PIN NAME	S	CO
DRIVE	85.8	93.2

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->CO	B&~CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0438	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.35	0.43	0.75
0.38	0.33	0.40	0.49	0.81
1.00	0.40	0.48	0.56	0.88
3.00	0.54	0.62	0.70	1.02

PATH CONDITION

PATH	CONDITION	FUNCTION
A->CO	B&~CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0196	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.47	0.56	0.65	0.94
0.38	0.46	0.56	0.65	0.93
1.00	0.49	0.59	0.68	0.96
3.00	0.65	0.75	0.84	1.13

PATH CONDITION

PATH	CONDITION	FUNCTION
A->CO	~B&CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0438	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.37	0.45	0.78
0.38	0.34	0.42	0.51	0.83
1.00	0.43	0.51	0.59	0.92
3.00	0.59	0.67	0.76	1.09

PATH CONDITION

PATH	CONDITION	FUNCTION
A->CO	~B&CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0196	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.58	0.67	0.95
0.38	0.48	0.58	0.67	0.94
1.00	0.51	0.60	0.69	0.96
3.00	0.64	0.74	0.83	1.11

FA1P | FA1P | 3/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	B&CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0487	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.62	0.70	0.80	1.15
0.38	0.69	0.77	0.87	1.23
1.00	0.75	0.84	0.93	1.29
3.00	0.86	0.94	1.04	1.39

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	B&CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0223	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.66	0.75	0.85	1.14
0.38	0.69	0.79	0.88	1.18
1.00	0.75	0.85	0.94	1.24
3.00	0.88	0.98	1.07	1.37

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	B&~CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0487	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.71	0.79	0.88	1.24
0.38	0.74	0.82	0.92	1.27
1.00	0.80	0.89	0.98	1.33
3.00	0.93	1.02	1.11	1.46

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	B&~CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0223	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.68	0.77	0.86	1.14
0.38	0.75	0.84	0.93	1.21
1.00	0.82	0.90	0.99	1.28
3.00	0.92	1.01	1.10	1.38

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	~B&CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0487	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.60	0.68	0.78	1.13
0.38	0.63	0.72	0.81	1.17
1.00	0.71	0.79	0.89	1.24
3.00	0.88	0.97	1.06	1.42

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	~B&CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0223	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.64	0.74	1.03
0.38	0.63	0.72	0.81	1.11
1.00	0.71	0.81	0.90	1.20
3.00	0.88	0.98	1.07	1.37

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	~B&~CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0487	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.59	0.68	0.77	1.12
0.38	0.67	0.76	0.85	1.20
1.00	0.76	0.85	0.94	1.29
3.00	0.93	1.01	1.10	1.46

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	~B&~CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0223	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.66	0.75	0.83	1.12
0.38	0.69	0.78	0.87	1.15
1.00	0.77	0.86	0.94	1.23
3.00	0.94	1.02	1.11	1.40

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->CO	A&~CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0438	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.35	0.43	0.75
0.38	0.36	0.43	0.52	0.84
1.00	0.47	0.55	0.63	0.95
3.00	0.69	0.77	0.85	1.17

PATH CONDITION

PATH	CONDITION	FUNCTION
B->CO	A&~CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0196	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.39	0.49	0.58	0.86
0.38	0.39	0.48	0.57	0.85
1.00	0.42	0.51	0.60	0.88
3.00	0.53	0.63	0.72	1.01

PATH CONDITION

PATH	CONDITION	FUNCTION
B->CO	~A&CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0438	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.36	0.45	0.77
0.38	0.34	0.42	0.51	0.83
1.00	0.40	0.49	0.58	0.91
3.00	0.53	0.61	0.70	1.03

PATH CONDITION

PATH	CONDITION	FUNCTION
B->CO	~A&CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0196	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.61	0.69	0.97
0.38	0.52	0.61	0.70	0.97
1.00	0.58	0.67	0.76	1.03
3.00	0.81	0.91	1.00	1.28

FA1P | FA1P | 6/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	A&CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0487	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.57	0.66	1.02
0.38	0.56	0.65	0.75	1.10
1.00	0.67	0.76	0.85	1.21
3.00	0.80	0.88	0.98	1.33

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	A&CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0223	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.57	0.66	0.76	1.05
0.38	0.60	0.70	0.79	1.09
1.00	0.66	0.76	0.85	1.15
3.00	0.78	0.87	0.96	1.26

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	A&~CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0487	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.62	0.70	0.80	1.15
0.38	0.65	0.74	0.83	1.18
1.00	0.71	0.80	0.89	1.24
3.00	0.83	0.91	1.00	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	A&~CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0223	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.64	0.72	1.01
0.38	0.63	0.72	0.81	1.09
1.00	0.74	0.83	0.92	1.20
3.00	0.87	0.96	1.04	1.33

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	~A&CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0487	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.58	0.67	1.03
0.38	0.52	0.61	0.71	1.06
1.00	0.59	0.68	0.77	1.13
3.00	0.75	0.83	0.93	1.29

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	~A&CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0223	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.56	0.65	0.95
0.38	0.54	0.64	0.73	1.03
1.00	0.60	0.70	0.79	1.09
3.00	0.70	0.79	0.89	1.18

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	~A&~CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0487	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.60	0.69	1.04
0.38	0.59	0.67	0.77	1.12
1.00	0.65	0.73	0.83	1.18
3.00	0.74	0.83	0.92	1.27

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	~A&~CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0223	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.56	0.65	0.74	1.02
0.38	0.59	0.68	0.77	1.05
1.00	0.66	0.75	0.83	1.12
3.00	0.81	0.90	0.99	1.27

FA1P | FA1P | 8/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->CO	A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0438	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.36	0.44	0.77
0.38	0.37	0.45	0.53	0.86
1.00	0.47	0.55	0.64	0.97
3.00	0.66	0.74	0.83	1.16

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->CO	A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0196	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.40	0.50	0.58	0.87
0.38	0.41	0.51	0.60	0.88
1.00	0.48	0.58	0.67	0.95
3.00	0.68	0.78	0.87	1.16

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->CO	~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0438	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.35	0.44	0.77
0.38	0.36	0.44	0.53	0.86
1.00	0.46	0.55	0.64	0.96
3.00	0.64	0.73	0.82	1.15

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->CO	~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0196	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.47	0.57	0.66	0.94
0.38	0.48	0.58	0.67	0.95
1.00	0.55	0.64	0.73	1.01
3.00	0.76	0.86	0.95	1.24

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0487	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.29	0.39	0.74
0.38	0.29	0.37	0.47	0.82
1.00	0.37	0.45	0.55	0.90
3.00	0.52	0.60	0.70	1.05

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0223	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.33	0.41	0.69
0.38	0.27	0.36	0.44	0.72
1.00	0.33	0.42	0.51	0.79
3.00	0.48	0.57	0.66	0.95

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0487	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.37	0.47	0.82
0.38	0.32	0.41	0.50	0.85
1.00	0.38	0.46	0.56	0.91
3.00	0.49	0.58	0.67	1.02

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0223	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.30	0.39	0.68
0.38	0.30	0.39	0.48	0.77
1.00	0.43	0.52	0.60	0.89
3.00	0.57	0.66	0.74	1.03

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0487	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.37	0.47	0.82
0.38	0.32	0.41	0.50	0.85
1.00	0.38	0.46	0.56	0.91
3.00	0.49	0.58	0.67	1.02

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0223	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.30	0.39	0.68
0.38	0.30	0.39	0.48	0.77
1.00	0.43	0.52	0.60	0.89
3.00	0.57	0.66	0.74	1.03

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	~A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0487	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.29	0.39	0.74
0.38	0.29	0.37	0.47	0.82
1.00	0.37	0.45	0.55	0.90
3.00	0.52	0.60	0.70	1.05

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	~A&~B	FALL

SLEW FACTOR

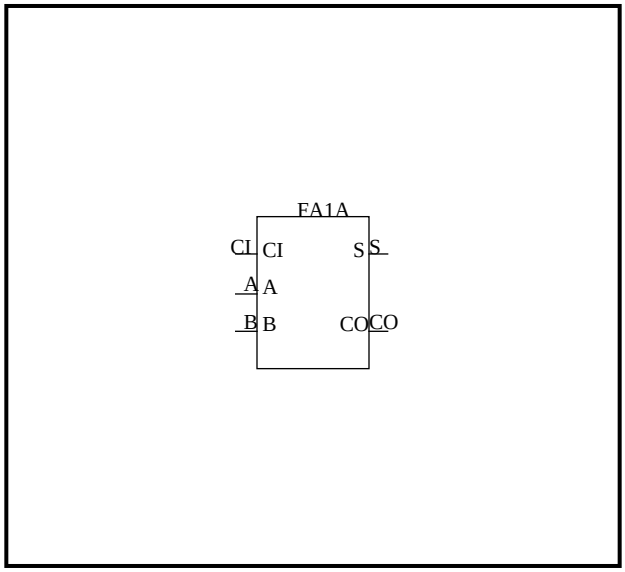
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0223	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.33	0.41	0.69
0.38	0.27	0.36	0.44	0.72
1.00	0.33	0.42	0.51	0.79
3.00	0.48	0.57	0.66	0.95

FA1A	FA1A	1/10

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FA1A	FULL ADDER	8	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT	
CI	A	B	S	CO
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

Verilog-HDL DESCRIPTION

```
FA1A  inst(S,CO,CI,A,B);
```

VHDL DESCRIPTION

```
inst:FA1A
   port   map(S,CO,CI,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	S,CO
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
CI	2.21
A	0.99
B	2.08

OUTPUT DRIVE (LU)

PIN NAME	S	CO
DRIVE	50.5	41.8

Rev.1.01.10

FA1A | FA1A | 2/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->CO	B&~CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.1010	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.68	0.83	1.00	1.69
0.38	0.76	0.91	1.09	1.77
1.00	0.86	1.01	1.18	1.87
3.00	1.03	1.18	1.35	2.04

PATH CONDITION

PATH	CONDITION	FUNCTION
A->CO	B&~CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0426	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.79	0.92	1.06	1.58
0.38	0.82	0.95	1.09	1.61
1.00	0.90	1.03	1.17	1.68
3.00	1.07	1.21	1.35	1.86

PATH CONDITION

PATH	CONDITION	FUNCTION
A->CO	~B&CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.1010	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.87	1.02	1.20	1.89
0.38	0.94	1.10	1.28	1.97
1.00	1.01	1.16	1.34	2.03
3.00	1.12	1.27	1.45	2.15

PATH CONDITION

PATH	CONDITION	FUNCTION
A->CO	~B&CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0426	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.83	0.97	1.11	1.62
0.38	0.86	1.00	1.14	1.65
1.00	0.93	1.06	1.21	1.72
3.00	1.05	1.19	1.34	1.85

FA1A | FA1A | 3/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	B&CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0844	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.66	0.79	0.94	1.54
0.38	0.74	0.87	1.03	1.62
1.00	0.84	0.97	1.12	1.71
3.00	1.01	1.14	1.30	1.89

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	B&CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0351	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.75	0.88	1.00	1.44
0.38	0.78	0.91	1.03	1.47
1.00	0.85	0.98	1.11	1.54
3.00	1.03	1.15	1.28	1.72

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	B&~CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0844	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.64	0.78	0.94	1.55
0.38	0.68	0.81	0.97	1.58
1.00	0.75	0.89	1.05	1.65
3.00	0.93	1.07	1.22	1.83

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	B&~CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0351	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.58	0.73	0.87	1.32
0.38	0.66	0.81	0.95	1.41
1.00	0.76	0.91	1.05	1.50
3.00	0.93	1.08	1.22	1.68

FA1A | FA1A | 4/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	~B&CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0844	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.81	0.94	1.09	1.69
0.38	0.84	0.97	1.13	1.72
1.00	0.90	1.04	1.19	1.78
3.00	1.03	1.16	1.32	1.91

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	~B&CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0351	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.78	0.91	1.04	1.48
0.38	0.86	0.99	1.12	1.56
1.00	0.92	1.05	1.18	1.62
3.00	1.03	1.16	1.29	1.73

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	~B&~CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0844	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.66	0.80	0.96	1.56
0.38	0.74	0.87	1.03	1.63
1.00	0.80	0.94	1.10	1.70
3.00	0.91	1.05	1.21	1.81

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	~B&~CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0351	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.72	0.86	1.00	1.45
0.38	0.75	0.89	1.03	1.48
1.00	0.81	0.96	1.09	1.54
3.00	0.94	1.09	1.22	1.67

FA1A | FA1A | 5/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->CO	A&~CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.1010	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.60	0.75	0.92	1.60
0.38	0.68	0.83	1.00	1.68
1.00	0.75	0.89	1.07	1.74
3.00	0.87	1.02	1.19	1.87

PATH CONDITION

PATH	CONDITION	FUNCTION
B->CO	A&~CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0426	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.45	0.59	1.09
0.38	0.35	0.49	0.62	1.12
1.00	0.42	0.56	0.70	1.20
3.00	0.57	0.72	0.86	1.36

PATH CONDITION

PATH	CONDITION	FUNCTION
B->CO	~A&CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.1010	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.40	0.57	1.26
0.38	0.34	0.48	0.65	1.33
1.00	0.43	0.57	0.74	1.42
3.00	0.59	0.74	0.91	1.58

PATH CONDITION

PATH	CONDITION	FUNCTION
B->CO	~A&CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0426	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.75	0.89	1.03	1.53
0.38	0.78	0.92	1.06	1.57
1.00	0.86	0.99	1.13	1.64
3.00	1.01	1.14	1.28	1.79

FA1A | FA1A | 6/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	A&CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0844	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.58	0.72	0.87	1.46
0.38	0.66	0.79	0.95	1.54
1.00	0.72	0.85	1.01	1.60
3.00	0.81	0.94	1.10	1.69

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	A&CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0351	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.68	0.81	0.94	1.38
0.38	0.70	0.84	0.96	1.40
1.00	0.78	0.91	1.04	1.48
3.00	0.97	1.10	1.23	1.67

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	A&~CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0844	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.58	0.72	0.88	1.48
0.38	0.60	0.74	0.90	1.50
1.00	0.68	0.81	0.97	1.57
3.00	0.87	1.01	1.16	1.77

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	A&~CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0351	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.66	0.79	1.25
0.38	0.58	0.73	0.87	1.33
1.00	0.64	0.79	0.93	1.39
3.00	0.73	0.88	1.02	1.48

FA1A | FA1A | 7/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	~A&CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0844	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.73	0.86	1.02	1.61
0.38	0.76	0.89	1.05	1.64
1.00	0.83	0.97	1.12	1.71
3.00	0.98	1.11	1.26	1.86

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	~A&CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0351	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.62	0.75	0.87	1.31
0.38	0.73	0.85	0.98	1.41
1.00	0.89	1.02	1.15	1.58
3.00	1.12	1.25	1.37	1.81

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	~A&~CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0844	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.65	0.81	1.42
0.38	0.62	0.76	0.92	1.52
1.00	0.78	0.92	1.08	1.68
3.00	1.01	1.15	1.31	1.91

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	~A&~CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0351	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.64	0.78	0.92	1.37
0.38	0.67	0.82	0.95	1.40
1.00	0.74	0.89	1.02	1.47
3.00	0.89	1.03	1.17	1.62

FA1A | FA1A | 8/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->CO	A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.1010	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.50	0.68	1.37
0.38	0.41	0.57	0.75	1.44
1.00	0.48	0.64	0.82	1.51
3.00	0.64	0.80	0.98	1.68

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->CO	A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0426	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.51	0.66	1.18
0.38	0.38	0.53	0.69	1.21
1.00	0.45	0.60	0.75	1.28
3.00	0.59	0.75	0.91	1.44

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->CO	~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.1010	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.49	0.67	1.36
0.38	0.41	0.56	0.74	1.44
1.00	0.48	0.64	0.82	1.51
3.00	0.64	0.80	0.98	1.68

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->CO	~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0426	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.51	0.66	1.18
0.38	0.38	0.53	0.68	1.21
1.00	0.45	0.60	0.75	1.28
3.00	0.59	0.75	0.91	1.44

FA1A | FA1A | 9/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0844	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.30	0.45	1.04
0.38	0.24	0.37	0.52	1.12
1.00	0.30	0.43	0.58	1.18
3.00	0.37	0.50	0.65	1.25

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0351	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.35	0.47	0.91
0.38	0.26	0.38	0.50	0.94
1.00	0.34	0.46	0.58	1.02
3.00	0.53	0.65	0.78	1.22

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0844	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.55	0.70	1.30
0.38	0.44	0.58	0.73	1.33
1.00	0.52	0.65	0.81	1.41
3.00	0.69	0.83	0.98	1.58

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0351	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.35	0.48	0.92
0.38	0.32	0.45	0.58	1.02
1.00	0.49	0.61	0.74	1.17
3.00	0.72	0.84	0.96	1.39

FA1A | FA1A | 10/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0844	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.55	0.70	1.30
0.38	0.44	0.58	0.73	1.33
1.00	0.52	0.65	0.81	1.41
3.00	0.69	0.83	0.98	1.58

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0351	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.35	0.48	0.92
0.38	0.32	0.45	0.58	1.02
1.00	0.49	0.61	0.74	1.17
3.00	0.72	0.84	0.96	1.39

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	~A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0844	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.30	0.45	1.04
0.38	0.24	0.37	0.52	1.12
1.00	0.30	0.43	0.58	1.18
3.00	0.36	0.49	0.65	1.25

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	~A&~B	FALL

SLEW FACTOR

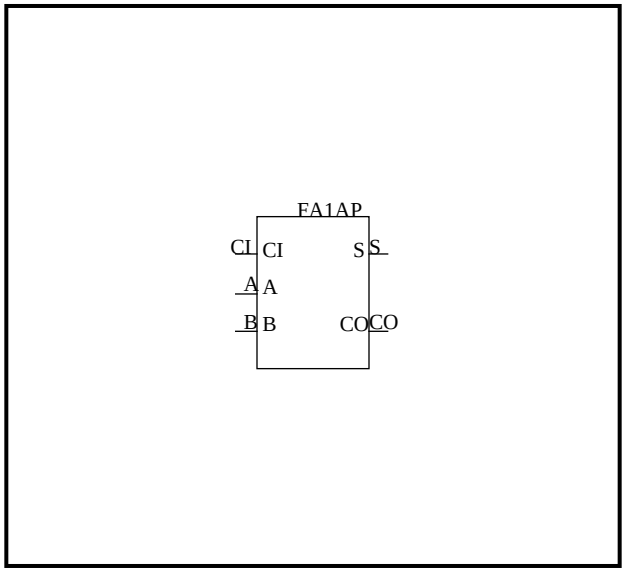
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0351	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.35	0.48	0.91
0.38	0.27	0.38	0.51	0.94
1.00	0.34	0.46	0.58	1.02
3.00	0.53	0.65	0.78	1.22

FA1AP	FA1AP	1/10

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FA1AP	FULL ADDER	9	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT	
CI	A	B	S	CO
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

Verilog-HDL DESCRIPTION

```
FA1AP  inst(S,CO,CI,A,B);
```

VHDL DESCRIPTION

```
inst:FA1AP
  port  map(S,CO,CI,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	S	CO
ELECTRO MIGRATION DRIVE	12880.0	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
CI	2.21
A	0.99
B	2.07

OUTPUT DRIVE (LU)

PIN NAME	S	CO
DRIVE	92.3	75.8

Rev.1.01.10

FA1AP | FA1AP | 2/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->CO	B&~CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0559	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.75	0.84	0.94	1.31
0.38	0.83	0.92	1.02	1.40
1.00	0.93	1.02	1.12	1.49
3.00	1.11	1.20	1.29	1.67

PATH CONDITION

PATH	CONDITION	FUNCTION
A->CO	B&~CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0249	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.80	0.89	0.99	1.30
0.38	0.83	0.92	1.02	1.33
1.00	0.91	1.00	1.09	1.41
3.00	1.09	1.18	1.27	1.59

PATH CONDITION

PATH	CONDITION	FUNCTION
A->CO	~B&CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0559	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.89	0.97	1.07	1.45
0.38	0.96	1.05	1.15	1.53
1.00	1.03	1.11	1.21	1.59
3.00	1.14	1.23	1.33	1.70

PATH CONDITION

PATH	CONDITION	FUNCTION
A->CO	~B&CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0249	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.83	0.92	1.01	1.33
0.38	0.86	0.95	1.04	1.36
1.00	0.92	1.02	1.11	1.42
3.00	1.05	1.14	1.24	1.55

FA1AP | FA1AP | 3/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	B&CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0447	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.66	0.73	0.82	1.14
0.38	0.74	0.82	0.90	1.22
1.00	0.83	0.91	1.00	1.32
3.00	1.01	1.09	1.17	1.50

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	B&CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0204	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.75	0.83	0.92	1.19
0.38	0.78	0.86	0.95	1.22
1.00	0.85	0.94	1.03	1.30
3.00	1.03	1.11	1.20	1.47

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	B&~CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0447	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.64	0.72	0.81	1.13
0.38	0.67	0.75	0.84	1.17
1.00	0.75	0.83	0.91	1.24
3.00	0.92	1.00	1.09	1.42

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	B&~CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0204	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.59	0.69	0.78	1.07
0.38	0.67	0.77	0.86	1.15
1.00	0.77	0.87	0.96	1.24
3.00	0.95	1.04	1.14	1.42

FA1AP | FA1AP | 4/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	~B&CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0447	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.81	0.88	0.97	1.29
0.38	0.84	0.92	1.00	1.33
1.00	0.90	0.98	1.07	1.39
3.00	1.03	1.11	1.19	1.52

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	~B&CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0204	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.78	0.87	0.96	1.23
0.38	0.86	0.94	1.03	1.31
1.00	0.92	1.01	1.10	1.37
3.00	1.03	1.12	1.21	1.48

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	~B&~CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0447	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.66	0.73	0.82	1.15
0.38	0.73	0.81	0.90	1.22
1.00	0.80	0.87	0.96	1.29
3.00	0.91	0.99	1.08	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	~B&~CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0204	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.73	0.83	0.92	1.20
0.38	0.77	0.86	0.95	1.23
1.00	0.83	0.92	1.01	1.29
3.00	0.96	1.05	1.14	1.42

FA1AP | FA1AP | 5/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->CO	A&~CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0559	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.68	0.76	0.86	1.24
0.38	0.75	0.84	0.94	1.31
1.00	0.82	0.91	1.01	1.38
3.00	0.95	1.04	1.14	1.52

PATH CONDITION

PATH	CONDITION	FUNCTION
B->CO	A&~CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0249	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.41	0.50	0.80
0.38	0.35	0.45	0.54	0.84
1.00	0.43	0.52	0.61	0.91
3.00	0.59	0.69	0.78	1.09

PATH CONDITION

PATH	CONDITION	FUNCTION
B->CO	~A&CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0559	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.35	0.46	0.86
0.38	0.33	0.42	0.52	0.91
1.00	0.42	0.51	0.61	0.98
3.00	0.59	0.68	0.78	1.16

PATH CONDITION

PATH	CONDITION	FUNCTION
B->CO	~A&CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0249	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.73	0.83	0.92	1.23
0.38	0.77	0.86	0.95	1.27
1.00	0.84	0.93	1.02	1.34
3.00	0.99	1.08	1.18	1.49

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	A&CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0447	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.58	0.66	0.74	1.07
0.38	0.66	0.74	0.82	1.14
1.00	0.72	0.80	0.88	1.21
3.00	0.82	0.89	0.98	1.30

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	A&CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0204	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.68	0.77	0.86	1.13
0.38	0.71	0.79	0.88	1.16
1.00	0.78	0.87	0.96	1.23
3.00	0.97	1.06	1.15	1.42

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	A&~CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0447	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.57	0.65	0.74	1.07
0.38	0.60	0.68	0.77	1.09
1.00	0.67	0.75	0.84	1.17
3.00	0.87	0.95	1.04	1.36

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	A&~CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0204	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.61	0.70	0.99
0.38	0.60	0.69	0.78	1.07
1.00	0.66	0.75	0.85	1.13
3.00	0.75	0.85	0.94	1.23

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	~A&CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0447	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.71	0.79	0.88	1.20
0.38	0.75	0.83	0.91	1.24
1.00	0.82	0.90	0.98	1.31
3.00	0.96	1.04	1.12	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	~A&CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0204	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.61	0.70	0.79	1.06
0.38	0.72	0.81	0.89	1.17
1.00	0.89	0.98	1.07	1.34
3.00	1.13	1.22	1.31	1.58

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	~A&~CI	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0447	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.50	0.58	0.67	1.00
0.38	0.61	0.69	0.78	1.10
1.00	0.78	0.86	0.95	1.27
3.00	1.02	1.10	1.18	1.51

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	~A&~CI	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0204	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.64	0.73	0.82	1.10
0.38	0.67	0.77	0.86	1.14
1.00	0.74	0.84	0.93	1.21
3.00	0.89	0.98	1.07	1.35

FA1AP | FA1AP | 8/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->CO	A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0559	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.45	0.55	0.93
0.38	0.43	0.52	0.62	1.00
1.00	0.48	0.57	0.67	1.05
3.00	0.62	0.71	0.82	1.20

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->CO	A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0249	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.43	0.53	0.85
0.38	0.37	0.46	0.56	0.89
1.00	0.44	0.53	0.63	0.96
3.00	0.59	0.70	0.80	1.13

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->CO	~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0559	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.44	0.54	0.92
0.38	0.42	0.51	0.61	0.99
1.00	0.48	0.56	0.67	1.05
3.00	0.62	0.71	0.82	1.20

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->CO	~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0249	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.43	0.53	0.85
0.38	0.37	0.46	0.56	0.89
1.00	0.44	0.53	0.63	0.96
3.00	0.59	0.70	0.80	1.13

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0447	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.25	0.34	0.66
0.38	0.26	0.33	0.42	0.74
1.00	0.33	0.41	0.50	0.82
3.00	0.45	0.53	0.62	0.94

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0204	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.33	0.41	0.67
0.38	0.28	0.36	0.44	0.70
1.00	0.35	0.43	0.51	0.77
3.00	0.52	0.61	0.69	0.96

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0447	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.48	0.57	0.90
0.38	0.44	0.52	0.61	0.93
1.00	0.53	0.60	0.69	1.01
3.00	0.73	0.80	0.89	1.21

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0204	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.32	0.41	0.68
0.38	0.33	0.41	0.50	0.77
1.00	0.50	0.58	0.67	0.94
3.00	0.77	0.85	0.93	1.19

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0447	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.48	0.57	0.90
0.38	0.44	0.52	0.61	0.93
1.00	0.53	0.60	0.69	1.01
3.00	0.73	0.80	0.89	1.21

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0204	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.32	0.41	0.68
0.38	0.33	0.41	0.50	0.77
1.00	0.50	0.58	0.67	0.94
3.00	0.77	0.85	0.93	1.19

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	~A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0447	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.25	0.34	0.66
0.38	0.26	0.33	0.42	0.74
1.00	0.33	0.41	0.50	0.82
3.00	0.45	0.53	0.62	0.94

PATH CONDITION

PATH	CONDITION	FUNCTION
CI->S	~A&~B	FALL

SLEW FACTOR

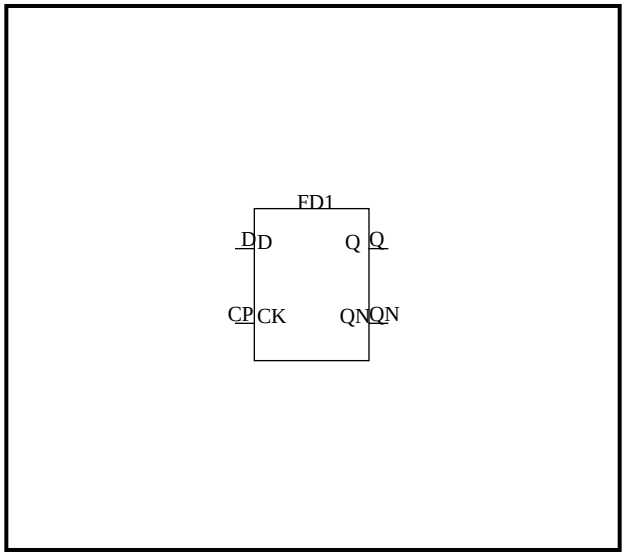
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0204	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.33	0.41	0.67
0.38	0.28	0.36	0.44	0.70
1.00	0.35	0.43	0.51	0.78
3.00	0.52	0.61	0.69	0.96

FD1	FD1	1/4

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FD1	D-TYPE FLIP FLOP	7	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
D	CP	Qn+1	QNn+1
L	Up	L	H
H	Up	H	L
X	Dn	Qn	QNn

Verilog-HDL DESCRIPTION

```
FD1  inst(Q,QN,D,CP);
```

VHDL DESCRIPTION

```
inst:FD1
   port   map(Q,QN,D,CP);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D,CP	0.99

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	42.5	44.6

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FD1 FD1 2/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.1002	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.60	0.77	1.45
0.38	0.54	0.68	0.85	1.53
1.00	0.61	0.75	0.92	1.61
3.00	0.74	0.88	1.05	1.73

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0419	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.67	0.80	1.30
0.38	0.62	0.75	0.88	1.37
1.00	0.70	0.82	0.95	1.45
3.00	0.82	0.94	1.07	1.57

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0963	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.67	0.81	0.97	1.63
0.38	0.75	0.88	1.05	1.71
1.00	0.82	0.96	1.12	1.78
3.00	0.94	1.08	1.24	1.91

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0395	0.09

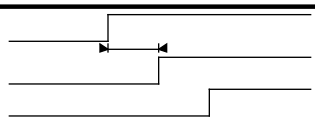
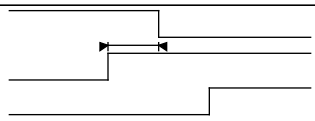
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.59	0.70	0.82	1.29
0.38	0.66	0.78	0.90	1.37
1.00	0.74	0.85	0.98	1.44
3.00	0.87	0.98	1.11	1.57

FD1	FD1	3/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	---

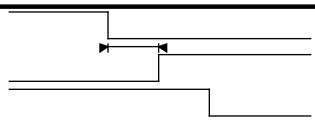
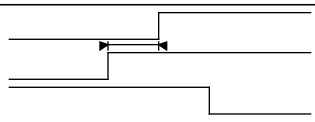
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.352	0.334	0.305	0.209
0.38	0.388	0.370	0.339	0.241
1.00	0.448	0.429	0.397	0.295
3.00	0.641	0.620	0.584	0.468

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.291	0.323	0.377	0.551
0.38	0.257	0.289	0.343	0.517
1.00	0.200	0.232	0.286	0.460
3.00	0.016	0.048	0.102	0.276

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.368	0.336	0.282	0.107
0.38	0.402	0.369	0.315	0.141
1.00	0.458	0.426	0.372	0.198
3.00	0.641	0.609	0.555	0.382

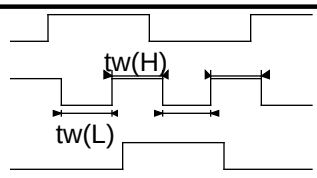
HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.305	0.322	0.352	0.447
0.38	0.269	0.287	0.318	0.416
1.00	0.209	0.228	0.260	0.362
3.00	0.016	0.038	0.074	0.190

FD1	FD1	4/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	---

ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.740

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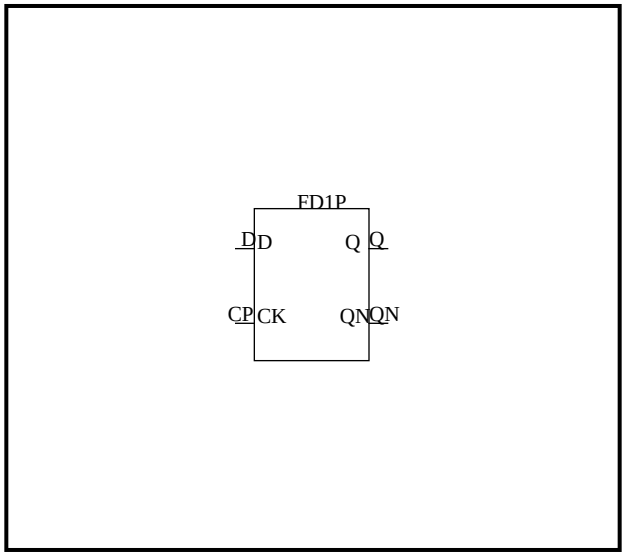
FD1P	FD1P	1/4

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FD1P	D-TYPE FLIP FLOP	8	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
D	CP	Qn+1	QNn+1
L	Up	L	H
H	Up	H	L
X	Dn	Qn	QNn

Verilog-HDL DESCRIPTION

```
FD1P  inst(Q,QN,D,CP);
```

VHDL DESCRIPTION

```
inst:FD1P
   port   map(Q,QN,D,CP);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q	QN
ELECTRO MIGRATION DRIVE	6880.0	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D,CP	0.99

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	86.5	97.7

Rev.1.01.10

FD1P | FD1P | 2/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0494	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.54	0.63	0.97
0.38	0.54	0.62	0.71	1.05
1.00	0.62	0.70	0.79	1.13
3.00	0.75	0.83	0.92	1.26

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0207	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.56	0.64	0.71	0.98
0.38	0.64	0.71	0.79	1.05
1.00	0.71	0.79	0.86	1.13
3.00	0.84	0.91	0.99	1.25

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0442	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.73	0.80	0.88	1.19
0.38	0.81	0.88	0.96	1.27
1.00	0.88	0.95	1.03	1.34
3.00	1.00	1.07	1.15	1.46

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0180	0.10

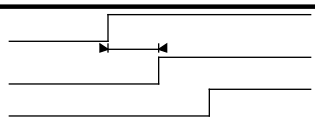
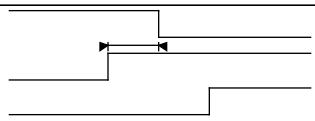
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.63	0.69	0.76	0.99
0.38	0.71	0.77	0.84	1.07
1.00	0.78	0.85	0.92	1.15
3.00	0.91	0.98	1.05	1.28

FD1P	FD1P	3/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	---

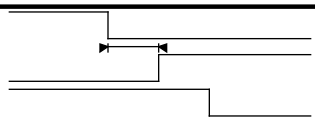
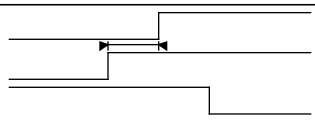
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.352	0.334	0.305	0.209
0.38	0.388	0.370	0.339	0.241
1.00	0.448	0.429	0.397	0.295
3.00	0.641	0.620	0.584	0.468

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.291	0.323	0.377	0.551
0.38	0.257	0.289	0.343	0.517
1.00	0.200	0.232	0.286	0.460
3.00	0.016	0.048	0.102	0.276

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.368	0.336	0.282	0.107
0.38	0.402	0.369	0.315	0.141
1.00	0.458	0.426	0.372	0.198
3.00	0.641	0.609	0.555	0.382

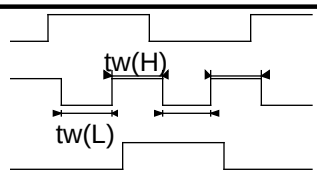
HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.305	0.322	0.352	0.447
0.38	0.269	0.287	0.318	0.416
1.00	0.209	0.228	0.260	0.362
3.00	0.016	0.038	0.074	0.190

FD1P	FD1P	4/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	---

ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.740

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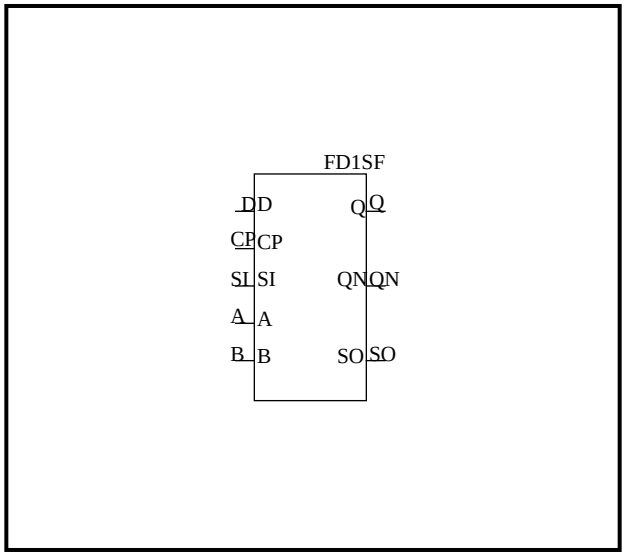
FD1SF	FD1SF	1/10

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FD1SF	D-TYPE FLIP FLOP with Independent two-phase SCAN clock	11	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT					OUTPUT		
D	SI	A	B	CP	Qn+1	QNn+1	SOn+1
X	X	X	L	X	X	X	SOn
X	L	H	H	L	L	H	L
X	H	H	H	L	H	L	H
L	X	L	H	Up	L	H	L
H	X	L	H	Up	H	L	H
X	X	L	H	Dn	Qn	QNn	Qn

Verilog-HDL DESCRIPTION

```
FD1SF  inst(Q,QN,SO,D,CP,SI,A,B);
```

VHDL DESCRIPTION

```
inst:FD1SF
   port   map(Q,QN,SO,D,CP,SI,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN,SO
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D,CP	0.99
SI	0.82
A	2.31
B	2.15

OUTPUT DRIVE (LU)

PIN NAME	Q	QN	SO
DRIVE	42.4	43.5	43.8

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&~A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0966	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.65	0.82	1.48
0.38	0.54	0.68	0.84	1.51
1.00	0.61	0.75	0.91	1.58
3.00	0.79	0.92	1.09	1.75

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&~A	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0399	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.59	0.70	0.82	1.28
0.38	0.63	0.73	0.85	1.32
1.00	0.69	0.80	0.92	1.38
3.00	0.83	0.94	1.06	1.52

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0966	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.56	0.72	1.39
0.38	0.51	0.65	0.81	1.48
1.00	0.64	0.78	0.94	1.60
3.00	0.77	0.91	1.07	1.74

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&A	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0399	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.44	0.55	0.67	1.13
0.38	0.53	0.63	0.75	1.22
1.00	0.63	0.74	0.85	1.32
3.00	0.81	0.91	1.03	1.49

FD1SF | FD1SF | 3/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.1003	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.44	0.58	0.76	1.44
0.38	0.53	0.67	0.85	1.53
1.00	0.66	0.81	0.98	1.67
3.00	0.79	0.94	1.11	1.80

PATH CONDITION

PATH	CONDITION	FUNCTION
A->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0423	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.47	0.60	0.73	1.23
0.38	0.55	0.68	0.81	1.31
1.00	0.66	0.78	0.92	1.41
3.00	0.83	0.96	1.09	1.59

PATH CONDITION

PATH	CONDITION	FUNCTION
A->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0964	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.60	0.74	0.90	1.57
0.38	0.68	0.82	0.99	1.65
1.00	0.79	0.93	1.09	1.75
3.00	0.96	1.10	1.27	1.93

PATH CONDITION

PATH	CONDITION	FUNCTION
A->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0402	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.56	0.67	0.80	1.27
0.38	0.65	0.76	0.89	1.36
1.00	0.78	0.90	1.02	1.49
3.00	0.92	1.03	1.15	1.62

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0966	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.44	0.61	1.26
0.38	0.41	0.54	0.70	1.35
1.00	0.51	0.65	0.81	1.46
3.00	0.63	0.77	0.93	1.57

PATH CONDITION

PATH	CONDITION	FUNCTION
B->SO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0399	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.41	0.53	0.99
0.38	0.37	0.47	0.59	1.06
1.00	0.43	0.54	0.66	1.13
3.00	0.53	0.65	0.77	1.26

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.1003	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.62	0.80	1.49
0.38	0.56	0.70	0.88	1.56
1.00	0.63	0.78	0.95	1.64
3.00	0.77	0.92	1.09	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0423	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.67	0.81	1.30
0.38	0.63	0.75	0.88	1.38
1.00	0.70	0.82	0.96	1.45
3.00	0.83	0.95	1.09	1.58

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0964	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.76	0.93	1.11	1.79
0.38	0.84	1.00	1.19	1.87
1.00	0.91	1.08	1.26	1.94
3.00	1.04	1.20	1.39	2.07

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0402	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.75	0.90	1.05	1.57
0.38	0.82	0.97	1.12	1.64
1.00	0.90	1.05	1.20	1.72
3.00	1.04	1.19	1.34	1.86

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0966	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.03	1.16	1.32	1.99
0.38	1.10	1.24	1.40	2.06
1.00	1.18	1.31	1.48	2.14
3.00	1.32	1.45	1.62	2.28

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->SO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0399	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.09	1.19	1.31	1.78
0.38	1.17	1.27	1.39	1.85
1.00	1.24	1.34	1.46	1.93
3.00	1.37	1.47	1.59	2.06

FD1SF | FD1SF | 6/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.1003	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.40	0.55	0.72	1.41
0.38	0.44	0.58	0.76	1.44
1.00	0.51	0.65	0.83	1.51
3.00	0.63	0.77	0.95	1.64

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0423	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.58	0.71	1.21
0.38	0.46	0.58	0.71	1.21
1.00	0.51	0.63	0.77	1.26
3.00	0.63	0.76	0.90	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0964	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.58	0.72	0.89	1.55
0.38	0.58	0.72	0.89	1.55
1.00	0.64	0.77	0.94	1.60
3.00	0.77	0.91	1.08	1.74

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0402	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.64	0.76	1.23
0.38	0.56	0.68	0.80	1.27
1.00	0.63	0.75	0.87	1.34
3.00	0.76	0.88	1.00	1.47

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0966	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.48	0.64	1.31
0.38	0.38	0.52	0.68	1.35
1.00	0.43	0.57	0.73	1.39
3.00	0.52	0.66	0.83	1.49

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->SO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0399	0.11

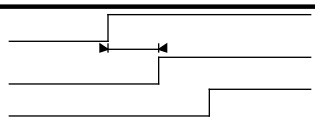
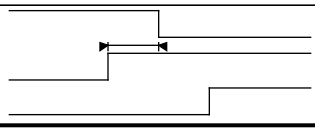
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.47	0.59	1.06
0.38	0.38	0.48	0.60	1.07
1.00	0.43	0.53	0.65	1.12
3.00	0.53	0.64	0.76	1.23

FD1SF	FD1SF	8/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	~A

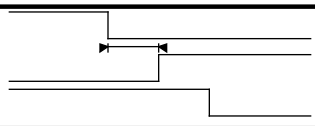
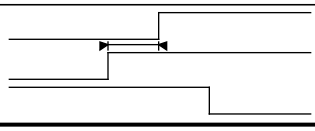
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.331	0.313	0.284	0.190
0.38	0.368	0.350	0.320	0.223
1.00	0.432	0.413	0.381	0.279
3.00	0.636	0.614	0.578	0.460

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.291	0.326	0.384	0.572
0.38	0.257	0.291	0.349	0.537
1.00	0.199	0.234	0.291	0.477
3.00	0.014	0.048	0.103	0.284

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	~A

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

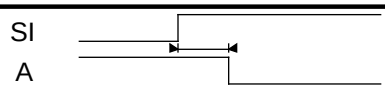
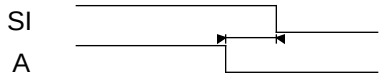
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.367	0.332	0.273	0.085
0.38	0.401	0.366	0.308	0.121
1.00	0.457	0.423	0.366	0.180
3.00	0.641	0.608	0.552	0.372

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.324	0.341	0.370	0.464
0.38	0.286	0.304	0.334	0.431
1.00	0.223	0.242	0.274	0.375
3.00	0.021	0.042	0.079	0.196

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
SI	A	~CP

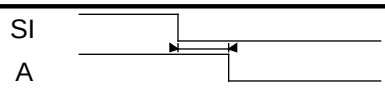
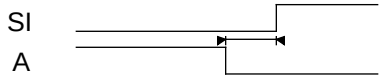
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.370	0.375	0.385	0.416
0.38	0.403	0.414	0.434	0.497
1.00	0.458	0.480	0.516	0.634
3.00	0.638	0.692	0.782	1.073

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.189	0.150	0.083	-0.130
0.38	0.166	0.122	0.048	-0.189
1.00	0.127	0.075	-0.010	-0.287
3.00	0.000	-0.075	-0.200	-0.605

TIMING CONDITION

DATA	CLOCK	CONDITION
SI	A	~CP

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

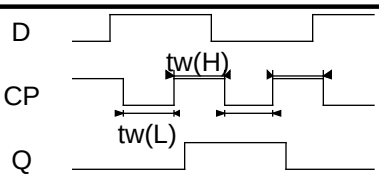
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.468	0.507	0.573	0.784
0.38	0.493	0.536	0.609	0.843
1.00	0.534	0.585	0.669	0.942
3.00	0.667	0.740	0.863	1.260

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.288	0.282	0.271	0.238
0.38	0.254	0.242	0.222	0.157
1.00	0.199	0.177	0.140	0.021
3.00	0.018	-0.035	-0.126	-0.417

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	---

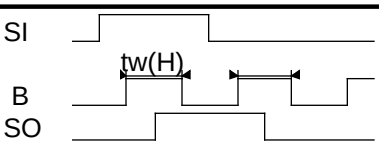
ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.710

MINIMUM PULSE WIDTH CONDITION

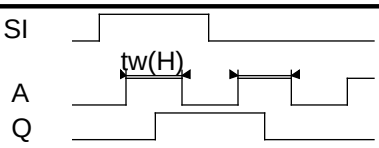
CLOCK	CONDITION
B	---

ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
A	---

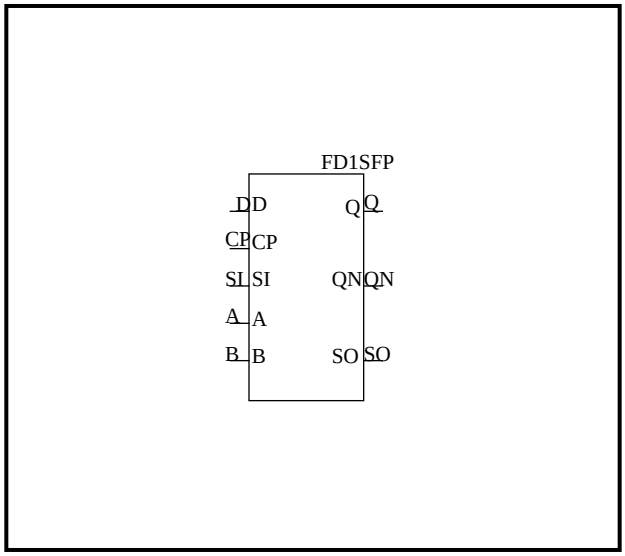
ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

FD1SFP	FD1SFP	1/10

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FD1SFP	D-TYPE FLIP FLOP with Independent two-phase SCAN clock	12	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT					OUTPUT		
D	SI	A	B	CP	Qn+1	QNn+1	SOn+1
X	X	X	L	X	X	X	SOn
X	L	H	H	L	L	H	L
X	H	H	H	L	H	L	H
L	X	L	H	Up	L	H	L
H	X	L	H	Up	H	L	H
X	X	L	H	Dn	Qn	QNn	Qn

Verilog-HDL DESCRIPTION

```
FD1SFP  inst(Q,QN,SO,D,CP,SI,A,B);
```

VHDL DESCRIPTION

```
inst:FD1SFP
  port  map(Q,QN,SO,D,CP,SI,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN,SO
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D	0.99
CP	1.00
SI	0.82
A	2.16
B	2.23

OUTPUT DRIVE (LU)

PIN NAME	Q	QN	SO
DRIVE	82.3	75.6	43.7

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&~A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0966	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.65	0.82	1.48
0.38	0.55	0.68	0.85	1.51
1.00	0.62	0.75	0.92	1.58
3.00	0.80	0.93	1.10	1.76

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&~A	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0399	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.61	0.72	0.84	1.30
0.38	0.64	0.75	0.87	1.33
1.00	0.71	0.81	0.93	1.40
3.00	0.85	0.96	1.08	1.54

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0966	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.43	0.56	0.73	1.39
0.38	0.52	0.65	0.82	1.48
1.00	0.65	0.78	0.95	1.61
3.00	0.79	0.92	1.09	1.75

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&A	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0399	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.55	0.67	1.14
0.38	0.53	0.64	0.76	1.22
1.00	0.64	0.74	0.86	1.33
3.00	0.82	0.92	1.04	1.50

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0512	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.54	0.63	0.98
0.38	0.55	0.63	0.72	1.07
1.00	0.68	0.76	0.86	1.20
3.00	0.82	0.90	1.00	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
A->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0216	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.50	0.57	0.65	0.92
0.38	0.58	0.66	0.73	1.00
1.00	0.69	0.76	0.84	1.11
3.00	0.86	0.94	1.02	1.28

PATH CONDITION

PATH	CONDITION	FUNCTION
A->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0547	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.67	0.75	0.85	1.22
0.38	0.75	0.83	0.93	1.30
1.00	0.86	0.94	1.04	1.41
3.00	1.04	1.12	1.22	1.59

PATH CONDITION

PATH	CONDITION	FUNCTION
A->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0244	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.63	0.71	0.79	1.08
0.38	0.72	0.80	0.88	1.17
1.00	0.86	0.94	1.02	1.31
3.00	1.00	1.08	1.16	1.45

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0966	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.45	0.61	1.25
0.38	0.41	0.54	0.70	1.35
1.00	0.52	0.65	0.81	1.46
3.00	0.64	0.77	0.93	1.57

PATH CONDITION

PATH	CONDITION	FUNCTION
B->SO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0399	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.40	0.52	0.99
0.38	0.37	0.47	0.59	1.06
1.00	0.43	0.54	0.66	1.12
3.00	0.53	0.64	0.77	1.25

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0512	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.57	0.67	1.02
0.38	0.57	0.65	0.74	1.10
1.00	0.65	0.73	0.82	1.18
3.00	0.79	0.87	0.96	1.32

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0216	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.57	0.64	0.72	0.99
0.38	0.64	0.72	0.80	1.07
1.00	0.72	0.79	0.87	1.14
3.00	0.85	0.92	1.00	1.27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0547	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.82	0.92	1.03	1.43
0.38	0.90	1.00	1.11	1.51
1.00	0.97	1.07	1.18	1.58
3.00	1.10	1.20	1.31	1.71

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0244	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.80	0.91	1.01	1.34
0.38	0.88	0.98	1.09	1.42
1.00	0.96	1.06	1.16	1.50
3.00	1.09	1.20	1.30	1.63

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0966	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.15	1.28	1.45	2.11
0.38	1.22	1.36	1.52	2.18
1.00	1.30	1.43	1.60	2.26
3.00	1.44	1.57	1.74	2.40

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->SO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0399	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.20	1.30	1.42	1.89
0.38	1.27	1.38	1.50	1.96
1.00	1.35	1.45	1.57	2.04
3.00	1.47	1.58	1.70	2.16

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0512	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.50	0.59	0.94
0.38	0.46	0.54	0.63	0.98
1.00	0.53	0.61	0.70	1.05
3.00	0.67	0.75	0.84	1.19

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0216	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.55	0.63	0.90
0.38	0.48	0.55	0.63	0.90
1.00	0.53	0.60	0.68	0.95
3.00	0.67	0.75	0.83	1.10

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0547	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.65	0.73	0.83	1.20
0.38	0.65	0.73	0.83	1.20
1.00	0.70	0.78	0.88	1.25
3.00	0.86	0.94	1.04	1.41

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0244	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.60	0.67	0.76	1.04
0.38	0.63	0.71	0.79	1.08
1.00	0.71	0.79	0.87	1.16
3.00	0.86	0.94	1.02	1.31

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0966	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.48	0.65	1.31
0.38	0.39	0.52	0.68	1.35
1.00	0.44	0.57	0.73	1.40
3.00	0.53	0.66	0.83	1.49

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->SO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0399	0.11

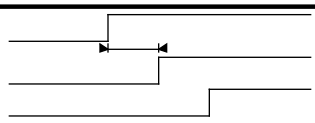
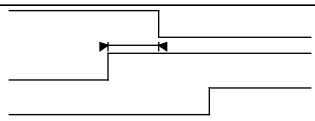
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.48	0.60	1.06
0.38	0.38	0.48	0.60	1.07
1.00	0.43	0.53	0.65	1.12
3.00	0.54	0.64	0.76	1.23

FD1SFP | FD1SFP | 8/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	~A

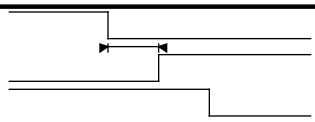
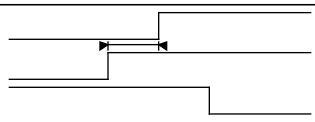
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.331	0.313	0.284	0.190
0.38	0.368	0.350	0.320	0.223
1.00	0.432	0.413	0.381	0.279
3.00	0.636	0.614	0.578	0.460

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.291	0.326	0.384	0.572
0.38	0.257	0.291	0.349	0.537
1.00	0.199	0.234	0.291	0.477
3.00	0.014	0.048	0.103	0.284

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	~A

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.367	0.332	0.273	0.085
0.38	0.401	0.366	0.308	0.121
1.00	0.457	0.423	0.366	0.180
3.00	0.641	0.608	0.552	0.372

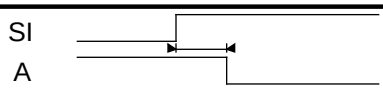
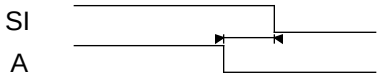
HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.324	0.341	0.370	0.464
0.38	0.286	0.304	0.334	0.431
1.00	0.223	0.242	0.274	0.375
3.00	0.021	0.042	0.079	0.196

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
SI	A	~CP

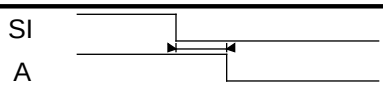
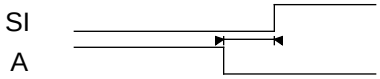
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.370	0.375	0.385	0.416
0.38	0.403	0.414	0.434	0.497
1.00	0.458	0.480	0.516	0.634
3.00	0.638	0.692	0.782	1.073

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.189	0.150	0.083	-0.130
0.38	0.166	0.122	0.048	-0.189
1.00	0.127	0.075	-0.010	-0.287
3.00	0.000	-0.075	-0.200	-0.605

TIMING CONDITION

DATA	CLOCK	CONDITION
SI	A	~CP

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

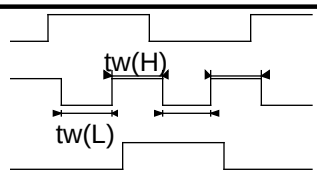
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.468	0.507	0.573	0.784
0.38	0.493	0.536	0.609	0.843
1.00	0.534	0.585	0.669	0.942
3.00	0.667	0.740	0.863	1.260

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.288	0.282	0.271	0.238
0.38	0.254	0.242	0.222	0.157
1.00	0.199	0.177	0.140	0.021
3.00	0.018	-0.035	-0.126	-0.417

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	---

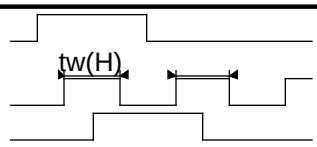
ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.710

MINIMUM PULSE WIDTH CONDITION

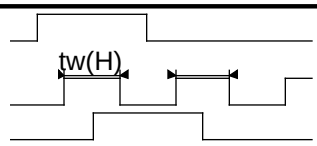
CLOCK	CONDITION
B	---

ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
A	---

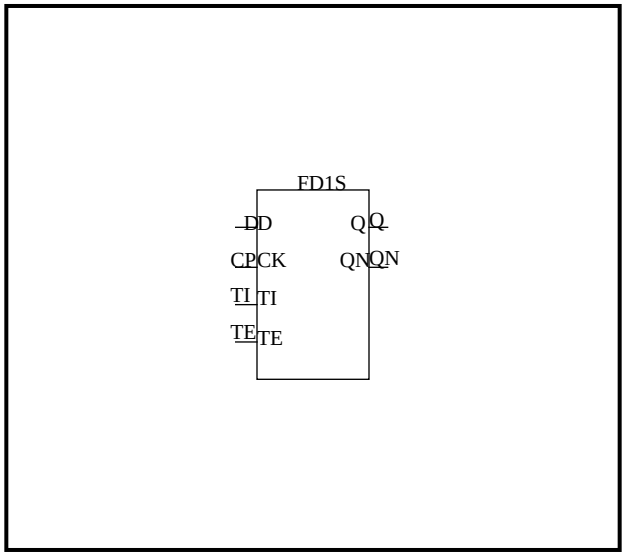
ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

FD1S	FD1S	1/6

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FD1S	D-TYPE FLIP FLOP with common single-phase SCAN clock	9	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT	
D	TI	TE	CP	Qn+1	QNn+1
L	X	L	Up	L	H
H	X	L	Up	H	L
X	L	H	Up	L	H
X	H	H	Up	H	L
X	X	X	Dn	Qn	QNn

Verilog-HDL DESCRIPTION

```
FD1S  inst(Q,QN,D,CP,TI,TE);
```

VHDL DESCRIPTION

```
inst:FD1S
  port  map(Q,QN,D,CP,TI,TE);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D,CP,TI	0.99
TE	1.97

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	42.5	44.6

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.1003	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.63	0.80	1.49
0.38	0.56	0.70	0.88	1.56
1.00	0.64	0.78	0.96	1.64
3.00	0.78	0.93	1.10	1.79

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0421	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.68	0.81	1.31
0.38	0.63	0.76	0.89	1.38
1.00	0.71	0.83	0.97	1.46
3.00	0.85	0.97	1.10	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0964	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.67	0.81	0.98	1.64
0.38	0.75	0.89	1.06	1.72
1.00	0.83	0.97	1.13	1.79
3.00	0.97	1.10	1.27	1.93

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0395	0.09

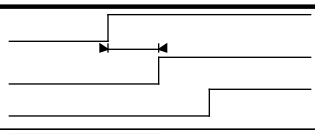
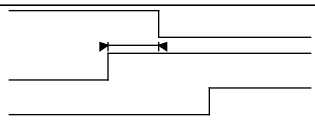
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.59	0.71	0.83	1.30
0.38	0.67	0.78	0.91	1.38
1.00	0.75	0.86	0.99	1.46
3.00	0.90	1.01	1.13	1.60

FD1S | FD1S | 3/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	~TE

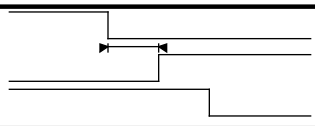
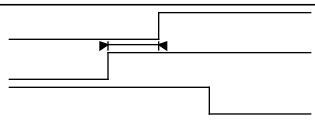
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.408	0.390	0.359	0.260
0.38	0.453	0.434	0.403	0.300
1.00	0.528	0.508	0.475	0.367
3.00	0.770	0.747	0.708	0.583

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.121	0.154	0.210	0.390
0.38	0.082	0.116	0.171	0.350
1.00	0.018	0.051	0.105	0.281
3.00	-0.190	-0.159	-0.107	0.061

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	~TE

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.536	0.503	0.447	0.266
0.38	0.575	0.542	0.486	0.307
1.00	0.639	0.606	0.552	0.375
3.00	0.847	0.815	0.763	0.595

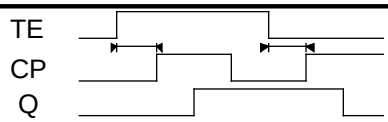
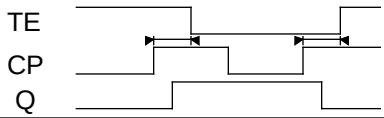
HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.242	0.260	0.291	0.390
0.38	0.197	0.216	0.247	0.350
1.00	0.122	0.142	0.175	0.283
3.00	-0.120	-0.097	-0.058	0.067

FD1S | FD1S | 4/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
TE	CP	(~D&TI D&~TI)

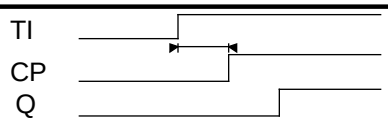
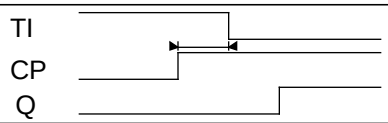
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	DCARE	
HOLD	POSEDGE	DCARE	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.449	0.431	0.400	0.302
0.38	0.500	0.482	0.450	0.349
1.00	0.586	0.567	0.534	0.428
3.00	0.864	0.842	0.804	0.683

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.208	0.226	0.256	0.353
0.38	0.157	0.175	0.206	0.306
1.00	0.070	0.090	0.122	0.227
3.00	-0.208	-0.186	-0.148	-0.026

TIMING CONDITION

DATA	CLOCK	CONDITION
TI	CP	TE

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.483	0.465	0.435	0.337
0.38	0.522	0.504	0.473	0.373
1.00	0.588	0.568	0.536	0.432
3.00	0.799	0.778	0.741	0.624

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.008	0.023	0.075	0.244
0.38	-0.031	-0.000	0.052	0.218
1.00	-0.069	-0.038	0.012	0.175
3.00	-0.190	-0.162	-0.115	0.037

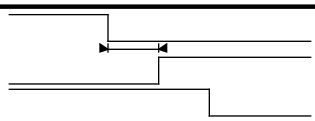
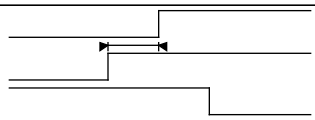
Rev.1.01.10

FD1S | FD1S | 5/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
TI	CP	TE

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

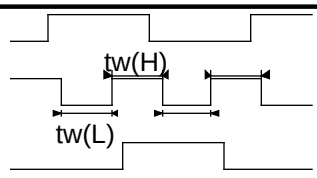
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.665	0.634	0.582	0.414
0.38	0.688	0.657	0.605	0.439
1.00	0.725	0.695	0.645	0.481
3.00	0.847	0.818	0.771	0.618

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.171	0.190	0.220	0.319
0.38	0.132	0.151	0.182	0.284
1.00	0.067	0.086	0.119	0.224
3.00	-0.144	-0.122	-0.086	0.032

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	---

ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

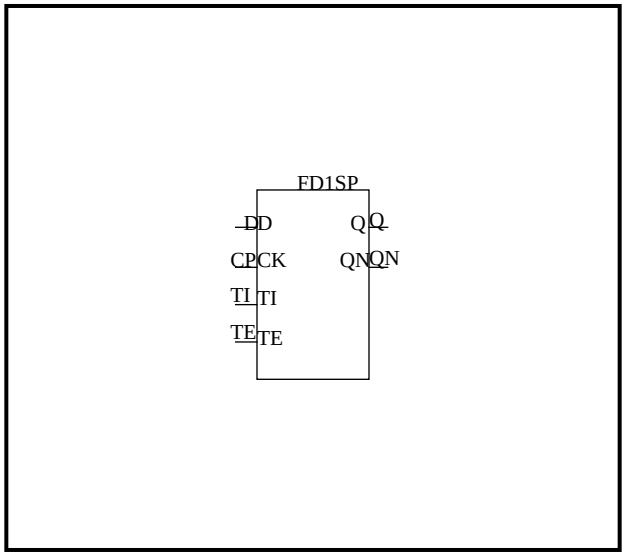
POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.770

FD1SP	FD1SP	1/6

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FD1SP	D-TYPE FLIP FLOP with common single-phase SCAN clock	10	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT	
D	TI	TE	CP	Qn+1	QNn+1
L	X	L	Up	L	H
H	X	L	Up	H	L
X	L	H	Up	L	H
X	H	H	Up	H	L
X	X	X	Dn	Qn	QNn

Verilog-HDL DESCRIPTION

```
FD1SP  inst(Q,QN,D,CP,TI,TE);
```

VHDL DESCRIPTION

```
inst:FD1SP
  port  map(Q,QN,D,CP,TI,TE);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q	QN
ELECTRO MIGRATION DRIVE	6880.0	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D,CP,TI	0.99
TE	1.97

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	77.0	97.7

Rev.1.01.10

FD1SP | FD1SP | 2/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0548	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.57	0.66	1.04
0.38	0.56	0.64	0.74	1.11
1.00	0.64	0.73	0.82	1.19
3.00	0.79	0.87	0.97	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0238	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.57	0.65	0.73	1.03
0.38	0.65	0.73	0.81	1.10
1.00	0.72	0.80	0.89	1.18
3.00	0.86	0.94	1.02	1.32

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0443	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.73	0.80	0.88	1.19
0.38	0.81	0.88	0.96	1.27
1.00	0.89	0.96	1.04	1.35
3.00	1.02	1.09	1.17	1.48

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0180	0.10

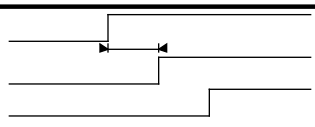
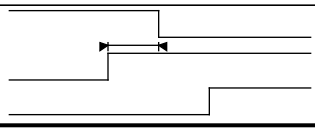
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.64	0.71	0.78	1.01
0.38	0.72	0.79	0.86	1.09
1.00	0.80	0.87	0.94	1.17
3.00	0.95	1.01	1.08	1.31

FD1SP	FD1SP	3/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	~TE

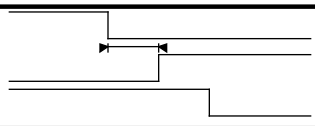
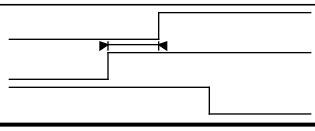
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.408	0.390	0.359	0.260
0.38	0.453	0.434	0.403	0.300
1.00	0.528	0.508	0.475	0.367
3.00	0.770	0.747	0.708	0.583

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.121	0.154	0.210	0.390
0.38	0.082	0.116	0.171	0.350
1.00	0.018	0.051	0.105	0.281
3.00	-0.190	-0.159	-0.107	0.061

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	~TE

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.536	0.503	0.447	0.266
0.38	0.575	0.542	0.486	0.307
1.00	0.639	0.606	0.552	0.375
3.00	0.847	0.815	0.763	0.595

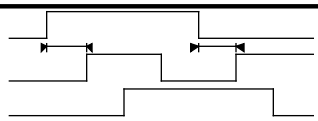
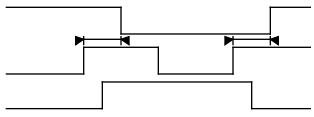
HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.242	0.260	0.291	0.390
0.38	0.197	0.216	0.247	0.350
1.00	0.122	0.142	0.175	0.283
3.00	-0.120	-0.097	-0.058	0.067

FD1SP | FD1SP | 4/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
TE	CP	(~D&TI D&~TI)

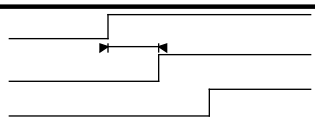
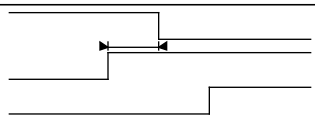
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	DCARE	
HOLD	POSEDGE	DCARE	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.449	0.431	0.400	0.302
0.38	0.500	0.482	0.450	0.349
1.00	0.586	0.567	0.534	0.428
3.00	0.864	0.842	0.804	0.683

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.208	0.226	0.256	0.353
0.38	0.157	0.175	0.206	0.306
1.00	0.070	0.090	0.122	0.227
3.00	-0.208	-0.186	-0.148	-0.026

TIMING CONDITION

DATA	CLOCK	CONDITION
TI	CP	TE

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.483	0.465	0.435	0.337
0.38	0.522	0.504	0.473	0.373
1.00	0.588	0.568	0.536	0.432
3.00	0.799	0.778	0.741	0.624

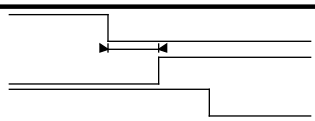
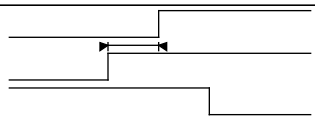
HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.008	0.023	0.075	0.244
0.38	-0.031	-0.000	0.052	0.218
1.00	-0.069	-0.038	0.012	0.175
3.00	-0.190	-0.162	-0.115	0.037

FD1SP | FD1SP | 5/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
TI	CP	TE

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.665	0.634	0.582	0.414
0.38	0.688	0.657	0.605	0.439
1.00	0.725	0.695	0.645	0.481
3.00	0.847	0.818	0.771	0.618

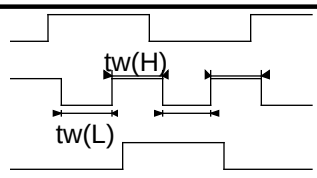
HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.171	0.190	0.220	0.319
0.38	0.132	0.151	0.182	0.284
1.00	0.067	0.086	0.119	0.224
3.00	-0.144	-0.122	-0.086	0.032

FD1SP	FD1SP	6/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	---

ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

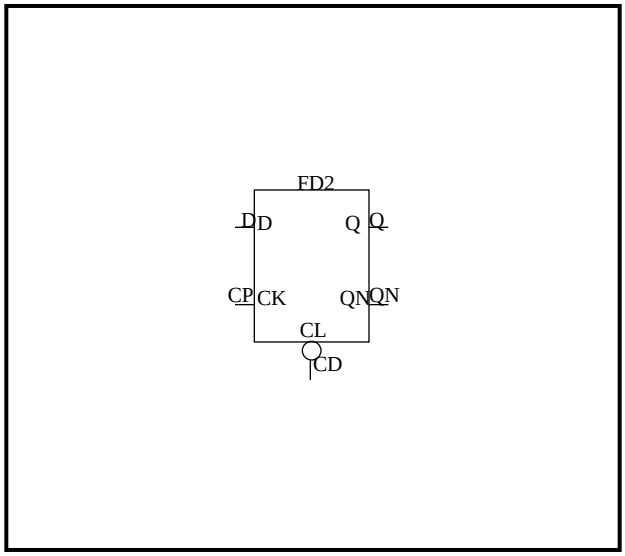
POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.770

FD2	FD2	1/6

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FD2	D-TYPE FLIP FLOP with CLEAR	8	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT	
CD	D	CP	Qn+1	QNn+1
L	X	X*	L	H
H	L	Up	L	H
H	H	Up	H	L
H	X	Dn	Qn	QNn

*:Consider the HOLD Time of CLEAR

Verilog-HDL DESCRIPTION

```
FD2  inst(Q,QN,D,CP,CD);
```

VHDL DESCRIPTION

```
inst:FD2
   port   map(Q,QN,D,CP,CD);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q	QN
ELECTRO MIGRATION DRIVE	6880.0	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D	0.99
CP	1.00
CD	2.12

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	42.6	51.2

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FD2 FD2 2/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0416	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.40	0.53	1.02
0.38	0.29	0.42	0.56	1.05
1.00	0.35	0.49	0.62	1.12
3.00	0.49	0.64	0.78	1.27

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0846	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.44	0.58	0.73	1.32
0.38	0.47	0.60	0.76	1.35
1.00	0.54	0.67	0.83	1.42
3.00	0.70	0.83	0.98	1.58

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0988	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.56	0.72	0.91	1.61
0.38	0.64	0.80	0.99	1.68
1.00	0.72	0.88	1.07	1.76
3.00	0.87	1.03	1.22	1.91

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0416	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.62	0.74	0.88	1.37
0.38	0.69	0.82	0.95	1.45
1.00	0.77	0.90	1.03	1.53
3.00	0.91	1.04	1.17	1.67

FD2 FD2 3/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0846	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.73	0.85	1.00	1.60
0.38	0.81	0.93	1.08	1.67
1.00	0.88	1.01	1.16	1.75
3.00	1.03	1.15	1.30	1.89

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0341	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.69	0.79	0.90	1.31
0.38	0.76	0.87	0.98	1.39
1.00	0.84	0.95	1.06	1.47
3.00	0.99	1.10	1.21	1.62

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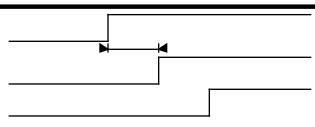
FD2 FD2 4/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

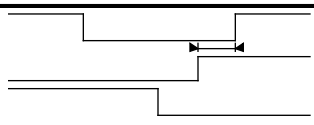
DATA	CLOCK	CONDITION
CD	CP	D

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.020	-0.060	-0.127	-0.342
0.38	-0.025	-0.065	-0.132	-0.347
1.00	-0.034	-0.074	-0.140	-0.354
3.00	-0.062	-0.101	-0.166	-0.378

TIMING CONDITION

DATA	CLOCK	CONDITION
CD	CP	D

ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.677	0.717	0.783	0.999
0.38	0.682	0.722	0.788	1.003
1.00	0.690	0.730	0.796	1.010
3.00	0.718	0.757	0.822	1.034

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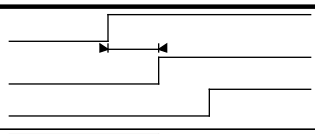
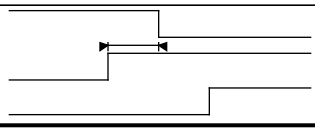
FD2	FD2	5/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD

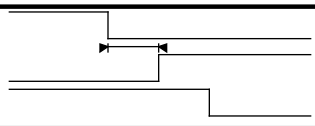
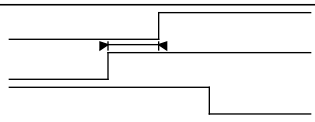
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.367	0.336	0.284	0.116
0.38	0.406	0.375	0.323	0.155
1.00	0.472	0.441	0.389	0.222
3.00	0.682	0.652	0.601	0.436

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.295	0.326	0.377	0.543
0.38	0.262	0.293	0.344	0.511
1.00	0.206	0.237	0.289	0.457
3.00	0.026	0.058	0.111	0.284

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.359	0.329	0.278	0.115
0.38	0.393	0.362	0.311	0.146
1.00	0.449	0.418	0.366	0.200
3.00	0.629	0.598	0.544	0.372

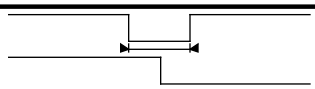
HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.290	0.321	0.373	0.542
0.38	0.251	0.282	0.334	0.502
1.00	0.185	0.216	0.268	0.435
3.00	-0.027	0.004	0.055	0.219

FD2	FD2	6/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

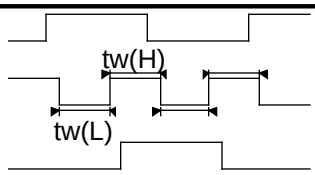
CLOCK	CONDITION
CD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.710

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	CD

ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.760

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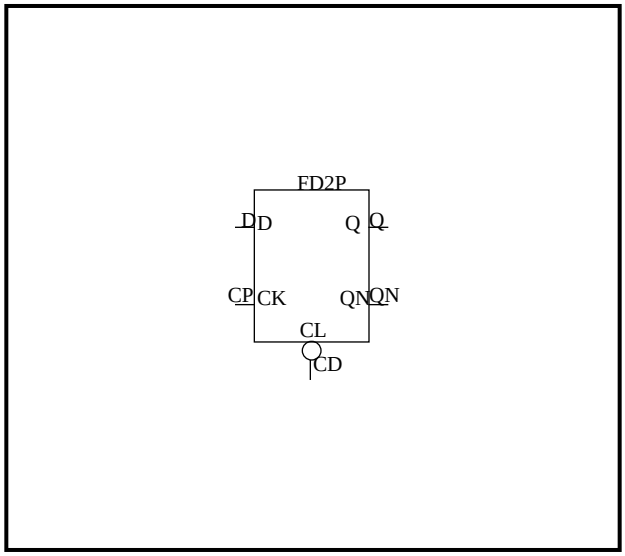
FD2P	FD2P	1/6

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FD2P	D-TYPE FLIP FLOP with CLEAR	9	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT	
CD	D	CP	Qn+1	QNn+1
L	X	X*	L	H
H	L	Up	L	H
H	H	Up	H	L
H	X	Dn	Qn	QNn

*:Consider the HOLD Time of CLEAR

Verilog-HDL DESCRIPTION

```
FD2P  inst(Q,QN,D,CP,CD);
```

VHDL DESCRIPTION

```
inst:FD2P
   port   map(Q,QN,D,CP,CD);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q	QN
ELECTRO MIGRATION DRIVE	6880.0	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D	0.99
CP	1.00
CD	2.12

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	83.0	97.9

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FD2P | FD2P | 2/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0182	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.32	0.39	0.63
0.38	0.27	0.34	0.42	0.66
1.00	0.34	0.41	0.49	0.73
3.00	0.48	0.57	0.65	0.89

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0444	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.55	0.63	0.95
0.38	0.50	0.58	0.66	0.97
1.00	0.58	0.65	0.73	1.05
3.00	0.76	0.83	0.91	1.23

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0546	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.56	0.65	0.75	1.13
0.38	0.64	0.73	0.83	1.21
1.00	0.72	0.81	0.91	1.29
3.00	0.87	0.96	1.06	1.44

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0182	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.61	0.68	0.75	0.99
0.38	0.69	0.76	0.83	1.07
1.00	0.76	0.84	0.91	1.15
3.00	0.91	0.98	1.05	1.29

FD2P | FD2P | 3/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0444	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.78	0.85	0.93	1.24
0.38	0.85	0.92	1.00	1.31
1.00	0.93	1.00	1.08	1.39
3.00	1.07	1.14	1.22	1.53

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0178	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.73	0.80	0.86	1.09
0.38	0.81	0.87	0.94	1.17
1.00	0.89	0.96	1.02	1.25
3.00	1.04	1.11	1.17	1.41

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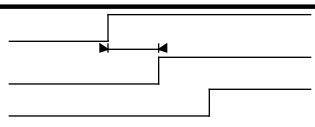
FD2P | FD2P | 4/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

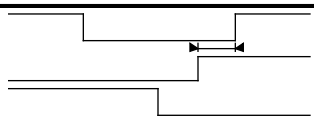
DATA	CLOCK	CONDITION
CD	CP	D

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.020	-0.060	-0.127	-0.342
0.38	-0.025	-0.065	-0.132	-0.347
1.00	-0.034	-0.074	-0.140	-0.354
3.00	-0.062	-0.101	-0.166	-0.378

TIMING CONDITION

DATA	CLOCK	CONDITION
CD	CP	D

ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.677	0.717	0.783	0.999
0.38	0.682	0.722	0.788	1.003
1.00	0.690	0.730	0.796	1.010
3.00	0.718	0.757	0.822	1.034

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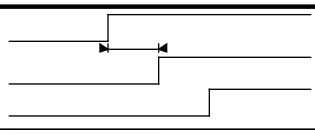
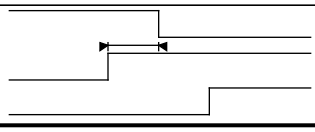
FD2P | FD2P | 5/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD

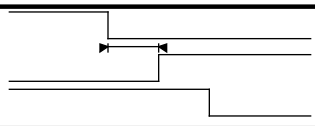
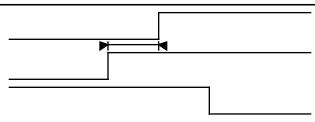
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.367	0.336	0.284	0.116
0.38	0.406	0.375	0.323	0.155
1.00	0.472	0.441	0.389	0.222
3.00	0.682	0.652	0.601	0.436

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.295	0.326	0.377	0.543
0.38	0.262	0.293	0.344	0.511
1.00	0.206	0.237	0.289	0.457
3.00	0.026	0.058	0.111	0.284

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.359	0.329	0.278	0.115
0.38	0.393	0.362	0.311	0.146
1.00	0.449	0.418	0.366	0.200
3.00	0.629	0.598	0.544	0.372

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.290	0.321	0.373	0.542
0.38	0.251	0.282	0.334	0.502
1.00	0.185	0.216	0.268	0.435
3.00	-0.027	0.004	0.055	0.219

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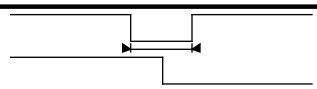
FD2P	FD2P	6/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

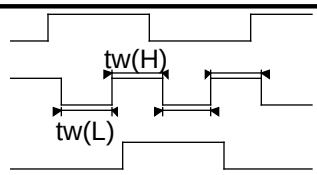
CLOCK	CONDITION
CD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.710

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	CD

ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

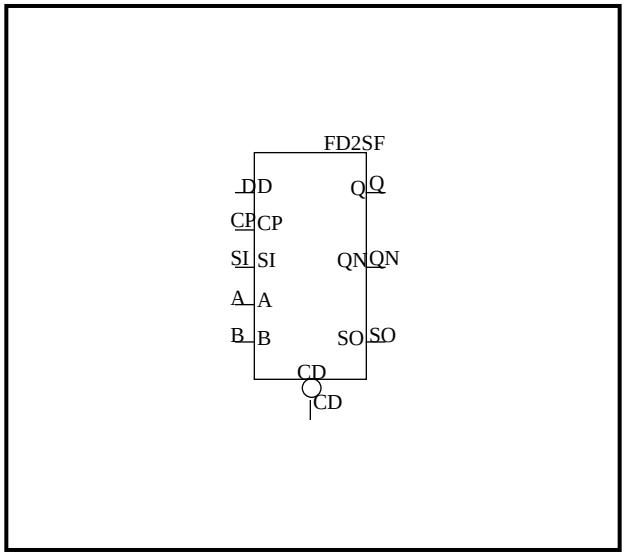
NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.760

Rev.1.01.10

FD2SF	FD2SF	1/13

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FD2SF	D-TYPE FLIP FLOP with Independent two-phase SCAN clock with CLEAR	12	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT						OUTPUT		
CD	D	SI	A	B	CP	Qn+1	QNn+1	SOn+1
X	X	X	X	L	X	X	X	SOn
L	X	X	L	H	X*	L	H	L
H	X	L	H	H	L	L	H	L
H	X	H	H	H	L	H	L	H
H	L	X	L	H	Up	L	H	L
H	H	X	L	H	Up	H	L	H
H	X	X	L	H	Dn	Qn	QNn	Qn

*:Consider the HOLD Time of CLEAR

Verilog-HDL DESCRIPTION

```
FD2SF  inst(Q,QN,SO,D,CP,CD,SI,A,B);
```

VHDL DESCRIPTION

```
inst:FD2SF
   port   map(Q,QN,SO,D,CP,CD,SI,
              A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN,SO
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D	1.02
CP	0.99
CD	2.18
SI	0.85
A	2.20
B	2.24

OUTPUT DRIVE (LU)

PIN NAME	Q	QN	SO
DRIVE	42.5	44.5	43.7

Rev.1.01.10

FD2SF | FD2SF | 2/13

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&~A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0967	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.66	0.82	1.48
0.38	0.55	0.68	0.85	1.51
1.00	0.62	0.75	0.92	1.58
3.00	0.79	0.93	1.09	1.76

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&~A	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0399	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.58	0.69	0.80	1.27
0.38	0.61	0.72	0.84	1.30
1.00	0.68	0.78	0.90	1.37
3.00	0.82	0.92	1.04	1.51

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0967	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.43	0.56	0.73	1.39
0.38	0.52	0.65	0.82	1.48
1.00	0.65	0.78	0.95	1.61
3.00	0.78	0.92	1.08	1.75

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&A	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0399	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.55	0.67	1.14
0.38	0.53	0.64	0.76	1.22
1.00	0.64	0.74	0.86	1.33
3.00	0.82	0.92	1.04	1.51

FD2SF | FD2SF | 3/13

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.1000	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.50	0.66	0.84	1.54
0.38	0.59	0.75	0.93	1.63
1.00	0.72	0.88	1.07	1.76
3.00	0.86	1.02	1.20	1.90

PATH CONDITION

PATH	CONDITION	FUNCTION
A->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0406	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.53	0.65	0.78	1.26
0.38	0.61	0.74	0.86	1.34
1.00	0.71	0.84	0.97	1.44
3.00	0.88	1.01	1.14	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
A->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0940	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.65	0.78	0.94	1.58
0.38	0.73	0.86	1.03	1.67
1.00	0.83	0.97	1.13	1.77
3.00	1.01	1.14	1.30	1.94

PATH CONDITION

PATH	CONDITION	FUNCTION
A->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0401	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.63	0.74	0.86	1.32
0.38	0.72	0.83	0.95	1.41
1.00	0.85	0.96	1.09	1.55
3.00	0.99	1.10	1.22	1.68

FD2SF | FD2SF | 4/13

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0967	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.45	0.61	1.26
0.38	0.41	0.54	0.70	1.35
1.00	0.52	0.65	0.81	1.46
3.00	0.63	0.77	0.93	1.57

PATH CONDITION

PATH	CONDITION	FUNCTION
B->SO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0399	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.40	0.52	0.98
0.38	0.37	0.47	0.59	1.05
1.00	0.43	0.53	0.66	1.12
3.00	0.53	0.64	0.77	1.25

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0406	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.36	0.50	0.98
0.38	0.26	0.39	0.53	1.00
1.00	0.31	0.44	0.58	1.06
3.00	0.40	0.55	0.69	1.18

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0940	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.62	0.81	1.49
0.38	0.48	0.65	0.84	1.52
1.00	0.54	0.71	0.90	1.58
3.00	0.67	0.84	1.03	1.70

FD2SF | FD2SF | 5/13

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->SO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0399	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.86	0.96	1.08	1.55
0.38	0.89	0.99	1.11	1.58
1.00	0.95	1.05	1.17	1.64
3.00	1.07	1.17	1.29	1.76

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.1000	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.72	0.91	1.62
0.38	0.63	0.80	0.99	1.70
1.00	0.71	0.88	1.07	1.78
3.00	0.85	1.02	1.21	1.93

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0406	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.61	0.74	0.88	1.35
0.38	0.69	0.82	0.95	1.43
1.00	0.76	0.90	1.03	1.51
3.00	0.90	1.03	1.17	1.64

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0940	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.82	0.98	1.15	1.82
0.38	0.90	1.06	1.23	1.90
1.00	0.97	1.13	1.31	1.97
3.00	1.11	1.27	1.44	2.11

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0401	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.83	0.98	1.13	1.64
0.38	0.91	1.06	1.21	1.72
1.00	0.99	1.14	1.29	1.80
3.00	1.13	1.28	1.43	1.94

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0967	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.11	1.24	1.41	2.07
0.38	1.19	1.32	1.49	2.15
1.00	1.27	1.40	1.57	2.23
3.00	1.41	1.55	1.71	2.37

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->SO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0399	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.13	1.24	1.36	1.82
0.38	1.21	1.31	1.43	1.90
1.00	1.29	1.39	1.51	1.98
3.00	1.42	1.52	1.64	2.11

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.1000	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.62	0.81	1.50
0.38	0.50	0.66	0.84	1.54
1.00	0.57	0.73	0.92	1.61
3.00	0.71	0.87	1.06	1.77

FD2SF | FD2SF | 7/13

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0406	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.50	0.63	0.76	1.23
0.38	0.50	0.63	0.76	1.23
1.00	0.55	0.68	0.81	1.28
3.00	0.69	0.83	0.96	1.44

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0940	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.62	0.76	0.92	1.56
0.38	0.63	0.76	0.92	1.56
1.00	0.67	0.81	0.97	1.61
3.00	0.82	0.96	1.12	1.76

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0401	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.59	0.70	0.82	1.28
0.38	0.63	0.74	0.86	1.32
1.00	0.70	0.81	0.94	1.40
3.00	0.84	0.96	1.08	1.54

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0967	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.48	0.64	1.31
0.38	0.38	0.52	0.68	1.34
1.00	0.43	0.57	0.73	1.39
3.00	0.52	0.66	0.82	1.48

FD2SF | FD2SF | 8/13

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->SO	---	FALL

SLEW FACTOR

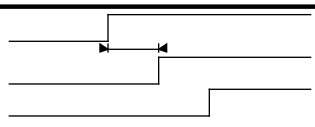
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0399	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.47	0.59	1.05
0.38	0.38	0.48	0.60	1.06
1.00	0.42	0.53	0.65	1.11
3.00	0.53	0.64	0.76	1.22

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

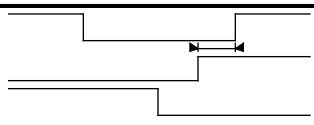
DATA	CLOCK	CONDITION
CD	CP	D&~A

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.039	-0.076	-0.139	-0.342
0.38	-0.044	-0.082	-0.145	-0.348
1.00	-0.054	-0.091	-0.154	-0.356
3.00	-0.085	-0.122	-0.184	-0.384

TIMING CONDITION

DATA	CLOCK	CONDITION
CD	CP	D&~A

ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

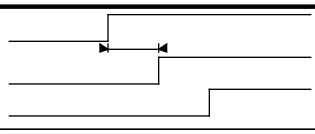
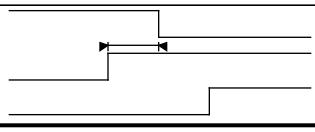
HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.693	0.731	0.794	0.999
0.38	0.699	0.736	0.800	1.004
1.00	0.709	0.746	0.809	1.013
3.00	0.741	0.778	0.840	1.040

FD2SF | FD2SF | 10/13

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD&~A

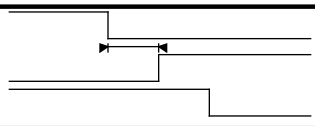
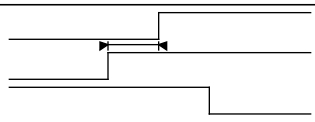
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.342	0.323	0.290	0.186
0.38	0.380	0.360	0.327	0.219
1.00	0.443	0.422	0.387	0.275
3.00	0.648	0.624	0.583	0.454

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.283	0.318	0.377	0.565
0.38	0.250	0.285	0.343	0.530
1.00	0.194	0.229	0.286	0.472
3.00	0.014	0.048	0.103	0.284

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD&~A

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.371	0.336	0.278	0.090
0.38	0.404	0.369	0.312	0.125
1.00	0.460	0.426	0.368	0.183
3.00	0.641	0.608	0.552	0.372

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.312	0.332	0.365	0.472
0.38	0.274	0.295	0.329	0.438
1.00	0.212	0.233	0.268	0.382
3.00	0.009	0.033	0.073	0.202

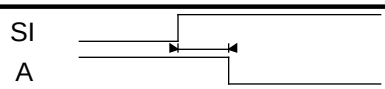
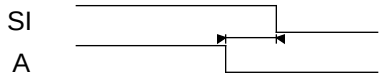
FD2SF

FD2SF

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
SI	A	CD&~CP

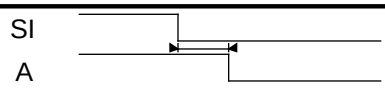
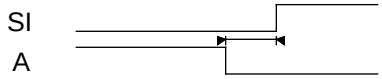
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.386	0.392	0.402	0.434
0.38	0.422	0.433	0.453	0.515
1.00	0.483	0.504	0.539	0.651
3.00	0.679	0.730	0.815	1.090

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.178	0.139	0.074	-0.134
0.38	0.152	0.109	0.038	-0.193
1.00	0.109	0.060	-0.023	-0.292
3.00	-0.029	-0.101	-0.221	-0.610

TIMING CONDITION

DATA	CLOCK	CONDITION
SI	A	CD&~CP

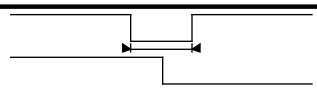
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

CLOCK SLEW (ns)

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

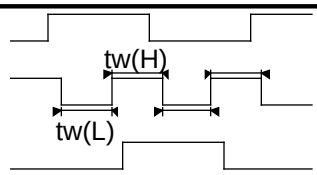
CLOCK	CONDITION
CD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.740

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	CD

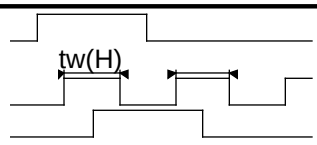
ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.720

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
B	CD

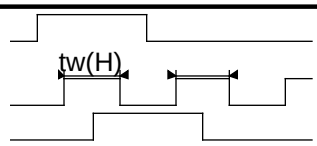
ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
A	CD

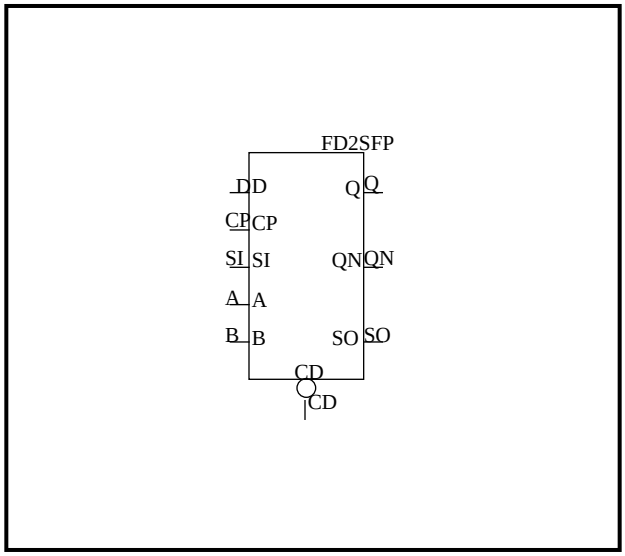
ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

FD2SFP	FD2SFP	1/13

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FD2SFP	D-TYPE FLIP FLOP with Independent two-phase SCAN clock with CLEAR	13	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT						OUTPUT		
CD	D	SI	A	B	CP	Qn+1	QNn+1	SOn+1
X	X	X	X	L	X	X	X	SOn
L	X	X	L	H	X*	L	H	L
H	X	L	H	H	L	L	H	L
H	X	H	H	H	L	H	L	H
H	L	X	L	H	Up	L	H	L
H	H	X	L	H	Up	H	L	H
H	X	X	L	H	Dn	Qn	QNn	Qn

*:Consider the HOLD Time of CLEAR

Verilog-HDL DESCRIPTION

```
FD2SFP  inst(Q,QN,SO,D,CP,CD,SI,A,
B);
```

VHDL DESCRIPTION

```
inst:FD2SFP
  port  map(Q,QN,SO,D,CP,CD,SI,
        A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN,SO
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D	1.02
CP	0.99
CD	2.18
SI	0.85
A	2.20
B	2.15

OUTPUT DRIVE (LU)

PIN NAME	Q	QN	SO
DRIVE	77.2	86.0	43.7

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&~A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0967	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.65	0.82	1.48
0.38	0.54	0.68	0.84	1.51
1.00	0.61	0.75	0.91	1.58
3.00	0.79	0.93	1.09	1.75

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&~A	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0399	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.58	0.69	0.81	1.27
0.38	0.62	0.72	0.84	1.30
1.00	0.68	0.78	0.90	1.37
3.00	0.82	0.92	1.04	1.51

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0967	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.55	0.72	1.38
0.38	0.51	0.64	0.81	1.47
1.00	0.64	0.78	0.94	1.60
3.00	0.78	0.91	1.07	1.74

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&A	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0399	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.55	0.67	1.14
0.38	0.53	0.64	0.76	1.22
1.00	0.64	0.74	0.86	1.32
3.00	0.82	0.92	1.04	1.50

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0545	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.61	0.71	1.09
0.38	0.61	0.70	0.80	1.18
1.00	0.75	0.84	0.94	1.32
3.00	0.89	0.97	1.07	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
A->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0237	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.50	0.58	0.66	0.96
0.38	0.58	0.66	0.75	1.04
1.00	0.68	0.76	0.85	1.14
3.00	0.86	0.94	1.03	1.32

PATH CONDITION

PATH	CONDITION	FUNCTION
A->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0479	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.68	0.75	0.84	1.17
0.38	0.77	0.84	0.92	1.25
1.00	0.87	0.94	1.03	1.36
3.00	1.04	1.11	1.20	1.53

PATH CONDITION

PATH	CONDITION	FUNCTION
A->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0210	0.21

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.73	0.80	0.87	1.12
0.38	0.82	0.89	0.96	1.21
1.00	0.96	1.02	1.10	1.35
3.00	1.09	1.16	1.23	1.49

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0967	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.44	0.60	1.25
0.38	0.40	0.54	0.70	1.35
1.00	0.51	0.64	0.81	1.45
3.00	0.63	0.76	0.93	1.57

PATH CONDITION

PATH	CONDITION	FUNCTION
B->SO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0399	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.40	0.52	0.99
0.38	0.37	0.47	0.59	1.06
1.00	0.43	0.54	0.66	1.12
3.00	0.53	0.64	0.77	1.25

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0237	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.33	0.42	0.71
0.38	0.28	0.36	0.45	0.74
1.00	0.35	0.43	0.52	0.81
3.00	0.49	0.59	0.68	0.98

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0479	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.64	0.74	1.11
0.38	0.58	0.67	0.77	1.14
1.00	0.65	0.74	0.85	1.21
3.00	0.84	0.93	1.04	1.40

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->SO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0399	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.99	1.09	1.21	1.68
0.38	1.01	1.12	1.24	1.70
1.00	1.09	1.19	1.31	1.78
3.00	1.27	1.37	1.49	1.96

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0545	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.54	0.63	0.73	1.11
0.38	0.62	0.71	0.81	1.19
1.00	0.71	0.79	0.89	1.27
3.00	0.85	0.94	1.03	1.41

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0237	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.58	0.66	0.74	1.04
0.38	0.66	0.74	0.82	1.12
1.00	0.73	0.82	0.90	1.19
3.00	0.87	0.95	1.03	1.33

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0479	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.84	0.93	1.03	1.38
0.38	0.92	1.01	1.10	1.46
1.00	1.00	1.08	1.18	1.54
3.00	1.13	1.22	1.31	1.67

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0210	0.21

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.89	0.99	1.08	1.37
0.38	0.97	1.06	1.16	1.45
1.00	1.05	1.15	1.24	1.53
3.00	1.20	1.29	1.38	1.68

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0967	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.22	1.35	1.52	2.18
0.38	1.30	1.43	1.60	2.26
1.00	1.38	1.51	1.68	2.34
3.00	1.52	1.65	1.82	2.48

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->SO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0399	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.20	1.30	1.42	1.89
0.38	1.27	1.38	1.50	1.96
1.00	1.35	1.46	1.58	2.04
3.00	1.48	1.59	1.71	2.17

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0545	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.57	0.67	1.05
0.38	0.53	0.61	0.71	1.09
1.00	0.62	0.71	0.81	1.18
3.00	0.82	0.91	1.01	1.39

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0237	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.56	0.64	0.94
0.38	0.48	0.56	0.64	0.94
1.00	0.52	0.60	0.69	0.98
3.00	0.63	0.72	0.81	1.11

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0479	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.66	0.73	0.82	1.15
0.38	0.66	0.73	0.82	1.15
1.00	0.71	0.78	0.86	1.19
3.00	0.84	0.91	1.00	1.33

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0210	0.21

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.69	0.76	0.83	1.09
0.38	0.73	0.80	0.87	1.13
1.00	0.83	0.90	0.97	1.22
3.00	1.05	1.12	1.19	1.44

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0967	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.48	0.64	1.31
0.38	0.38	0.51	0.68	1.34
1.00	0.43	0.57	0.73	1.39
3.00	0.52	0.66	0.82	1.48

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->SO	---	FALL

SLEW FACTOR

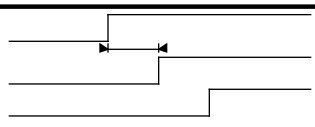
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0399	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.47	0.59	1.06
0.38	0.38	0.48	0.60	1.06
1.00	0.43	0.53	0.65	1.11
3.00	0.53	0.64	0.76	1.22

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

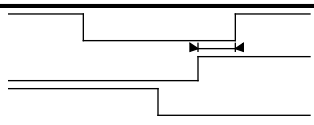
DATA	CLOCK	CONDITION
CD	CP	D&~A

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.039	-0.076	-0.139	-0.342
0.38	-0.044	-0.082	-0.145	-0.348
1.00	-0.054	-0.091	-0.154	-0.356
3.00	-0.085	-0.122	-0.184	-0.384

TIMING CONDITION

DATA	CLOCK	CONDITION
CD	CP	D&~A

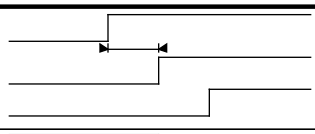
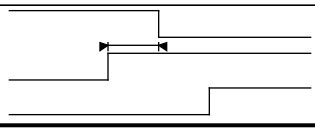
ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.693	0.731	0.794	0.999
0.38	0.699	0.736	0.800	1.004
1.00	0.709	0.746	0.809	1.013
3.00	0.741	0.778	0.840	1.040

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD&~A

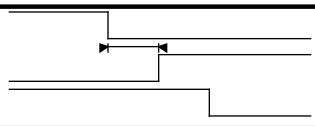
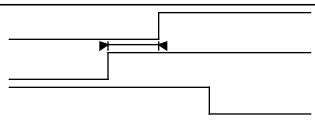
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.342	0.323	0.290	0.186
0.38	0.380	0.360	0.327	0.219
1.00	0.443	0.422	0.387	0.275
3.00	0.648	0.624	0.583	0.454

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.283	0.318	0.377	0.565
0.38	0.250	0.285	0.343	0.530
1.00	0.194	0.229	0.286	0.472
3.00	0.014	0.048	0.103	0.284

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD&~A

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

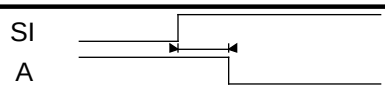
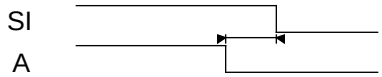
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.371	0.336	0.278	0.090
0.38	0.404	0.369	0.312	0.125
1.00	0.460	0.426	0.368	0.183
3.00	0.641	0.608	0.552	0.372

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.312	0.332	0.365	0.472
0.38	0.274	0.295	0.329	0.438
1.00	0.212	0.233	0.268	0.382
3.00	0.009	0.033	0.073	0.202

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
SI	A	CD&~CP

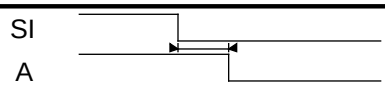
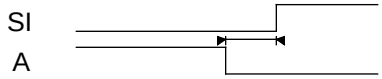
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.386	0.392	0.402	0.434
0.38	0.422	0.433	0.453	0.515
1.00	0.483	0.504	0.539	0.651
3.00	0.679	0.730	0.815	1.090

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.178	0.139	0.074	-0.134
0.38	0.152	0.109	0.038	-0.193
1.00	0.109	0.060	-0.023	-0.292
3.00	-0.029	-0.101	-0.221	-0.610

TIMING CONDITION

DATA	CLOCK	CONDITION
SI	A	CD&~CP

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

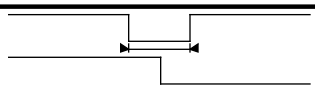
SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.485	0.523	0.588	0.797
0.38	0.511	0.553	0.625	0.855
1.00	0.555	0.604	0.686	0.952
3.00	0.696	0.767	0.885	1.266

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.269	0.263	0.253	0.221
0.38	0.233	0.221	0.202	0.140
1.00	0.173	0.152	0.117	0.004
3.00	-0.022	-0.073	-0.159	-0.435

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

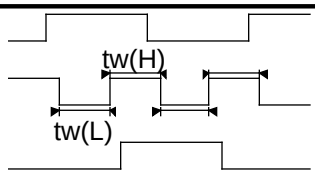
CLOCK	CONDITION
CD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.740

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	CD

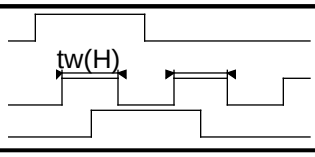
ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.720

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
B	CD

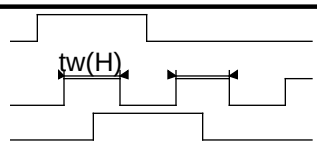
ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
A	CD

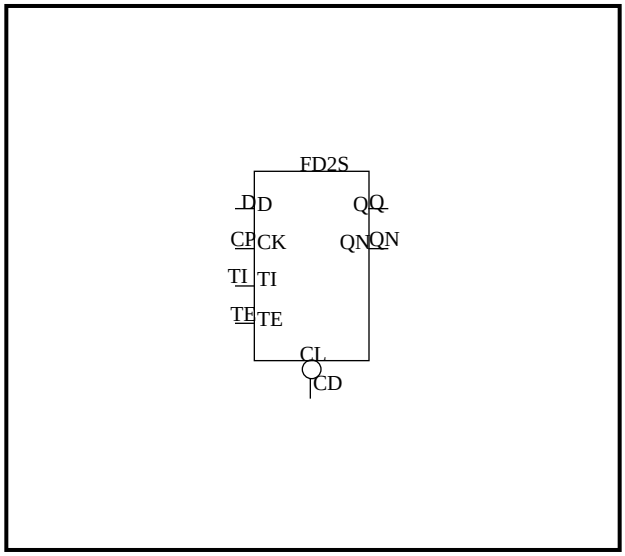
ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

FD2S	FD2S	1/8

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FD2S	D-TYPE FLIP FLOP with common single-phase SCAN clock with CLEAR	10	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT					OUTPUT	
CD	D	TI	TE	CP	Qn+1	QNn+1
L	X	X	X	X*	L	H
H	L	X	L	Up	L	H
H	H	X	L	Up	H	L
H	X	L	H	Up	L	H
H	X	H	H	Up	H	L
H	X	X	X	Dn	Qn	QNn

*:Consider the HOLD Time of CLEAR

Verilog-HDL DESCRIPTION

```
FD2S  inst(Q,QN,D,CP,CD,TI,TE);
```

VHDL DESCRIPTION

```
inst:FD2S
   port   map(Q,QN,D,CP,CD,TI,TE);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D,TI	0.99
CP	0.98
CD	2.26
TE	1.97

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	47.3	48.1

Rev.1.01.10

FD2S | FD2S | 2/8

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0393	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.38	0.51	0.98
0.38	0.28	0.41	0.54	1.01
1.00	0.35	0.48	0.61	1.08
3.00	0.49	0.63	0.76	1.24

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0865	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.60	0.75	1.36
0.38	0.49	0.62	0.78	1.38
1.00	0.56	0.69	0.85	1.45
3.00	0.73	0.86	1.01	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0881	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.69	0.85	1.47
0.38	0.63	0.77	0.93	1.55
1.00	0.71	0.85	1.01	1.63
3.00	0.87	1.01	1.17	1.79

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0393	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.57	0.70	0.83	1.30
0.38	0.65	0.78	0.91	1.38
1.00	0.73	0.86	0.99	1.46
3.00	0.88	1.01	1.14	1.61

FD2S | FD2S | 3/8

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0865	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.71	0.84	0.99	1.59
0.38	0.79	0.91	1.06	1.66
1.00	0.87	0.99	1.14	1.74
3.00	1.02	1.14	1.30	1.90

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	FALL

SLEW FACTOR

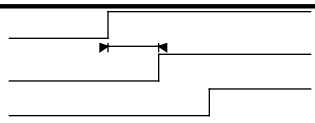
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0395	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.71	0.82	0.95	1.42
0.38	0.78	0.90	1.02	1.49
1.00	0.87	0.98	1.11	1.58
3.00	1.03	1.14	1.27	1.74

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

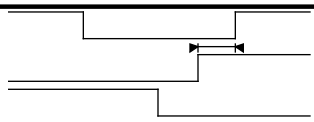
DATA	CLOCK	CONDITION
CD	CP	(~TE&D TE&TI)

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.050	-0.090	-0.157	-0.372
0.38	-0.055	-0.095	-0.161	-0.376
1.00	-0.063	-0.103	-0.169	-0.384
3.00	-0.091	-0.130	-0.195	-0.407

TIMING CONDITION

DATA	CLOCK	CONDITION
CD	CP	(~TE&D TE&TI)

ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

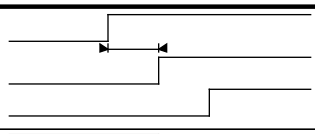
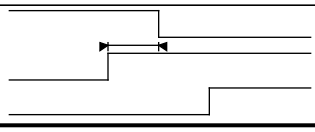
HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.706	0.745	0.812	1.028
0.38	0.711	0.750	0.817	1.032
1.00	0.719	0.759	0.825	1.039
3.00	0.747	0.786	0.852	1.063

FD2S	FD2S	5/8

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD&~TE

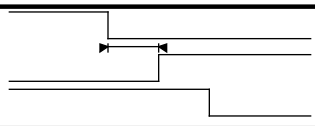
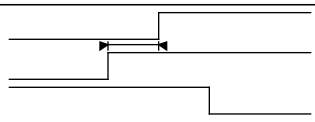
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.438	0.416	0.379	0.260
0.38	0.482	0.460	0.422	0.301
1.00	0.557	0.534	0.495	0.369
3.00	0.799	0.773	0.730	0.589

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.110	0.145	0.204	0.395
0.38	0.072	0.107	0.165	0.354
1.00	0.008	0.043	0.100	0.286
3.00	-0.197	-0.164	-0.109	0.067

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD&~TE

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.548	0.512	0.452	0.260
0.38	0.585	0.550	0.491	0.300
1.00	0.649	0.614	0.556	0.369
3.00	0.852	0.820	0.765	0.589

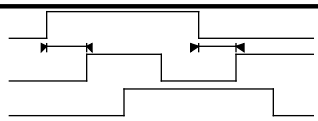
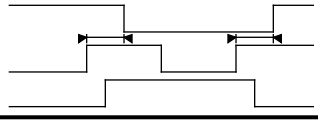
HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.220	0.241	0.277	0.394
0.38	0.175	0.197	0.234	0.353
1.00	0.099	0.122	0.161	0.286
3.00	-0.144	-0.118	-0.074	0.067

FD2S | FD2S | 6/8

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
TE	CP	CD&(~D&TI D&~TI)

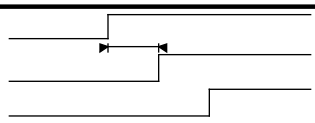
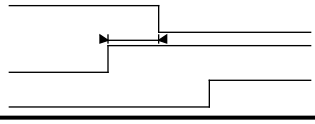
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	DCARE	
HOLD	POSEDGE	DCARE	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.479	0.457	0.420	0.302
0.38	0.530	0.507	0.470	0.349
1.00	0.616	0.593	0.554	0.428
3.00	0.893	0.867	0.823	0.683

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.179	0.200	0.237	0.353
0.38	0.127	0.149	0.187	0.306
1.00	0.041	0.064	0.103	0.227
3.00	-0.238	-0.211	-0.168	-0.026

TIMING CONDITION

DATA	CLOCK	CONDITION
TI	CP	CD&TE

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.512	0.490	0.454	0.337
0.38	0.551	0.529	0.492	0.373
1.00	0.617	0.594	0.556	0.432
3.00	0.828	0.803	0.761	0.624

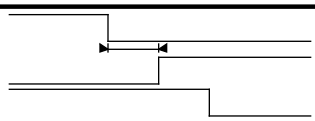
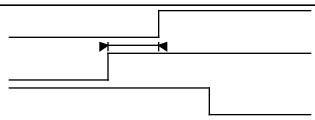
HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.008	0.025	0.081	0.262
0.38	-0.032	0.002	0.057	0.237
1.00	-0.071	-0.038	0.017	0.195
3.00	-0.197	-0.165	-0.111	0.061

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
TI	CP	CD&TE

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

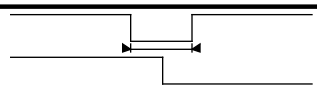
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.665	0.632	0.576	0.396
0.38	0.688	0.655	0.600	0.420
1.00	0.727	0.694	0.639	0.461
3.00	0.852	0.820	0.767	0.595

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.142	0.164	0.201	0.319
0.38	0.103	0.125	0.163	0.284
1.00	0.038	0.061	0.099	0.224
3.00	-0.173	-0.148	-0.105	0.032

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

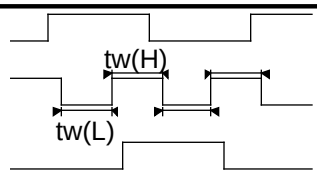
CLOCK	CONDITION
CD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.710

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	CD

ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

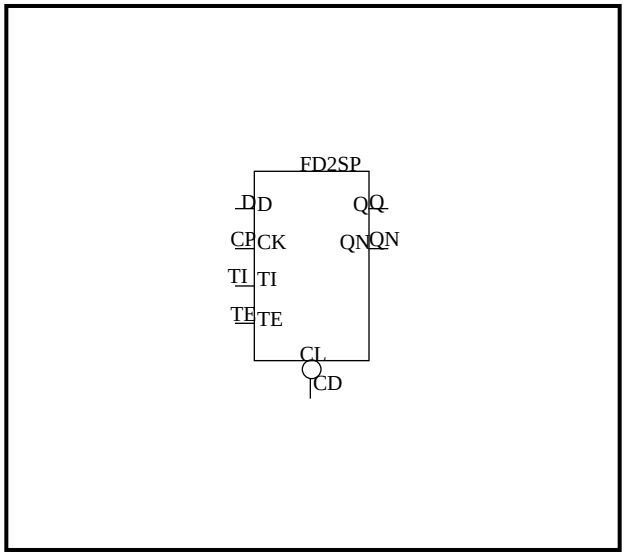
POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.760

FD2SP	FD2SP	1/8

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FD2SP	D-TYPE FLIP FLOP with common single-phase SCAN clock with CLEAR	11	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT					OUTPUT	
CD	D	TI	TE	CP	Qn+1	QNn+1
L	X	X	X	X*	L	H
H	L	X	L	Up	L	H
H	H	X	L	Up	H	L
H	X	L	H	Up	L	H
H	X	H	H	Up	H	L
H	X	X	X	Dn	Qn	QNn

*:Consider the HOLD Time of CLEAR

Verilog-HDL DESCRIPTION

```
FD2SP  inst(Q,QN,D,CP,CD,TI,TE);
```

VHDL DESCRIPTION

```
inst:FD2SP
   port   map(Q,QN,D,CP,CD,TI,TE);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q	QN
ELECTRO MIGRATION DRIVE	6880.0	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D,TI	0.99
CP	0.98
CD	2.26
TE	1.97

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	94.5	89.5

Rev.1.01.10

FD2SP | FD2SP | 2/8

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0197	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.34	0.41	0.67
0.38	0.28	0.36	0.44	0.69
1.00	0.35	0.43	0.51	0.77
3.00	0.51	0.60	0.68	0.94

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0442	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.60	0.68	1.01
0.38	0.55	0.62	0.71	1.03
1.00	0.62	0.70	0.78	1.11
3.00	0.81	0.88	0.97	1.29

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0442	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.56	0.64	0.73	1.05
0.38	0.64	0.72	0.80	1.13
1.00	0.72	0.80	0.89	1.21
3.00	0.88	0.96	1.05	1.37

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0197	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.58	0.66	0.74	0.99
0.38	0.66	0.74	0.81	1.07
1.00	0.74	0.82	0.89	1.15
3.00	0.89	0.97	1.04	1.30

FD2SP | FD2SP | 3/8

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0442	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.77	0.85	0.93	1.24
0.38	0.85	0.92	1.01	1.32
1.00	0.93	1.01	1.09	1.40
3.00	1.08	1.15	1.24	1.55

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0236	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.78	0.86	0.94	1.23
0.38	0.86	0.94	1.02	1.31
1.00	0.94	1.02	1.10	1.39
3.00	1.10	1.18	1.26	1.55

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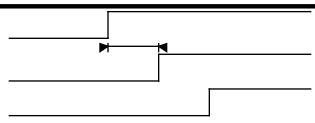
CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

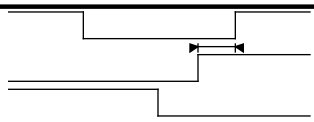
DATA	CLOCK	CONDITION
CD	CP	(~TE&D TE&TI)

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.050	-0.090	-0.157	-0.372
0.38	-0.055	-0.095	-0.161	-0.376
1.00	-0.063	-0.103	-0.169	-0.384
3.00	-0.091	-0.130	-0.195	-0.407

TIMING CONDITION

DATA	CLOCK	CONDITION
CD	CP	(~TE&D TE&TI)

ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

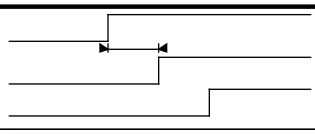
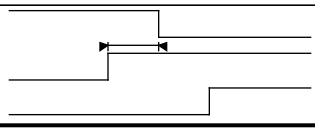
HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.706	0.745	0.812	1.028
0.38	0.711	0.750	0.817	1.032
1.00	0.719	0.759	0.825	1.039
3.00	0.747	0.786	0.852	1.063

FD2SP | FD2SP | 5/8

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD&~TE

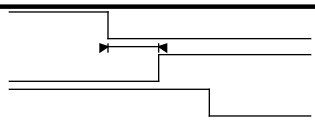
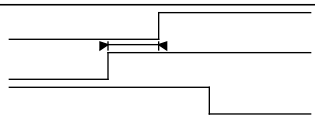
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.438	0.416	0.379	0.260
0.38	0.482	0.460	0.422	0.301
1.00	0.557	0.534	0.495	0.369
3.00	0.799	0.773	0.730	0.589

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.110	0.145	0.204	0.395
0.38	0.072	0.107	0.165	0.354
1.00	0.008	0.043	0.100	0.286
3.00	-0.197	-0.164	-0.109	0.067

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD&~TE

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

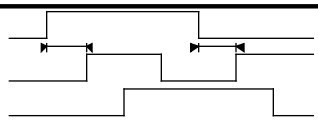
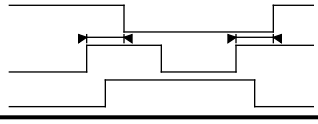
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.548	0.512	0.452	0.260
0.38	0.585	0.550	0.491	0.300
1.00	0.649	0.614	0.556	0.369
3.00	0.852	0.820	0.765	0.589

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.220	0.241	0.277	0.394
0.38	0.175	0.197	0.234	0.353
1.00	0.099	0.122	0.161	0.286
3.00	-0.144	-0.118	-0.074	0.067

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
TE	CP	CD&(~D&TI D&~TI)

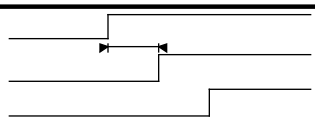
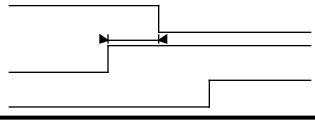
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	DCARE	
HOLD	POSEDGE	DCARE	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.479	0.457	0.420	0.302
0.38	0.530	0.507	0.470	0.349
1.00	0.616	0.593	0.554	0.428
3.00	0.893	0.867	0.823	0.683

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.179	0.200	0.237	0.353
0.38	0.127	0.149	0.187	0.306
1.00	0.041	0.064	0.103	0.227
3.00	-0.238	-0.211	-0.168	-0.026

TIMING CONDITION

DATA	CLOCK	CONDITION
TI	CP	CD&TE

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

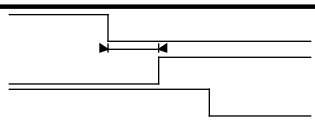
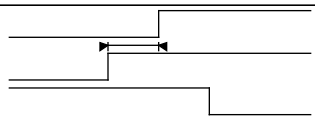
SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.512	0.490	0.454	0.337
0.38	0.551	0.529	0.492	0.373
1.00	0.617	0.594	0.556	0.432
3.00	0.828	0.803	0.761	0.624

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.008	0.025	0.081	0.262
0.38	-0.032	0.002	0.057	0.237
1.00	-0.071	-0.038	0.017	0.195
3.00	-0.197	-0.165	-0.111	0.061

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
TI	CP	CD&TE

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

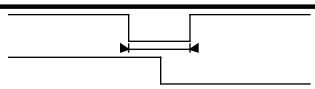
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.665	0.632	0.576	0.396
0.38	0.688	0.655	0.600	0.420
1.00	0.727	0.694	0.639	0.461
3.00	0.852	0.820	0.767	0.595

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.142	0.164	0.201	0.319
0.38	0.103	0.125	0.163	0.284
1.00	0.038	0.061	0.099	0.224
3.00	-0.173	-0.148	-0.105	0.032

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

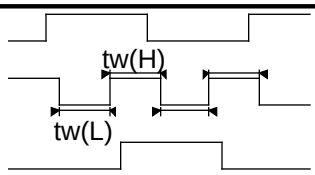
CLOCK	CONDITION
CD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.710

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	CD

ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

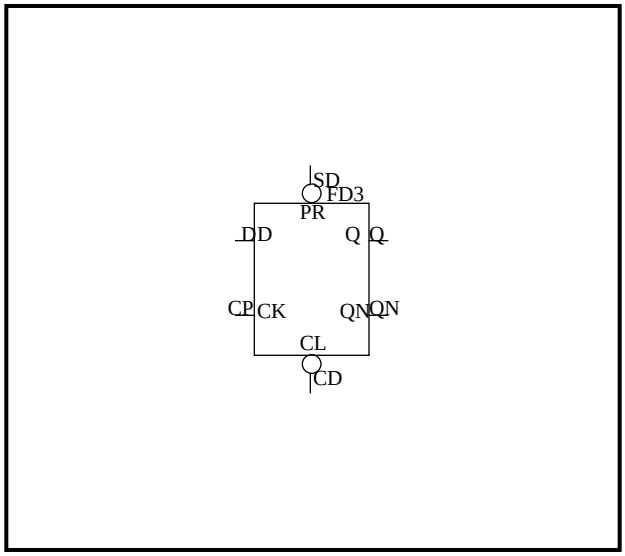
POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.760

FD3	FD3	1/8

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FD3	D-TYPE FLIP FLOP with CLEAR and PRESET	9	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT	
CD	SD	D	CP	Qn+1	QNn+1
L	H	X	X*	L	H
H	L	X	X*	H	L
L	L	X	X	L	L
H	H	L	Up	L	H
H	H	H	Up	H	L
H	H	X	Dn	Qn	QNn

*:Consider the HOLD Time of CLEAR or PRESET

Verilog-HDL DESCRIPTION

```
FD3  inst(Q,QN,D,CP,CD,SD);
```

VHDL DESCRIPTION

```
inst:FD3
   port   map(Q,QN,D,CP,CD,SD);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D,CP	0.99
CD	2.28
SD	2.18

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	47.0	48.3

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FD3 FD3 2/8

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0861	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.35	0.50	1.10
0.38	0.27	0.40	0.55	1.15
1.00	0.33	0.46	0.62	1.22
3.00	0.45	0.59	0.75	1.36

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0395	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.45	0.59	1.08
0.38	0.34	0.48	0.62	1.10
1.00	0.42	0.55	0.69	1.18
3.00	0.58	0.73	0.87	1.36

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0423	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.37	0.51	1.00
0.38	0.28	0.40	0.53	1.03
1.00	0.34	0.47	0.60	1.10
3.00	0.48	0.62	0.76	1.26

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0860	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.36	0.52	1.12
0.38	0.28	0.41	0.57	1.17
1.00	0.34	0.47	0.63	1.23
3.00	0.46	0.60	0.76	1.37

FD3 FD3 3/8

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0861	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.66	0.82	1.42
0.38	0.55	0.69	0.84	1.44
1.00	0.62	0.76	0.91	1.51
3.00	0.78	0.92	1.07	1.67

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0860	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.53	0.67	0.82	1.43
0.38	0.61	0.75	0.90	1.51
1.00	0.69	0.82	0.98	1.58
3.00	0.82	0.95	1.11	1.71

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0423	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.59	0.71	0.84	1.34
0.38	0.66	0.79	0.92	1.42
1.00	0.74	0.86	0.99	1.49
3.00	0.86	0.98	1.12	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0861	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.75	0.88	1.03	1.63
0.38	0.83	0.96	1.11	1.70
1.00	0.90	1.03	1.18	1.78
3.00	1.03	1.16	1.31	1.90

FD3 FD3 4/8

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0395	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.68	0.80	0.92	1.39
0.38	0.76	0.87	1.00	1.47
1.00	0.84	0.95	1.08	1.54
3.00	0.96	1.08	1.20	1.67

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0860	0.11

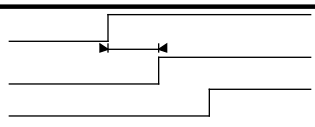
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.58	0.71	0.86	1.46
0.38	0.60	0.73	0.89	1.48
1.00	0.68	0.81	0.97	1.56
3.00	0.86	0.99	1.14	1.73

FD3	FD3	5/8

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

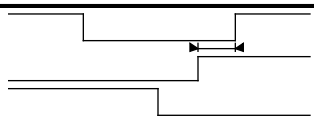
DATA	CLOCK	CONDITION
CD	CP	SD&D

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.050	-0.085	-0.145	-0.336
0.38	-0.057	-0.093	-0.152	-0.343
1.00	-0.069	-0.105	-0.164	-0.356
3.00	-0.109	-0.144	-0.204	-0.395

TIMING CONDITION

DATA	CLOCK	CONDITION
CD	CP	SD&D

ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

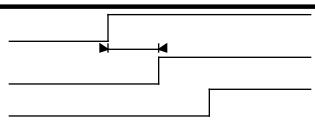
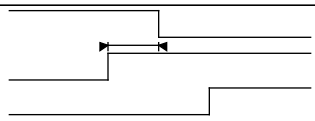
HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.706	0.741	0.800	0.992
0.38	0.713	0.748	0.808	1.000
1.00	0.725	0.760	0.820	1.012
3.00	0.764	0.800	0.859	1.052

FD3 FD3 6/8

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD&SD

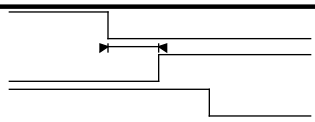
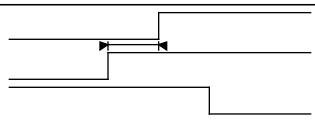
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.367	0.349	0.318	0.219
0.38	0.404	0.385	0.353	0.252
1.00	0.464	0.445	0.412	0.307
3.00	0.659	0.638	0.601	0.484

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.250	0.283	0.337	0.513
0.38	0.217	0.249	0.303	0.478
1.00	0.161	0.192	0.246	0.418
3.00	-0.020	0.010	0.061	0.225

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD&SD

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.407	0.375	0.320	0.144
0.38	0.441	0.408	0.354	0.180
1.00	0.497	0.465	0.411	0.239
3.00	0.677	0.646	0.595	0.431

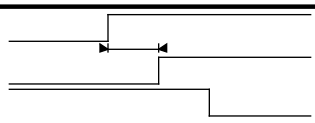
HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.290	0.308	0.338	0.435
0.38	0.254	0.272	0.303	0.402
1.00	0.193	0.212	0.244	0.348
3.00	-0.003	0.019	0.055	0.173

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

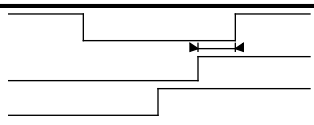
DATA	CLOCK	CONDITION
SD	CP	CD&~D

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.131	0.098	0.042	-0.137
0.38	0.160	0.127	0.072	-0.105
1.00	0.207	0.175	0.121	-0.052
3.00	0.360	0.331	0.281	0.120

TIMING CONDITION

DATA	CLOCK	CONDITION
SD	CP	CD&~D

ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

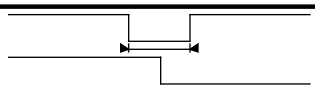
HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.523	0.556	0.612	0.793
0.38	0.495	0.528	0.583	0.761
1.00	0.448	0.480	0.534	0.708
3.00	0.296	0.326	0.375	0.535

FD3	FD3	8/8

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

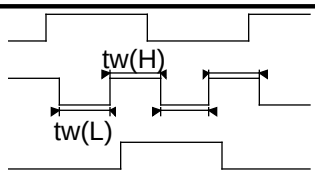
CLOCK	CONDITION
CD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.730

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	CD&SD

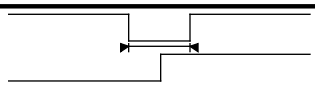
ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.760

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
SD	---

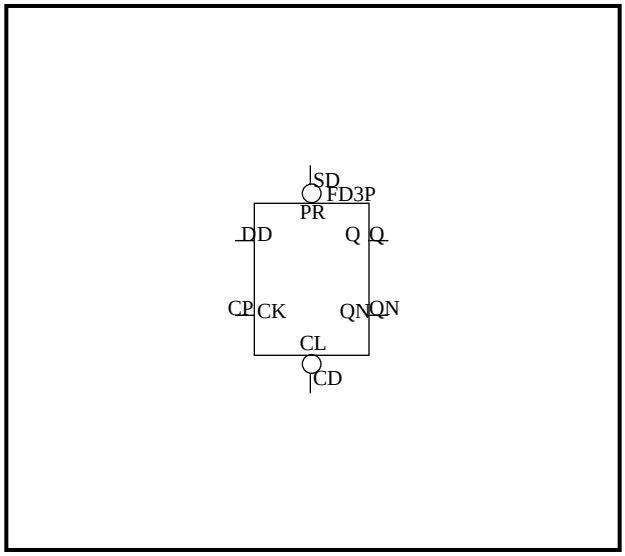
ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.780

FD3P	FD3P	1/8

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FD3P	D-TYPE FLIP FLOP with CLEAR and PRESET	10	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT	
CD	SD	D	CP	Qn+1	QNn+1
L	H	X	X*	L	H
H	L	X	X*	H	L
L	L	X	X	L	L
H	H	L	Up	L	H
H	H	H	Up	H	L
H	H	X	Dn	Qn	QNn

*:Consider the HOLD Time of CLEAR or PRESET

Verilog-HDL DESCRIPTION

```
FD3P  inst(Q,QN,D,CP,CD,SD);
```

VHDL DESCRIPTION

```
inst:FD3P
   port   map(Q,QN,D,CP,CD,SD);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q	QN
ELECTRO MIGRATION DRIVE	6880.0	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D,CP	0.99
CD	2.28
SD	2.18

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	89.1	98.0

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0440	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.30	0.38	0.70
0.38	0.28	0.35	0.43	0.75
1.00	0.35	0.42	0.51	0.82
3.00	0.49	0.57	0.66	0.98

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0179	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.40	0.48	0.74
0.38	0.34	0.43	0.51	0.76
1.00	0.42	0.50	0.58	0.84
3.00	0.59	0.68	0.77	1.03

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0238	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.33	0.42	0.71
0.38	0.28	0.36	0.44	0.74
1.00	0.35	0.43	0.51	0.81
3.00	0.50	0.59	0.68	0.98

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0441	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.31	0.39	0.71
0.38	0.28	0.36	0.44	0.76
1.00	0.35	0.43	0.51	0.83
3.00	0.49	0.57	0.66	0.98

FD3P | FD3P | 3/8

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0440	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.60	0.68	0.76	1.09
0.38	0.62	0.70	0.79	1.12
1.00	0.70	0.78	0.86	1.19
3.00	0.88	0.96	1.05	1.37

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0441	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.53	0.61	0.70	1.02
0.38	0.61	0.69	0.78	1.10
1.00	0.69	0.77	0.85	1.17
3.00	0.82	0.89	0.98	1.30

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0238	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.59	0.67	0.76	1.05
0.38	0.67	0.75	0.83	1.13
1.00	0.74	0.82	0.91	1.20
3.00	0.87	0.95	1.03	1.32

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0440	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.83	0.90	0.99	1.30
0.38	0.90	0.98	1.06	1.38
1.00	0.98	1.05	1.14	1.45
3.00	1.10	1.18	1.26	1.58

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0179	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.74	0.81	0.88	1.11
0.38	0.82	0.89	0.96	1.19
1.00	0.90	0.97	1.03	1.27
3.00	1.02	1.09	1.16	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->O	---	RISE

SLEW FACTOR

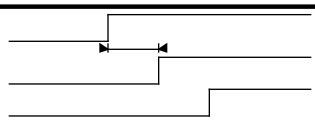
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0441	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.65	0.73	0.81	1.13
0.38	0.68	0.75	0.84	1.16
1.00	0.76	0.84	0.92	1.24
3.00	0.95	1.03	1.11	1.43

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

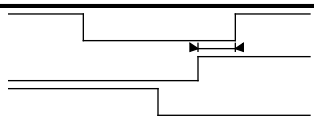
DATA	CLOCK	CONDITION
CD	CP	SD&D

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.050	-0.085	-0.145	-0.336
0.38	-0.057	-0.093	-0.152	-0.343
1.00	-0.069	-0.105	-0.164	-0.356
3.00	-0.109	-0.144	-0.204	-0.395

TIMING CONDITION

DATA	CLOCK	CONDITION
CD	CP	SD&D

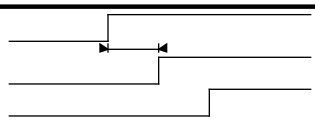
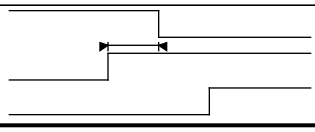
ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.706	0.741	0.800	0.992
0.38	0.713	0.748	0.808	1.000
1.00	0.725	0.760	0.820	1.012
3.00	0.764	0.800	0.859	1.052

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD&SD

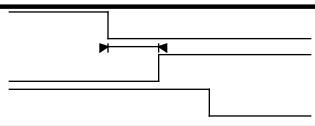
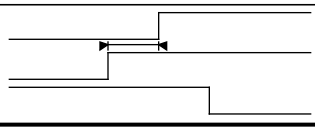
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.367	0.349	0.318	0.219
0.38	0.404	0.385	0.353	0.252
1.00	0.464	0.445	0.412	0.307
3.00	0.659	0.638	0.601	0.484

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.250	0.283	0.337	0.513
0.38	0.217	0.249	0.303	0.478
1.00	0.161	0.192	0.246	0.418
3.00	-0.020	0.010	0.061	0.225

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD&SD

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

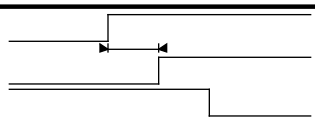
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.407	0.375	0.320	0.144
0.38	0.441	0.408	0.354	0.180
1.00	0.497	0.465	0.411	0.239
3.00	0.677	0.646	0.595	0.431

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.290	0.308	0.338	0.435
0.38	0.254	0.272	0.303	0.402
1.00	0.193	0.212	0.244	0.348
3.00	-0.003	0.019	0.055	0.173

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

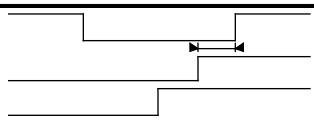
DATA	CLOCK	CONDITION
SD	CP	CD&~D

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.131	0.098	0.042	-0.137
0.38	0.160	0.127	0.072	-0.105
1.00	0.207	0.175	0.121	-0.052
3.00	0.360	0.331	0.281	0.120

TIMING CONDITION

DATA	CLOCK	CONDITION
SD	CP	CD&~D

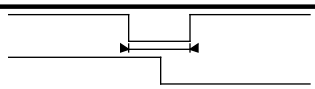
ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.523	0.556	0.612	0.793
0.38	0.495	0.528	0.583	0.761
1.00	0.448	0.480	0.534	0.708
3.00	0.296	0.326	0.375	0.535

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

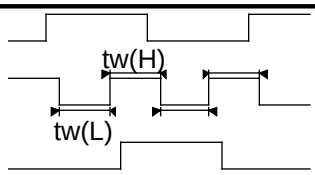
CLOCK	CONDITION
CD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.730

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	CD&SD

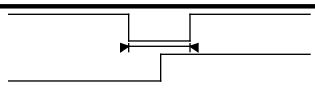
ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.760

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
SD	---

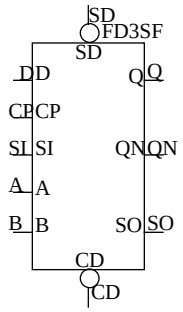
ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.780

FD3SF	FD3SF	1/15

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FD3SF	D-TYPE FLIP FLOP with Independent two-phase SCAN clock with CLEAR and PRESET	13	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT							OUTPUT		
CD	SD	D	SI	A	B	CP	Qn+1	QNn+1	SOn+1
X	X	X	X	X	L	X	X	X	SOn
L	L	X	X	L	H	X	L	L	L
L	H	X	X	L	H	X*	L	H	L
H	L	X	X	L	H	X*	H	L	H
H	H	X	L	H	H	L	L	H	L
H	H	X	H	H	H	L	H	L	H
H	H	L	X	L	H	Up	L	H	L
H	H	H	X	L	H	Up	H	L	H
H	H	X	X	L	H	Dn	Qn	QNn	Qn

*:Consider the HOLD Time of CLEAR or PRESET

Verilog-HDL DESCRIPTION

```
FD3SF  inst(Q,QN,SO,D,CP,CD,SD,SI,
A,B);
```

VHDL DESCRIPTION

```
inst:FD3SF
  port  map(Q,QN,SO,D,CP,CD,SD,
SI,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN,SO
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D,CP	0.99
CD,SD	2.28
SI	0.89
A	2.07
B	2.03

OUTPUT DRIVE (LU)

PIN NAME	Q	QN	SO
DRIVE	47.0	47.1	43.8

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&~A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.1005	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.64	0.82	1.50
0.38	0.53	0.67	0.85	1.53
1.00	0.60	0.74	0.91	1.59
3.00	0.77	0.91	1.08	1.76

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&~A	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0363	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.63	0.72	0.83	1.26
0.38	0.66	0.76	0.87	1.29
1.00	0.72	0.82	0.93	1.35
3.00	0.85	0.94	1.05	1.48

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.1005	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.43	0.57	0.74	1.42
0.38	0.52	0.65	0.83	1.51
1.00	0.64	0.78	0.95	1.63
3.00	0.76	0.90	1.07	1.75

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&A	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0363	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.55	0.66	1.08
0.38	0.53	0.63	0.74	1.16
1.00	0.64	0.74	0.85	1.27
3.00	0.82	0.92	1.03	1.45

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0862	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.65	0.81	1.41
0.38	0.61	0.74	0.90	1.50
1.00	0.74	0.88	1.03	1.64
3.00	0.86	1.00	1.15	1.76

PATH CONDITION

PATH	CONDITION	FUNCTION
A->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0423	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.50	0.62	0.76	1.25
0.38	0.58	0.71	0.84	1.34
1.00	0.69	0.81	0.94	1.44
3.00	0.86	0.99	1.12	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
A->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0861	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.67	0.80	0.95	1.54
0.38	0.75	0.88	1.03	1.62
1.00	0.85	0.98	1.13	1.73
3.00	1.03	1.16	1.31	1.90

PATH CONDITION

PATH	CONDITION	FUNCTION
A->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0403	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.67	0.79	0.91	1.38
0.38	0.76	0.88	1.00	1.47
1.00	0.90	1.01	1.14	1.61
3.00	1.01	1.13	1.26	1.73

FD3SF | FD3SF | 4/15

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.1005	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.45	0.61	1.28
0.38	0.40	0.54	0.71	1.38
1.00	0.50	0.64	0.81	1.48
3.00	0.61	0.75	0.92	1.58

PATH CONDITION

PATH	CONDITION	FUNCTION
B->SO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0363	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.38	0.49	0.91
0.38	0.36	0.45	0.56	0.98
1.00	0.42	0.52	0.63	1.05
3.00	0.52	0.62	0.74	1.19

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0861	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.51	0.69	1.32
0.38	0.40	0.56	0.74	1.38
1.00	0.49	0.65	0.83	1.46
3.00	0.71	0.86	1.04	1.67

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0403	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.44	0.62	0.79	1.32
0.38	0.47	0.65	0.81	1.35
1.00	0.55	0.73	0.89	1.42
3.00	0.77	0.95	1.11	1.65

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0423	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.38	0.52	1.01
0.38	0.28	0.41	0.54	1.04
1.00	0.35	0.48	0.61	1.11
3.00	0.49	0.63	0.77	1.27

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0862	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.37	0.52	1.12
0.38	0.28	0.42	0.57	1.17
1.00	0.34	0.48	0.63	1.24
3.00	0.47	0.61	0.77	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0861	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.61	0.79	0.97	1.62
0.38	0.64	0.82	1.00	1.65
1.00	0.71	0.89	1.07	1.72
3.00	0.88	1.06	1.24	1.88

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->SO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0363	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.05	1.15	1.26	1.69
0.38	1.08	1.18	1.29	1.71
1.00	1.15	1.25	1.36	1.78
3.00	1.32	1.41	1.52	1.95

FD3SF | FD3SF | 6/15

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0862	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.53	0.67	0.82	1.43
0.38	0.61	0.75	0.90	1.51
1.00	0.69	0.83	0.98	1.59
3.00	0.82	0.96	1.11	1.72

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0423	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.59	0.71	0.84	1.34
0.38	0.67	0.79	0.92	1.42
1.00	0.74	0.86	1.00	1.49
3.00	0.86	0.99	1.12	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0861	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.89	1.05	1.22	1.85
0.38	0.96	1.12	1.30	1.93
1.00	1.04	1.20	1.37	2.00
3.00	1.16	1.32	1.49	2.12

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0403	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.85	1.00	1.16	1.69
0.38	0.93	1.08	1.24	1.77
1.00	1.00	1.16	1.32	1.84
3.00	1.13	1.29	1.44	1.97

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.1005	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.14	1.28	1.45	2.13
0.38	1.22	1.36	1.53	2.21
1.00	1.29	1.43	1.61	2.29
3.00	1.42	1.56	1.73	2.41

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->SO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0363	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.23	1.33	1.44	1.86
0.38	1.31	1.41	1.52	1.94
1.00	1.38	1.48	1.59	2.01
3.00	1.50	1.60	1.71	2.13

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0862	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.92	1.06	1.21	1.81
0.38	0.95	1.09	1.24	1.84
1.00	1.02	1.16	1.31	1.91
3.00	1.24	1.38	1.53	2.13

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.1005	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.79	0.93	1.11	1.79
0.38	0.82	0.96	1.13	1.81
1.00	0.89	1.03	1.20	1.89
3.00	1.11	1.25	1.42	2.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0862	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.62	0.78	1.38
0.38	0.53	0.66	0.82	1.42
1.00	0.61	0.75	0.91	1.51
3.00	0.80	0.94	1.10	1.71

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0423	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.60	0.74	1.24
0.38	0.48	0.61	0.74	1.24
1.00	0.53	0.65	0.78	1.28
3.00	0.62	0.76	0.90	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0861	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.65	0.78	0.93	1.52
0.38	0.65	0.78	0.93	1.53
1.00	0.69	0.82	0.97	1.57
3.00	0.81	0.94	1.09	1.68

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0403	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.64	0.76	0.88	1.35
0.38	0.68	0.80	0.92	1.39
1.00	0.77	0.89	1.01	1.48
3.00	0.96	1.08	1.21	1.68

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.1005	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.50	0.67	1.35
0.38	0.39	0.53	0.70	1.39
1.00	0.44	0.58	0.75	1.43
3.00	0.52	0.66	0.83	1.52

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->SO	---	FALL

SLEW FACTOR

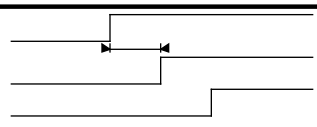
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0363	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.47	0.58	1.00
0.38	0.38	0.48	0.58	1.01
1.00	0.43	0.53	0.64	1.06
3.00	0.55	0.65	0.76	1.19

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

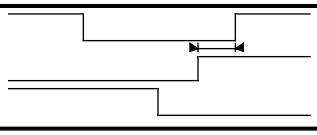
DATA	CLOCK	CONDITION
CD	CP	SD&D&~A

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.050	-0.085	-0.143	-0.331
0.38	-0.057	-0.092	-0.150	-0.339
1.00	-0.069	-0.104	-0.163	-0.351
3.00	-0.109	-0.144	-0.202	-0.390

TIMING CONDITION

DATA	CLOCK	CONDITION
CD	CP	SD&D&~A

ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

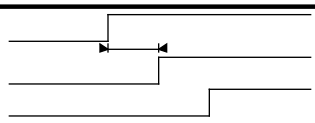
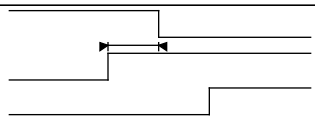
HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.706	0.740	0.798	0.986
0.38	0.713	0.747	0.806	0.993
1.00	0.725	0.760	0.818	1.006
3.00	0.764	0.799	0.857	1.045

FD3SF	FD3SF	11/15

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD&SD&~A

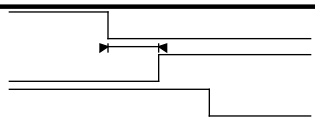
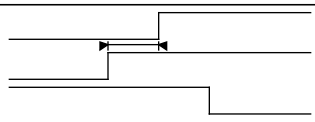
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.367	0.349	0.318	0.219
0.38	0.404	0.385	0.353	0.252
1.00	0.464	0.445	0.412	0.307
3.00	0.659	0.638	0.601	0.484

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.250	0.283	0.337	0.513
0.38	0.217	0.249	0.303	0.478
1.00	0.161	0.192	0.246	0.418
3.00	-0.020	0.010	0.061	0.225

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD&SD&~A

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.407	0.375	0.320	0.144
0.38	0.441	0.408	0.354	0.180
1.00	0.497	0.465	0.411	0.239
3.00	0.677	0.646	0.595	0.431

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.290	0.308	0.338	0.435
0.38	0.254	0.272	0.303	0.402
1.00	0.193	0.212	0.244	0.348
3.00	-0.003	0.019	0.055	0.173

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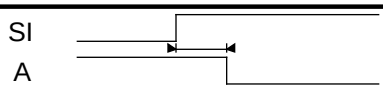
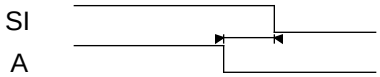
CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
SI	A	CD&SD&~CP

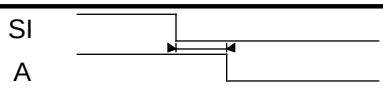
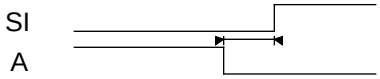
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.432	0.441	0.455	0.499
0.38	0.477	0.490	0.512	0.583
1.00	0.551	0.572	0.608	0.724
3.00	0.790	0.838	0.918	1.178

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.170	0.131	0.065	-0.147
0.38	0.151	0.107	0.033	-0.204
1.00	0.118	0.066	-0.020	-0.300
3.00	0.012	-0.065	-0.194	-0.610

TIMING CONDITION

DATA	CLOCK	CONDITION
SI	A	CD&SD&~CP

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

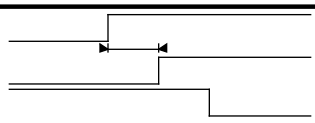
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.485	0.525	0.592	0.810
0.38	0.506	0.551	0.626	0.866
1.00	0.543	0.595	0.681	0.961
3.00	0.662	0.736	0.862	1.266

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.222	0.214	0.201	0.156
0.38	0.178	0.165	0.143	0.072
1.00	0.104	0.083	0.047	-0.068
3.00	-0.134	-0.182	-0.263	-0.523

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

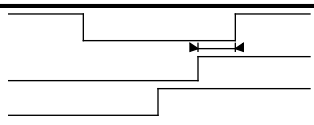
DATA	CLOCK	CONDITION
SD	CP	CD&~D&~A

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.131	0.098	0.042	-0.137
0.38	0.160	0.127	0.072	-0.106
1.00	0.207	0.175	0.121	-0.054
3.00	0.360	0.330	0.279	0.115

TIMING CONDITION

DATA	CLOCK	CONDITION
SD	CP	CD&~D&~A

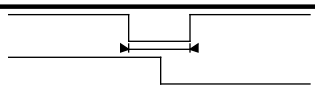
ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.523	0.556	0.612	0.793
0.38	0.495	0.528	0.583	0.762
1.00	0.448	0.480	0.534	0.710
3.00	0.296	0.326	0.377	0.542

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

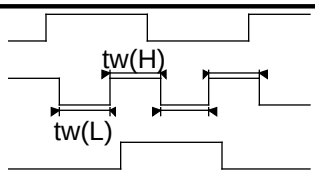
CLOCK	CONDITION
CD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.810

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	CD&SD

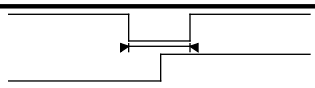
ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.760

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
SD	---

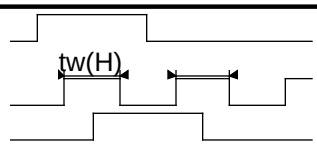
ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.930

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

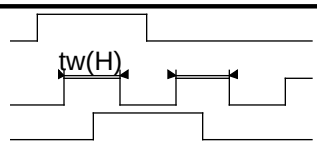
CLOCK	CONDITION
B	CD&SD

ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
A	CD&SD

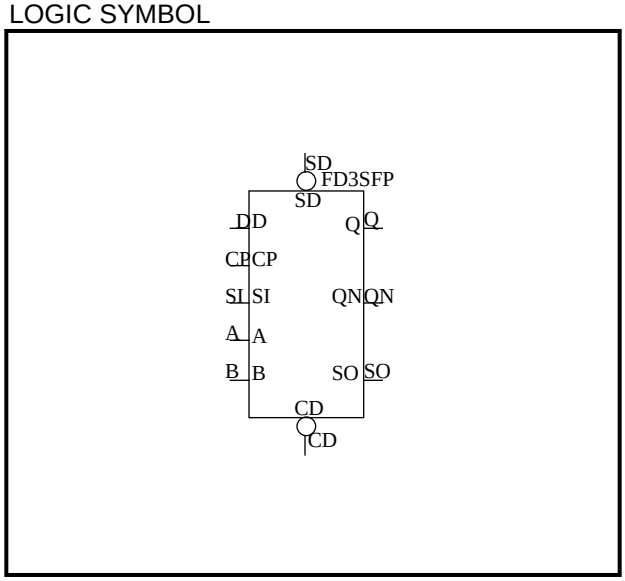
ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

FD3SFP	FD3SFP	1/15

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FD3SFP	D-TYPE FLIP FLOP with Independent two-phase SCAN clock with CLEAR and PRESET	14	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT							OUTPUT		
CD	SD	D	SI	A	B	CP	Qn+1	QNn+1	SOn+1
X	X	X	X	X	L	X	X	X	SOn
L	L	X	X	L	H	X	L	L	L
L	H	X	X	L	H	X*	L	H	L
H	L	X	X	L	H	X*	H	L	H
H	H	X	L	H	H	L	L	H	L
H	H	X	H	H	H	L	H	L	H
H	H	L	X	L	H	Up	L	H	L
H	H	H	X	L	H	Up	H	L	H
H	H	X	X	L	H	Dn	Qn	QNn	Qn

*:Consider the HOLD Time of CLEAR or PRESET

Verilog-HDL DESCRIPTION

```
FD3SFP  inst(Q,QN,SO,D,CP,CD,SD,
SI,A,B);
```

VHDL DESCRIPTION

```
inst:FD3SFP
  port  map(Q,QN,SO,D,CP,CD,SD,
SI,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN,SO
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D,CP	0.99
CD	2.28
SD	2.27
SI	0.92
A	2.10
B	2.02

OUTPUT DRIVE (LU)

PIN NAME	Q	QN	SO
DRIVE	87.7	90.5	42.6

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&~A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.1005	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.65	0.82	1.50
0.38	0.54	0.68	0.85	1.53
1.00	0.61	0.75	0.92	1.60
3.00	0.79	0.92	1.09	1.77

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&~A	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0400	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.66	0.76	0.88	1.34
0.38	0.69	0.79	0.91	1.38
1.00	0.75	0.85	0.97	1.44
3.00	0.88	0.99	1.11	1.57

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.1005	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.44	0.57	0.74	1.42
0.38	0.53	0.66	0.83	1.51
1.00	0.66	0.80	0.96	1.64
3.00	0.79	0.92	1.09	1.77

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&A	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0400	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.56	0.68	1.14
0.38	0.54	0.64	0.76	1.23
1.00	0.65	0.75	0.87	1.33
3.00	0.83	0.94	1.06	1.52

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0464	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.53	0.61	0.70	1.03
0.38	0.63	0.70	0.79	1.12
1.00	0.76	0.84	0.93	1.26
3.00	0.90	0.97	1.06	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
A->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0226	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.58	0.67	0.95
0.38	0.59	0.67	0.75	1.03
1.00	0.69	0.77	0.85	1.14
3.00	0.87	0.95	1.03	1.32

PATH CONDITION

PATH	CONDITION	FUNCTION
A->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0432	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.75	0.83	0.91	1.22
0.38	0.83	0.91	0.99	1.31
1.00	0.94	1.01	1.10	1.41
3.00	1.12	1.19	1.28	1.59

PATH CONDITION

PATH	CONDITION	FUNCTION
A->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0213	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.75	0.82	0.89	1.14
0.38	0.84	0.91	0.98	1.23
1.00	0.98	1.05	1.12	1.37
3.00	1.11	1.18	1.25	1.50

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.1005	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.45	0.62	1.28
0.38	0.41	0.55	0.71	1.38
1.00	0.52	0.66	0.82	1.49
3.00	0.64	0.77	0.94	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION
B->SO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0400	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.39	0.51	0.97
0.38	0.36	0.47	0.58	1.05
1.00	0.42	0.53	0.65	1.12
3.00	0.52	0.64	0.77	1.25

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0432	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.46	0.57	0.91
0.38	0.43	0.52	0.62	0.97
1.00	0.53	0.62	0.72	1.06
3.00	0.77	0.86	0.95	1.30

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0213	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.43	0.54	0.64	0.96
0.38	0.46	0.57	0.67	0.98
1.00	0.53	0.64	0.75	1.06
3.00	0.75	0.86	0.97	1.28

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0226	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.33	0.41	0.70
0.38	0.28	0.36	0.44	0.72
1.00	0.35	0.43	0.51	0.80
3.00	0.49	0.58	0.67	0.96

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0464	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.31	0.40	0.73
0.38	0.28	0.36	0.45	0.78
1.00	0.35	0.43	0.52	0.85
3.00	0.49	0.57	0.67	1.00

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0432	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.71	0.81	0.92	1.28
0.38	0.74	0.84	0.95	1.31
1.00	0.81	0.91	1.02	1.38
3.00	1.00	1.10	1.20	1.57

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->SO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0400	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.20	1.30	1.42	1.88
0.38	1.22	1.33	1.45	1.91
1.00	1.30	1.40	1.52	1.98
3.00	1.48	1.58	1.70	2.17

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0464	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.54	0.62	0.71	1.04
0.38	0.62	0.70	0.78	1.11
1.00	0.70	0.77	0.86	1.19
3.00	0.82	0.90	0.99	1.32

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0226	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.59	0.67	0.75	1.03
0.38	0.67	0.75	0.83	1.11
1.00	0.74	0.82	0.90	1.18
3.00	0.87	0.94	1.02	1.30

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0432	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.98	1.07	1.17	1.52
0.38	1.06	1.15	1.25	1.60
1.00	1.13	1.22	1.32	1.67
3.00	1.25	1.34	1.44	1.79

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0213	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.89	0.99	1.09	1.38
0.38	0.97	1.07	1.17	1.46
1.00	1.05	1.15	1.24	1.54
3.00	1.18	1.27	1.37	1.67

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.1005	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.26	1.40	1.56	2.24
0.38	1.34	1.47	1.64	2.32
1.00	1.41	1.55	1.72	2.40
3.00	1.54	1.68	1.85	2.52

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->SO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0400	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.37	1.48	1.60	2.06
0.38	1.45	1.56	1.68	2.14
1.00	1.53	1.63	1.75	2.21
3.00	1.65	1.75	1.87	2.33

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0464	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.01	1.09	1.18	1.51
0.38	1.04	1.12	1.21	1.54
1.00	1.11	1.18	1.27	1.60
3.00	1.33	1.41	1.50	1.83

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.1005	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.86	1.00	1.17	1.84
0.38	0.88	1.02	1.19	1.87
1.00	0.95	1.09	1.26	1.94
3.00	1.17	1.31	1.48	2.16

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0464	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.50	0.58	0.67	1.00
0.38	0.54	0.62	0.71	1.04
1.00	0.63	0.71	0.80	1.13
3.00	0.84	0.92	1.01	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0226	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.56	0.64	0.93
0.38	0.49	0.57	0.65	0.93
1.00	0.53	0.61	0.69	0.97
3.00	0.64	0.72	0.81	1.10

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0432	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.73	0.80	0.89	1.20
0.38	0.73	0.81	0.89	1.20
1.00	0.78	0.85	0.93	1.25
3.00	0.91	0.99	1.07	1.39

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0213	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.71	0.79	0.86	1.11
0.38	0.75	0.82	0.90	1.15
1.00	0.85	0.92	0.99	1.24
3.00	1.06	1.13	1.21	1.46

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.1005	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.50	0.67	1.35
0.38	0.40	0.54	0.71	1.39
1.00	0.45	0.59	0.76	1.44
3.00	0.54	0.68	0.85	1.53

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->SO	---	FALL

SLEW FACTOR

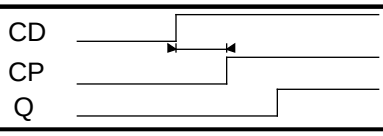
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0400	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.38	0.48	0.60	1.06
0.38	0.39	0.49	0.61	1.07
1.00	0.44	0.54	0.66	1.12
3.00	0.54	0.65	0.77	1.23

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

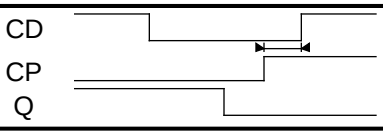
DATA	CLOCK	CONDITION
CD	CP	SD&D&~A

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.050	-0.085	-0.143	-0.331
0.38	-0.057	-0.092	-0.150	-0.339
1.00	-0.069	-0.104	-0.163	-0.351
3.00	-0.109	-0.144	-0.202	-0.390

TIMING CONDITION

DATA	CLOCK	CONDITION
CD	CP	SD&D&~A

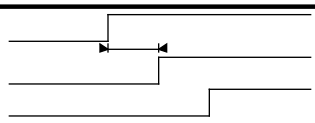
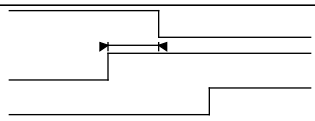
ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.706	0.740	0.798	0.986
0.38	0.713	0.747	0.806	0.993
1.00	0.725	0.760	0.818	1.006
3.00	0.764	0.799	0.857	1.045

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD&SD&~A

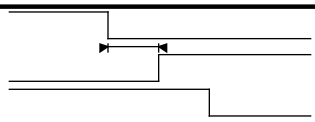
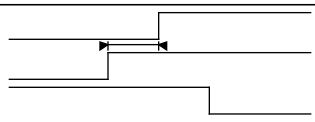
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.367	0.349	0.318	0.219
0.38	0.404	0.385	0.353	0.252
1.00	0.464	0.445	0.412	0.307
3.00	0.659	0.638	0.601	0.484

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.250	0.283	0.337	0.513
0.38	0.217	0.249	0.303	0.478
1.00	0.161	0.192	0.246	0.418
3.00	-0.020	0.010	0.061	0.225

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD&SD&~A

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

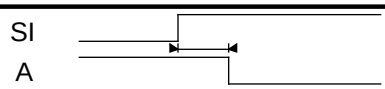
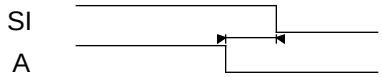
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.407	0.375	0.320	0.144
0.38	0.441	0.408	0.354	0.180
1.00	0.497	0.465	0.411	0.239
3.00	0.677	0.646	0.595	0.431

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.290	0.308	0.338	0.435
0.38	0.254	0.272	0.303	0.402
1.00	0.193	0.212	0.244	0.348
3.00	-0.003	0.019	0.055	0.173

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
SI	A	CD&SD&~CP

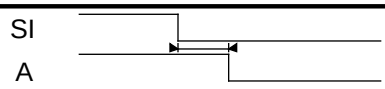
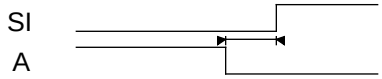
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.432	0.441	0.455	0.499
0.38	0.477	0.490	0.512	0.583
1.00	0.551	0.572	0.608	0.724
3.00	0.790	0.838	0.918	1.178

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.170	0.131	0.065	-0.147
0.38	0.151	0.107	0.033	-0.204
1.00	0.118	0.066	-0.020	-0.300
3.00	0.012	-0.065	-0.194	-0.610

TIMING CONDITION

DATA	CLOCK	CONDITION
SI	A	CD&SD&~CP

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

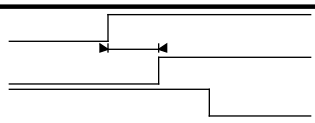
SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.485	0.525	0.592	0.810
0.38	0.506	0.551	0.626	0.866
1.00	0.543	0.595	0.681	0.961
3.00	0.662	0.736	0.862	1.266

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.222	0.214	0.201	0.156
0.38	0.178	0.165	0.143	0.072
1.00	0.104	0.083	0.047	-0.068
3.00	-0.134	-0.182	-0.263	-0.523

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

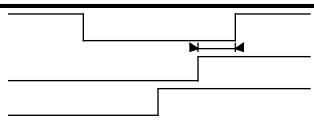
DATA	CLOCK	CONDITION
SD	CP	CD&~D&~A

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.131	0.098	0.042	-0.137
0.38	0.160	0.127	0.072	-0.106
1.00	0.207	0.175	0.121	-0.054
3.00	0.360	0.330	0.279	0.115

TIMING CONDITION

DATA	CLOCK	CONDITION
SD	CP	CD&~D&~A

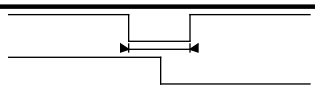
ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.523	0.556	0.612	0.793
0.38	0.495	0.528	0.583	0.762
1.00	0.448	0.480	0.534	0.710
3.00	0.296	0.326	0.377	0.542

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

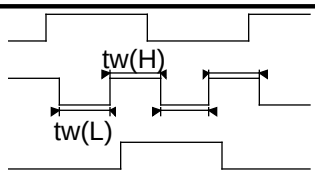
CLOCK	CONDITION
CD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.810

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	CD&SD

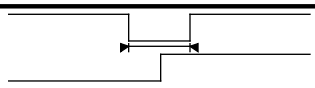
ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.760

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
SD	---

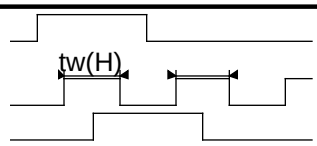
ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.930

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

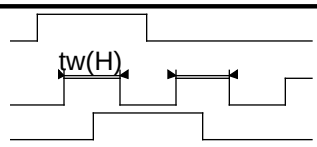
CLOCK	CONDITION
B	CD&SD

ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
A	CD&SD

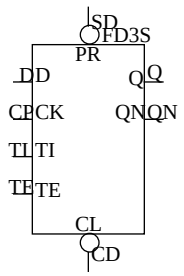
ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

FD3S	FD3S	1/10

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FD3S	D-TYPE FLIP FLOP with common single-phase SCAN clock with CLEAR and PRESET	11	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT						OUTPUT	
CD	SD	D	TI	TE	CP	Qn+1	QNn+1
L	H	X	X	X	X*	L	H
H	L	X	X	X	X*	H	L
L	L	X	X	X	X	L	L
H	H	L	X	L	Up	L	H
H	H	H	X	L	Up	H	L
H	H	X	L	H	Up	L	H
H	H	X	H	H	Up	H	L
H	H	X	X	X	Dn	Qn	QNn

*:Consider the HOLD Time of CLEAR or PRESET

Verilog-HDL DESCRIPTION

```
FD3S  inst(Q,QN,D,CP,CD,SD,TI,TE);
```

VHDL DESCRIPTION

```
inst:FD3S
  port  map(Q,QN,D,CP,CD,SD,TI,
            TE);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D,TI	0.99
CP	0.98
CD	2.28
SD	2.18
TE	1.97

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	47.1	48.3

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0862	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.35	0.51	1.11
0.38	0.27	0.41	0.56	1.16
1.00	0.34	0.47	0.62	1.23
3.00	0.46	0.60	0.75	1.36

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0395	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.46	0.60	1.08
0.38	0.35	0.49	0.63	1.11
1.00	0.42	0.56	0.70	1.19
3.00	0.59	0.74	0.88	1.37

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0428	0.82

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.00	0.00	0.01	0.50
0.38	0.00	0.00	0.06	0.70
1.00	0.11	0.72	0.90	1.12
3.00	0.80	0.78	0.80	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0861	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.36	0.52	1.12
0.38	0.28	0.41	0.57	1.17
1.00	0.34	0.48	0.63	1.23
3.00	0.46	0.60	0.76	1.38

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0862	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	-0.21	-0.16	0.10	0.80
0.38	-0.20	0.13	0.38	1.11
1.00	0.78	0.79	0.86	1.47
3.00	0.56	0.66	0.93	1.64

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0861	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.68	0.84	1.44
0.38	0.63	0.76	0.92	1.52
1.00	0.71	0.84	1.00	1.61
3.00	0.87	1.00	1.16	1.76

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0428	0.82

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.58	0.71	0.84	1.34
0.38	0.66	0.79	0.92	1.42
1.00	0.74	0.87	1.00	1.49
3.00	0.89	1.01	1.15	1.64

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0862	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.75	0.88	1.03	1.63
0.38	0.83	0.96	1.11	1.71
1.00	0.91	1.04	1.19	1.79
3.00	1.06	1.19	1.34	1.93

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0395	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.69	0.81	0.93	1.40
0.38	0.77	0.89	1.01	1.48
1.00	0.86	0.97	1.10	1.56
3.00	1.01	1.13	1.25	1.72

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->O	---	RISE

SLEW FACTOR

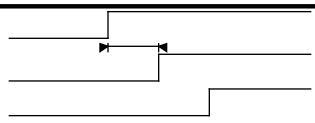
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0861	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.58	0.71	0.87	1.46
0.38	0.61	0.74	0.89	1.49
1.00	0.69	0.82	0.97	1.57
3.00	0.87	1.00	1.15	1.75

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

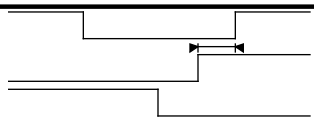
DATA	CLOCK	CONDITION
CD	CP	SD&(~TE&D TE&TI)

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.061	-0.101	-0.167	-0.383
0.38	-0.067	-0.107	-0.174	-0.389
1.00	-0.078	-0.118	-0.185	-0.399
3.00	-0.114	-0.153	-0.219	-0.431

TIMING CONDITION

DATA	CLOCK	CONDITION
CD	CP	SD&(~TE&D TE&TI)

ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

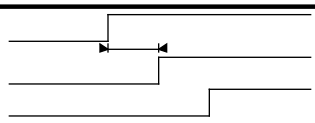
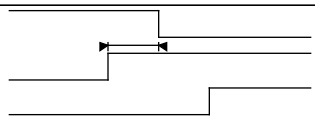
HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.718	0.758	0.825	1.040
0.38	0.725	0.764	0.831	1.046
1.00	0.735	0.775	0.841	1.055
3.00	0.771	0.810	0.875	1.086

FD3S | FD3S | 6/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD&SD&~TE

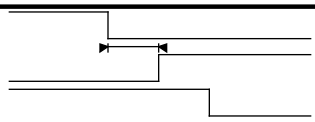
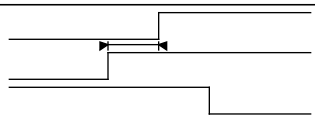
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.438	0.416	0.379	0.260
0.38	0.482	0.460	0.422	0.301
1.00	0.557	0.534	0.495	0.369
3.00	0.799	0.773	0.730	0.589

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.068	0.104	0.163	0.354
0.38	0.030	0.065	0.124	0.314
1.00	-0.035	-0.000	0.058	0.246
3.00	-0.243	-0.210	-0.154	0.026

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD&SD&~TE

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.588	0.553	0.493	0.302
0.38	0.627	0.592	0.533	0.342
1.00	0.691	0.656	0.598	0.410
3.00	0.899	0.866	0.810	0.630

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.220	0.241	0.277	0.394
0.38	0.175	0.197	0.234	0.353
1.00	0.099	0.122	0.161	0.286
3.00	-0.144	-0.118	-0.074	0.067

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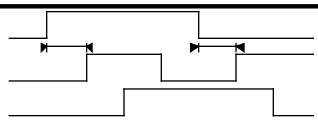
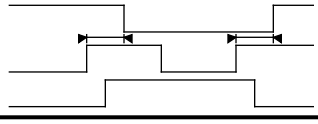
FD3S | FD3S | 7/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
TE	CP	CD&SD&(~D&TI D&~TI)

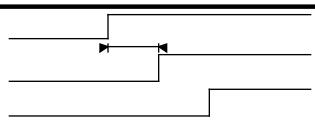
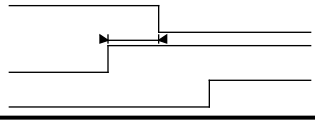
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	DCARE	
HOLD	POSEDGE	DCARE	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.479	0.457	0.420	0.302
0.38	0.530	0.507	0.470	0.349
1.00	0.616	0.593	0.554	0.428
3.00	0.893	0.867	0.823	0.683

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.179	0.200	0.237	0.353
0.38	0.127	0.149	0.187	0.306
1.00	0.041	0.064	0.103	0.227
3.00	-0.238	-0.211	-0.168	-0.026

TIMING CONDITION

DATA	CLOCK	CONDITION
TI	CP	CD&SD&TE

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.512	0.490	0.454	0.337
0.38	0.551	0.529	0.492	0.373
1.00	0.615	0.592	0.554	0.432
3.00	0.823	0.798	0.757	0.624

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.056	-0.023	0.033	0.214
0.38	-0.079	-0.046	0.010	0.189
1.00	-0.118	-0.085	-0.030	0.148
3.00	-0.243	-0.211	-0.158	0.015

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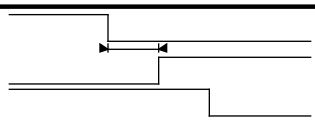
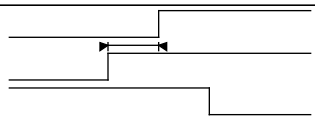
CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
TI	CP	CD&SD&TE

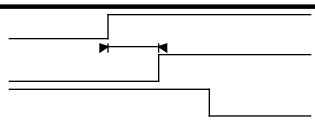
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.710	0.677	0.622	0.443
0.38	0.734	0.701	0.646	0.467
1.00	0.773	0.740	0.685	0.509
3.00	0.899	0.868	0.814	0.642

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.142	0.164	0.201	0.319
0.38	0.104	0.126	0.163	0.284
1.00	0.039	0.062	0.101	0.224
3.00	-0.168	-0.143	-0.102	0.032

TIMING CONDITION

DATA	CLOCK	CONDITION
SD	CP	CD&(~TE&~DTE&~TI)

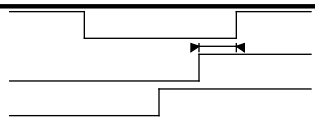
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.131	0.094	0.031	-0.172
0.38	0.159	0.122	0.059	-0.141
1.00	0.205	0.169	0.108	-0.089
3.00	0.354	0.320	0.263	0.079

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
SD	CP	CD&(~TE&~D TE&~TI)

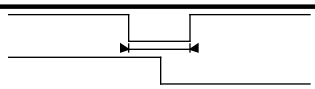
ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.523	0.561	0.624	0.829
0.38	0.495	0.533	0.596	0.798
1.00	0.450	0.486	0.547	0.745
3.00	0.302	0.336	0.393	0.576

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

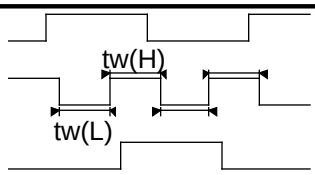
CLOCK	CONDITION
CD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.730

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	CD&SD

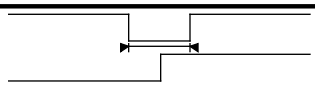
ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.790

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
SD	---

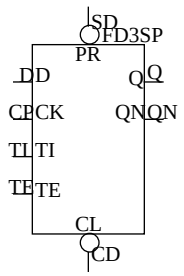
ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.780

FD3SP	FD3SP	1/10

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FD3SP	D-TYPE FLIP FLOP with common single-phase SCAN clock with CLEAR and PRESET	12	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT						OUTPUT	
CD	SD	D	TI	TE	CP	Qn+1	QNn+1
L	H	X	X	X	X*	L	H
H	L	X	X	X	X*	H	L
L	L	X	X	X	X	L	L
H	H	L	X	L	Up	L	H
H	H	H	X	L	Up	H	L
H	H	X	L	H	Up	L	H
H	H	X	H	H	Up	H	L
H	H	X	X	X	Dn	Qn	QNn

*:Consider the HOLD Time
of CLEAR or PRESET

Verilog-HDL DESCRIPTION

```
FD3SP  inst(Q,QN,D,CP,CD,SD,TI,TE);
```

VHDL DESCRIPTION

```
inst:FD3SP
  port  map(Q,QN,D,CP,CD,SD,TI,
            TE);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q	QN
ELECTRO MIGRATION DRIVE	6880.0	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D,TI	0.99
CP	0.98
CD	2.28
SD	2.18
TE	1.97

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	88.8	97.7

Rev.1.01.10

FD3SP | FD3SP | 2/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0440	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.30	0.38	0.70
0.38	0.28	0.35	0.43	0.75
1.00	0.35	0.42	0.51	0.82
3.00	0.49	0.57	0.66	0.98

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0180	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.40	0.48	0.73
0.38	0.34	0.42	0.50	0.76
1.00	0.41	0.50	0.58	0.83
3.00	0.58	0.68	0.76	1.02

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0298	0.86

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	-0.00	-0.00	0.00	0.10
0.38	-0.00	0.00	0.01	0.42
1.00	0.20	0.57	0.72	0.97
3.00	0.72	0.71	0.73	0.93

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0441	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.31	0.39	0.71
0.38	0.28	0.36	0.44	0.76
1.00	0.35	0.42	0.51	0.83
3.00	0.49	0.57	0.66	0.98

FD3SP | FD3SP | 3/10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0440	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	-0.21	-0.19	-0.07	0.36
0.38	-0.09	0.15	0.31	0.77
1.00	0.80	0.79	0.82	1.16
3.00	0.63	0.82	0.95	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0441	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.63	0.71	1.04
0.38	0.63	0.71	0.79	1.11
1.00	0.71	0.79	0.88	1.20
3.00	0.87	0.95	1.04	1.36

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0298	0.86

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.59	0.67	0.75	1.05
0.38	0.67	0.75	0.83	1.13
1.00	0.75	0.83	0.91	1.21
3.00	0.90	0.98	1.06	1.36

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0440	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.82	0.90	0.98	1.30
0.38	0.90	0.98	1.06	1.38
1.00	0.98	1.06	1.14	1.46
3.00	1.13	1.21	1.29	1.61

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0180	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.76	0.83	0.90	1.13
0.38	0.84	0.91	0.97	1.21
1.00	0.92	0.99	1.06	1.29
3.00	1.08	1.15	1.22	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->O	---	RISE

SLEW FACTOR

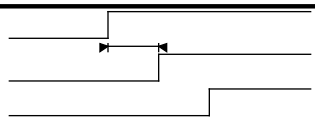
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0441	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.65	0.72	0.81	1.13
0.38	0.67	0.75	0.83	1.15
1.00	0.75	0.83	0.91	1.23
3.00	0.94	1.02	1.11	1.43

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

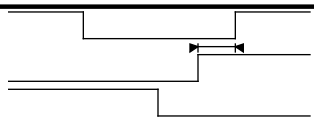
DATA	CLOCK	CONDITION
CD	CP	SD&(~TE&D TE&TI)

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.061	-0.101	-0.167	-0.383
0.38	-0.067	-0.107	-0.174	-0.389
1.00	-0.078	-0.118	-0.185	-0.399
3.00	-0.114	-0.153	-0.219	-0.431

TIMING CONDITION

DATA	CLOCK	CONDITION
CD	CP	SD&(~TE&D TE&TI)

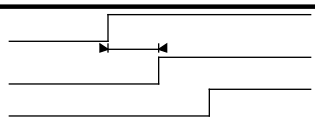
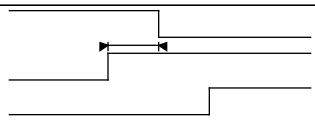
ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.718	0.758	0.825	1.040
0.38	0.725	0.764	0.831	1.046
1.00	0.735	0.775	0.841	1.055
3.00	0.771	0.810	0.875	1.086

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD&SD&~TE

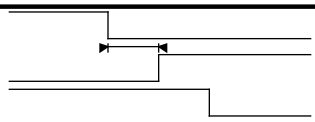
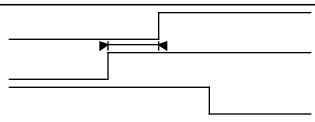
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.438	0.416	0.379	0.260
0.38	0.482	0.460	0.422	0.301
1.00	0.557	0.534	0.495	0.369
3.00	0.799	0.773	0.730	0.589

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.068	0.104	0.163	0.354
0.38	0.030	0.065	0.124	0.314
1.00	-0.035	-0.000	0.058	0.246
3.00	-0.243	-0.210	-0.154	0.026

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD&SD&~TE

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

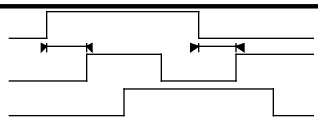
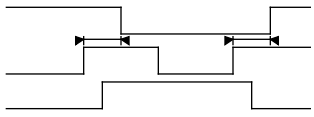
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.588	0.553	0.493	0.302
0.38	0.627	0.592	0.533	0.342
1.00	0.691	0.656	0.598	0.410
3.00	0.899	0.866	0.810	0.630

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.220	0.241	0.277	0.394
0.38	0.175	0.197	0.234	0.353
1.00	0.099	0.122	0.161	0.286
3.00	-0.144	-0.118	-0.074	0.067

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
TE	CP	CD&SD&(~D&TI D&~TI)

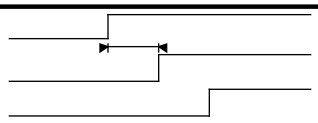
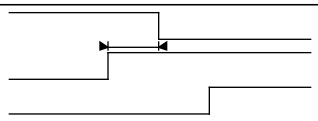
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	DCARE	
HOLD	POSEDGE	DCARE	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.479	0.457	0.420	0.302
0.38	0.530	0.507	0.470	0.349
1.00	0.616	0.593	0.554	0.428
3.00	0.893	0.867	0.823	0.683

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.179	0.200	0.237	0.353
0.38	0.127	0.149	0.187	0.306
1.00	0.041	0.064	0.103	0.227
3.00	-0.238	-0.211	-0.168	-0.026

TIMING CONDITION

DATA	CLOCK	CONDITION
TI	CP	CD&SD&TE

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

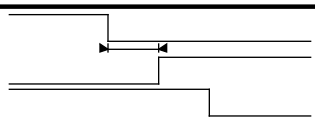
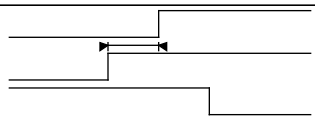
SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.512	0.490	0.454	0.337
0.38	0.551	0.529	0.492	0.373
1.00	0.615	0.592	0.554	0.432
3.00	0.823	0.798	0.757	0.624

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.056	-0.023	0.033	0.214
0.38	-0.079	-0.046	0.010	0.189
1.00	-0.118	-0.085	-0.030	0.148
3.00	-0.243	-0.211	-0.158	0.015

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
TI	CP	CD&SD&TE

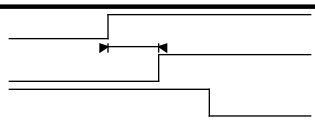
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.710	0.677	0.622	0.443
0.38	0.734	0.701	0.646	0.467
1.00	0.773	0.740	0.685	0.509
3.00	0.899	0.868	0.814	0.642

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.142	0.164	0.201	0.319
0.38	0.104	0.126	0.163	0.284
1.00	0.039	0.062	0.101	0.224
3.00	-0.168	-0.143	-0.102	0.032

TIMING CONDITION

DATA	CLOCK	CONDITION
SD	CP	CD&(~TE&~DTE&~TI)

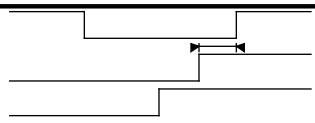
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.131	0.094	0.031	-0.172
0.38	0.159	0.122	0.059	-0.141
1.00	0.205	0.169	0.108	-0.089
3.00	0.354	0.320	0.263	0.079

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
SD	CP	CD&(~TE&~D TE&~TI)

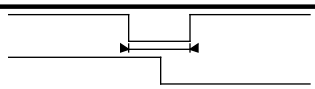
ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.523	0.561	0.624	0.829
0.38	0.495	0.533	0.596	0.798
1.00	0.450	0.486	0.547	0.745
3.00	0.302	0.336	0.393	0.576

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

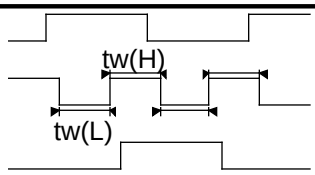
CLOCK	CONDITION
CD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.730

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	CD&SD

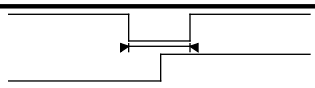
ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.790

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
SD	---

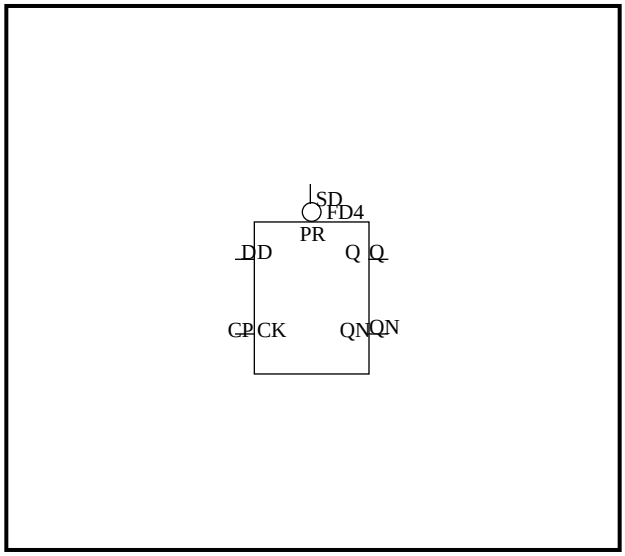
ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.780

FD4	FD4	1/6

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FD4	D-TYPE FLIP FLOP with PRESET	8	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT	
SD	D	CP	Qn+1	QNn+1
L	X	X*	H	L
H	L	Up	L	H
H	H	Up	H	L
H	X	Dn	Qn	QNn

*:Consider the HOLD Time of PRESET

Verilog-HDL DESCRIPTION

```
FD4  inst(Q,QN,D,CP,SD);
```

VHDL DESCRIPTION

```
inst:FD4
  port  map(Q,QN,D,CP,SD);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D,CP	0.99
SD	2.23

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	46.1	45.9

Rev.1.01.10

FD4 FD4 2/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0963	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.50	0.64	0.81	1.48
0.38	0.57	0.72	0.89	1.56
1.00	0.65	0.79	0.96	1.64
3.00	0.78	0.92	1.09	1.76

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0349	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.60	0.71	0.83	1.26
0.38	0.68	0.79	0.91	1.33
1.00	0.75	0.86	0.98	1.41
3.00	0.88	0.99	1.10	1.53

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0960	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.79	0.94	1.11	1.77
0.38	0.87	1.01	1.18	1.85
1.00	0.94	1.09	1.26	1.92
3.00	1.07	1.21	1.38	2.05

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0360	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.61	0.71	0.82	1.25
0.38	0.69	0.79	0.90	1.33
1.00	0.77	0.87	0.98	1.41
3.00	0.89	1.00	1.11	1.53

FD4 FD4 3/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0963	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.54	0.68	0.85	1.51
0.38	0.57	0.71	0.88	1.54
1.00	0.65	0.79	0.95	1.62
3.00	0.82	0.96	1.12	1.79

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0360	0.08

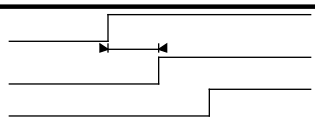
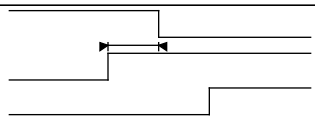
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.44	0.56	1.01
0.38	0.33	0.47	0.59	1.03
1.00	0.41	0.54	0.67	1.11
3.00	0.58	0.72	0.85	1.29

FD4	FD4	4/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	SD

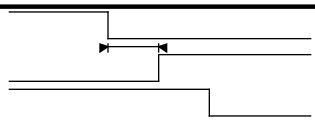
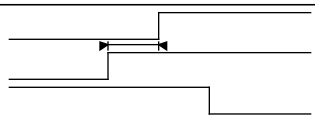
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.360	0.341	0.310	0.208
0.38	0.395	0.376	0.344	0.241
1.00	0.453	0.434	0.401	0.295
3.00	0.641	0.620	0.585	0.472

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.238	0.271	0.327	0.506
0.38	0.205	0.238	0.293	0.470
1.00	0.149	0.181	0.235	0.411
3.00	-0.032	-0.001	0.051	0.219

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	SD

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.418	0.385	0.329	0.148
0.38	0.452	0.419	0.363	0.184
1.00	0.508	0.475	0.420	0.243
3.00	0.688	0.657	0.605	0.436

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.295	0.314	0.346	0.447
0.38	0.260	0.280	0.312	0.415
1.00	0.202	0.222	0.255	0.360
3.00	0.014	0.035	0.071	0.185

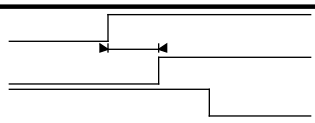
Rev.1.01.10

FD4 FD4 5/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

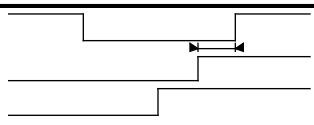
DATA	CLOCK	CONDITION
SD	CP	~D

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.161	0.127	0.072	-0.109
0.38	0.194	0.161	0.106	-0.072
1.00	0.250	0.218	0.163	-0.012
3.00	0.430	0.400	0.349	0.185

TIMING CONDITION

DATA	CLOCK	CONDITION
SD	CP	~D

ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.494	0.527	0.583	0.763
0.38	0.461	0.494	0.549	0.727
1.00	0.407	0.439	0.493	0.666
3.00	0.232	0.261	0.311	0.471

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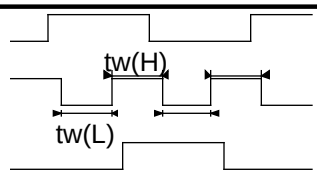
FD4	FD4	6/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	SD

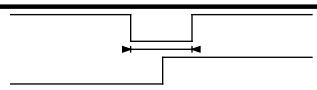
ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.770

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
SD	---

ITEM	WAVE_FORM
NEGLIMIT	

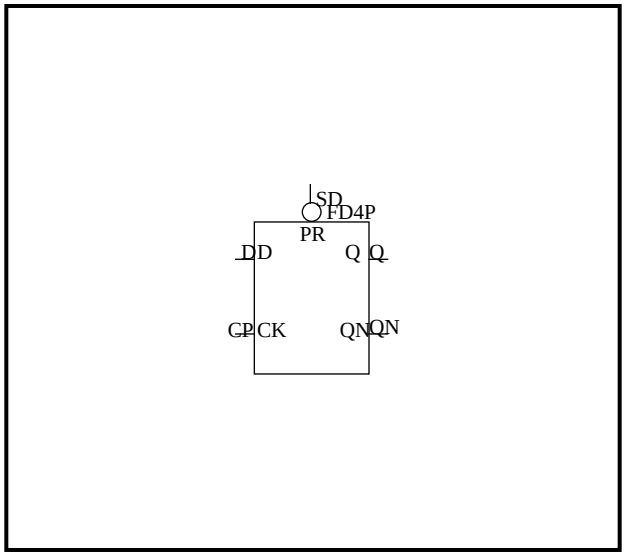
NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.760

Rev.1.01.10

FD4P	FD4P	1/6

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FD4P	D-TYPE FLIP FLOP with PRESET	9	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT	
SD	D	CP	Qn+1	QNn+1
L	X	X*	H	L
H	L	Up	L	H
H	H	Up	H	L
H	X	Dn	Qn	QNn

*:Consider the HOLD Time of PRESET

Verilog-HDL DESCRIPTION

```
FD4P  inst(Q,QN,D,CP,SD);
```

VHDL DESCRIPTION

```
inst:FD4P
  port  map(Q,QN,D,CP,SD);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q	QN
ELECTRO MIGRATION DRIVE	6880.0	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D,CP	0.99
SD	2.23

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	89.8	97.3

Rev.1.01.10

FD4P | FD4P | 2/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0494	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.57	0.66	1.01
0.38	0.57	0.65	0.74	1.09
1.00	0.65	0.73	0.82	1.16
3.00	0.78	0.86	0.95	1.29

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0181	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.61	0.69	0.76	1.00
0.38	0.69	0.76	0.84	1.08
1.00	0.77	0.84	0.91	1.15
3.00	0.89	0.96	1.03	1.27

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0445	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.86	0.94	1.03	1.35
0.38	0.94	1.02	1.11	1.43
1.00	1.02	1.09	1.18	1.50
3.00	1.14	1.22	1.30	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0179	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.66	0.73	0.80	1.03
0.38	0.74	0.81	0.88	1.10
1.00	0.82	0.89	0.95	1.18
3.00	0.95	1.01	1.08	1.31

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0494	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.60	0.67	0.76	1.10
0.38	0.62	0.70	0.79	1.13
1.00	0.70	0.78	0.87	1.21
3.00	0.89	0.97	1.06	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0179	0.09

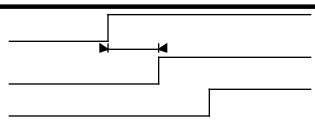
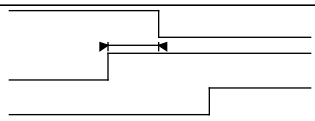
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.39	0.47	0.72
0.38	0.33	0.42	0.50	0.75
1.00	0.41	0.50	0.58	0.83
3.00	0.59	0.68	0.77	1.02

FD4P | FD4P | 4/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	SD

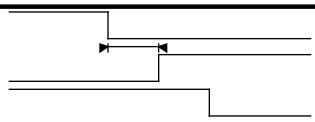
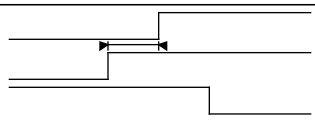
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.360	0.341	0.310	0.208
0.38	0.395	0.376	0.344	0.241
1.00	0.453	0.434	0.401	0.295
3.00	0.641	0.620	0.585	0.472

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.238	0.271	0.327	0.506
0.38	0.205	0.238	0.293	0.470
1.00	0.149	0.181	0.235	0.411
3.00	-0.032	-0.001	0.051	0.219

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	SD

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.418	0.385	0.329	0.148
0.38	0.452	0.419	0.363	0.184
1.00	0.508	0.475	0.420	0.243
3.00	0.688	0.657	0.605	0.436

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.295	0.314	0.346	0.447
0.38	0.260	0.280	0.312	0.415
1.00	0.202	0.222	0.255	0.360
3.00	0.014	0.035	0.071	0.185

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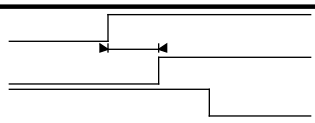
CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

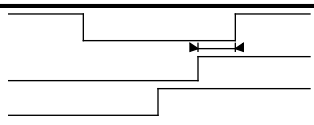
DATA	CLOCK	CONDITION
SD	CP	~D

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.161	0.127	0.072	-0.109
0.38	0.194	0.161	0.106	-0.072
1.00	0.250	0.218	0.163	-0.012
3.00	0.430	0.400	0.349	0.185

TIMING CONDITION

DATA	CLOCK	CONDITION
SD	CP	~D

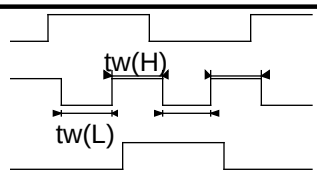
ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.494	0.527	0.583	0.763
0.38	0.461	0.494	0.549	0.727
1.00	0.407	0.439	0.493	0.666
3.00	0.232	0.261	0.311	0.471

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	SD

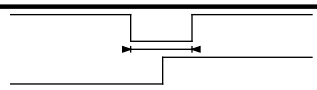
ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.770

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
SD	---

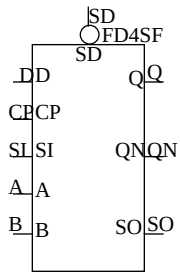
ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.760

FD4SF	FD4SF	1/13

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FD4SF	D-TYPE FLIP FLOP with Independent two-phase SCAN clock with PRESET	12	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT						OUTPUT		
SD	D	SI	A	B	CP	Qn+1	QNn+1	SOn+1
X	X	X	X	L	X	X	X	SOn
L	X	X	L	H	X*	H	L	H
H	X	L	H	H	L	L	H	L
H	X	H	H	H	L	H	L	H
H	L	X	L	H	Up	L	H	L
H	H	X	L	H	Up	H	L	H
H	X	X	L	H	Dn	Qn	QNn	Qn

*:Consider the HOLD Time of PRESET

Verilog-HDL DESCRIPTION

```
FD4SF  inst(Q,QN,SO,D,CP,SD,SI,A,B);
```

VHDL DESCRIPTION

```
inst:FD4SF
   port   map(Q,QN,SO,D,CP,SD,SI,
              A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN,SO
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D,CP	0.99
SD	2.23
SI	0.92
A	2.10
B	2.02

OUTPUT DRIVE (LU)

PIN NAME	Q	QN	SO
DRIVE	46.0	44.0	43.8

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&~A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.1006	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.50	0.64	0.81	1.49
0.38	0.53	0.67	0.84	1.52
1.00	0.59	0.73	0.90	1.59
3.00	0.76	0.90	1.07	1.75

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&~A	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0363	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.65	0.75	0.86	1.28
0.38	0.68	0.78	0.89	1.32
1.00	0.74	0.84	0.95	1.37
3.00	0.87	0.97	1.08	1.50

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.1006	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.43	0.57	0.74	1.42
0.38	0.52	0.66	0.83	1.51
1.00	0.64	0.78	0.95	1.64
3.00	0.76	0.90	1.07	1.75

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&A	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0363	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.55	0.66	1.08
0.38	0.54	0.63	0.74	1.17
1.00	0.64	0.74	0.85	1.27
3.00	0.83	0.93	1.04	1.46

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0964	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.47	0.61	0.78	1.45
0.38	0.56	0.70	0.87	1.54
1.00	0.69	0.83	1.00	1.67
3.00	0.81	0.95	1.12	1.79

PATH CONDITION

PATH	CONDITION	FUNCTION
A->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0351	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.50	0.61	0.72	1.15
0.38	0.58	0.69	0.81	1.23
1.00	0.69	0.80	0.91	1.34
3.00	0.87	0.98	1.10	1.53

PATH CONDITION

PATH	CONDITION	FUNCTION
A->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0959	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.70	0.84	1.01	1.68
0.38	0.78	0.92	1.09	1.76
1.00	0.88	1.03	1.20	1.87
3.00	1.07	1.22	1.39	2.05

PATH CONDITION

PATH	CONDITION	FUNCTION
A->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0392	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.59	0.70	0.82	1.27
0.38	0.68	0.79	0.91	1.36
1.00	0.81	0.92	1.04	1.49
3.00	0.93	1.04	1.16	1.61

FD4SF | FD4SF | 4/13

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.1006	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.44	0.61	1.28
0.38	0.40	0.54	0.70	1.37
1.00	0.50	0.64	0.81	1.48
3.00	0.61	0.75	0.92	1.58

PATH CONDITION

PATH	CONDITION	FUNCTION
B->SO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0363	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.38	0.49	0.91
0.38	0.36	0.45	0.56	0.98
1.00	0.42	0.52	0.63	1.05
3.00	0.52	0.62	0.74	1.19

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0964	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.50	0.64	0.81	1.48
0.38	0.58	0.72	0.89	1.56
1.00	0.65	0.80	0.97	1.64
3.00	0.78	0.93	1.10	1.77

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0351	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.60	0.71	0.83	1.25
0.38	0.68	0.79	0.91	1.33
1.00	0.76	0.86	0.98	1.41
3.00	0.88	0.99	1.10	1.53

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0959	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.96	1.14	1.33	2.03
0.38	1.04	1.21	1.41	2.11
1.00	1.11	1.29	1.48	2.18
3.00	1.23	1.41	1.60	2.30

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0392	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.76	0.90	1.05	1.55
0.38	0.84	0.98	1.13	1.63
1.00	0.91	1.06	1.21	1.71
3.00	1.04	1.19	1.33	1.84

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.1006	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.06	1.19	1.37	2.05
0.38	1.13	1.27	1.44	2.13
1.00	1.21	1.35	1.52	2.20
3.00	1.34	1.48	1.65	2.33

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->SO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0363	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.29	1.39	1.50	1.92
0.38	1.37	1.47	1.58	2.00
1.00	1.44	1.54	1.65	2.07
3.00	1.56	1.66	1.77	2.19

FD4SF | FD4SF | 6/13

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0964	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.85	1.00	1.16	1.83
0.38	0.88	1.02	1.19	1.86
1.00	0.95	1.10	1.26	1.93
3.00	1.17	1.31	1.48	2.14

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0392	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.43	0.60	0.76	1.27
0.38	0.46	0.63	0.79	1.30
1.00	0.54	0.71	0.86	1.38
3.00	0.74	0.92	1.08	1.59

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.1006	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.79	0.93	1.10	1.78
0.38	0.82	0.96	1.13	1.81
1.00	0.89	1.03	1.20	1.88
3.00	1.10	1.24	1.41	2.09

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0964	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.44	0.58	0.75	1.42
0.38	0.48	0.62	0.79	1.46
1.00	0.55	0.69	0.86	1.53
3.00	0.68	0.83	1.00	1.67

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0351	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.59	0.70	1.13
0.38	0.48	0.59	0.71	1.13
1.00	0.53	0.64	0.76	1.18
3.00	0.66	0.79	0.91	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0959	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.68	0.82	0.99	1.66
0.38	0.68	0.83	1.00	1.66
1.00	0.73	0.88	1.05	1.71
3.00	0.89	1.03	1.20	1.87

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0392	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.56	0.67	0.79	1.24
0.38	0.60	0.71	0.83	1.28
1.00	0.67	0.78	0.90	1.35
3.00	0.81	0.92	1.04	1.49

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.1006	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.49	0.66	1.35
0.38	0.39	0.53	0.70	1.38
1.00	0.44	0.58	0.75	1.43
3.00	0.52	0.66	0.83	1.51

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->SO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0363	0.10

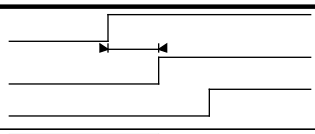
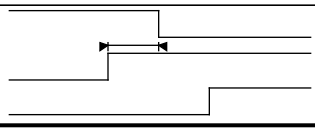
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.47	0.58	1.00
0.38	0.38	0.48	0.58	1.01
1.00	0.43	0.53	0.64	1.06
3.00	0.55	0.65	0.76	1.19

FD4SF | FD4SF | 9/13

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	SD&~A

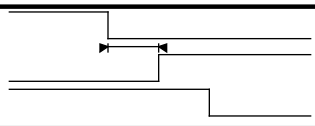
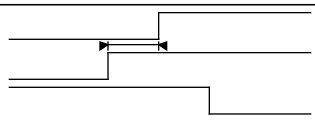
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.360	0.341	0.310	0.208
0.38	0.395	0.376	0.344	0.241
1.00	0.453	0.434	0.401	0.295
3.00	0.641	0.620	0.585	0.472

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.238	0.271	0.327	0.506
0.38	0.205	0.238	0.293	0.470
1.00	0.149	0.181	0.235	0.411
3.00	-0.032	-0.001	0.051	0.219

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	SD&~A

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.418	0.385	0.329	0.148
0.38	0.452	0.419	0.363	0.184
1.00	0.508	0.475	0.420	0.243
3.00	0.688	0.657	0.605	0.436

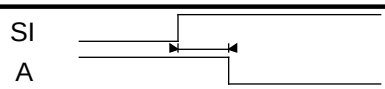
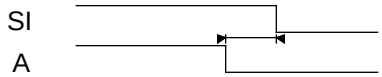
HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.295	0.314	0.346	0.447
0.38	0.260	0.280	0.312	0.415
1.00	0.202	0.222	0.255	0.360
3.00	0.014	0.035	0.071	0.185

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
SI	A	SD&~CP

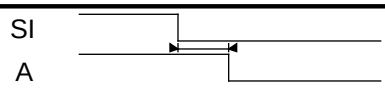
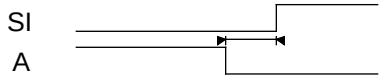
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.399	0.407	0.420	0.464
0.38	0.432	0.446	0.469	0.544
1.00	0.488	0.511	0.551	0.679
3.00	0.667	0.722	0.815	1.114

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.165	0.124	0.054	-0.171
0.38	0.140	0.094	0.018	-0.229
1.00	0.097	0.045	-0.042	-0.324
3.00	-0.041	-0.114	-0.237	-0.634

TIMING CONDITION

DATA	CLOCK	CONDITION
SI	A	SD&~CP

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

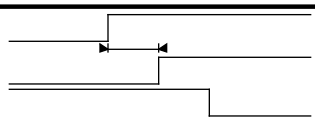
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.502	0.543	0.613	0.839
0.38	0.530	0.575	0.651	0.895
1.00	0.578	0.629	0.714	0.988
3.00	0.732	0.801	0.916	1.290

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.258	0.250	0.236	0.193
0.38	0.225	0.211	0.187	0.112
1.00	0.169	0.145	0.105	-0.023
3.00	-0.012	-0.067	-0.159	-0.458

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

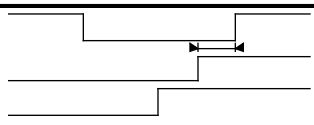
DATA	CLOCK	CONDITION
SD	CP	~D&~A

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.161	0.127	0.072	-0.109
0.38	0.193	0.160	0.105	-0.073
1.00	0.248	0.216	0.162	-0.013
3.00	0.425	0.394	0.343	0.179

TIMING CONDITION

DATA	CLOCK	CONDITION
SD	CP	~D&~A

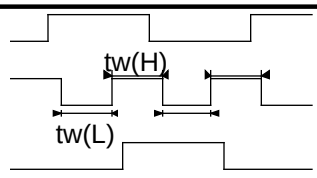
ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.494	0.527	0.583	0.763
0.38	0.461	0.494	0.550	0.728
1.00	0.407	0.439	0.494	0.669
3.00	0.232	0.262	0.313	0.477

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	SD

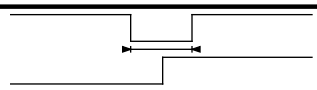
ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.770

MINIMUM PULSE WIDTH CONDITION

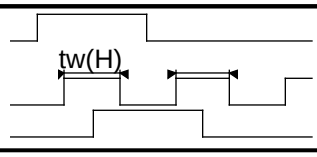
CLOCK	CONDITION
SD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.890

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
B	SD

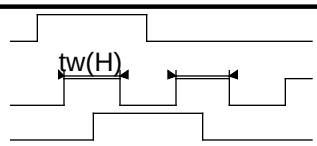
ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
A	SD

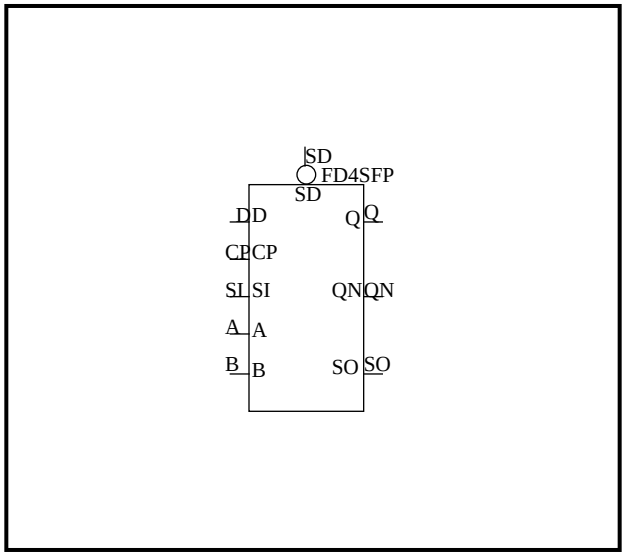
ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

FD4SFP	FD4SFP	1/13

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FD4SFP	D-TYPE FLIP FLOP with Independent two-phase SCAN clock with PRESET	13	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT						OUTPUT		
SD	D	SI	A	B	CP	Qn+1	QNn+1	SOn+1
X	X	X	X	L	X	X	X	SOn
L	X	X	L	H	X*	H	L	H
H	X	L	H	H	L	L	H	L
H	X	H	H	H	L	H	L	H
H	L	X	L	H	Up	L	H	L
H	H	X	L	H	Up	H	L	H
H	X	X	L	H	Dn	Qn	QNn	Qn

*:Consider the HOLD Time of PRESET

Verilog-HDL DESCRIPTION

```
FD4SFP  inst(Q,QN,SO,D,CP,SD,SI,A,
B);
```

VHDL DESCRIPTION

```
inst:FD4SFP
  port  map(Q,QN,SO,D,CP,SD,SI,
        A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN,SO
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D,CP	0.99
SD	2.23
SI	0.92
A	2.08
B	2.03

OUTPUT DRIVE (LU)

PIN NAME	Q	QN	SO
DRIVE	82.5	87.9	43.8

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&~A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.1006	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.63	0.80	1.49
0.38	0.52	0.66	0.84	1.52
1.00	0.59	0.73	0.90	1.59
3.00	0.76	0.90	1.07	1.75

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&~A	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0363	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.65	0.75	0.86	1.28
0.38	0.68	0.78	0.89	1.31
1.00	0.74	0.84	0.95	1.37
3.00	0.87	0.97	1.08	1.50

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.1006	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.43	0.57	0.74	1.42
0.38	0.52	0.66	0.83	1.51
1.00	0.64	0.78	0.95	1.64
3.00	0.76	0.90	1.07	1.75

PATH CONDITION

PATH	CONDITION	FUNCTION
A->SO	B&A	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0363	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.55	0.66	1.08
0.38	0.54	0.63	0.74	1.17
1.00	0.64	0.74	0.85	1.27
3.00	0.83	0.93	1.04	1.46

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0548	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.56	0.66	1.03
0.38	0.56	0.65	0.74	1.12
1.00	0.70	0.78	0.88	1.25
3.00	0.82	0.90	1.00	1.37

PATH CONDITION

PATH	CONDITION	FUNCTION
A->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0188	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.58	0.65	0.90
0.38	0.59	0.66	0.73	0.98
1.00	0.69	0.77	0.84	1.09
3.00	0.88	0.95	1.03	1.27

PATH CONDITION

PATH	CONDITION	FUNCTION
A->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0482	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.77	0.85	0.94	1.28
0.38	0.85	0.93	1.02	1.36
1.00	0.96	1.04	1.13	1.47
3.00	1.14	1.22	1.31	1.65

PATH CONDITION

PATH	CONDITION	FUNCTION
A->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0198	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.66	0.73	0.80	1.04
0.38	0.75	0.82	0.89	1.13
1.00	0.89	0.96	1.03	1.26
3.00	1.01	1.08	1.15	1.38

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.1006	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.44	0.61	1.28
0.38	0.40	0.54	0.70	1.37
1.00	0.50	0.64	0.81	1.48
3.00	0.61	0.75	0.92	1.58

PATH CONDITION

PATH	CONDITION	FUNCTION
B->SO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0363	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.38	0.49	0.91
0.38	0.36	0.45	0.56	0.98
1.00	0.42	0.52	0.63	1.05
3.00	0.52	0.62	0.74	1.19

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0548	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.58	0.67	1.05
0.38	0.57	0.66	0.75	1.13
1.00	0.65	0.74	0.83	1.20
3.00	0.78	0.87	0.96	1.33

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0188	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.61	0.68	0.76	1.00
0.38	0.69	0.76	0.83	1.08
1.00	0.76	0.84	0.91	1.15
3.00	0.88	0.96	1.03	1.28

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0482	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.03	1.12	1.23	1.60
0.38	1.10	1.20	1.31	1.68
1.00	1.18	1.27	1.38	1.76
3.00	1.30	1.40	1.50	1.88

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0198	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.82	0.92	1.01	1.29
0.38	0.90	1.00	1.09	1.37
1.00	0.98	1.07	1.17	1.45
3.00	1.10	1.20	1.29	1.58

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.1006	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.18	1.32	1.49	2.17
0.38	1.26	1.40	1.57	2.25
1.00	1.33	1.47	1.64	2.33
3.00	1.46	1.60	1.77	2.45

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->SO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0363	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.41	1.51	1.62	2.04
0.38	1.49	1.59	1.70	2.12
1.00	1.56	1.66	1.77	2.19
3.00	1.68	1.78	1.89	2.31

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0548	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.92	1.01	1.10	1.47
0.38	0.95	1.04	1.13	1.51
1.00	1.02	1.10	1.20	1.57
3.00	1.24	1.33	1.42	1.79

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0198	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.52	0.63	0.93
0.38	0.44	0.55	0.65	0.95
1.00	0.52	0.63	0.73	1.03
3.00	0.73	0.85	0.95	1.25

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.1006	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.84	0.98	1.15	1.83
0.38	0.87	1.01	1.18	1.86
1.00	0.94	1.08	1.25	1.93
3.00	1.15	1.29	1.47	2.15

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0548	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.44	0.53	0.62	1.00
0.38	0.48	0.57	0.66	1.04
1.00	0.56	0.65	0.74	1.11
3.00	0.71	0.80	0.89	1.27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0188	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.56	0.63	0.88
0.38	0.49	0.56	0.64	0.88
1.00	0.54	0.61	0.68	0.93
3.00	0.68	0.76	0.84	1.10

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0482	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.75	0.83	0.92	1.26
0.38	0.75	0.83	0.92	1.26
1.00	0.80	0.88	0.97	1.31
3.00	0.98	1.06	1.15	1.49

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0198	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.63	0.70	0.77	1.01
0.38	0.67	0.74	0.81	1.05
1.00	0.75	0.82	0.89	1.13
3.00	0.91	0.98	1.05	1.29

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->SO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.1006	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.49	0.66	1.35
0.38	0.39	0.53	0.70	1.38
1.00	0.44	0.58	0.75	1.43
3.00	0.52	0.66	0.83	1.51

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SI->SO	---	FALL

SLEW FACTOR

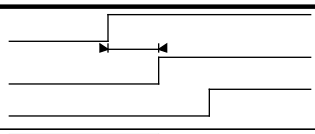
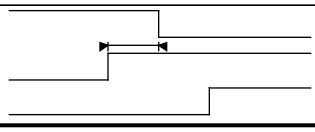
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
SO	0.0363	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.47	0.58	1.00
0.38	0.38	0.48	0.59	1.01
1.00	0.43	0.53	0.64	1.06
3.00	0.55	0.65	0.76	1.19

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	SD&~A

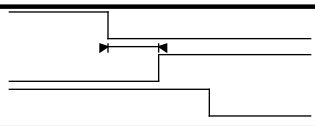
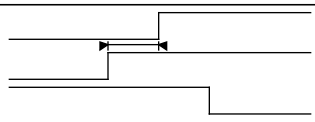
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.360	0.341	0.310	0.208
0.38	0.395	0.376	0.344	0.241
1.00	0.453	0.434	0.401	0.295
3.00	0.641	0.620	0.585	0.472

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.238	0.271	0.327	0.506
0.38	0.205	0.238	0.293	0.470
1.00	0.149	0.181	0.235	0.411
3.00	-0.032	-0.001	0.051	0.219

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	SD&~A

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

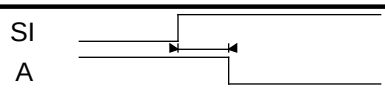
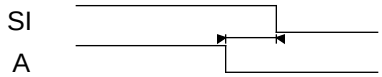
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.418	0.385	0.329	0.148
0.38	0.452	0.419	0.363	0.184
1.00	0.508	0.475	0.420	0.243
3.00	0.688	0.657	0.605	0.436

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.295	0.314	0.346	0.447
0.38	0.260	0.280	0.312	0.415
1.00	0.202	0.222	0.255	0.360
3.00	0.014	0.035	0.071	0.185

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
SI	A	SD&~CP

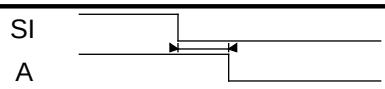
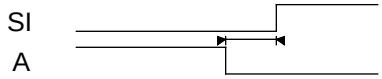
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.399	0.407	0.420	0.464
0.38	0.432	0.446	0.469	0.544
1.00	0.488	0.511	0.551	0.679
3.00	0.667	0.722	0.815	1.114

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.165	0.124	0.054	-0.171
0.38	0.140	0.094	0.018	-0.229
1.00	0.097	0.045	-0.042	-0.324
3.00	-0.041	-0.114	-0.237	-0.634

TIMING CONDITION

DATA	CLOCK	CONDITION
SI	A	SD&~CP

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

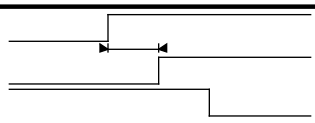
SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.502	0.543	0.613	0.839
0.38	0.530	0.575	0.651	0.895
1.00	0.578	0.629	0.714	0.988
3.00	0.732	0.801	0.916	1.290

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.258	0.250	0.236	0.193
0.38	0.225	0.211	0.187	0.112
1.00	0.169	0.145	0.105	-0.023
3.00	-0.012	-0.067	-0.159	-0.458

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

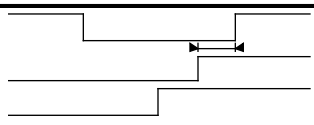
DATA	CLOCK	CONDITION
SD	CP	~D&~A

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.161	0.127	0.072	-0.109
0.38	0.193	0.160	0.105	-0.073
1.00	0.248	0.216	0.162	-0.013
3.00	0.425	0.394	0.343	0.179

TIMING CONDITION

DATA	CLOCK	CONDITION
SD	CP	~D&~A

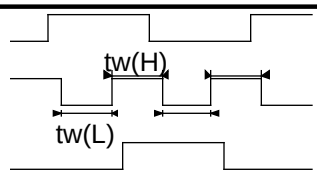
ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.494	0.527	0.583	0.763
0.38	0.461	0.494	0.550	0.728
1.00	0.407	0.439	0.494	0.669
3.00	0.232	0.262	0.313	0.477

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	SD

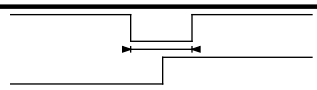
ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.770

MINIMUM PULSE WIDTH CONDITION

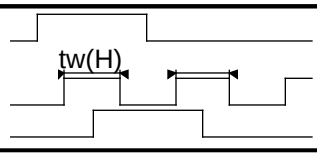
CLOCK	CONDITION
SD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.890

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
B	SD

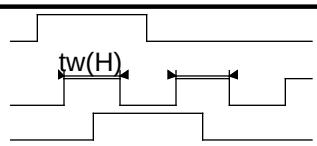
ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
A	SD

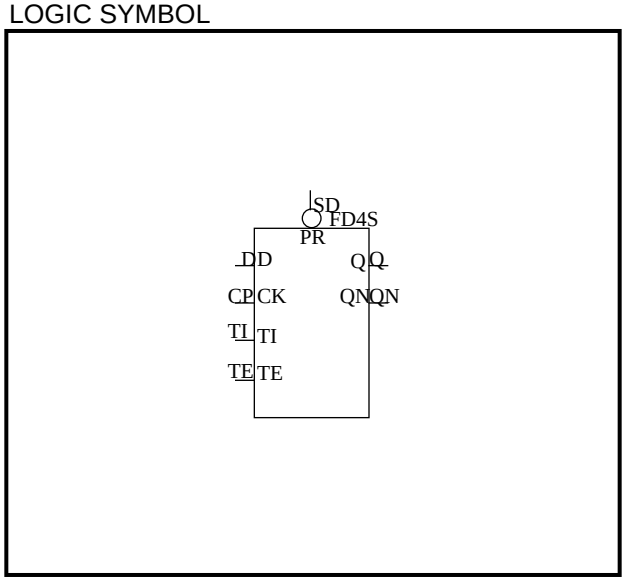
ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

FD4S	FD4S	1/8

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FD4S	D-TYPE FLIP FLOP with common single-phase SCAN clock with PRESET	10	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT					OUTPUT	
SD	D	TI	TE	CP	Qn+1	QNn+1
L	X	X	X	X*	H	L
H	L	X	L	Up	L	H
H	H	X	L	Up	H	L
H	X	L	H	Up	L	H
H	X	H	H	Up	H	L
H	X	X	X	Dn	Qn	QNn

*:Consider the HOLD Time of PRESET

Verilog-HDL DESCRIPTION

```
FD4S  inst(Q,QN,D,CP,SD,TI,TE);
```

VHDL DESCRIPTION

```
inst:FD4S
   port   map(Q,QN,D,CP,SD,TI,TE);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D,TI	0.99
CP	0.98
SD	2.23
TE	1.97

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	46.1	46.0

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0964	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.65	0.83	1.50
0.38	0.59	0.73	0.90	1.57
1.00	0.67	0.82	0.99	1.66
3.00	0.83	0.97	1.14	1.81

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0349	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.60	0.71	0.83	1.25
0.38	0.68	0.79	0.91	1.33
1.00	0.76	0.87	0.99	1.41
3.00	0.91	1.02	1.14	1.56

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0960	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.79	0.93	1.10	1.77
0.38	0.87	1.01	1.18	1.85
1.00	0.95	1.09	1.26	1.93
3.00	1.10	1.24	1.41	2.08

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0360	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.63	0.73	0.84	1.27
0.38	0.71	0.81	0.92	1.35
1.00	0.79	0.89	1.00	1.43
3.00	0.94	1.05	1.16	1.59

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0964	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.54	0.68	0.85	1.51
0.38	0.57	0.71	0.88	1.54
1.00	0.64	0.79	0.95	1.62
3.00	0.82	0.96	1.12	1.79

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0360	0.08

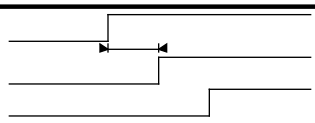
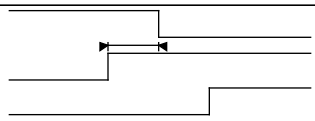
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.44	0.56	1.01
0.38	0.33	0.47	0.59	1.03
1.00	0.41	0.54	0.67	1.11
3.00	0.58	0.72	0.85	1.29

FD4S | FD4S | 4/8

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	SD&~TE

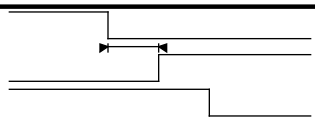
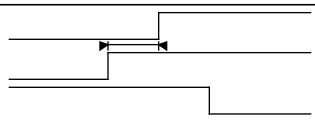
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.425	0.405	0.369	0.256
0.38	0.470	0.448	0.412	0.296
1.00	0.544	0.521	0.484	0.362
3.00	0.782	0.757	0.714	0.577

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.062	0.097	0.157	0.348
0.38	0.023	0.058	0.117	0.308
1.00	-0.041	-0.006	0.052	0.240
3.00	-0.249	-0.216	-0.160	0.020

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	SD&~TE

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.595	0.559	0.499	0.307
0.38	0.633	0.598	0.539	0.347
1.00	0.698	0.663	0.604	0.416
3.00	0.905	0.872	0.816	0.635

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.231	0.252	0.287	0.401
0.38	0.186	0.208	0.244	0.361
1.00	0.113	0.135	0.173	0.295
3.00	-0.126	-0.100	-0.058	0.079

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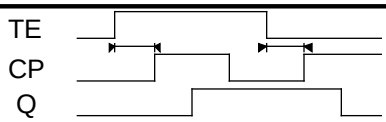
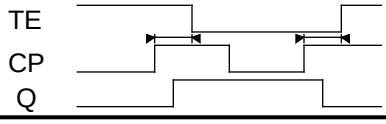
CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
TE	CP	SD&(~D&TI D&~TI)

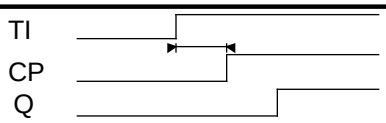
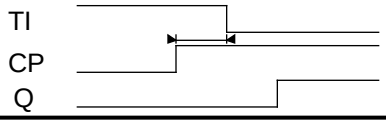
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	DCARE	
HOLD	POSEDGE	DCARE	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.467	0.446	0.411	0.297
0.38	0.518	0.496	0.460	0.343
1.00	0.602	0.580	0.542	0.421
3.00	0.876	0.850	0.808	0.671

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.190	0.211	0.246	0.360
0.38	0.139	0.161	0.197	0.314
1.00	0.054	0.077	0.114	0.236
3.00	-0.220	-0.195	-0.152	-0.015

TIMING CONDITION

DATA	CLOCK	CONDITION
TI	CP	SD&TE

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

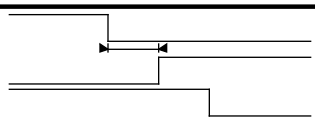
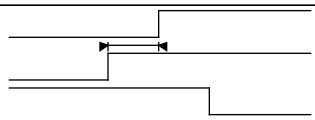
SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.501	0.479	0.443	0.326
0.38	0.538	0.516	0.480	0.362
1.00	0.602	0.579	0.542	0.421
3.00	0.806	0.782	0.742	0.613

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.073	-0.040	0.016	0.195
0.38	-0.096	-0.063	-0.008	0.171
1.00	-0.135	-0.102	-0.048	0.130
3.00	-0.261	-0.229	-0.176	-0.004

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
TI	CP	SD&TE

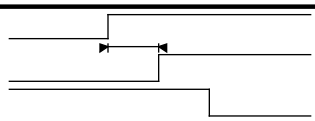
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.723	0.689	0.632	0.447
0.38	0.746	0.712	0.655	0.472
1.00	0.785	0.752	0.695	0.513
3.00	0.911	0.879	0.824	0.647

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.154	0.176	0.213	0.331
0.38	0.116	0.139	0.176	0.296
1.00	0.054	0.076	0.114	0.236
3.00	-0.149	-0.126	-0.085	0.044

TIMING CONDITION

DATA	CLOCK	CONDITION
SD	CP	(~TE&~D TE&~TI)

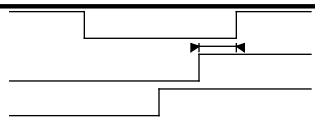
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.156	0.119	0.057	-0.143
0.38	0.189	0.152	0.091	-0.107
1.00	0.243	0.207	0.147	-0.048
3.00	0.418	0.384	0.327	0.144

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
SD	CP	(~TE&~D TE&~TI)

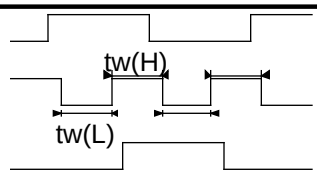
ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.500	0.537	0.600	0.800
0.38	0.468	0.504	0.566	0.764
1.00	0.413	0.449	0.510	0.705
3.00	0.237	0.271	0.328	0.513

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	SD

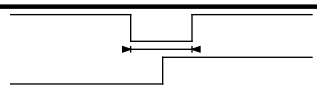
ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.810

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
SD	---

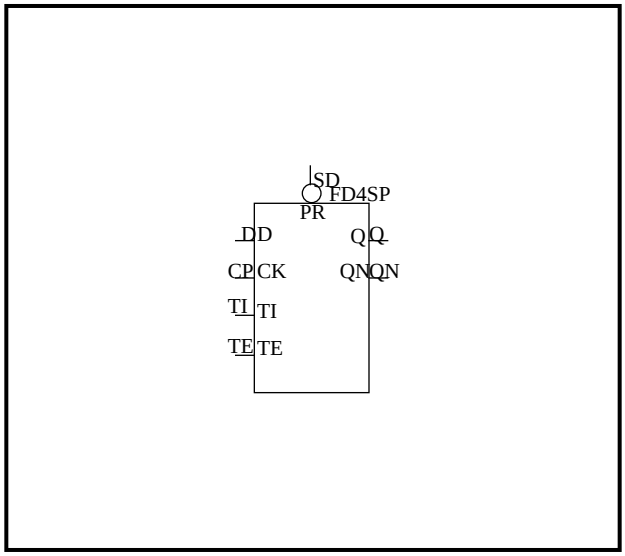
ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.760

FD4SP	FD4SP	1/8

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FD4SP	D-TYPE FLIP FLOP with common single-phase SCAN clock with PRESET	11	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT					OUTPUT	
SD	D	TI	TE	CP	Qn+1	QNn+1
L	X	X	X	X*	H	L
H	L	X	L	Up	L	H
H	H	X	L	Up	H	L
H	X	L	H	Up	L	H
H	X	H	H	Up	H	L
H	X	X	X	Dn	Qn	QNn

*:Consider the HOLD Time of PRESET

Verilog-HDL DESCRIPTION

```
FD4SP  inst(Q,QN,D,CP,SD,TI,TE);
```

VHDL DESCRIPTION

```
inst:FD4SP
   port   map(Q,QN,D,CP,SD,TI,TE);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q	QN
ELECTRO MIGRATION DRIVE	6880.0	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D,TI	0.99
CP	0.98
SD	2.23
TE	1.97

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	89.8	97.3

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0494	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.59	0.68	1.02
0.38	0.59	0.67	0.76	1.10
1.00	0.67	0.75	0.84	1.18
3.00	0.83	0.91	1.00	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->O	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0181	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.61	0.68	0.75	1.00
0.38	0.69	0.76	0.83	1.08
1.00	0.77	0.84	0.91	1.15
3.00	0.92	0.99	1.06	1.30

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0445	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.86	0.94	1.02	1.35
0.38	0.94	1.02	1.10	1.43
1.00	1.02	1.10	1.18	1.51
3.00	1.17	1.25	1.33	1.66

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0179	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.68	0.75	0.81	1.04
0.38	0.76	0.83	0.89	1.12
1.00	0.84	0.91	0.97	1.20
3.00	1.00	1.07	1.13	1.36

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->O	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
O	0.0494	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.60	0.67	0.76	1.10
0.38	0.62	0.70	0.79	1.13
1.00	0.70	0.78	0.87	1.21
3.00	0.89	0.97	1.06	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0179	0.09

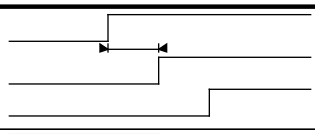
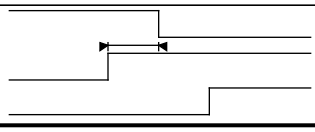
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.39	0.47	0.72
0.38	0.33	0.42	0.50	0.75
1.00	0.41	0.50	0.58	0.83
3.00	0.58	0.68	0.77	1.02

FD4SP | FD4SP | 4/8

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	SD&~TE

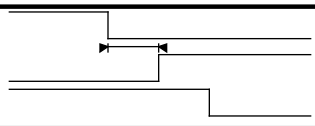
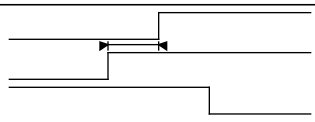
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.425	0.405	0.369	0.256
0.38	0.470	0.448	0.412	0.296
1.00	0.544	0.521	0.484	0.362
3.00	0.782	0.757	0.714	0.577

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.062	0.097	0.157	0.348
0.38	0.023	0.058	0.117	0.308
1.00	-0.041	-0.006	0.052	0.240
3.00	-0.249	-0.216	-0.160	0.020

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	SD&~TE

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.595	0.559	0.499	0.307
0.38	0.633	0.598	0.539	0.347
1.00	0.698	0.663	0.604	0.416
3.00	0.905	0.872	0.816	0.635

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.231	0.252	0.287	0.401
0.38	0.186	0.208	0.244	0.361
1.00	0.113	0.135	0.173	0.295
3.00	-0.126	-0.100	-0.058	0.079

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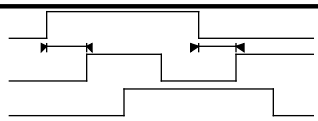
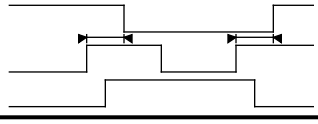
CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
TE	CP	SD&(~D&TI D&~TI)

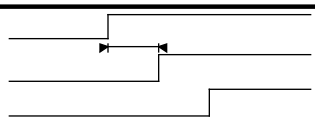
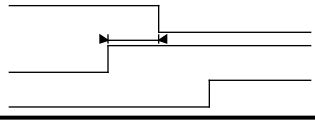
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	DCARE	
HOLD	POSEDGE	DCARE	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.467	0.446	0.411	0.297
0.38	0.518	0.496	0.460	0.343
1.00	0.602	0.580	0.542	0.421
3.00	0.876	0.850	0.808	0.671

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.190	0.211	0.246	0.360
0.38	0.139	0.161	0.197	0.314
1.00	0.054	0.077	0.114	0.236
3.00	-0.220	-0.195	-0.152	-0.015

TIMING CONDITION

DATA	CLOCK	CONDITION
TI	CP	SD&TE

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

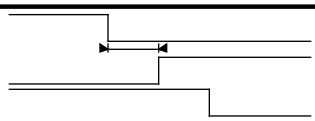
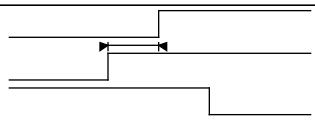
SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.501	0.479	0.443	0.326
0.38	0.538	0.516	0.480	0.362
1.00	0.602	0.579	0.542	0.421
3.00	0.806	0.782	0.742	0.613

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.073	-0.040	0.016	0.195
0.38	-0.096	-0.063	-0.008	0.171
1.00	-0.135	-0.102	-0.048	0.130
3.00	-0.261	-0.229	-0.176	-0.004

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
TI	CP	SD&TE

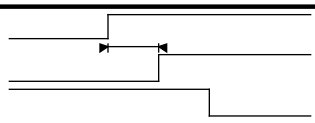
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.723	0.689	0.632	0.447
0.38	0.746	0.712	0.655	0.472
1.00	0.785	0.752	0.695	0.513
3.00	0.911	0.879	0.824	0.647

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.154	0.176	0.213	0.331
0.38	0.116	0.139	0.176	0.296
1.00	0.054	0.076	0.114	0.236
3.00	-0.149	-0.126	-0.085	0.044

TIMING CONDITION

DATA	CLOCK	CONDITION
SD	CP	(~TE&~D TE&~TI)

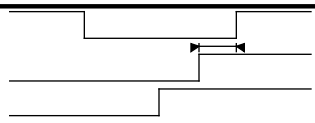
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.156	0.119	0.057	-0.143
0.38	0.189	0.152	0.091	-0.107
1.00	0.243	0.207	0.147	-0.048
3.00	0.418	0.384	0.327	0.144

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
SD	CP	(~TE&~D TE&~TI)

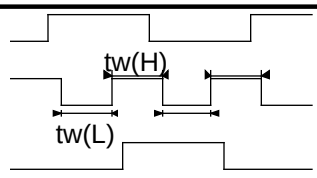
ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.500	0.537	0.600	0.800
0.38	0.468	0.504	0.566	0.764
1.00	0.413	0.449	0.510	0.705
3.00	0.237	0.271	0.328	0.513

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	SD

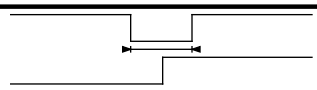
ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.810

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
SD	---

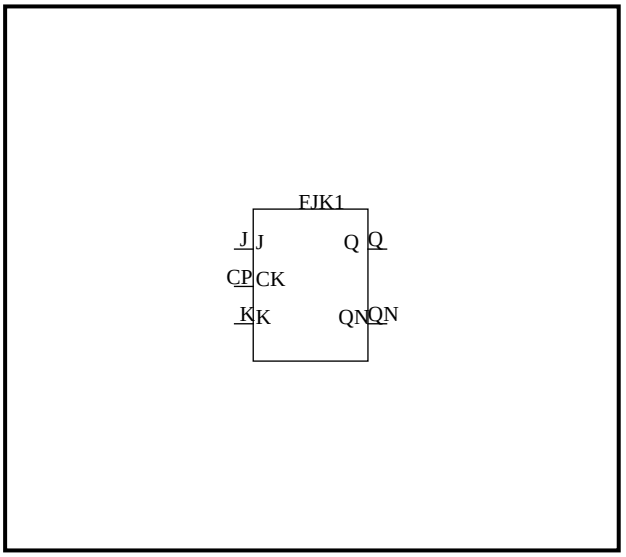
ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.760

FJK1	FJK1	1/4

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FJK1	J-K FLIP FLOP	9	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT	
J	K	CP	Qn+1	QNn+1
L	L	Up	Qn	QNn
L	H	Up	L	H
H	L	Up	H	L
H	H	Up	QNn	Qn
X	X	Dn	Qn	QNn

Verilog-HDL DESCRIPTION

```
FJK1  inst(Q,QN,J,K,CP);
```

VHDL DESCRIPTION

```
inst:FJK1
   port   map(Q,QN,J,K,CP);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q	QN
ELECTRO MIGRATION DRIVE	6880.0	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
J	0.98
K	1.00
CP	1.01

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	42.2	50.0

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FJK1 FJK1 2/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0982	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.66	0.84	1.54
0.38	0.57	0.74	0.92	1.62
1.00	0.65	0.81	1.00	1.70
3.00	0.78	0.95	1.13	1.83

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0417	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.44	0.59	0.74	1.27
0.38	0.52	0.67	0.82	1.35
1.00	0.60	0.75	0.90	1.43
3.00	0.74	0.90	1.05	1.57

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0858	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.58	0.72	0.88	1.49
0.38	0.66	0.80	0.95	1.57
1.00	0.74	0.88	1.04	1.65
3.00	0.89	1.02	1.18	1.80

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0345	0.11

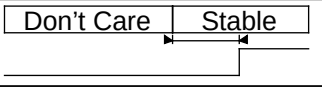
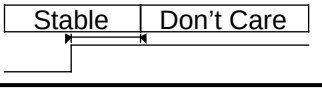
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.63	0.75	0.87	1.29
0.38	0.71	0.83	0.94	1.37
1.00	0.79	0.90	1.02	1.45
3.00	0.92	1.04	1.16	1.58

FJK1 FJK1 3/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
J	CP	---

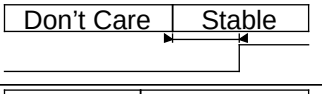
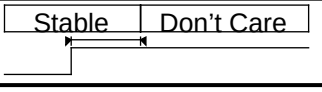
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	DCARE	
HOLD	POSEDGE	DCARE	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.549	0.514	0.456	0.267
0.38	0.585	0.550	0.492	0.304
1.00	0.645	0.611	0.553	0.366
3.00	0.840	0.806	0.749	0.565

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.109	0.143	0.202	0.390
0.38	0.072	0.107	0.165	0.353
1.00	0.011	0.046	0.104	0.290
3.00	-0.185	-0.151	-0.094	0.090

TIMING CONDITION

DATA	CLOCK	CONDITION
K	CP	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	DCARE	
HOLD	POSEDGE	DCARE	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.483	0.465	0.435	0.337
0.38	0.537	0.519	0.488	0.387
1.00	0.629	0.609	0.576	0.471
3.00	0.923	0.900	0.863	0.741

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.171	0.190	0.220	0.319
0.38	0.117	0.136	0.168	0.269
1.00	0.026	0.046	0.079	0.185
3.00	-0.267	-0.244	-0.207	-0.085

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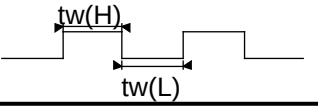
FJK1	FJK1	4/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	---

ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

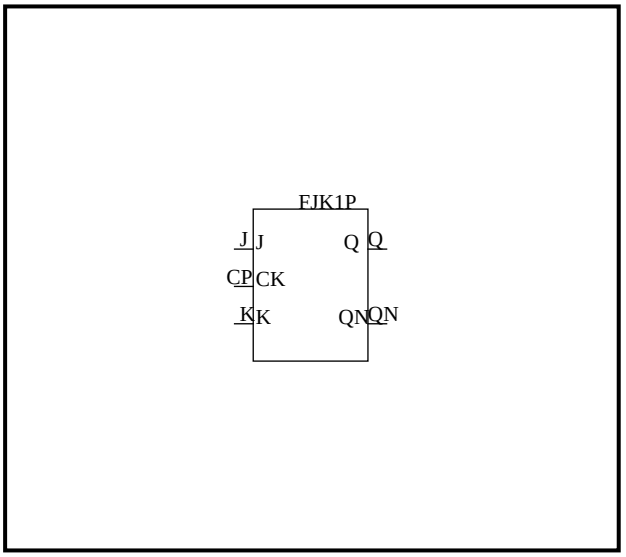
NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.770

Rev.1.01.10

FJK1P	FJK1P	1/4

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FJK1P	J-K FLIP FLOP	10	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT	
J	K	CP	Qn+1	QNn+1
L	L	Up	Qn	QNn
L	H	Up	L	H
H	L	Up	H	L
H	H	Up	QNn	Qn
X	X	Dn	Qn	QNn

Verilog-HDL DESCRIPTION

```
FJK1P  inst(Q,QN,J,K,CP);
```

VHDL DESCRIPTION

```
inst:FJK1P
   port   map(Q,QN,J,K,CP);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q	QN
ELECTRO MIGRATION DRIVE	6880.0	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
J	0.98
K	1.00
CP	1.01

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	75.2	96.9

Rev.1.01.10

FJK1P | FJK1P | 2/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0541	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.57	0.68	1.06
0.38	0.56	0.65	0.75	1.14
1.00	0.64	0.73	0.83	1.21
3.00	0.77	0.87	0.97	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0253	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.43	0.53	0.63	0.96
0.38	0.51	0.61	0.71	1.04
1.00	0.59	0.69	0.79	1.12
3.00	0.74	0.84	0.94	1.27

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0443	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.64	0.71	0.80	1.11
0.38	0.72	0.79	0.87	1.19
1.00	0.80	0.87	0.96	1.27
3.00	0.95	1.02	1.10	1.42

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0181	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.69	0.76	0.84	1.08
0.38	0.77	0.84	0.91	1.15
1.00	0.85	0.92	0.99	1.23
3.00	0.98	1.05	1.13	1.37

FJK1P | FJK1P | 3/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
J	CP	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	DCARE	J,K: Don't Care | Stable; CP
HOLD	POSEDGE	DCARE	J,K: Stable | Don't Care; CP

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.549	0.514	0.456	0.267
0.38	0.585	0.550	0.492	0.304
1.00	0.645	0.611	0.553	0.366
3.00	0.840	0.806	0.749	0.565

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.109	0.143	0.202	0.390
0.38	0.072	0.107	0.165	0.353
1.00	0.011	0.046	0.104	0.290
3.00	-0.185	-0.151	-0.094	0.090

TIMING CONDITION

DATA	CLOCK	CONDITION
K	CP	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	DCARE	J,K: Don't Care | Stable; CP
HOLD	POSEDGE	DCARE	J,K: Stable | Don't Care; CP

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.483	0.465	0.435	0.337
0.38	0.537	0.519	0.488	0.387
1.00	0.629	0.609	0.576	0.471
3.00	0.923	0.900	0.863	0.741

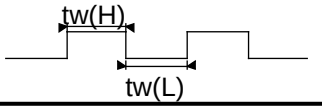
HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.171	0.190	0.220	0.319
0.38	0.117	0.136	0.168	0.269
1.00	0.026	0.046	0.079	0.185
3.00	-0.267	-0.244	-0.207	-0.085

FJK1P	FJK1P	4/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	---

ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.770

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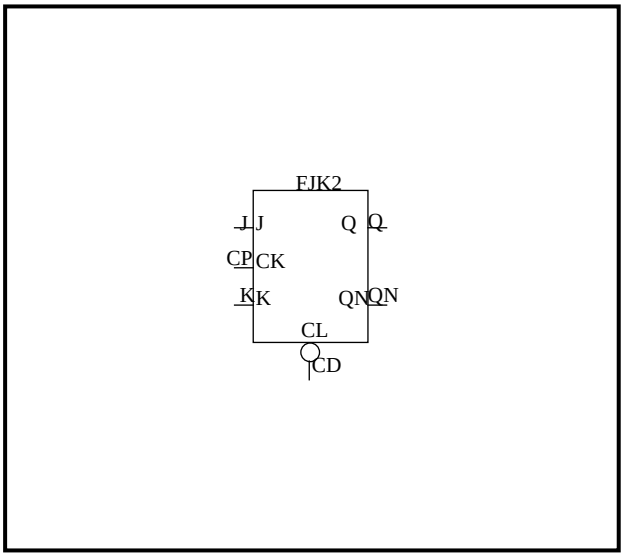
FJK2	FJK2	1/6

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FJK2	J-K FLIP FLOP with CLEAR	10	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT	
CD	J	K	CP	Qn+1	QNn+1
L	X	X	X*	L	H
H	L	L	Up	Qn	QNn
H	L	H	Up	L	H
H	H	L	Up	H	L
H	H	H	Up	QNn	Qn
H	X	X	Dn	Qn	QNn

*:Consider the HOLD Time of CLEAR

Verilog-HDL DESCRIPTION

```
FJK2  inst(Q,QN,J,K,CP,CD);
```

VHDL DESCRIPTION

```
inst:FJK2
   port   map(Q,QN,J,K,CP,CD);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
J	0.98
K	0.99
CP	1.02
CD	2.26

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	44.8	42.5

Rev.1.01.10

FJK2 FJK2 2/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0399	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.64	0.79	1.29
0.38	0.49	0.65	0.80	1.30
1.00	0.55	0.71	0.86	1.36
3.00	0.74	0.91	1.06	1.56

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.1001	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.64	0.78	0.95	1.62
0.38	0.65	0.79	0.96	1.64
1.00	0.71	0.85	1.02	1.70
3.00	0.91	1.05	1.22	1.90

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0924	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.53	0.69	0.86	1.52
0.38	0.61	0.76	0.94	1.60
1.00	0.69	0.84	1.02	1.68
3.00	0.82	0.98	1.16	1.82

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0399	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.43	0.57	0.72	1.22
0.38	0.51	0.65	0.80	1.30
1.00	0.59	0.73	0.88	1.38
3.00	0.73	0.88	1.03	1.53

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.1001	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.57	0.71	0.88	1.57
0.38	0.65	0.79	0.96	1.64
1.00	0.73	0.87	1.04	1.72
3.00	0.88	1.02	1.19	1.87

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0420	0.11

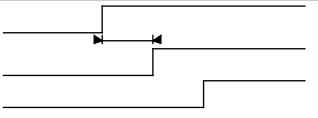
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.68	0.81	0.94	1.44
0.38	0.76	0.88	1.02	1.51
1.00	0.84	0.96	1.10	1.59
3.00	0.98	1.10	1.23	1.73

FJK2 FJK2 4/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

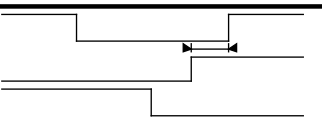
DATA	CLOCK	CONDITION
CD	CP	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.156	0.121	0.063	-0.125
0.38	0.192	0.157	0.099	-0.087
1.00	0.251	0.217	0.160	-0.024
3.00	0.442	0.410	0.355	0.179

TIMING CONDITION

DATA	CLOCK	CONDITION
CD	CP	---

ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.500	0.535	0.594	0.782
0.38	0.465	0.499	0.557	0.744
1.00	0.405	0.439	0.497	0.681
3.00	0.213	0.246	0.301	0.477

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FJK2 FJK2 5/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
J	CP	CD

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	DCARE	J,K: Don't Care | Stable; CP
HOLD	POSEDGE	DCARE	J,K: Stable | Don't Care; CP

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.619	0.591	0.543	0.389
0.38	0.655	0.627	0.579	0.425
1.00	0.716	0.687	0.640	0.486
3.00	0.911	0.883	0.836	0.683

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.038	0.066	0.113	0.265
0.38	0.002	0.030	0.077	0.229
1.00	-0.059	-0.031	0.016	0.168
3.00	-0.255	-0.227	-0.179	-0.026

TIMING CONDITION

DATA	CLOCK	CONDITION
K	CP	CD

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	DCARE	J,K: Don't Care | Stable; CP
HOLD	POSEDGE	DCARE	J,K: Stable | Don't Care; CP

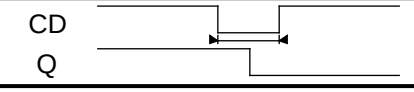
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.525	0.496	0.449	0.297
0.38	0.583	0.555	0.507	0.356
1.00	0.680	0.652	0.605	0.454
3.00	0.993	0.966	0.919	0.771

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.131	0.159	0.207	0.360
0.38	0.073	0.101	0.149	0.302
1.00	-0.024	0.004	0.051	0.203
3.00	-0.338	-0.310	-0.264	-0.115

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

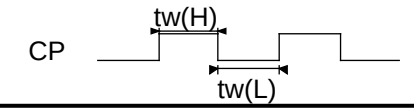
CLOCK	CONDITION
CD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.840

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	CD

ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

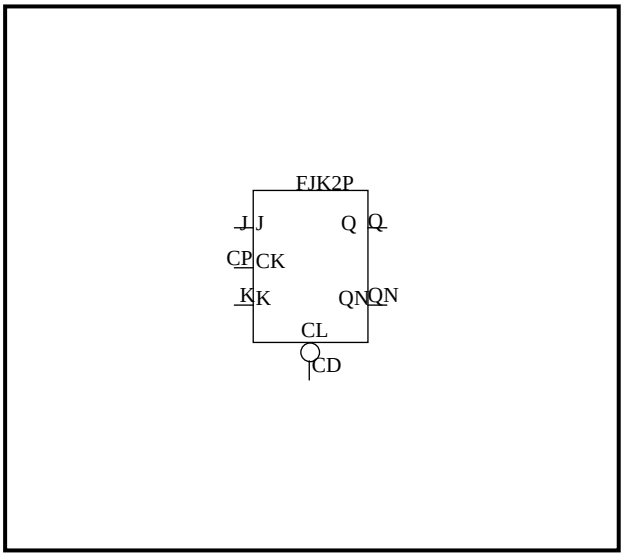
POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.790

FJK2P	FJK2P	1/6

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FJK2P	J-K FLIP FLOP with CLEAR	11	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT	
CD	J	K	CP	Qn+1	QNn+1
L	X	X	X*	L	H
H	L	L	Up	Qn	QNn
H	L	H	Up	L	H
H	H	L	Up	H	L
H	H	H	Up	QNn	Qn
H	X	X	Dn	Qn	QNn

*:Consider the HOLD Time of CLEAR

Verilog-HDL DESCRIPTION

```
FJK2P  inst(Q,QN,J,K,CP,CD);
```

VHDL DESCRIPTION

```
inst:FJK2P
   port   map(Q,QN,J,K,CP,CD);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
J	0.98
K	0.99
CP	1.02
CD	2.31

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	74.5	77.4

Rev.1.01.10

FJK2P | FJK2P | 2/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0256	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.59	0.70	1.04
0.38	0.50	0.61	0.71	1.05
1.00	0.56	0.67	0.77	1.11
3.00	0.75	0.87	0.98	1.32

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0546	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.72	0.80	0.90	1.27
0.38	0.73	0.81	0.91	1.28
1.00	0.79	0.87	0.97	1.34
3.00	1.00	1.08	1.18	1.55

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0539	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.65	0.76	1.15
0.38	0.63	0.72	0.83	1.23
1.00	0.71	0.80	0.91	1.30
3.00	0.85	0.94	1.05	1.44

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0256	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.44	0.54	0.64	0.97
0.38	0.52	0.62	0.72	1.05
1.00	0.60	0.70	0.80	1.13
3.00	0.75	0.85	0.95	1.28

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0546	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.65	0.73	0.83	1.20
0.38	0.73	0.81	0.91	1.28
1.00	0.81	0.89	0.99	1.36
3.00	0.96	1.04	1.14	1.51

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	FALL

SLEW FACTOR

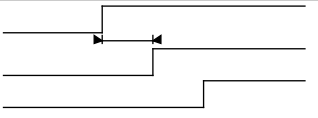
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0235	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.77	0.85	0.94	1.23
0.38	0.85	0.93	1.02	1.31
1.00	0.93	1.01	1.09	1.39
3.00	1.07	1.15	1.23	1.53

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

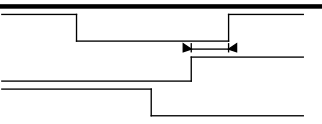
DATA	CLOCK	CONDITION
CD	CP	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.156	0.121	0.063	-0.125
0.38	0.192	0.157	0.099	-0.087
1.00	0.251	0.217	0.160	-0.024
3.00	0.442	0.410	0.355	0.179

TIMING CONDITION

DATA	CLOCK	CONDITION
CD	CP	---

ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

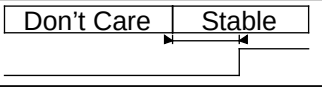
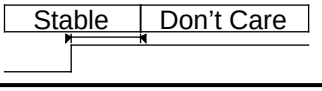
HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.500	0.535	0.594	0.782
0.38	0.465	0.499	0.557	0.744
1.00	0.405	0.439	0.497	0.681
3.00	0.213	0.246	0.301	0.477

FJK2P | FJK2P | 5/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
J	CP	CD

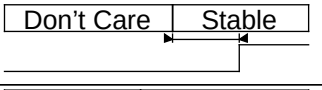
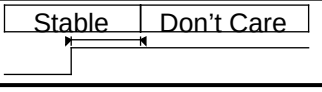
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	DCARE	
HOLD	POSEDGE	DCARE	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.619	0.591	0.543	0.389
0.38	0.655	0.627	0.579	0.425
1.00	0.716	0.687	0.640	0.486
3.00	0.911	0.883	0.836	0.683

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.038	0.066	0.113	0.265
0.38	0.002	0.030	0.077	0.229
1.00	-0.059	-0.031	0.016	0.168
3.00	-0.255	-0.227	-0.179	-0.026

TIMING CONDITION

DATA	CLOCK	CONDITION
K	CP	CD

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	DCARE	
HOLD	POSEDGE	DCARE	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.525	0.496	0.449	0.297
0.38	0.583	0.555	0.507	0.356
1.00	0.680	0.652	0.605	0.454
3.00	0.993	0.966	0.919	0.771

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.131	0.159	0.207	0.360
0.38	0.073	0.101	0.149	0.302
1.00	-0.024	0.004	0.051	0.203
3.00	-0.338	-0.310	-0.264	-0.115

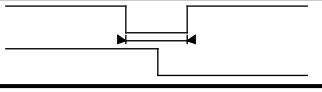
Rev.1.01.10

FJK2P	FJK2P	6/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

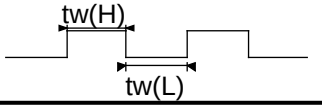
CLOCK	CONDITION
CD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.840

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	CD

ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

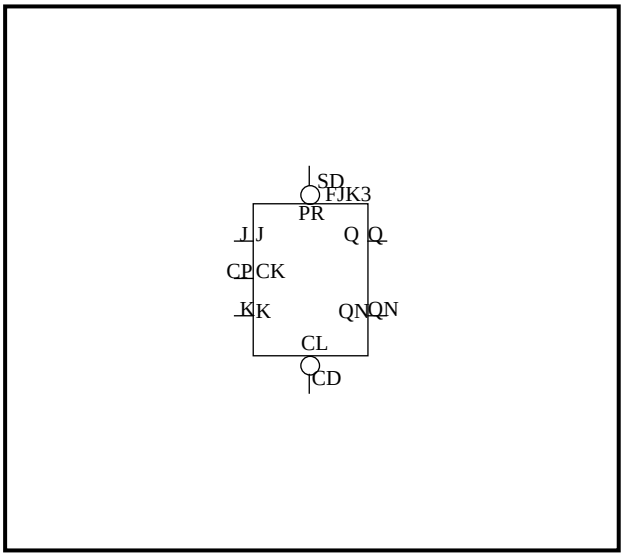
NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.790

Rev.1.01.10

FJK3	FJK3	1/8

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FJK3	J-K FLIP FLOP with CLEAR and PRESET	11	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT					OUTPUT	
CD	SD	J	K	CP	Qn+1	QNn+1
L	H	X	X	X*	L	H
H	L	X	X	X*	H	L
L	L	X	X	X	L	L
H	H	L	L	Up	Qn	QNn
H	H	L	H	Up	L	H
H	H	H	L	Up	H	L
H	H	H	H	Up	QNn	Qn
H	H	X	X	Dn	Qn	QNn

*:Consider the HOLD Time
of CLEAR or PRESET

Verilog-HDL DESCRIPTION

```
FJK3 inst(Q,QN,J,K,CP,CD,SD);
```

VHDL DESCRIPTION

```
inst:FJK3
  port map(Q,QN,J,K,CP,CD,SD);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
J	0.99
K	0.98
CP	1.02
CD	2.20
SD	2.32

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	43.3	50.0

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0837	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.43	0.58	1.18
0.38	0.34	0.48	0.64	1.24
1.00	0.42	0.56	0.71	1.31
3.00	0.57	0.71	0.87	1.48

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0364	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.57	0.71	1.17
0.38	0.44	0.58	0.72	1.18
1.00	0.50	0.64	0.78	1.24
3.00	0.69	0.84	0.98	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0399	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.33	0.46	0.93
0.38	0.25	0.36	0.48	0.96
1.00	0.30	0.42	0.54	1.01
3.00	0.39	0.52	0.65	1.13

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0961	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.37	0.54	1.21
0.38	0.29	0.44	0.61	1.28
1.00	0.38	0.53	0.70	1.37
3.00	0.56	0.71	0.89	1.56

FJK3 FJK3 3/8

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0837	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.70	0.86	1.47
0.38	0.58	0.72	0.88	1.49
1.00	0.63	0.78	0.94	1.54
3.00	0.76	0.90	1.06	1.66

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0961	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.70	0.87	1.55
0.38	0.63	0.78	0.95	1.62
1.00	0.71	0.86	1.03	1.71
3.00	0.86	1.01	1.18	1.85

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0399	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.66	0.78	0.90	1.38
0.38	0.74	0.86	0.98	1.45
1.00	0.82	0.93	1.06	1.53
3.00	0.96	1.08	1.20	1.67

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0837	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.91	1.05	1.21	1.80
0.38	0.99	1.13	1.28	1.88
1.00	1.07	1.21	1.36	1.96
3.00	1.21	1.35	1.51	2.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0364	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.75	0.87	1.00	1.45
0.38	0.83	0.95	1.08	1.53
1.00	0.91	1.03	1.16	1.61
3.00	1.06	1.18	1.31	1.76

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->Q	---	RISE

SLEW FACTOR

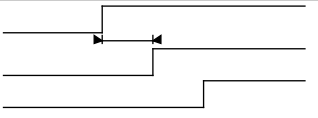
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0961	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.69	0.84	1.01	1.68
0.38	0.70	0.85	1.02	1.69
1.00	0.76	0.91	1.08	1.75
3.00	0.97	1.11	1.28	1.98

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

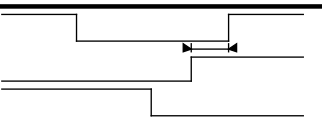
DATA	CLOCK	CONDITION
CD	CP	SD

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.039	-0.077	-0.141	-0.349
0.38	-0.043	-0.081	-0.146	-0.353
1.00	-0.050	-0.089	-0.153	-0.360
3.00	-0.073	-0.112	-0.176	-0.384

TIMING CONDITION

DATA	CLOCK	CONDITION
CD	CP	SD

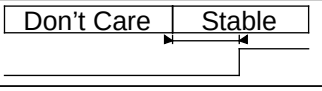
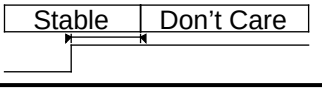
ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.693	0.731	0.796	1.003
0.38	0.697	0.736	0.800	1.008
1.00	0.705	0.743	0.808	1.015
3.00	0.730	0.768	0.832	1.040

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
J	CP	CD&SD

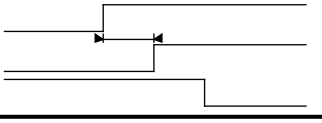
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	DCARE	
HOLD	POSEDGE	DCARE	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.560	0.529	0.476	0.308
0.38	0.618	0.587	0.535	0.367
1.00	0.717	0.686	0.634	0.467
3.00	1.034	1.004	0.953	0.788

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.097	0.128	0.180	0.348
0.38	0.038	0.069	0.121	0.289
1.00	-0.061	-0.030	0.022	0.189
3.00	-0.378	-0.348	-0.297	-0.132

TIMING CONDITION

DATA	CLOCK	CONDITION
SD	CP	CD

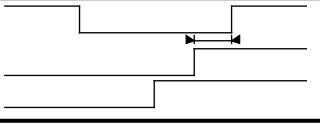
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.057	0.021	-0.040	-0.236
0.38	0.108	0.072	0.012	-0.181
1.00	0.194	0.159	0.100	-0.089
3.00	0.471	0.439	0.384	0.208

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

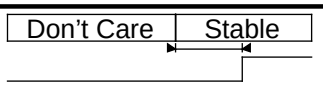
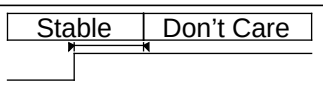
DATA	CLOCK	CONDITION
SD	CP	CD

ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.600	0.636	0.697	0.893
0.38	0.549	0.584	0.644	0.838
1.00	0.462	0.497	0.556	0.745
3.00	0.184	0.217	0.272	0.448

TIMING CONDITION

DATA	CLOCK	CONDITION
K	CP	CD&SD

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	DCARE	
HOLD	POSEDGE	DCARE	

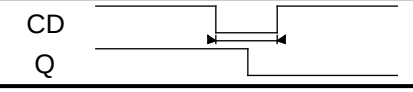
SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.566	0.538	0.491	0.337
0.38	0.603	0.574	0.527	0.374
1.00	0.663	0.635	0.587	0.434
3.00	0.858	0.830	0.783	0.630

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.090	0.119	0.166	0.319
0.38	0.054	0.082	0.130	0.283
1.00	-0.007	0.022	0.069	0.222
3.00	-0.202	-0.174	-0.126	0.026

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

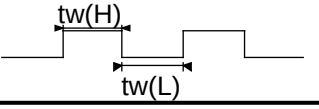
CLOCK	CONDITION
CD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.740

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	SD&CD

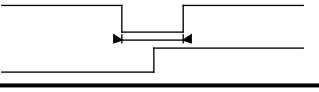
ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.800

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
SD	---

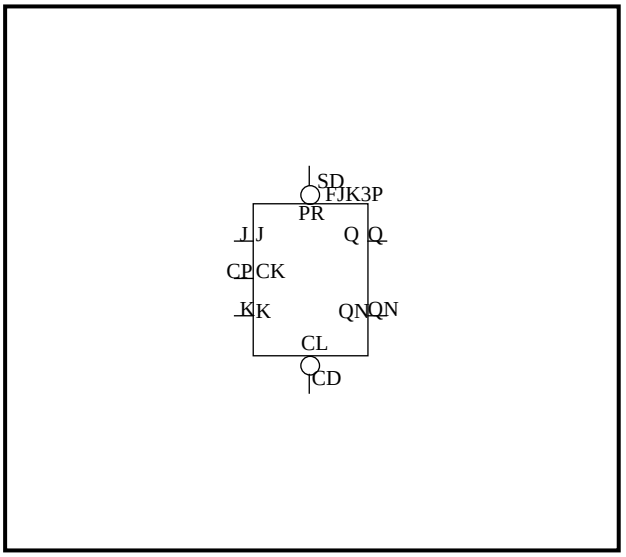
ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.850

FJK3P	FJK3P	1/8

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FJK3P	J-K FLIP FLOP with CLEAR and PRESET	12	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT					OUTPUT	
CD	SD	J	K	CP	Qn+1	QNn+1
L	H	X	X	X*	L	H
H	L	X	X	X*	H	L
L	L	X	X	X	L	L
H	H	L	L	Up	Qn	QNn
H	H	L	H	Up	L	H
H	H	H	L	Up	H	L
H	H	H	H	Up	QNn	Qn
H	H	X	X	Dn	Qn	QNn

*:Consider the HOLD Time
of CLEAR or PRESET

Verilog-HDL DESCRIPTION

```
FJK3P  inst(Q,QN,J,K,CP,CD,SD);
```

VHDL DESCRIPTION

```
inst:FJK3P
   port   map(Q,QN,J,K,CP,CD,SD);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
J	1.00
K	0.98
CP	1.01
CD	2.35
SD	2.09

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	82.9	80.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0543	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.39	0.49	0.88
0.38	0.36	0.45	0.55	0.93
1.00	0.44	0.52	0.63	1.01
3.00	0.60	0.70	0.80	1.18

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0205	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.51	0.61	0.90
0.38	0.42	0.53	0.62	0.91
1.00	0.49	0.59	0.68	0.98
3.00	0.69	0.80	0.89	1.19

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0182	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.32	0.39	0.63
0.38	0.27	0.35	0.42	0.66
1.00	0.35	0.42	0.49	0.74
3.00	0.50	0.58	0.66	0.91

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0547	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.32	0.42	0.79
0.38	0.28	0.37	0.47	0.84
1.00	0.35	0.43	0.53	0.91
3.00	0.48	0.57	0.67	1.05

FJK3P | FJK3P | 3/8

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0543	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.69	0.78	0.88	1.27
0.38	0.71	0.80	0.91	1.30
1.00	0.78	0.87	0.98	1.36
3.00	0.96	1.06	1.16	1.55

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0547	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.54	0.63	0.73	1.10
0.38	0.62	0.71	0.81	1.18
1.00	0.70	0.79	0.89	1.27
3.00	0.85	0.94	1.04	1.41

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0182	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.61	0.68	0.75	1.00
0.38	0.69	0.76	0.83	1.07
1.00	0.77	0.84	0.91	1.15
3.00	0.91	0.98	1.05	1.29

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0543	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.94	1.03	1.13	1.51
0.38	1.02	1.11	1.21	1.59
1.00	1.10	1.19	1.29	1.67
3.00	1.24	1.33	1.43	1.81

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0205	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.82	0.91	0.99	1.27
0.38	0.90	0.99	1.07	1.35
1.00	0.98	1.07	1.15	1.43
3.00	1.13	1.22	1.30	1.58

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->Q	---	RISE

SLEW FACTOR

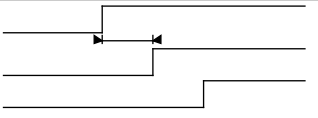
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0547	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.77	0.86	0.96	1.33
0.38	0.78	0.87	0.97	1.34
1.00	0.84	0.93	1.03	1.40
3.00	1.07	1.15	1.25	1.63

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

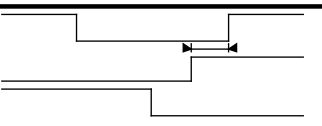
DATA	CLOCK	CONDITION
CD	CP	SD

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.039	-0.077	-0.141	-0.349
0.38	-0.043	-0.081	-0.146	-0.353
1.00	-0.050	-0.089	-0.153	-0.360
3.00	-0.073	-0.112	-0.176	-0.384

TIMING CONDITION

DATA	CLOCK	CONDITION
CD	CP	SD

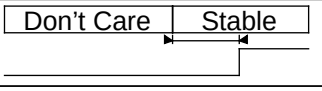
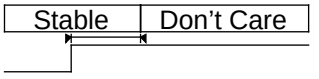
ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.693	0.731	0.796	1.003
0.38	0.697	0.736	0.800	1.008
1.00	0.705	0.743	0.808	1.015
3.00	0.730	0.768	0.832	1.040

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
J	CP	CD&SD

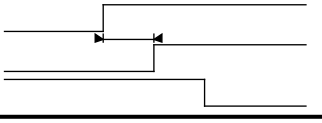
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	DCARE	
HOLD	POSEDGE	DCARE	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.560	0.529	0.476	0.308
0.38	0.618	0.587	0.535	0.367
1.00	0.717	0.686	0.634	0.467
3.00	1.034	1.004	0.953	0.788

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.097	0.128	0.180	0.348
0.38	0.038	0.069	0.121	0.289
1.00	-0.061	-0.030	0.022	0.189
3.00	-0.378	-0.348	-0.297	-0.132

TIMING CONDITION

DATA	CLOCK	CONDITION
SD	CP	CD

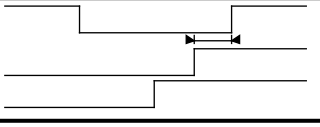
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.057	0.021	-0.040	-0.236
0.38	0.108	0.072	0.012	-0.181
1.00	0.194	0.159	0.100	-0.089
3.00	0.471	0.439	0.384	0.208

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

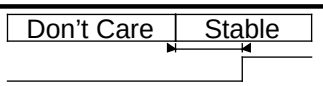
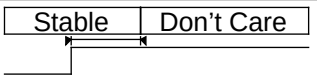
DATA	CLOCK	CONDITION
SD	CP	CD

ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.600	0.636	0.697	0.893
0.38	0.549	0.584	0.644	0.838
1.00	0.462	0.497	0.556	0.745
3.00	0.184	0.217	0.272	0.448

TIMING CONDITION

DATA	CLOCK	CONDITION
K	CP	CD&SD

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	DCARE	
HOLD	POSEDGE	DCARE	

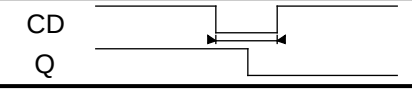
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.566	0.538	0.491	0.337
0.38	0.603	0.574	0.527	0.374
1.00	0.663	0.635	0.587	0.434
3.00	0.858	0.830	0.783	0.630

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.090	0.119	0.166	0.319
0.38	0.054	0.082	0.130	0.283
1.00	-0.007	0.022	0.069	0.222
3.00	-0.202	-0.174	-0.126	0.026

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

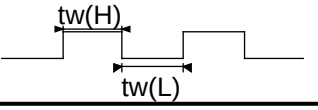
CLOCK	CONDITION
CD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.740

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	SD&CD

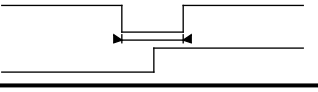
ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.800

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
SD	---

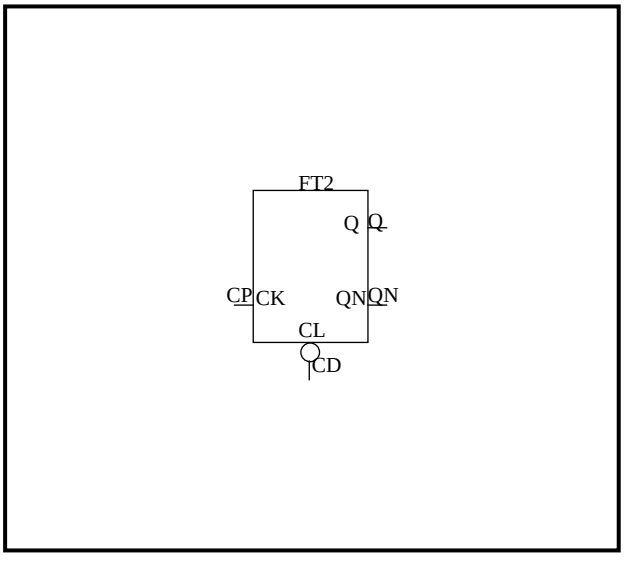
ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.850

FT2	FT2	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FT2	TOGGLE FLIP FLOP with CLEAR	8	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
CD	CP	Qn+1	QNn+1
L	X*	L	H
H	Up	QNn	Qn
H	Dn	Qn	QNn

*:Consider the HOLD Time of CLEAR

Verilog-HDL DESCRIPTION

```
FT2  inst(Q,QN,CP,CD);
```

VHDL DESCRIPTION

```
inst:FT2
   port   map(Q,QN,CP,CD);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
CP	0.99
CD	2.17

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	47.3	48.8

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0339	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.35	0.46	0.88
0.38	0.26	0.37	0.49	0.90
1.00	0.33	0.44	0.56	0.97
3.00	0.46	0.59	0.71	1.13

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0885	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.63	0.79	1.41
0.38	0.52	0.66	0.82	1.44
1.00	0.59	0.73	0.89	1.51
3.00	0.75	0.89	1.05	1.67

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0935	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.53	0.67	0.84	1.49
0.38	0.61	0.75	0.92	1.56
1.00	0.69	0.83	1.00	1.65
3.00	0.85	0.99	1.16	1.81

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0339	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.65	0.77	1.18
0.38	0.63	0.73	0.85	1.26
1.00	0.71	0.81	0.93	1.34
3.00	0.85	0.96	1.08	1.49

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0885	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.70	0.83	0.98	1.59
0.38	0.78	0.91	1.06	1.67
1.00	0.86	0.99	1.14	1.75
3.00	1.01	1.13	1.29	1.90

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0356	0.10

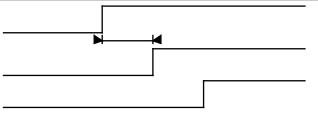
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.69	0.80	0.92	1.35
0.38	0.77	0.88	1.00	1.43
1.00	0.85	0.97	1.08	1.52
3.00	1.01	1.13	1.24	1.68

FT2	FT2	4/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

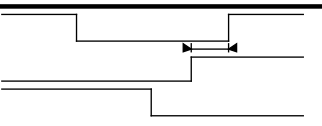
DATA	CLOCK	CONDITION
CD	CP	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.027	-0.067	-0.133	-0.349
0.38	-0.029	-0.069	-0.135	-0.350
1.00	-0.033	-0.072	-0.138	-0.351
3.00	-0.044	-0.083	-0.147	-0.355

TIMING CONDITION

DATA	CLOCK	CONDITION
CD	CP	---

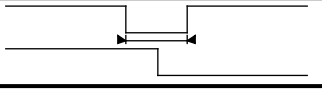
ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.681	0.721	0.788	1.003
0.38	0.684	0.723	0.790	1.004
1.00	0.687	0.727	0.793	1.006
3.00	0.700	0.738	0.802	1.010

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

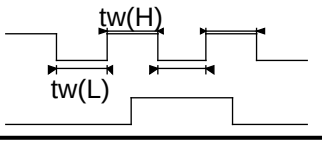
CLOCK	CONDITION
CD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.910

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	CD

ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

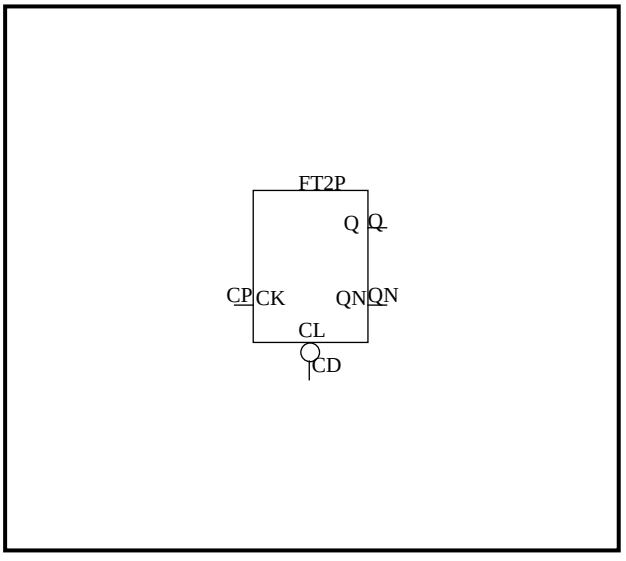
POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.930

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

FT2P	FT2P	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FT2P	TOGGLE FLIP FLOP with CLEAR	9	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
CD	CP	Qn+1	QNn+1
L	X*	L	H
H	Up	QNn	Qn
H	Dn	Qn	QNn

*:Consider the HOLD Time of CLEAR

Verilog-HDL DESCRIPTION

```
FT2P  inst(Q,QN,CP,CD);
```

VHDL DESCRIPTION

```
inst:FT2P
   port   map(Q,QN,CP,CD);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q	QN
ELECTRO MIGRATION DRIVE	6880.0	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
CP	0.99
CD	2.17

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	82.9	97.6

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FT2P | FT2P | 2/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0182	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.32	0.39	0.63
0.38	0.27	0.34	0.42	0.66
1.00	0.34	0.41	0.49	0.73
3.00	0.48	0.57	0.65	0.89

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0441	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.63	0.72	1.04
0.38	0.58	0.66	0.75	1.07
1.00	0.66	0.73	0.82	1.15
3.00	0.84	0.92	1.00	1.33

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0546	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.63	0.73	1.11
0.38	0.62	0.71	0.81	1.19
1.00	0.71	0.80	0.90	1.27
3.00	0.87	0.96	1.06	1.43

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0182	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.56	0.63	0.70	0.94
0.38	0.64	0.71	0.78	1.02
1.00	0.72	0.79	0.86	1.10
3.00	0.87	0.94	1.01	1.25

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0441	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.76	0.83	0.91	1.23
0.38	0.84	0.91	0.99	1.30
1.00	0.92	0.99	1.07	1.39
3.00	1.07	1.14	1.22	1.53

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0180	0.11

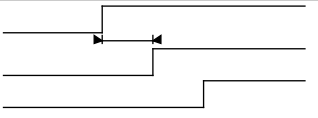
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.76	0.83	0.90	1.14
0.38	0.84	0.91	0.98	1.22
1.00	0.92	0.99	1.06	1.30
3.00	1.08	1.15	1.22	1.46

FT2P	FT2P	4/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

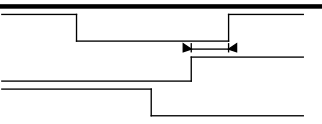
DATA	CLOCK	CONDITION
CD	CP	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.027	-0.067	-0.133	-0.349
0.38	-0.029	-0.069	-0.135	-0.350
1.00	-0.033	-0.072	-0.138	-0.351
3.00	-0.044	-0.083	-0.147	-0.355

TIMING CONDITION

DATA	CLOCK	CONDITION
CD	CP	---

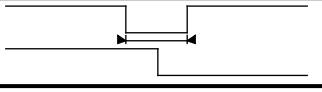
ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.681	0.721	0.788	1.003
0.38	0.684	0.723	0.790	1.004
1.00	0.687	0.727	0.793	1.006
3.00	0.700	0.738	0.802	1.010

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

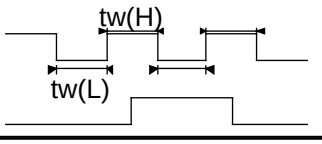
CLOCK	CONDITION
CD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.910

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	CD

ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.930

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

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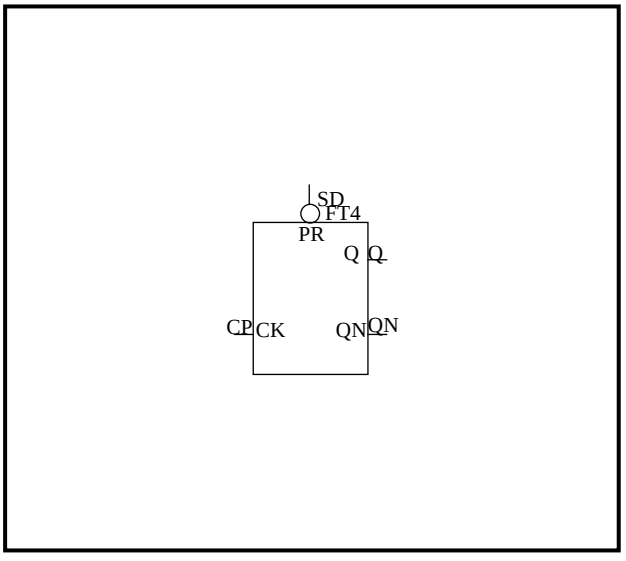
FT4	FT4	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FT4	TOGGLE FLIP FLOP with PRESET	8	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
SD	CP	Qn+1	QNn+1
L	X*	H	L
H	Up	QNn	Qn
H	Dn	Qn	QNn

*:Consider the HOLD Time of PRESET

Verilog-HDL DESCRIPTION

```
FT4  inst(Q,QN,CP,SD);
```

VHDL DESCRIPTION

```
inst:FT4
   port   map(Q,QN,CP,SD);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q	QN
ELECTRO MIGRATION DRIVE	6880.0	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
CP	0.99
SD	2.17

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	42.3	51.2

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.1002	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.47	0.62	0.79	1.47
0.38	0.55	0.70	0.87	1.55
1.00	0.64	0.78	0.95	1.63
3.00	0.80	0.94	1.11	1.79

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0423	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.57	0.69	0.82	1.32
0.38	0.65	0.77	0.90	1.40
1.00	0.73	0.85	0.98	1.48
3.00	0.88	1.00	1.13	1.63

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0838	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.79	0.93	1.08	1.67
0.38	0.87	1.01	1.16	1.75
1.00	0.95	1.09	1.24	1.84
3.00	1.10	1.24	1.39	1.98

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0339	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.65	0.76	0.88	1.30
0.38	0.73	0.84	0.96	1.38
1.00	0.82	0.93	1.04	1.46
3.00	0.97	1.08	1.20	1.62

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.1002	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.63	0.77	0.94	1.62
0.38	0.66	0.80	0.97	1.64
1.00	0.73	0.87	1.04	1.72
3.00	0.93	1.07	1.24	1.92

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0339	0.11

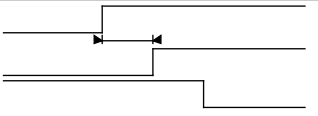
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.56	0.69	1.13
0.38	0.44	0.58	0.71	1.15
1.00	0.52	0.66	0.79	1.22
3.00	0.71	0.86	0.99	1.43

FT4	FT4	4/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

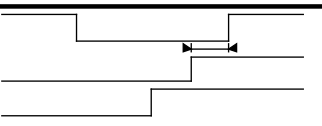
DATA	CLOCK	CONDITION
SD	CP	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.156	0.118	0.055	-0.150
0.38	0.189	0.151	0.088	-0.114
1.00	0.243	0.206	0.144	-0.055
3.00	0.418	0.384	0.325	0.137

TIMING CONDITION

DATA	CLOCK	CONDITION
SD	CP	---

ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.500	0.538	0.601	0.804
0.38	0.468	0.505	0.567	0.769
1.00	0.413	0.450	0.511	0.709
3.00	0.237	0.272	0.330	0.518

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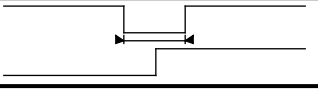
CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

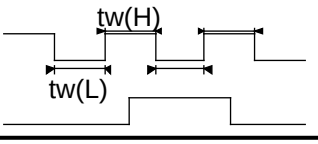
CLOCK	CONDITION
SD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	1.120

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	SD

ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

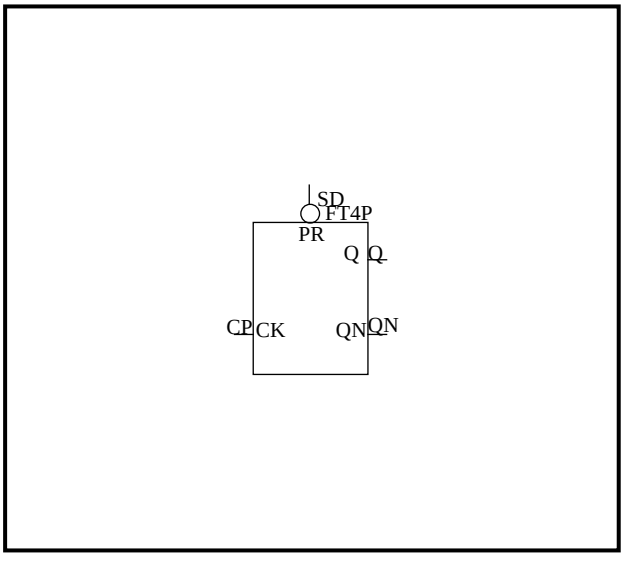
POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.960

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.920

FT4P	FT4P	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
FT4P	TOGGLE FLIP FLOP with PRESET	9	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
SD	CP	Qn+1	QNn+1
L	X*	H	L
H	Up	QNn	Qn
H	Dn	Qn	QNn

*:Consider the HOLD Time of PRESET

Verilog-HDL DESCRIPTION

```
FT4P  inst(Q,QN,CP,SD);
```

VHDL DESCRIPTION

```
inst:FT4P
   port   map(Q,QN,CP,SD);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q	QN
ELECTRO MIGRATION DRIVE	6880.0	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
CP	0.99
SD	2.19

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	77.1	95.9

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0549	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.47	0.55	0.65	1.02
0.38	0.55	0.63	0.73	1.10
1.00	0.64	0.72	0.82	1.19
3.00	0.79	0.88	0.97	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0238	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.57	0.65	0.73	1.03
0.38	0.65	0.73	0.81	1.11
1.00	0.73	0.81	0.90	1.19
3.00	0.88	0.96	1.04	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0444	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.84	0.92	1.00	1.32
0.38	0.92	1.00	1.08	1.40
1.00	1.00	1.08	1.16	1.48
3.00	1.15	1.22	1.31	1.63

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0185	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.69	0.77	0.84	1.09
0.38	0.77	0.85	0.92	1.17
1.00	0.86	0.93	1.01	1.25
3.00	1.02	1.09	1.16	1.41

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0549	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.69	0.77	0.87	1.24
0.38	0.72	0.80	0.90	1.27
1.00	0.79	0.87	0.97	1.34
3.00	1.02	1.10	1.20	1.57

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0185	0.11

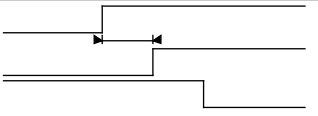
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.51	0.60	0.87
0.38	0.44	0.54	0.62	0.89
1.00	0.51	0.61	0.70	0.97
3.00	0.72	0.83	0.92	1.19

FT4P	FT4P	4/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

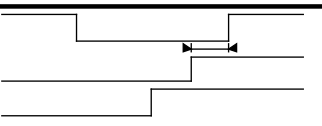
DATA	CLOCK	CONDITION
SD	CP	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.156	0.118	0.055	-0.150
0.38	0.189	0.151	0.088	-0.114
1.00	0.243	0.206	0.144	-0.055
3.00	0.418	0.384	0.325	0.137

TIMING CONDITION

DATA	CLOCK	CONDITION
SD	CP	---

ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.500	0.538	0.601	0.804
0.38	0.468	0.505	0.567	0.769
1.00	0.413	0.450	0.511	0.709
3.00	0.237	0.272	0.330	0.518

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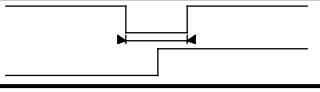
CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

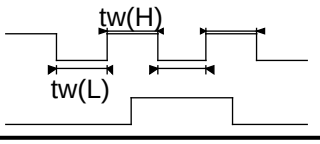
CLOCK	CONDITION
SD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	1.120

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	SD

ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

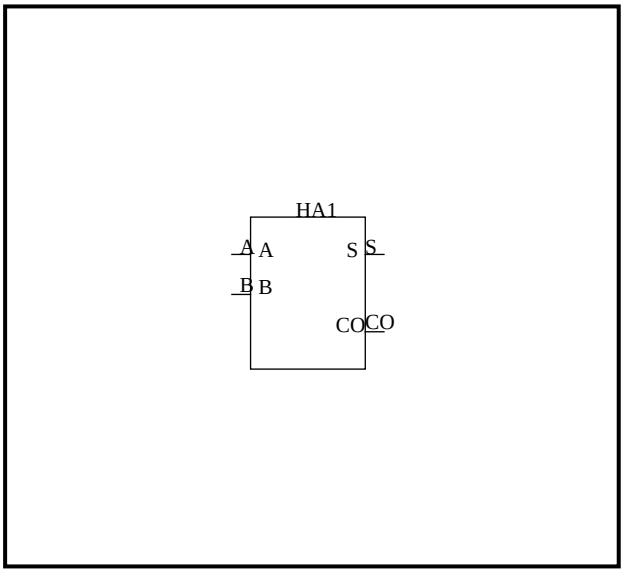
POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.960

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.920

HA1	HA1	1/4

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
HA1	HALF ADDER	5	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	B	S	CO
L	L	L	L
H	L	H	L
L	H	H	L
H	H	L	H

Verilog-HDL DESCRIPTION

```
HA1  inst(S,CO,A,B);
```

VHDL DESCRIPTION

```
inst:HA1
   port   map(S,CO,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	S,CO
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	2.00
B	3.19

OUTPUT DRIVE (LU)

PIN NAME	S	CO
DRIVE	47.6	48.7

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HA1 HA1 2/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->CO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0865	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.31	0.46	1.07
0.38	0.25	0.38	0.53	1.14
1.00	0.32	0.45	0.61	1.22
3.00	0.49	0.63	0.78	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
A->CO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0391	0.06

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.27	0.39	0.84
0.38	0.20	0.30	0.42	0.87
1.00	0.24	0.34	0.46	0.92
3.00	0.29	0.41	0.53	0.99

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0897	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.40	0.54	0.70	1.33
0.38	0.43	0.57	0.74	1.36
1.00	0.50	0.64	0.80	1.42
3.00	0.63	0.77	0.93	1.55

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0374	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.49	0.62	1.08
0.38	0.44	0.57	0.70	1.15
1.00	0.50	0.63	0.76	1.22
3.00	0.61	0.74	0.87	1.33

HA1 HA1 3/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0897	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.40	0.56	1.19
0.38	0.34	0.48	0.64	1.27
1.00	0.43	0.57	0.73	1.36
3.00	0.59	0.73	0.90	1.53

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0374	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.46	0.60	1.06
0.38	0.36	0.49	0.63	1.09
1.00	0.43	0.57	0.70	1.17
3.00	0.59	0.74	0.88	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION
B->CO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0865	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.30	0.45	1.05
0.38	0.23	0.36	0.51	1.11
1.00	0.29	0.42	0.57	1.17
3.00	0.39	0.53	0.68	1.29

PATH CONDITION

PATH	CONDITION	FUNCTION
B->CO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0391	0.06

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.32	0.43	0.89
0.38	0.24	0.35	0.46	0.92
1.00	0.30	0.41	0.53	0.98
3.00	0.42	0.54	0.66	1.12

HA1 HA1 4/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0897	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.41	0.57	1.20
0.38	0.30	0.44	0.60	1.23
1.00	0.36	0.50	0.66	1.28
3.00	0.46	0.60	0.76	1.39

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	A	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0374	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.35	0.48	0.93
0.38	0.30	0.42	0.55	1.01
1.00	0.41	0.53	0.65	1.11
3.00	0.53	0.65	0.78	1.23

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	~A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0897	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.33	0.49	1.12
0.38	0.27	0.41	0.57	1.20
1.00	0.34	0.48	0.64	1.27
3.00	0.45	0.59	0.75	1.39

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	~A	FALL

SLEW FACTOR

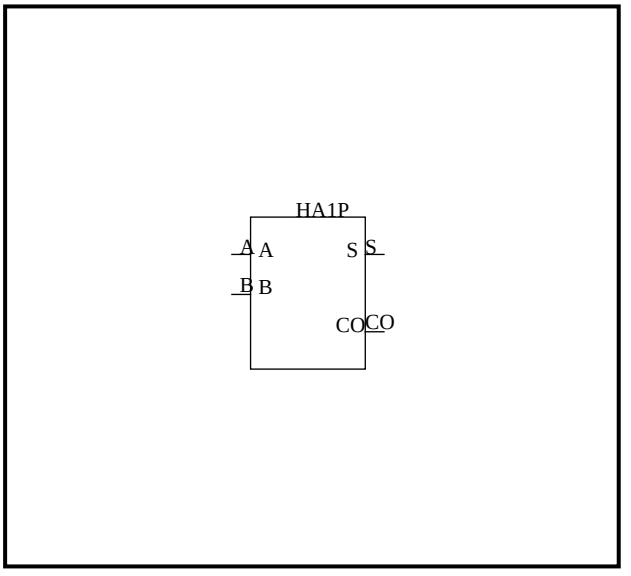
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0374	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.34	0.47	0.92
0.38	0.25	0.37	0.50	0.95
1.00	0.31	0.44	0.56	1.02
3.00	0.45	0.58	0.71	1.17

HA1P	HA1P	1/4

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
HA1P	HALF ADDER	6	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	B	S	CO
L	L	L	L
H	L	H	L
L	H	H	L
H	H	L	H

Verilog-HDL DESCRIPTION

```
HA1P  inst(S,CO,A,B);
```

VHDL DESCRIPTION

```
inst:HA1P
   port   map(S,CO,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	S,CO
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.98
B	3.19

OUTPUT DRIVE (LU)

PIN NAME	S	CO
DRIVE	94.8	99.6

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HA1P | HA1P | 2/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->CO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0442	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.24	0.32	0.63
0.38	0.24	0.32	0.40	0.71
1.00	0.33	0.40	0.49	0.80
3.00	0.52	0.59	0.67	0.99

PATH CONDITION

PATH	CONDITION	FUNCTION
A->CO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0180	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.23	0.29	0.51
0.38	0.20	0.26	0.32	0.54
1.00	0.25	0.31	0.37	0.60
3.00	0.33	0.40	0.47	0.70

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0439	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.49	0.58	0.90
0.38	0.45	0.52	0.61	0.93
1.00	0.51	0.59	0.67	0.99
3.00	0.64	0.72	0.80	1.12

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0200	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.45	0.54	0.80
0.38	0.45	0.53	0.61	0.88
1.00	0.51	0.59	0.68	0.94
3.00	0.62	0.71	0.79	1.06

HA1P HA1P 3/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0439	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.35	0.43	0.75
0.38	0.35	0.43	0.51	0.83
1.00	0.45	0.52	0.61	0.93
3.00	0.63	0.71	0.80	1.12

PATH CONDITION

PATH	CONDITION	FUNCTION
A->S	~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0200	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.42	0.51	0.78
0.38	0.37	0.45	0.54	0.81
1.00	0.44	0.53	0.61	0.88
3.00	0.61	0.71	0.80	1.07

PATH CONDITION

PATH	CONDITION	FUNCTION
B->CO	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0442	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.25	0.33	0.65
0.38	0.23	0.31	0.39	0.70
1.00	0.30	0.37	0.45	0.77
3.00	0.42	0.50	0.58	0.90

PATH CONDITION

PATH	CONDITION	FUNCTION
B->CO	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
CO	0.0180	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.26	0.32	0.55
0.38	0.23	0.29	0.36	0.58
1.00	0.29	0.36	0.42	0.65
3.00	0.42	0.50	0.57	0.80

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HA1P HA1P 4/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0439	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.36	0.45	0.77
0.38	0.32	0.39	0.48	0.80
1.00	0.38	0.45	0.54	0.86
3.00	0.50	0.57	0.66	0.98

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	A	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0200	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.31	0.39	0.66
0.38	0.30	0.38	0.46	0.73
1.00	0.42	0.51	0.59	0.85
3.00	0.55	0.63	0.71	0.97

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	~A	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0439	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.28	0.37	0.69
0.38	0.28	0.36	0.45	0.77
1.00	0.37	0.44	0.53	0.85
3.00	0.53	0.60	0.69	1.01

PATH CONDITION

PATH	CONDITION	FUNCTION
B->S	~A	FALL

SLEW FACTOR

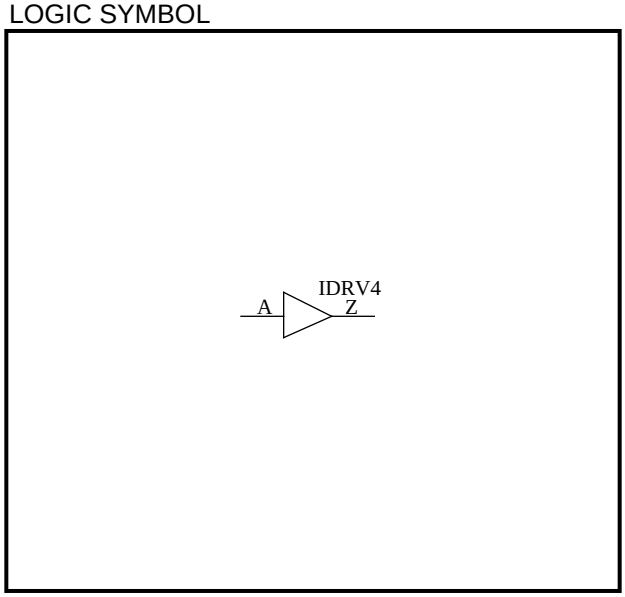
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
S	0.0200	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.30	0.38	0.64
0.38	0.25	0.33	0.41	0.67
1.00	0.31	0.39	0.47	0.73
3.00	0.46	0.54	0.63	0.90

IDRV4	IDRV4	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
IDRV4	INTERNAL CLOCK DRIVER (equal 4mA DRIVER)	0	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	L
H	H

Verilog-HDL DESCRIPTION

```
IDRV4  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:IDRV4
  port  map(Z,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	44123.9

INPUT LOAD (LU)

PIN NAME	LOAD
A	5.55

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	551.5

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IDRV4 IDRV4 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0047	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	266.67	800.00	1600.00	2666.67
0.01	0.80	1.69	3.02	4.79
0.38	0.89	1.77	3.10	4.88
1.00	1.00	1.89	3.22	4.99
3.00	1.25	2.14	3.47	5.24

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.43

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	266.67	800.00	1600.00	2666.67
0.01	1.33	2.88	5.18	8.04
0.38	1.36	2.91	5.22	8.10
1.00	1.43	2.98	5.29	8.20
3.00	1.57	3.11	5.42	8.40

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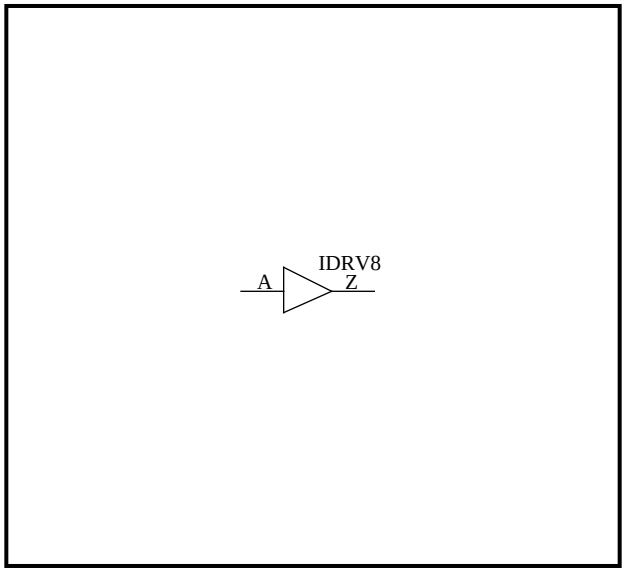
IDRV8	IDRV8	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
IDRV8	INTERNAL CLOCK DRIVER (equal 8mA DRIVER)	0	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	L
H	H

Verilog-HDL DESCRIPTION

```
IDRV8  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:IDRV8
   port   map(Z,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	92825.5

INPUT LOAD (LU)

PIN NAME	LOAD
A	5.55

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	1160.3

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IDRV8 IDRV8 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0024	0.26

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	266.67	800.00	1600.00	2666.67
0.01	0.61	1.07	1.74	2.63
0.38	0.70	1.16	1.83	2.72
1.00	0.84	1.30	1.97	2.85
3.00	1.14	1.60	2.27	3.16

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.31

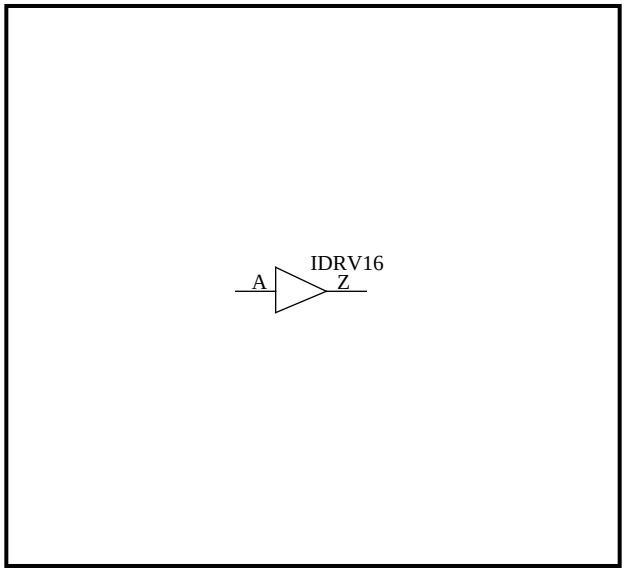
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	266.67	800.00	1600.00	2666.67
0.01	0.99	1.78	2.94	4.49
0.38	1.02	1.81	2.98	4.52
1.00	1.09	1.89	3.05	4.59
3.00	1.28	2.07	3.23	4.77

Rev.1.01.10

IDRV16	IDRV16	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
IDRV16	INTERNAL CLOCK DRIVER (equal 16mA DRIVER)	0	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	L
H	H

Verilog-HDL DESCRIPTION

```
IDRV16  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:IDRV16
  port  map(Z,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	191415.2

INPUT LOAD (LU)

PIN NAME	LOAD
A	9.08

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	2392.7

Rev.1.01.10

IDRV16 IDRV16 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	400.00	1333.33	2666.67	4000.00
0.01	0.51	0.92	1.48	2.04
0.38	0.60	1.01	1.57	2.12
1.00	0.74	1.15	1.71	2.26
3.00	1.04	1.45	2.02	2.57

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0013	0.21

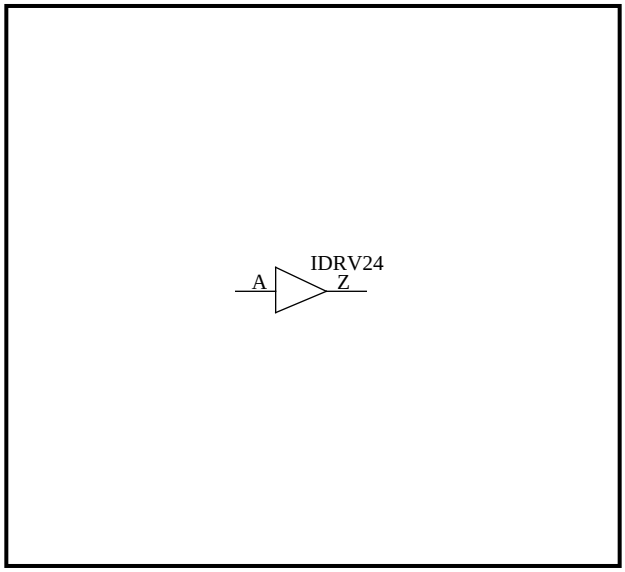
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	400.00	1333.33	2666.67	4000.00
0.01	0.79	1.49	2.46	3.43
0.38	0.82	1.52	2.50	3.47
1.00	0.89	1.59	2.57	3.54
3.00	1.06	1.76	2.73	3.70

Rev.1.01.10

IDRV24	IDRV24	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
IDRV24	INTERNAL CLOCK DRIVER (equal 24mA DRIVER)	0	2	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	L
H	H

Verilog-HDL DESCRIPTION

```
IDRV24  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:IDRV24
  port  map(Z,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	288343.7

INPUT LOAD (LU)

PIN NAME	LOAD
A	17.93

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	3604.3

Rev.1.01.10

IDRV24 IDRV24 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	400.00	1333.33	2666.67	4000.00
0.01	0.46	0.74	1.11	1.49
0.38	0.55	0.83	1.20	1.57
1.00	0.68	0.96	1.34	1.71
3.00	0.98	1.27	1.65	2.02

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

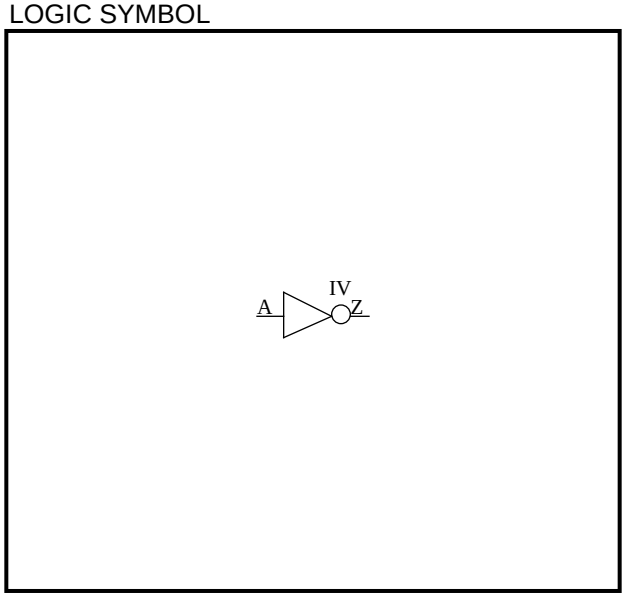
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.25

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	400.00	1333.33	2666.67	4000.00
0.01	0.70	1.18	1.83	2.47
0.38	0.73	1.21	1.86	2.50
1.00	0.80	1.28	1.93	2.57
3.00	0.97	1.45	2.10	2.74

IV	IV	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
IV	INVERTER	1	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	H
H	L

Verilog-HDL DESCRIPTION

```
IV  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:IV
  port  map(Z,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.00

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	45.7

Rev.1.01.10

IV IV 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0842	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.08	0.20	0.35	0.94
0.38	0.10	0.23	0.38	0.97
1.00	0.14	0.28	0.44	1.03
3.00	0.20	0.39	0.59	1.23

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0359	0.09

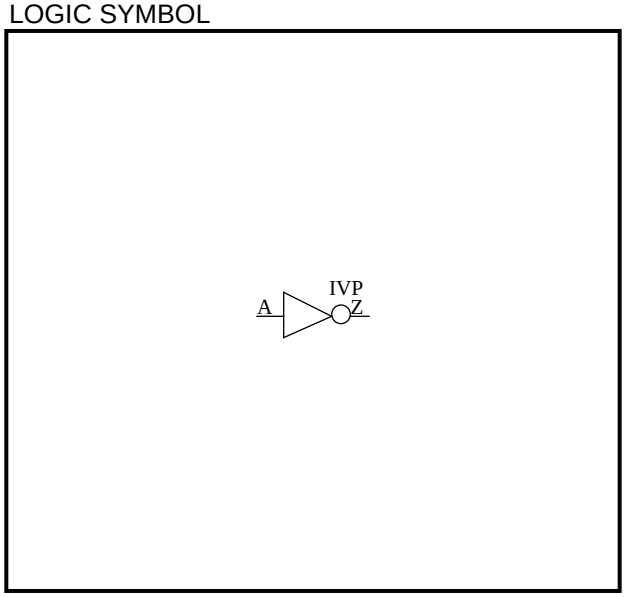
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.06	0.14	0.25	0.68
0.38	0.11	0.22	0.34	0.77
1.00	0.15	0.31	0.45	0.91
3.00	0.20	0.44	0.65	1.27

Rev.1.01.10

IVP	IVP	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
IVP	INVERTER	1	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	H
H	L

Verilog-HDL DESCRIPTION

```
IVP  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:IVP
  port  map(Z,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	2.01

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	76.6

Rev.1.01.10

IVP | IVP | 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0442	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.05	0.12	0.20	0.51
0.38	0.07	0.14	0.23	0.54
1.00	0.09	0.18	0.27	0.60
3.00	0.12	0.24	0.36	0.75

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

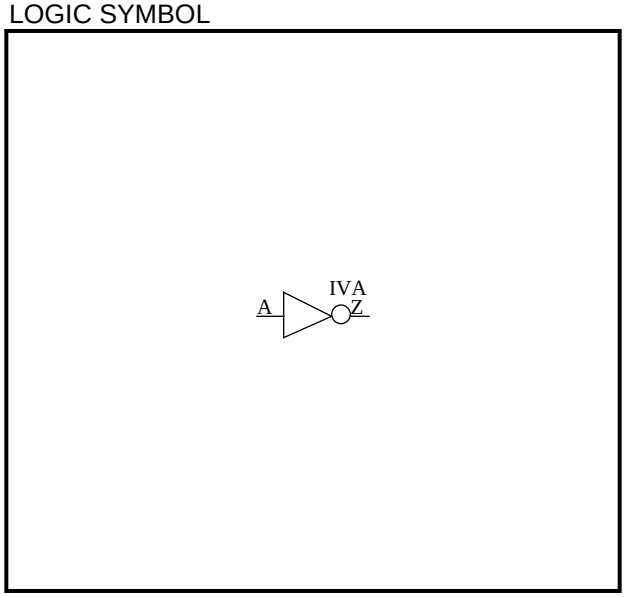
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0225	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.04	0.10	0.16	0.43
0.38	0.08	0.16	0.24	0.52
1.00	0.11	0.22	0.32	0.64
3.00	0.13	0.30	0.45	0.90

IVA	IVA	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
IVA	INVERTER with PARALLEL Pch TRANSISTORS	1	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	H
H	L

Verilog-HDL DESCRIPTION

```
IVA  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:IVA
  port  map(Z,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.54

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	61.0

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IVA | IVA | 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0540	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.06	0.13	0.22	0.59
0.38	0.06	0.15	0.25	0.61
1.00	0.06	0.17	0.28	0.67
3.00	-0.00	0.15	0.30	0.77

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

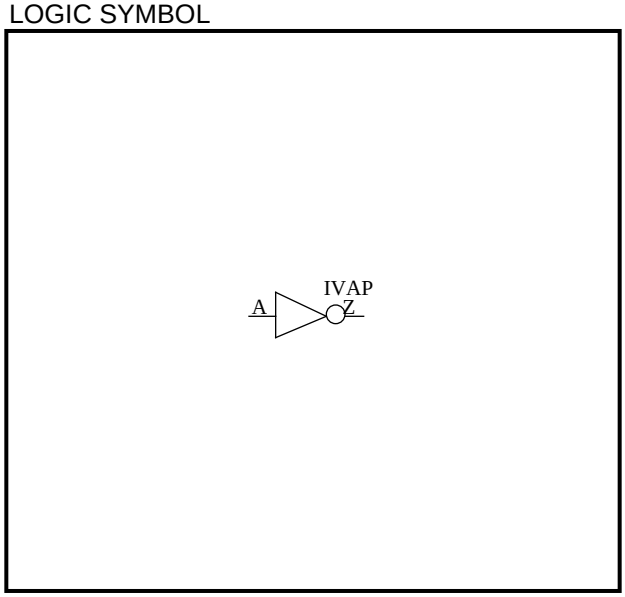
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0332	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.05	0.14	0.24	0.64
0.38	0.12	0.22	0.32	0.73
1.00	0.17	0.31	0.45	0.87
3.00	0.31	0.51	0.70	1.26

IVAP	IVAP	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
IVAP	INVERTER with PARALLEL Pch TRANSISTORS	2	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	H
H	L

Verilog-HDL DESCRIPTION

```
IVAP  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:IVAP
  port  map(Z,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	3.02

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	105.1

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IVAP | IVAP | 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0206	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.03	0.07	0.11	0.26
0.38	0.03	0.08	0.12	0.29
1.00	-0.00	0.06	0.13	0.32
3.00	-0.13	-0.04	0.05	0.32

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

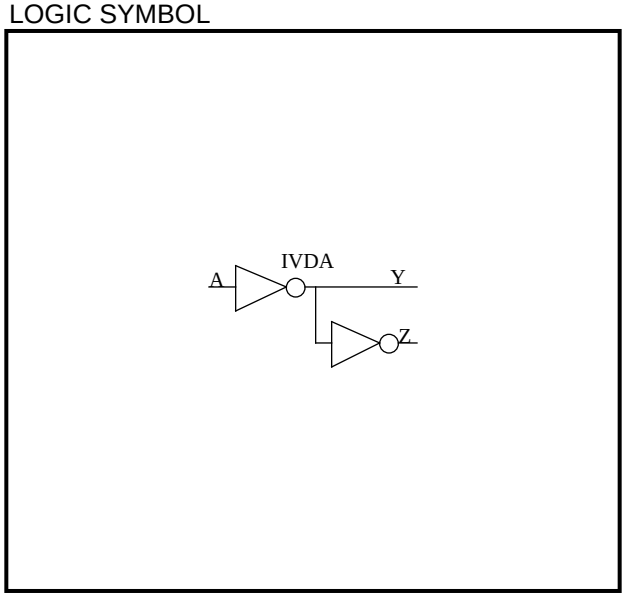
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0228	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.05	0.11	0.18	0.44
0.38	0.11	0.18	0.25	0.53
1.00	0.17	0.26	0.35	0.66
3.00	0.33	0.47	0.59	0.98

IVDA	IVDA	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
IVDA	INVERTER into INVERTER	1	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT	
A	Y	Z
L	H	L
H	L	H

Verilog-HDL DESCRIPTION

```
IVDA  inst(Y,Z,A);
```

VHDL DESCRIPTION

```
inst:IVDA
   port   map(Y,Z,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Y,Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	0.99

OUTPUT DRIVE (LU)

PIN NAME	Y	Z
DRIVE	42.8	39.7

Rev.1.01.10

IVDA | IVDA | 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Y	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Y	0.0869	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.24	0.39	1.00
0.38	0.14	0.27	0.42	1.02
1.00	0.18	0.32	0.48	1.09
3.00	0.25	0.44	0.63	1.29

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Y	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Y	0.0395	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.08	0.18	0.30	0.76
0.38	0.15	0.26	0.38	0.85
1.00	0.20	0.35	0.50	0.99
3.00	0.29	0.52	0.73	1.37

PATH CONDITION

PATH	CONDITION	FUNCTION
Y->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0983	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.39	1.06
0.38	0.12	0.26	0.43	1.10
1.00	0.16	0.32	0.50	1.17
3.00	0.25	0.46	0.67	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
Y->Z	---	FALL

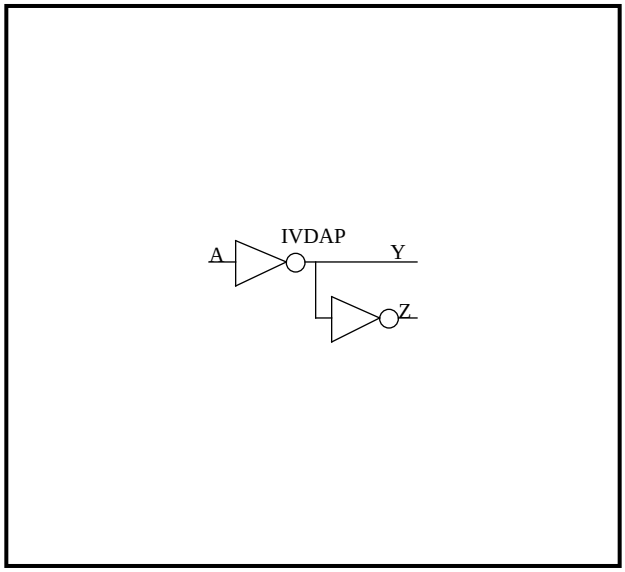
SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0385	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.06	0.14	0.25	0.70
0.38	0.11	0.22	0.34	0.78
1.00	0.14	0.30	0.45	0.92
3.00	0.16	0.41	0.63	1.27

IVDAP				IVDAP	1/2
CELL NAME	FUNCTION	CELL COUNT		CONDITION	
IVDAP	INVERTER into INVERTER	GATE	I/O	VDD=3.3V, Ta=25°C, Typ.	
		2	0		

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT	
A	Y	Z
L	H	L
H	L	H

Verilog-HDL DESCRIPTION

```
IVDAP  inst(Y,Z,A);
```

VHDL DESCRIPTION

```
inst:IVDAP
  port  map(Y,Z,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Y,Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	2.06

OUTPUT DRIVE (LU)

PIN NAME	Y	Z
DRIVE	77.4	67.1

Rev.1.01.10

IVDAP | IVDAP | 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Y	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Y	0.0444	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.15	0.23	0.54
0.38	0.11	0.18	0.26	0.57
1.00	0.14	0.22	0.31	0.63
3.00	0.19	0.30	0.41	0.78

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Y	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Y	0.0231	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.07	0.13	0.20	0.47
0.38	0.13	0.20	0.27	0.55
1.00	0.17	0.27	0.36	0.68
3.00	0.25	0.38	0.52	0.94

PATH CONDITION

PATH	CONDITION	FUNCTION
Y->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0576	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.08	0.17	0.27	0.66
0.38	0.11	0.20	0.30	0.69
1.00	0.14	0.24	0.35	0.76
3.00	0.23	0.36	0.49	0.94

PATH CONDITION

PATH	CONDITION	FUNCTION
Y->Z	---	FALL

SLEW FACTOR

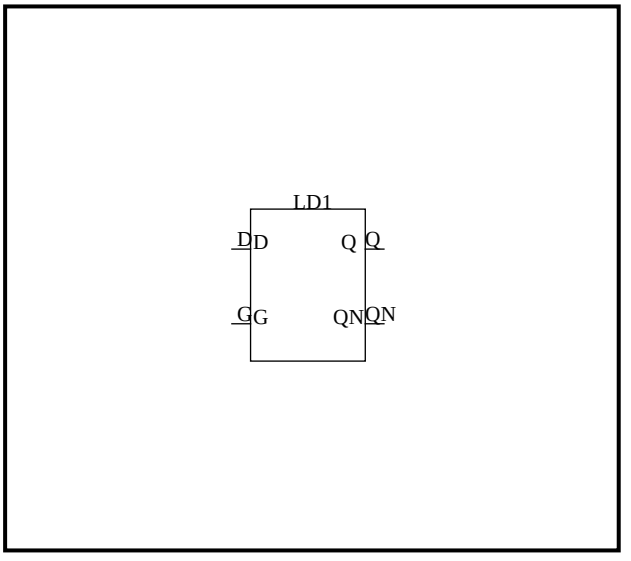
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0204	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.05	0.10	0.16	0.40
0.38	0.10	0.17	0.24	0.50
1.00	0.12	0.22	0.32	0.62
3.00	0.12	0.28	0.44	0.87

LD1	LD1	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
LD1	D-TYPE TRANSPARENT LATCH (HIGH ENABLE)	5	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
G	D	Q	QN
H	L	L	H
H	H	H	L
L	X	HOLD	

Verilog-HDL DESCRIPTION

```
LD1  inst(Q,QN,D,G);
```

VHDL DESCRIPTION

```
inst:LD1
   port   map(Q,QN,D,G);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q	QN
ELECTRO MIGRATION DRIVE	6880.0	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D,G	0.99

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	42.2	50.2

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LD1 LD1 2/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0982	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.47	0.65	1.35
0.38	0.37	0.54	0.72	1.42
1.00	0.45	0.62	0.80	1.50
3.00	0.61	0.77	0.96	1.66

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0417	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.49	0.64	1.17
0.38	0.37	0.52	0.67	1.20
1.00	0.44	0.59	0.74	1.27
3.00	0.59	0.75	0.91	1.44

PATH CONDITION

PATH	CONDITION	FUNCTION
D->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0860	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.61	0.77	1.38
0.38	0.51	0.64	0.80	1.41
1.00	0.58	0.71	0.87	1.48
3.00	0.74	0.88	1.03	1.64

PATH CONDITION

PATH	CONDITION	FUNCTION
D->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0343	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.56	0.68	1.10
0.38	0.52	0.63	0.75	1.17
1.00	0.60	0.71	0.83	1.25
3.00	0.76	0.87	0.99	1.42

LD1 LD1 3/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0982	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.58	0.76	1.46
0.38	0.48	0.65	0.84	1.54
1.00	0.55	0.72	0.90	1.60
3.00	0.67	0.84	1.03	1.73

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0417	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.52	0.67	1.20
0.38	0.45	0.60	0.75	1.27
1.00	0.52	0.67	0.82	1.34
3.00	0.65	0.80	0.96	1.48

PATH CONDITION

PATH	CONDITION	FUNCTION
G->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0860	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.65	0.80	1.41
0.38	0.59	0.72	0.88	1.49
1.00	0.66	0.79	0.95	1.56
3.00	0.79	0.93	1.08	1.69

PATH CONDITION

PATH	CONDITION	FUNCTION
G->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0343	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.67	0.78	1.20
0.38	0.63	0.74	0.86	1.28
1.00	0.70	0.81	0.92	1.35
3.00	0.82	0.93	1.05	1.47

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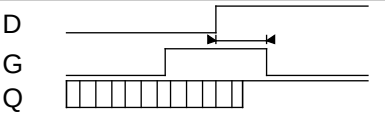
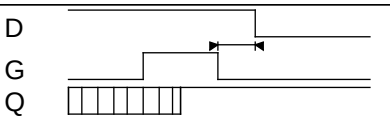
LD1	LD1	4/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	G	---

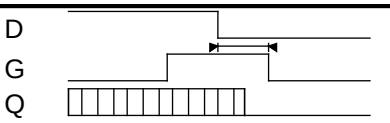
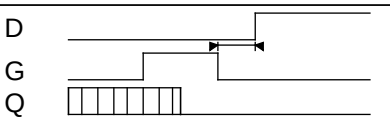
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.340	0.308	0.255	0.083
0.38	0.381	0.350	0.297	0.126
1.00	0.450	0.419	0.367	0.198
3.00	0.672	0.642	0.592	0.428

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.277	0.291	0.315	0.391
0.38	0.245	0.260	0.284	0.362
1.00	0.192	0.207	0.232	0.314
3.00	0.018	0.036	0.064	0.157

TIMING CONDITION

DATA	CLOCK	CONDITION
D	G	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.439	0.426	0.404	0.333
0.38	0.472	0.458	0.436	0.363
1.00	0.526	0.512	0.489	0.413
3.00	0.702	0.687	0.660	0.575

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.380	0.409	0.458	0.615
0.38	0.340	0.369	0.418	0.576
1.00	0.272	0.301	0.351	0.510
3.00	0.053	0.083	0.134	0.298

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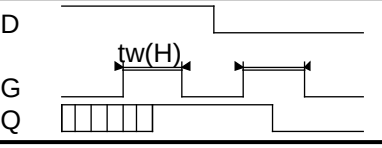
LD1	LD1	5/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
G	---

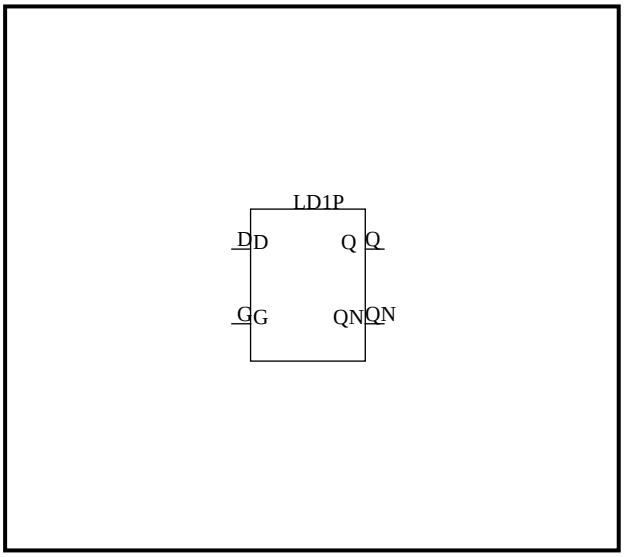
ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

LD1P	LD1P	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
LD1P	D-TYPE TRANSPARENT LATCH (HIGH ENABLE)	6	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
G	D	Q	QN
H	L	L	H
H	H	H	L
L	X	HOLD	

Verilog-HDL DESCRIPTION

```
LD1P  inst(Q,QN,D,G);
```

VHDL DESCRIPTION

```
inst:LD1P
   port   map(Q,QN,D,G);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q	QN
ELECTRO MIGRATION DRIVE	6880.0	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D,G	0.99

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	75.1	97.9

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LD1P | LD1P | 2/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0543	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.38	0.49	0.87
0.38	0.36	0.45	0.56	0.94
1.00	0.45	0.54	0.64	1.03
3.00	0.62	0.71	0.81	1.20

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0255	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.42	0.52	0.85
0.38	0.35	0.45	0.55	0.88
1.00	0.42	0.52	0.62	0.95
3.00	0.59	0.69	0.79	1.13

PATH CONDITION

PATH	CONDITION	FUNCTION
D->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0441	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.53	0.60	0.69	1.00
0.38	0.56	0.64	0.72	1.03
1.00	0.64	0.71	0.79	1.11
3.00	0.82	0.89	0.97	1.28

PATH CONDITION

PATH	CONDITION	FUNCTION
D->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0178	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.50	0.58	0.65	0.89
0.38	0.57	0.65	0.72	0.96
1.00	0.66	0.74	0.81	1.05
3.00	0.84	0.92	0.99	1.23

LD1P | LD1P | 3/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0543	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.40	0.49	0.59	0.98
0.38	0.47	0.56	0.67	1.05
1.00	0.54	0.63	0.73	1.12
3.00	0.66	0.75	0.86	1.24

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0255	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.45	0.55	0.88
0.38	0.43	0.53	0.63	0.95
1.00	0.50	0.60	0.70	1.02
3.00	0.63	0.73	0.83	1.16

PATH CONDITION

PATH	CONDITION	FUNCTION
G->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0441	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.56	0.63	0.72	1.03
0.38	0.64	0.71	0.79	1.11
1.00	0.71	0.78	0.86	1.18
3.00	0.84	0.91	1.00	1.31

PATH CONDITION

PATH	CONDITION	FUNCTION
G->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0178	0.12

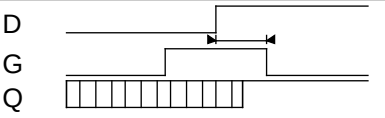
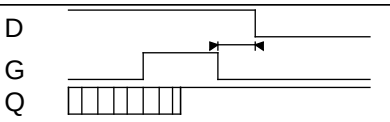
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.61	0.68	0.75	0.99
0.38	0.68	0.76	0.83	1.07
1.00	0.75	0.82	0.90	1.13
3.00	0.87	0.95	1.02	1.26

LD1P	LD1P	4/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	G	---

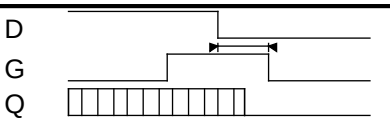
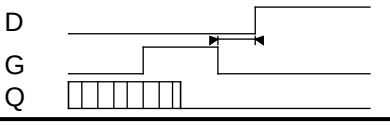
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.514	0.472	0.401	0.172
0.38	0.565	0.523	0.453	0.225
1.00	0.650	0.609	0.539	0.315
3.00	0.925	0.885	0.819	0.605

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.178	0.201	0.241	0.368
0.38	0.136	0.160	0.200	0.329
1.00	0.067	0.091	0.132	0.263
3.00	-0.158	-0.132	-0.088	0.052

TIMING CONDITION

DATA	CLOCK	CONDITION
D	G	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.690	0.667	0.628	0.503
0.38	0.733	0.710	0.671	0.545
1.00	0.805	0.781	0.742	0.614
3.00	1.036	1.012	0.971	0.838

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.369	0.406	0.470	0.673
0.38	0.318	0.356	0.419	0.623
1.00	0.233	0.271	0.335	0.539
3.00	-0.041	-0.002	0.062	0.268

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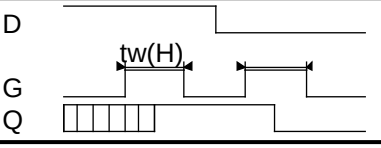
LD1P	LD1P	5/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
G	---

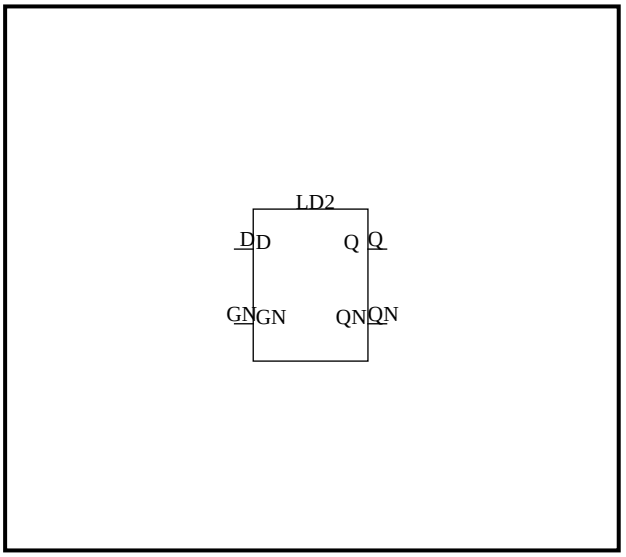
ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.990

LD2	LD2	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
LD2	D-TYPE TRANSPARENT LATCH (LOW ENABLE)	5	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
GN	D	Q	QN
L	L	L	H
L	H	H	L
H	X	HOLD	

Verilog-HDL DESCRIPTION

```
LD2  inst(Q,QN,D,GN);
```

VHDL DESCRIPTION

```
inst:LD2
   port   map(Q,QN,D,GN);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D,GN	0.99

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	47.7	48.1

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LD2 LD2 2/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0855	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.42	0.58	1.19
0.38	0.35	0.49	0.65	1.26
1.00	0.43	0.57	0.73	1.34
3.00	0.59	0.73	0.89	1.50

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0398	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.47	0.62	1.12
0.38	0.35	0.50	0.65	1.15
1.00	0.42	0.57	0.72	1.23
3.00	0.58	0.73	0.89	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
D->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0840	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.59	0.74	1.32
0.38	0.49	0.62	0.77	1.35
1.00	0.56	0.69	0.84	1.42
3.00	0.73	0.85	1.00	1.59

PATH CONDITION

PATH	CONDITION	FUNCTION
D->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0417	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.57	0.70	1.20
0.38	0.52	0.64	0.77	1.27
1.00	0.60	0.72	0.86	1.35
3.00	0.76	0.89	1.02	1.52

LD2 LD2 3/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0855	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.55	0.71	1.32
0.38	0.44	0.58	0.74	1.35
1.00	0.51	0.65	0.81	1.42
3.00	0.65	0.79	0.95	1.56

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0398	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.57	0.71	1.22
0.38	0.45	0.60	0.74	1.25
1.00	0.52	0.67	0.81	1.32
3.00	0.66	0.80	0.95	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0840	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.56	0.68	0.83	1.42
0.38	0.59	0.72	0.87	1.45
1.00	0.66	0.78	0.93	1.52
3.00	0.80	0.92	1.07	1.66

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0417	0.11

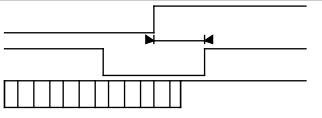
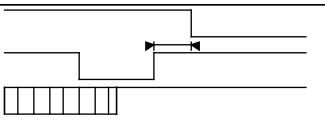
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.58	0.70	0.83	1.33
0.38	0.61	0.73	0.87	1.36
1.00	0.68	0.80	0.93	1.43
3.00	0.82	0.94	1.07	1.57

LD2	LD2	4/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	GN	---

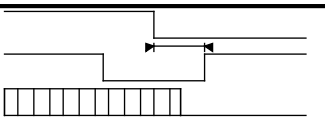
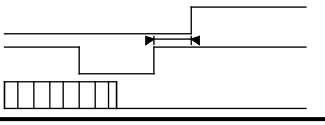
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.413	0.401	0.382	0.319
0.38	0.453	0.441	0.420	0.354
1.00	0.521	0.508	0.486	0.414
3.00	0.741	0.725	0.697	0.606

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.254	0.283	0.330	0.484
0.38	0.221	0.249	0.296	0.448
1.00	0.165	0.193	0.239	0.389
3.00	-0.015	0.011	0.055	0.196

TIMING CONDITION

DATA	CLOCK	CONDITION
D	GN	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.429	0.402	0.356	0.207
0.38	0.463	0.436	0.391	0.243
1.00	0.521	0.494	0.449	0.304
3.00	0.706	0.680	0.638	0.501

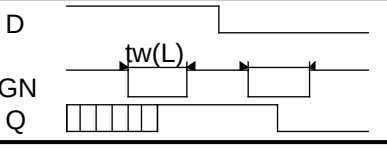
HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.290	0.299	0.313	0.360
0.38	0.251	0.261	0.276	0.326
1.00	0.187	0.197	0.214	0.269
3.00	-0.020	-0.007	0.014	0.085

LD2	LD2	5/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
GN	---

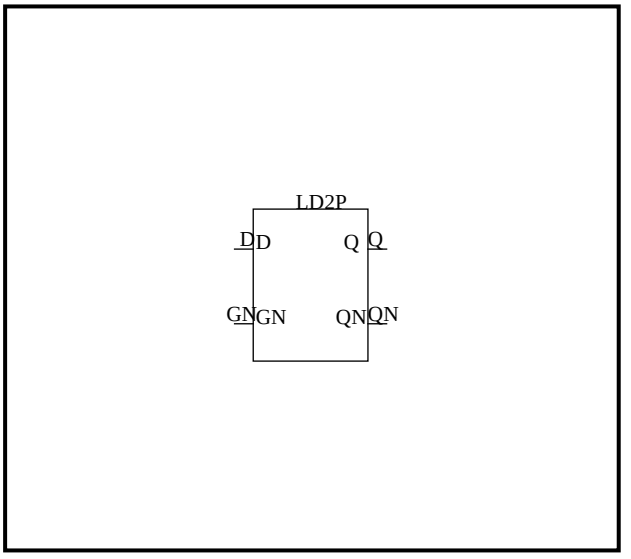
ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.730

LD2P	LD2P	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
LD2P	D-TYPE TRANSPARENT LATCH (LOW ENABLE)	6	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
GN	D	Q	QN
L	L	L	H
L	H	H	L
H	X	HOLD	

Verilog-HDL DESCRIPTION

```
LD2P  inst(Q,QN,D,GN);
```

VHDL DESCRIPTION

```
inst:LD2P
   port   map(Q,QN,D,GN);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q	QN
ELECTRO MIGRATION DRIVE	12880.0	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D,GN	0.99

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	91.8	90.0

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LD2P | LD2P | 2/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0440	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.37	0.46	0.79
0.38	0.36	0.44	0.53	0.86
1.00	0.45	0.53	0.62	0.94
3.00	0.62	0.70	0.79	1.12

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0215	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.42	0.51	0.80
0.38	0.36	0.45	0.54	0.83
1.00	0.43	0.52	0.61	0.90
3.00	0.59	0.69	0.78	1.08

PATH CONDITION

PATH	CONDITION	FUNCTION
D->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0440	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.54	0.61	0.70	1.01
0.38	0.57	0.64	0.73	1.04
1.00	0.64	0.72	0.80	1.12
3.00	0.82	0.90	0.98	1.29

PATH CONDITION

PATH	CONDITION	FUNCTION
D->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0233	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.61	0.69	0.98
0.38	0.59	0.68	0.76	1.06
1.00	0.68	0.77	0.85	1.14
3.00	0.87	0.95	1.03	1.33

LD2P | LD2P | 3/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0440	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.50	0.59	0.92
0.38	0.46	0.54	0.63	0.95
1.00	0.52	0.60	0.69	1.02
3.00	0.67	0.75	0.84	1.16

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0215	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.50	0.60	0.89
0.38	0.44	0.54	0.63	0.92
1.00	0.51	0.60	0.70	0.99
3.00	0.65	0.74	0.84	1.13

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0440	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.63	0.70	0.78	1.10
0.38	0.66	0.73	0.82	1.13
1.00	0.73	0.80	0.88	1.20
3.00	0.87	0.94	1.02	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0233	0.12

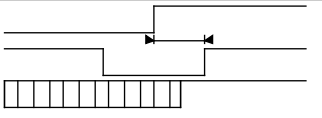
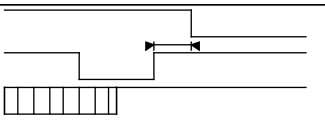
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.66	0.74	0.82	1.12
0.38	0.69	0.77	0.86	1.15
1.00	0.76	0.84	0.92	1.22
3.00	0.90	0.98	1.07	1.36

LD2P	LD2P	4/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	GN	---

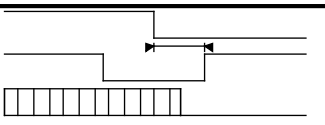
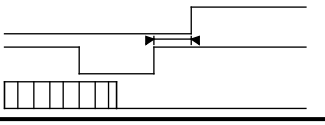
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.653	0.633	0.601	0.496
0.38	0.704	0.684	0.650	0.543
1.00	0.789	0.768	0.733	0.620
3.00	1.063	1.039	0.999	0.870

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.068	0.099	0.152	0.320
0.38	0.025	0.056	0.108	0.276
1.00	-0.047	-0.016	0.036	0.201
3.00	-0.278	-0.249	-0.199	-0.038

TIMING CONDITION

DATA	CLOCK	CONDITION
D	GN	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.718	0.690	0.644	0.495
0.38	0.762	0.734	0.688	0.540
1.00	0.836	0.808	0.762	0.614
3.00	1.075	1.047	1.001	0.853

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.171	0.182	0.199	0.253
0.38	0.124	0.134	0.153	0.211
1.00	0.044	0.056	0.075	0.139
3.00	-0.214	-0.199	-0.173	-0.091

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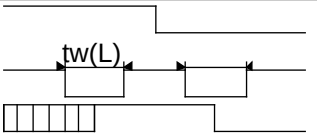
LD2P	LD2P	5/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
GN	---

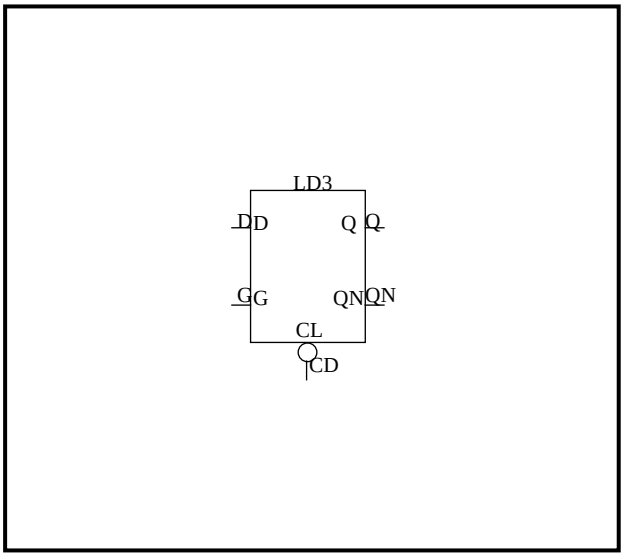
ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	1.050

LD3	LD3	1/7

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
LD3	D-TYPE TRANSPARENT LATCH with CLEAR (HIGH ENABLE)	5	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT	
CD	G	D	Q	QN
L	X*	X	L	H
H	H	L	L	H
H	H	H	H	L
H	L	X	HOLD	

*:Consider the Hold Time of CLEAR

Verilog-HDL DESCRIPTION

```
LD3  inst(Q,QN,D,G,CD);
```

VHDL DESCRIPTION

```
inst:LD3
   port   map(Q,QN,D,G,CD);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D	1.01
G	0.99
CD	0.98

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	47.6	48.7

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LD3 LD3 2/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0366	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.50	0.64	1.10
0.38	0.38	0.52	0.66	1.12
1.00	0.45	0.59	0.73	1.19
3.00	0.62	0.77	0.91	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0885	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.62	0.78	1.39
0.38	0.52	0.65	0.80	1.41
1.00	0.59	0.72	0.87	1.48
3.00	0.77	0.90	1.06	1.67

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0875	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.39	0.54	0.72	1.38
0.38	0.46	0.62	0.80	1.46
1.00	0.58	0.74	0.92	1.58
3.00	0.86	1.02	1.20	1.86

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0366	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.44	0.58	1.05
0.38	0.34	0.48	0.62	1.08
1.00	0.40	0.54	0.67	1.14
3.00	0.49	0.63	0.78	1.26

LD3 LD3 3/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0885	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.58	0.73	1.35
0.38	0.48	0.61	0.77	1.38
1.00	0.54	0.67	0.83	1.44
3.00	0.64	0.78	0.93	1.54

PATH CONDITION

PATH	CONDITION	FUNCTION
D->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0357	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.54	0.65	0.77	1.21
0.38	0.61	0.73	0.85	1.29
1.00	0.74	0.85	0.97	1.41
3.00	1.02	1.14	1.26	1.70

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0875	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.44	0.60	0.77	1.43
0.38	0.51	0.67	0.85	1.51
1.00	0.58	0.74	0.91	1.58
3.00	0.70	0.86	1.03	1.70

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0366	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.48	0.62	1.08
0.38	0.42	0.56	0.69	1.16
1.00	0.49	0.63	0.76	1.23
3.00	0.62	0.76	0.90	1.36

LD3 LD3 4/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
G->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0885	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.62	0.77	1.39
0.38	0.56	0.69	0.85	1.46
1.00	0.63	0.76	0.92	1.53
3.00	0.76	0.90	1.05	1.66

PATH CONDITION

PATH	CONDITION	FUNCTION
G->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0357	0.12

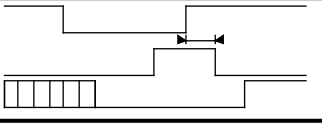
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.59	0.70	0.83	1.26
0.38	0.66	0.78	0.90	1.34
1.00	0.73	0.85	0.97	1.40
3.00	0.85	0.97	1.09	1.52

LD3	LD3	5/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

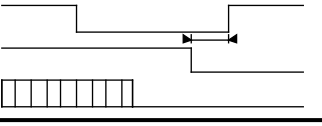
DATA	CLOCK	CONDITION
CD	G	D

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.498	0.466	0.413	0.242
0.38	0.533	0.501	0.449	0.280
1.00	0.591	0.560	0.509	0.343
3.00	0.778	0.749	0.701	0.545

TIMING CONDITION

DATA	CLOCK	CONDITION
CD	G	D

ITEM	CLOCK	DATA	WAVE_FORM
HOLD	NEGEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.251	0.282	0.332	0.496
0.38	0.219	0.249	0.299	0.462
1.00	0.164	0.194	0.244	0.405
3.00	-0.012	0.017	0.066	0.222

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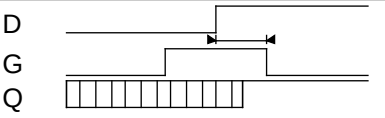
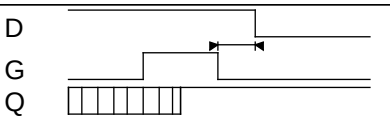
LD3	LD3	6/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	G	CD

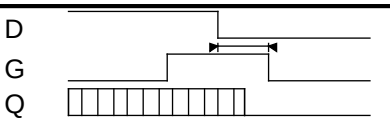
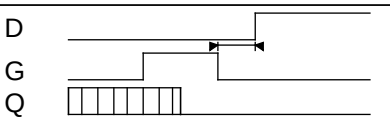
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.481	0.449	0.396	0.224
0.38	0.542	0.511	0.458	0.288
1.00	0.645	0.615	0.563	0.396
3.00	0.978	0.949	0.901	0.745

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.293	0.309	0.334	0.416
0.38	0.272	0.287	0.313	0.397
1.00	0.235	0.251	0.278	0.365
3.00	0.118	0.136	0.166	0.263

TIMING CONDITION

DATA	CLOCK	CONDITION
D	G	CD

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.409	0.396	0.373	0.300
0.38	0.433	0.419	0.395	0.319
1.00	0.472	0.457	0.432	0.352
3.00	0.597	0.580	0.551	0.457

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.269	0.300	0.352	0.519
0.38	0.208	0.239	0.290	0.456
1.00	0.106	0.137	0.187	0.351
3.00	-0.222	-0.194	-0.145	0.011

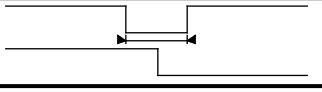
Rev.1.01.10

LD3	LD3	7/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

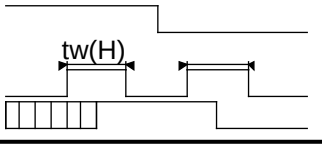
CLOCK	CONDITION
CD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.760

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
G	CD

ITEM	WAVE_FORM
POSLIMIT	

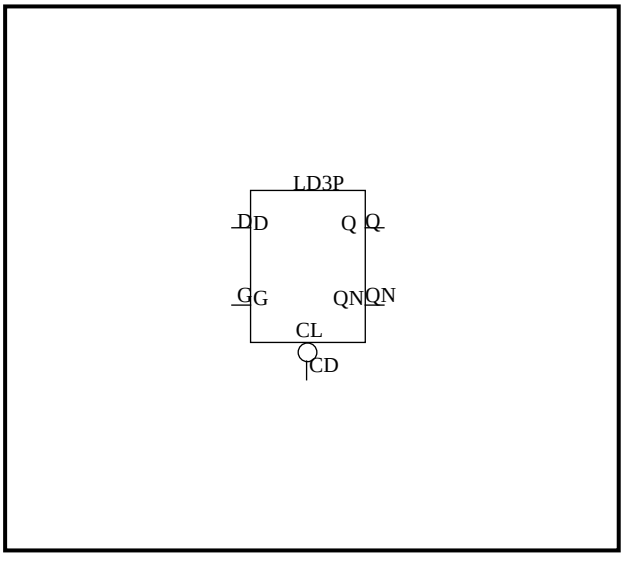
POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

Rev.1.01.10

LD3P	LD3P	1/7

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
LD3P	D-TYPE TRANSPARENT LATCH with CLEAR (HIGH ENABLE)	6	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT	
CD	G	D	Q	QN
L	X*	X	L	H
H	H	L	L	H
H	H	H	H	L
H	L	X	HOLD	

*:Consider the Hold Time of CLEAR

Verilog-HDL DESCRIPTION

```
LD3P  inst(Q,QN,D,G,CD);
```

VHDL DESCRIPTION

```
inst:LD3P
   port   map(Q,QN,D,G,CD);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q	QN
ELECTRO MIGRATION DRIVE	6880.0	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D	1.01
G	0.99
CD	0.98

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	80.3	97.4

Rev.1.01.10

LD3P | LD3P | 2/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0227	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.46	0.55	0.85
0.38	0.38	0.48	0.57	0.87
1.00	0.45	0.55	0.64	0.94
3.00	0.63	0.73	0.83	1.13

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0441	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.56	0.63	0.71	1.02
0.38	0.58	0.65	0.73	1.04
1.00	0.65	0.72	0.80	1.11
3.00	0.85	0.92	1.00	1.31

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0516	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.50	0.60	0.98
0.38	0.49	0.58	0.68	1.06
1.00	0.61	0.70	0.80	1.18
3.00	0.91	1.00	1.10	1.48

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0227	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.40	0.50	0.80
0.38	0.35	0.44	0.53	0.83
1.00	0.41	0.50	0.59	0.89
3.00	0.51	0.61	0.70	1.01

LD3P | LD3P | 3/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0441	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.58	0.66	0.98
0.38	0.55	0.62	0.70	1.01
1.00	0.61	0.68	0.76	1.07
3.00	0.73	0.80	0.88	1.20

PATH CONDITION

PATH	CONDITION	FUNCTION
D->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0180	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.63	0.70	0.78	1.02
0.38	0.71	0.78	0.86	1.10
1.00	0.84	0.91	0.98	1.23
3.00	1.14	1.21	1.29	1.53

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0516	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.55	0.65	1.03
0.38	0.53	0.62	0.73	1.11
1.00	0.60	0.69	0.79	1.17
3.00	0.72	0.81	0.91	1.29

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0227	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.44	0.53	0.83
0.38	0.42	0.51	0.61	0.90
1.00	0.49	0.58	0.68	0.98
3.00	0.62	0.71	0.81	1.11

LD3P | LD3P | 4/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
G->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0441	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.54	0.62	0.70	1.01
0.38	0.62	0.69	0.77	1.09
1.00	0.69	0.76	0.84	1.16
3.00	0.82	0.89	0.98	1.29

PATH CONDITION

PATH	CONDITION	FUNCTION
G->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0180	0.13

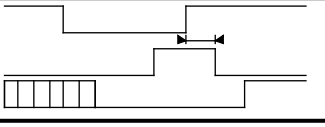
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.68	0.75	0.83	1.07
0.38	0.76	0.83	0.90	1.14
1.00	0.82	0.90	0.97	1.21
3.00	0.94	1.02	1.09	1.33

LD3P	LD3P	5/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

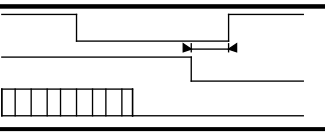
DATA	CLOCK	CONDITION
CD	G	D

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.809	0.771	0.708	0.504
0.38	0.847	0.810	0.747	0.544
1.00	0.911	0.874	0.811	0.609
3.00	1.118	1.081	1.020	0.821

TIMING CONDITION

DATA	CLOCK	CONDITION
CD	G	D

ITEM	CLOCK	DATA	WAVE_FORM
HOLD	NEGEDGE	LOW	

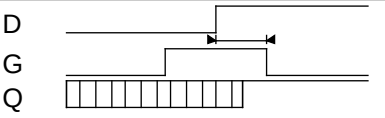
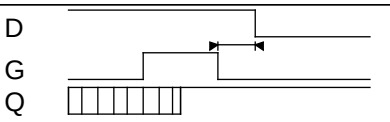
HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.136	0.176	0.244	0.462
0.38	0.099	0.139	0.206	0.422
1.00	0.037	0.076	0.142	0.355
3.00	-0.163	-0.126	-0.063	0.140

LD3P | LD3P | 6/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	G	CD

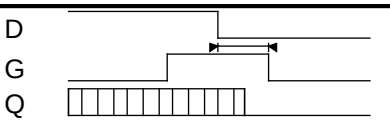
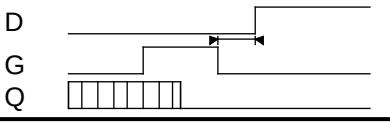
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.780	0.742	0.679	0.475
0.38	0.849	0.812	0.749	0.545
1.00	0.965	0.928	0.865	0.663
3.00	1.341	1.304	1.242	1.044

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.189	0.214	0.255	0.387
0.38	0.153	0.177	0.219	0.353
1.00	0.092	0.117	0.159	0.295
3.00	-0.105	-0.079	-0.034	0.110

TIMING CONDITION

DATA	CLOCK	CONDITION
D	G	CD

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.650	0.627	0.588	0.463
0.38	0.688	0.665	0.625	0.499
1.00	0.752	0.728	0.689	0.560
3.00	0.960	0.935	0.892	0.756

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.169	0.210	0.278	0.496
0.38	0.101	0.141	0.208	0.425
1.00	-0.015	0.025	0.091	0.305
3.00	-0.386	-0.349	-0.286	-0.083

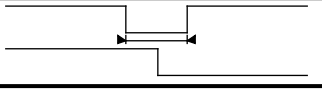
Rev.1.01.10

LD3P	LD3P	7/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

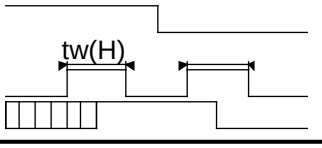
CLOCK	CONDITION
CD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	1.090

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
G	CD

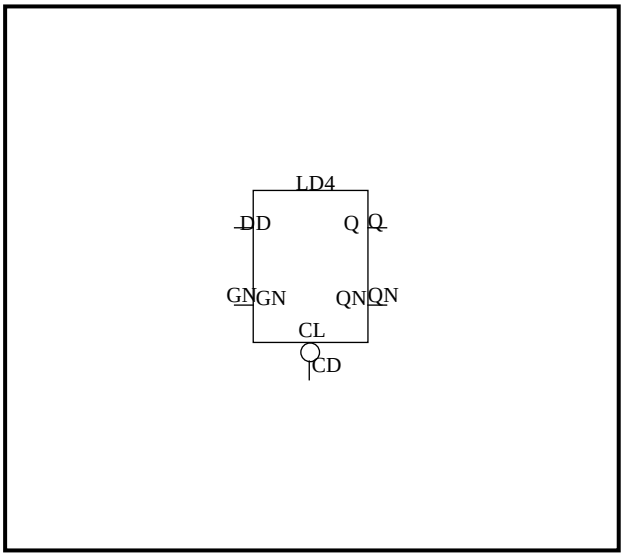
ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	1.160

LD4	LD4	1/7

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
LD4	D-TYPE TRANSPARENT LATCH with CLEAR (LOW ENABLE)	5	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT	
CD	GN	D	Q	QN
L	X*	X	L	H
H	L	L	L	H
H	L	H	H	L
H	H	X	HOLD	

*:Consider the Hold Time of CLEAR

Verilog-HDL DESCRIPTION

```
LD4  inst(Q,QN,D,GN,CD);
```

VHDL DESCRIPTION

```
inst:LD4
   port   map(Q,QN,D,GN,CD);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D	1.01
GN	0.99
CD	0.98

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	47.7	48.7

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LD4 LD4 2/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0366	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.50	0.64	1.10
0.38	0.38	0.52	0.66	1.12
1.00	0.45	0.59	0.73	1.19
3.00	0.62	0.77	0.91	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0885	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.62	0.78	1.39
0.38	0.52	0.65	0.80	1.41
1.00	0.58	0.71	0.87	1.48
3.00	0.77	0.90	1.05	1.66

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0875	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.39	0.54	0.72	1.38
0.38	0.47	0.62	0.80	1.46
1.00	0.58	0.74	0.92	1.58
3.00	0.86	1.02	1.20	1.86

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0366	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.44	0.58	1.04
0.38	0.34	0.48	0.61	1.08
1.00	0.40	0.53	0.67	1.14
3.00	0.48	0.63	0.78	1.25

LD4 LD4 3/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0885	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.58	0.73	1.35
0.38	0.48	0.61	0.77	1.38
1.00	0.54	0.67	0.83	1.44
3.00	0.64	0.77	0.93	1.54

PATH CONDITION

PATH	CONDITION	FUNCTION
D->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0356	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.54	0.65	0.77	1.21
0.38	0.62	0.73	0.85	1.29
1.00	0.74	0.85	0.97	1.41
3.00	1.02	1.14	1.26	1.70

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0875	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.61	0.79	1.45
0.38	0.49	0.64	0.82	1.48
1.00	0.55	0.71	0.89	1.55
3.00	0.68	0.84	1.01	1.68

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0366	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.39	0.53	0.66	1.13
0.38	0.42	0.56	0.70	1.16
1.00	0.49	0.62	0.76	1.22
3.00	0.61	0.75	0.88	1.35

LD4 LD4 4/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->ON	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0885	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.53	0.66	0.82	1.43
0.38	0.57	0.70	0.85	1.47
1.00	0.63	0.76	0.92	1.53
3.00	0.75	0.89	1.04	1.65

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->ON	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ON	0.0356	0.12

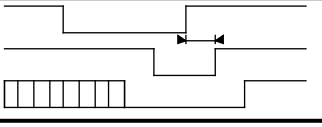
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.60	0.72	0.84	1.28
0.38	0.64	0.75	0.87	1.31
1.00	0.70	0.82	0.94	1.38
3.00	0.83	0.94	1.07	1.50

LD4	LD4	5/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

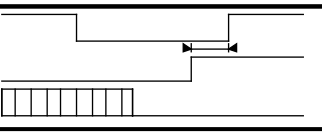
DATA	CLOCK	CONDITION
CD	GN	D

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.566	0.550	0.524	0.437
0.38	0.600	0.584	0.557	0.468
1.00	0.657	0.640	0.612	0.520
3.00	0.840	0.821	0.790	0.688

TIMING CONDITION

DATA	CLOCK	CONDITION
CD	GN	D

ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.171	0.182	0.201	0.261
0.38	0.140	0.151	0.170	0.231
1.00	0.087	0.098	0.118	0.181
3.00	-0.085	-0.072	-0.050	0.020

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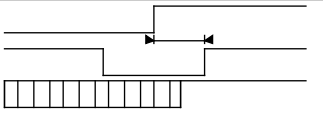
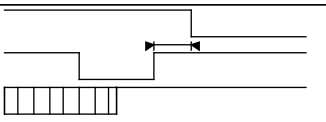
LD4	LD4	6/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	GN	CD

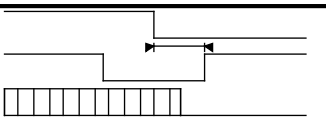
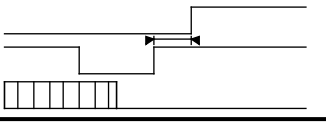
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.541	0.526	0.501	0.419
0.38	0.603	0.587	0.561	0.475
1.00	0.707	0.690	0.661	0.570
3.00	1.040	1.020	0.986	0.876

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.267	0.296	0.346	0.506
0.38	0.242	0.271	0.321	0.479
1.00	0.201	0.230	0.278	0.434
3.00	0.067	0.095	0.141	0.290

TIMING CONDITION

DATA	CLOCK	CONDITION
D	GN	CD

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.412	0.383	0.334	0.177
0.38	0.437	0.409	0.360	0.205
1.00	0.480	0.452	0.404	0.251
3.00	0.618	0.591	0.546	0.401

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.190	0.201	0.219	0.278
0.38	0.131	0.142	0.161	0.223
1.00	0.031	0.043	0.064	0.130
3.00	-0.290	-0.275	-0.250	-0.167

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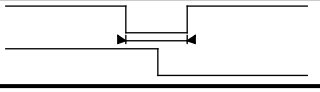
LD4	LD4	7/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

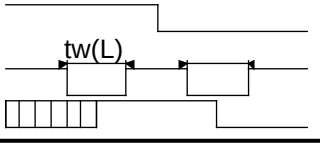
CLOCK	CONDITION
CD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.760

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
GN	CD

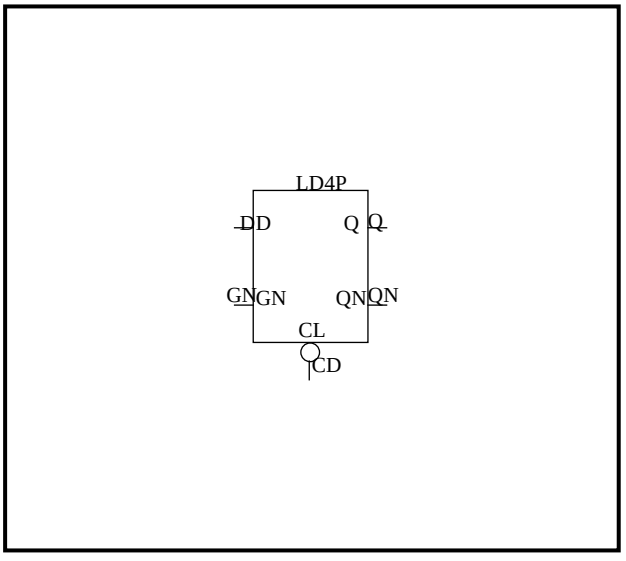
ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.780

LD4P	LD4P	1/7

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
LD4P	D-TYPE TRANSPARENT LATCH with CLEAR (LOW ENABLE)	6	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT	
CD	GN	D	Q	QN
L	X*	X	L	H
H	L	L	L	H
H	L	H	H	L
H	H	X	HOLD	

*:Consider the Hold Time of CLEAR

Verilog-HDL DESCRIPTION

```
LD4P  inst(Q,QN,D,GN,CD);
```

VHDL DESCRIPTION

```
inst:LD4P
   port   map(Q,QN,D,GN,CD);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q	QN
ELECTRO MIGRATION DRIVE	6880.0	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D	1.01
GN	0.99
CD	0.98

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	80.5	97.4

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LD4P | LD4P | 2/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0225	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.46	0.55	0.85
0.38	0.38	0.48	0.57	0.87
1.00	0.45	0.55	0.64	0.93
3.00	0.62	0.73	0.83	1.13

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0441	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.56	0.63	0.71	1.02
0.38	0.58	0.65	0.73	1.04
1.00	0.65	0.72	0.80	1.11
3.00	0.85	0.92	1.00	1.31

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0517	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.50	0.60	0.98
0.38	0.49	0.58	0.68	1.06
1.00	0.61	0.70	0.81	1.18
3.00	0.91	1.00	1.10	1.48

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0225	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.40	0.49	0.79
0.38	0.35	0.44	0.53	0.83
1.00	0.41	0.50	0.59	0.89
3.00	0.51	0.60	0.70	1.01

LD4P | LD4P | 3/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0441	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.58	0.66	0.98
0.38	0.55	0.62	0.70	1.01
1.00	0.61	0.68	0.76	1.07
3.00	0.73	0.80	0.88	1.20

PATH CONDITION

PATH	CONDITION	FUNCTION
D->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0180	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.63	0.71	0.78	1.02
0.38	0.71	0.79	0.86	1.10
1.00	0.84	0.91	0.98	1.23
3.00	1.14	1.21	1.29	1.53

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0517	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.57	0.67	1.05
0.38	0.51	0.60	0.71	1.09
1.00	0.57	0.67	0.77	1.15
3.00	0.70	0.79	0.90	1.28

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0225	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.39	0.48	0.57	0.87
0.38	0.42	0.51	0.61	0.91
1.00	0.49	0.58	0.67	0.97
3.00	0.61	0.70	0.80	1.09

LD4P | LD4P | 4/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0441	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.59	0.66	0.74	1.05
0.38	0.62	0.69	0.78	1.09
1.00	0.69	0.76	0.84	1.15
3.00	0.81	0.88	0.96	1.28

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0180	0.13

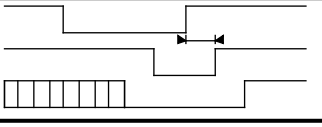
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.70	0.78	0.85	1.09
0.38	0.74	0.81	0.88	1.12
1.00	0.80	0.87	0.95	1.19
3.00	0.93	1.00	1.07	1.32

LD4P	LD4P	5/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

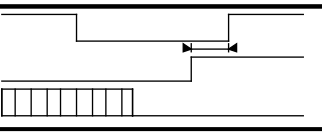
DATA	CLOCK	CONDITION
CD	GN	D

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.929	0.904	0.862	0.725
0.38	0.968	0.942	0.899	0.761
1.00	1.032	1.006	0.962	0.821
3.00	1.239	1.212	1.166	1.016

TIMING CONDITION

DATA	CLOCK	CONDITION
CD	GN	D

ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.028	-0.015	0.007	0.079
0.38	-0.063	-0.050	-0.027	0.046
1.00	-0.123	-0.109	-0.085	-0.010
3.00	-0.314	-0.299	-0.273	-0.191

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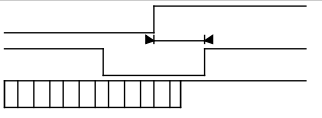
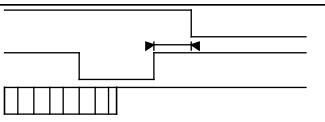
LD4P | LD4P | 6/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	GN	CD

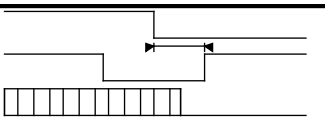
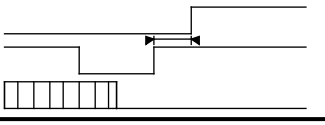
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.900	0.874	0.832	0.696
0.38	0.968	0.943	0.900	0.762
1.00	1.084	1.058	1.014	0.874
3.00	1.456	1.428	1.382	1.234

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.091	0.123	0.176	0.348
0.38	0.053	0.085	0.138	0.309
1.00	-0.012	0.020	0.073	0.244
3.00	-0.220	-0.189	-0.137	0.032

TIMING CONDITION

DATA	CLOCK	CONDITION
D	GN	CD

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.681	0.652	0.602	0.443
0.38	0.720	0.691	0.641	0.482
1.00	0.786	0.757	0.707	0.547
3.00	0.998	0.969	0.919	0.759

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.001	0.015	0.037	0.108
0.38	-0.065	-0.051	-0.028	0.046
1.00	-0.177	-0.162	-0.138	-0.059
3.00	-0.537	-0.519	-0.490	-0.395

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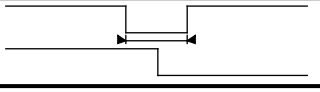
LD4P	LD4P	7/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

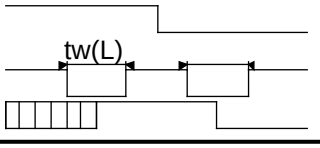
CLOCK	CONDITION
CD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	1.090

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
GN	CD

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	1.200

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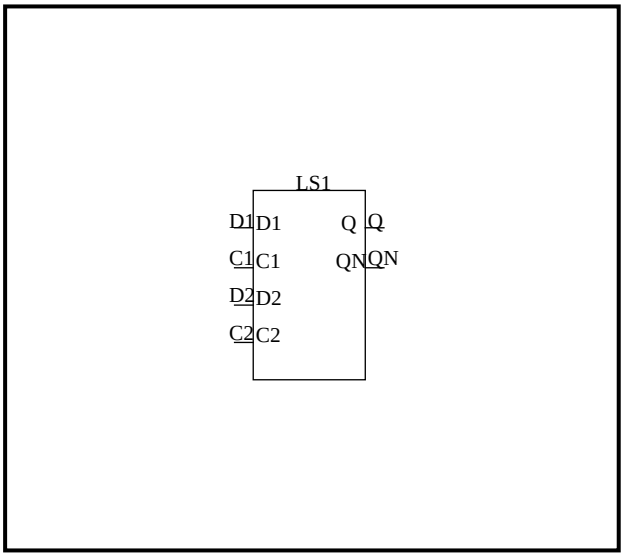
LS1	LS1	1/14

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
LS1	D-TYPE TRANSPARENT LATCH with SCAN TEST INPUT	7	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT	
D1	C1	D2	C2	Q	QN
L	H	X	L	L	H
H	H	X	L	H	L
X	L	L	H	L	H
X	L	H	H	H	L
X	L	X	L	HOLD	
H	H	X	H	H	L
X	H	H	H	H	L
L	H	L	H	L	H

Verilog-HDL DESCRIPTION

```
LS1  inst(Q,QN,D1,C1,D2,C2);
```

VHDL DESCRIPTION

```
inst:LS1
   port   map(Q,QN,D1,C1,D2,C2);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q	QN
ELECTRO MIGRATION DRIVE	6880.0	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D1	0.98
C1	2.00
D2	0.99
C2	1.97

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	41.7	50.2

Rev.1.01.10

LS1 LS1 2/14

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q	C2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0977	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.59	0.78	1.49
0.38	0.47	0.64	0.83	1.54
1.00	0.55	0.72	0.91	1.62
3.00	0.70	0.87	1.06	1.77

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q	C2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0433	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.71	0.90	1.08	1.66
0.38	0.70	0.89	1.07	1.66
1.00	0.72	0.91	1.09	1.68
3.00	0.86	1.06	1.24	1.83

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q	~C2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0977	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.66	0.85	1.56
0.38	0.56	0.73	0.92	1.62
1.00	0.64	0.81	1.00	1.70
3.00	0.81	0.98	1.18	1.89

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q	~C2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0433	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.38	0.55	0.71	1.26
0.38	0.46	0.63	0.79	1.34
1.00	0.53	0.70	0.86	1.41
3.00	0.64	0.81	0.96	1.51

LS1 LS1 3/14

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->QN	C2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0859	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.88	1.02	1.17	1.78
0.38	0.88	1.01	1.17	1.78
1.00	0.89	1.03	1.19	1.80
3.00	1.04	1.18	1.34	1.94

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->QN	C2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0342	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.57	0.69	0.80	1.23
0.38	0.63	0.74	0.86	1.28
1.00	0.70	0.82	0.93	1.36
3.00	0.86	0.97	1.09	1.51

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->QN	~C2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0342	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.64	0.75	0.87	1.29
0.38	0.71	0.82	0.94	1.36
1.00	0.79	0.90	1.02	1.44
3.00	0.97	1.08	1.20	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->QN	~C2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0859	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.00	0.06	0.33	1.06
0.38	0.01	0.31	0.53	1.30
1.00	0.98	1.00	1.04	1.60
3.00	0.76	1.10	1.18	1.71

LS1 LS1 4/14

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q	C1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0977	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.59	0.78	1.49
0.38	0.47	0.64	0.84	1.54
1.00	0.54	0.72	0.91	1.62
3.00	0.67	0.84	1.04	1.75

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q	C1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0433	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.64	0.83	1.01	1.59
0.38	0.65	0.84	1.02	1.60
1.00	0.72	0.91	1.09	1.67
3.00	0.98	1.17	1.35	1.94

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q	~C1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0977	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.65	0.85	1.55
0.38	0.55	0.72	0.92	1.63
1.00	0.62	0.79	0.99	1.69
3.00	0.76	0.94	1.13	1.85

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q	~C1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0433	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.54	0.70	1.25
0.38	0.45	0.62	0.78	1.33
1.00	0.51	0.68	0.84	1.39
3.00	0.58	0.75	0.91	1.45

LS1 LS1 5/14

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->QN	C1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0859	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.81	0.95	1.11	1.71
0.38	0.82	0.96	1.12	1.72
1.00	0.89	1.03	1.19	1.80
3.00	1.16	1.29	1.45	2.06

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->QN	C1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0342	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.57	0.68	0.80	1.22
0.38	0.63	0.74	0.86	1.28
1.00	0.70	0.81	0.93	1.36
3.00	0.83	0.95	1.07	1.49

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->QN	~C1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0859	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.65	0.81	1.42
0.38	0.60	0.73	0.89	1.50
1.00	0.66	0.79	0.95	1.56
3.00	0.72	0.86	1.02	1.63

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->QN	~C1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0342	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.63	0.75	0.87	1.29
0.38	0.71	0.82	0.94	1.36
1.00	0.78	0.89	1.01	1.43
3.00	0.93	1.04	1.16	1.58

LS1 LS1 6/14

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q	C1&C2&~D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0977	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.58	0.77	1.48
0.38	0.49	0.66	0.85	1.55
1.00	0.60	0.77	0.96	1.66
3.00	0.82	0.99	1.18	1.89

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q	C1&C2&~D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0433	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.63	0.81	0.99	1.56
0.38	0.62	0.81	0.99	1.56
1.00	0.64	0.83	1.00	1.58
3.00	0.75	0.94	1.12	1.70

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q	C1&~C2&D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0977	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.43	0.60	0.79	1.50
0.38	0.51	0.68	0.87	1.57
1.00	0.62	0.79	0.98	1.69
3.00	0.86	1.03	1.22	1.92

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q	C1&~C2&D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0433	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.68	0.88	1.05	1.63
0.38	0.68	0.87	1.05	1.63
1.00	0.70	0.89	1.07	1.64
3.00	0.81	1.00	1.18	1.76

LS1 LS1 7/14

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q	C1&~C2&~D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0977	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.59	0.78	1.49
0.38	0.50	0.67	0.86	1.57
1.00	0.62	0.79	0.98	1.68
3.00	0.86	1.03	1.22	1.92

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q	C1&~C2&~D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0433	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.70	0.87	1.42
0.38	0.53	0.71	0.87	1.43
1.00	0.56	0.74	0.91	1.47
3.00	0.68	0.87	1.04	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->QN	C1&C2&~D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0859	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.79	0.93	1.09	1.69
0.38	0.79	0.93	1.08	1.69
1.00	0.81	0.94	1.10	1.71
3.00	0.92	1.06	1.22	1.83

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->QN	C1&C2&~D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0342	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.56	0.68	0.79	1.22
0.38	0.64	0.75	0.87	1.30
1.00	0.75	0.87	0.98	1.41
3.00	0.98	1.10	1.22	1.64

LS1 LS1 8/14

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->QN	C1&~C2&D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0859	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.86	0.99	1.15	1.76
0.38	0.85	0.99	1.15	1.76
1.00	0.87	1.00	1.16	1.77
3.00	0.98	1.12	1.28	1.89

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->QN	C1&~C2&D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0342	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.58	0.70	0.81	1.24
0.38	0.66	0.77	0.89	1.31
1.00	0.78	0.89	1.01	1.43
3.00	1.02	1.13	1.25	1.68

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->QN	C1&~C2&~D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0859	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.68	0.81	0.97	1.58
0.38	0.69	0.82	0.98	1.59
1.00	0.72	0.86	1.01	1.62
3.00	0.85	0.98	1.14	1.75

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->QN	C1&~C2&~D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0342	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.57	0.69	0.80	1.23
0.38	0.65	0.77	0.88	1.31
1.00	0.77	0.88	1.00	1.43
3.00	1.02	1.13	1.25	1.68

LS1 LS1 9/14

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q	C1&C2&~D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0977	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.40	0.58	0.77	1.48
0.38	0.48	0.65	0.85	1.55
1.00	0.58	0.75	0.95	1.65
3.00	0.77	0.94	1.13	1.84

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q	C1&C2&~D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0433	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.58	0.77	0.94	1.52
0.38	0.60	0.79	0.96	1.53
1.00	0.67	0.85	1.03	1.60
3.00	0.90	1.09	1.27	1.85

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q	~C1&C2&D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0977	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.59	0.79	1.50
0.38	0.50	0.67	0.87	1.58
1.00	0.61	0.78	0.97	1.68
3.00	0.80	0.97	1.17	1.88

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q	~C1&C2&D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0433	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.66	0.85	1.03	1.62
0.38	0.68	0.87	1.05	1.63
1.00	0.74	0.94	1.12	1.70
3.00	0.99	1.18	1.37	1.95

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q	~C1&C2&~D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0977	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.40	0.58	0.77	1.48
0.38	0.48	0.65	0.85	1.55
1.00	0.58	0.76	0.95	1.65
3.00	0.79	0.96	1.15	1.86

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q	~C1&C2&~D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0433	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.50	0.67	0.84	1.40
0.38	0.52	0.69	0.86	1.42
1.00	0.59	0.76	0.93	1.49
3.00	0.79	0.97	1.14	1.70

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->QN	C1&C2&~D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0859	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.75	0.89	1.04	1.65
0.38	0.77	0.90	1.06	1.67
1.00	0.84	0.97	1.13	1.74
3.00	1.08	1.21	1.37	1.98

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->QN	C1&C2&~D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0342	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.56	0.67	0.79	1.21
0.38	0.64	0.75	0.87	1.29
1.00	0.74	0.85	0.97	1.39
3.00	0.93	1.05	1.17	1.59

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->QN	~C1&C2&D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0859	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.83	0.97	1.13	1.74
0.38	0.85	0.98	1.14	1.75
1.00	0.92	1.05	1.21	1.82
3.00	1.17	1.30	1.46	2.07

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->QN	~C1&C2&D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0342	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.58	0.69	0.81	1.23
0.38	0.66	0.77	0.89	1.31
1.00	0.76	0.88	1.00	1.42
3.00	0.97	1.08	1.20	1.63

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->QN	~C1&C2&~D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0859	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.66	0.79	0.95	1.56
0.38	0.68	0.81	0.97	1.58
1.00	0.75	0.88	1.04	1.65
3.00	0.96	1.09	1.25	1.86

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->QN	~C1&C2&~D1	FALL

SLEW FACTOR

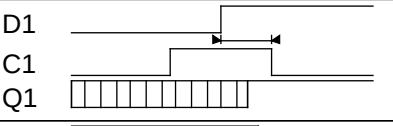
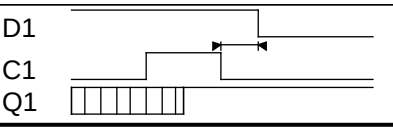
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0342	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.56	0.67	0.79	1.21
0.38	0.64	0.75	0.87	1.29
1.00	0.74	0.85	0.97	1.40
3.00	0.95	1.07	1.19	1.61

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D1	C1	~C2

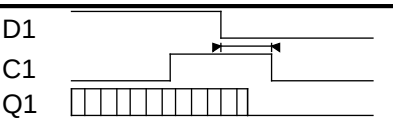
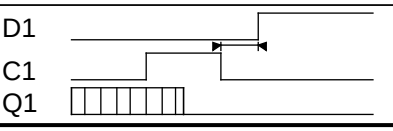
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.539	0.510	0.461	0.304
0.38	0.560	0.527	0.474	0.301
1.00	0.595	0.558	0.495	0.295
3.00	0.708	0.654	0.565	0.276

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.165	0.121	0.046	-0.194
0.38	0.109	0.065	-0.008	-0.244
1.00	0.015	-0.027	-0.098	-0.328
3.00	-0.287	-0.326	-0.390	-0.599

TIMING CONDITION

DATA	CLOCK	CONDITION
D1	C1	~C2

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

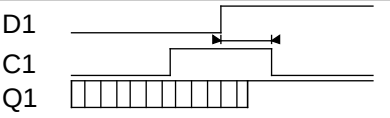
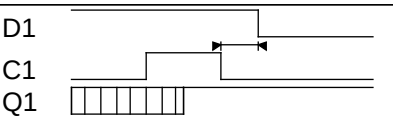
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.555	0.596	0.663	0.881
0.38	0.613	0.653	0.719	0.933
1.00	0.711	0.749	0.813	1.020
3.00	1.024	1.059	1.116	1.302

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.223	0.252	0.300	0.457
0.38	0.205	0.237	0.292	0.468
1.00	0.174	0.213	0.278	0.486
3.00	0.077	0.134	0.231	0.544

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D2	C2	~C1

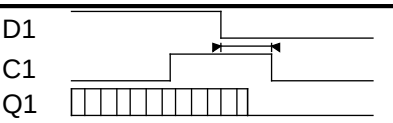
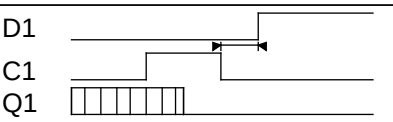
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.531	0.490	0.422	0.200
0.38	0.569	0.526	0.453	0.220
1.00	0.632	0.585	0.507	0.253
3.00	0.837	0.778	0.678	0.358

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.169	0.132	0.068	-0.135
0.38	0.121	0.084	0.023	-0.174
1.00	0.040	0.005	-0.053	-0.240
3.00	-0.222	-0.251	-0.298	-0.452

TIMING CONDITION

DATA	CLOCK	CONDITION
D2	C2	~C1

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

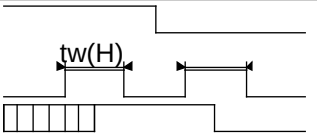
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.555	0.590	0.648	0.833
0.38	0.607	0.640	0.696	0.876
1.00	0.693	0.725	0.777	0.948
3.00	0.972	0.997	1.040	1.178

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.223	0.266	0.337	0.568
0.38	0.188	0.233	0.309	0.553
1.00	0.130	0.179	0.262	0.529
3.00	-0.058	0.005	0.110	0.450

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

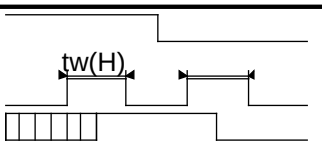
CLOCK	CONDITION
C1	---

ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.910

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
C2	---

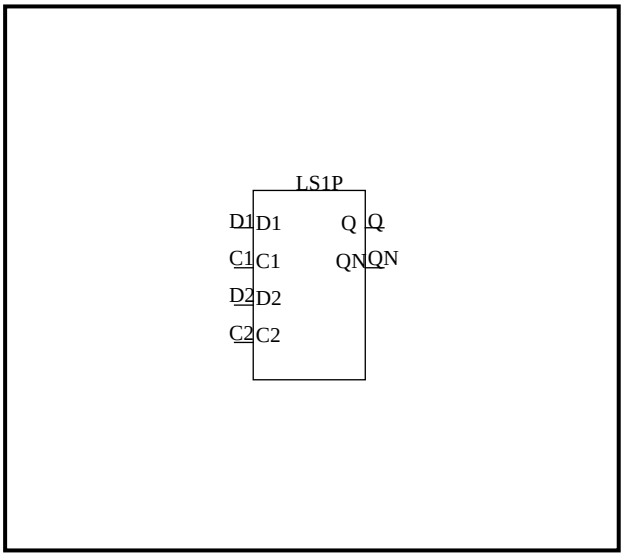
ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.930

LS1P	LS1P	1/14

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
LS1P	D-TYPE TRANSPARENT LATCH with SCAN TEST INPUT	8	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT	
D1	C1	D2	C2	Q	QN
L	H	X	L	L	H
H	H	X	L	H	L
X	L	L	H	L	H
X	L	H	H	H	L
X	L	X	L	HOLD	
H	H	X	H	H	L
X	H	H	H	H	L
L	H	L	H	L	H

Verilog-HDL DESCRIPTION

```
LS1P  inst(Q,QN,D1,C1,D2,C2);
```

VHDL DESCRIPTION

```
inst:LS1P
   port   map(Q,QN,D1,C1,D2,C2);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q	QN
ELECTRO MIGRATION DRIVE	6880.0	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D1	0.98
C1	2.00
D2	0.99
C2	1.97

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	73.0	98.0

Rev.1.01.10

LS1P | LS1P | 2/14

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q	C2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0541	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.51	0.62	1.01
0.38	0.47	0.57	0.67	1.06
1.00	0.55	0.64	0.75	1.14
3.00	0.71	0.80	0.91	1.30

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q	C2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0274	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.71	0.84	0.96	1.34
0.38	0.71	0.83	0.95	1.33
1.00	0.73	0.85	0.97	1.35
3.00	0.87	0.99	1.12	1.50

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q	~C2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0541	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.58	0.68	1.07
0.38	0.55	0.65	0.75	1.14
1.00	0.63	0.73	0.83	1.22
3.00	0.81	0.91	1.02	1.41

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q	~C2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0274	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.47	0.58	0.93
0.38	0.44	0.55	0.66	1.01
1.00	0.51	0.62	0.73	1.08
3.00	0.62	0.73	0.83	1.18

LS1P | LS1P | 3/14

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->QN	C2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0440	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.99	1.06	1.15	1.46
0.38	0.99	1.06	1.14	1.46
1.00	1.00	1.08	1.16	1.48
3.00	1.15	1.22	1.31	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->QN	C2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0177	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.65	0.72	0.79	1.03
0.38	0.70	0.77	0.84	1.09
1.00	0.78	0.85	0.92	1.17
3.00	0.95	1.02	1.09	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->QN	~C2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0440	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.59	0.66	0.74	1.06
0.38	0.67	0.74	0.82	1.14
1.00	0.74	0.81	0.89	1.21
3.00	0.84	0.91	1.00	1.31

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->QN	~C2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0177	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.71	0.78	0.85	1.09
0.38	0.78	0.85	0.92	1.16
1.00	0.86	0.93	1.00	1.24
3.00	1.05	1.12	1.20	1.44

LS1P | LS1P | 4/14

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q	C1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0541	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.51	0.62	1.01
0.38	0.47	0.57	0.67	1.07
1.00	0.55	0.64	0.75	1.14
3.00	0.69	0.78	0.89	1.29

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q	C1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0274	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.65	0.77	0.89	1.26
0.38	0.65	0.78	0.90	1.27
1.00	0.73	0.85	0.97	1.34
3.00	0.99	1.11	1.23	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q	~C1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0541	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.57	0.68	1.07
0.38	0.55	0.64	0.75	1.15
1.00	0.62	0.71	0.82	1.22
3.00	0.77	0.87	0.98	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q	~C1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0274	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.47	0.57	0.93
0.38	0.43	0.54	0.65	1.00
1.00	0.49	0.60	0.71	1.06
3.00	0.56	0.67	0.78	1.13

LS1P | LS1P | 5/14

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->QN	C1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0440	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.92	0.99	1.07	1.39
0.38	0.93	1.00	1.08	1.40
1.00	1.00	1.07	1.15	1.47
3.00	1.27	1.34	1.43	1.74

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->QN	C1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0177	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.65	0.72	0.79	1.04
0.38	0.70	0.78	0.85	1.09
1.00	0.78	0.86	0.93	1.17
3.00	0.93	1.01	1.08	1.32

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->QN	~C1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0440	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.59	0.66	0.74	1.06
0.38	0.66	0.74	0.82	1.14
1.00	0.72	0.80	0.88	1.20
3.00	0.79	0.86	0.94	1.26

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->QN	~C1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0177	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.71	0.78	0.86	1.10
0.38	0.78	0.85	0.93	1.17
1.00	0.85	0.93	1.00	1.24
3.00	1.01	1.09	1.16	1.41

LS1P | LS1P | 6/14

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q	C1&C2&~D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0541	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.50	0.61	1.00
0.38	0.49	0.58	0.69	1.08
1.00	0.60	0.69	0.80	1.19
3.00	0.84	0.94	1.04	1.43

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q	C1&C2&~D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0274	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.63	0.75	0.87	1.24
0.38	0.63	0.75	0.87	1.24
1.00	0.65	0.77	0.88	1.25
3.00	0.76	0.88	1.00	1.37

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q	C1&~C2&D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0541	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.43	0.52	0.63	1.02
0.38	0.50	0.60	0.70	1.09
1.00	0.62	0.72	0.82	1.21
3.00	0.87	0.97	1.07	1.46

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q	C1&~C2&D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0274	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.69	0.81	0.93	1.31
0.38	0.69	0.81	0.93	1.31
1.00	0.70	0.82	0.94	1.32
3.00	0.81	0.93	1.06	1.43

LS1P | LS1P | 7/14

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q	C1&~C2&~D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0541	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.51	0.62	1.01
0.38	0.50	0.59	0.70	1.09
1.00	0.62	0.71	0.82	1.21
3.00	0.88	0.97	1.07	1.46

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q	C1&~C2&~D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0274	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.63	0.74	1.10
0.38	0.52	0.64	0.75	1.11
1.00	0.56	0.67	0.78	1.14
3.00	0.68	0.80	0.91	1.28

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->QN	C1&C2&~D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0440	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.90	0.97	1.05	1.37
0.38	0.90	0.97	1.05	1.37
1.00	0.91	0.99	1.07	1.38
3.00	1.03	1.10	1.19	1.50

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->QN	C1&C2&~D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0177	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.63	0.71	0.78	1.02
0.38	0.71	0.79	0.86	1.10
1.00	0.83	0.90	0.97	1.22
3.00	1.08	1.15	1.23	1.47

LS1P | LS1P | 8/14

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->QN	C1&~C2&D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0440	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.96	1.03	1.12	1.43
0.38	0.96	1.03	1.12	1.43
1.00	0.97	1.05	1.13	1.45
3.00	1.09	1.16	1.25	1.56

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->QN	C1&~C2&D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0177	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.65	0.73	0.80	1.04
0.38	0.73	0.80	0.88	1.12
1.00	0.85	0.92	1.00	1.24
3.00	1.11	1.19	1.26	1.50

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->QN	C1&~C2&~D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0440	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.76	0.83	0.92	1.23
0.38	0.77	0.84	0.92	1.24
1.00	0.80	0.88	0.96	1.27
3.00	0.94	1.01	1.10	1.41

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->QN	C1&~C2&~D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0177	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.64	0.72	0.79	1.03
0.38	0.72	0.80	0.87	1.11
1.00	0.84	0.92	0.99	1.23
3.00	1.11	1.19	1.26	1.50

Rev.1.01.10

LS1P | LS1P | 9/14

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q	C1&C2&~D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0541	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.40	0.50	0.61	1.00
0.38	0.48	0.58	0.69	1.08
1.00	0.59	0.68	0.79	1.18
3.00	0.79	0.89	1.00	1.39

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q	C1&C2&~D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0274	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.59	0.71	0.83	1.20
0.38	0.61	0.73	0.84	1.21
1.00	0.67	0.79	0.91	1.28
3.00	0.91	1.04	1.15	1.53

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q	~C1&C2&D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0541	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.52	0.62	1.02
0.38	0.50	0.60	0.70	1.10
1.00	0.61	0.71	0.81	1.21
3.00	0.82	0.92	1.03	1.42

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q	~C1&C2&D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0274	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.67	0.79	0.91	1.29
0.38	0.68	0.81	0.93	1.31
1.00	0.75	0.87	0.99	1.37
3.00	1.00	1.12	1.25	1.63

LS1P | LS1P | 10/14

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q	~C1&C2&~D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0541	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.40	0.50	0.61	1.00
0.38	0.48	0.58	0.68	1.08
1.00	0.59	0.68	0.79	1.18
3.00	0.81	0.91	1.01	1.41

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q	~C1&C2&~D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0274	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.50	0.61	0.72	1.07
0.38	0.52	0.63	0.74	1.10
1.00	0.59	0.70	0.81	1.17
3.00	0.79	0.91	1.02	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->QN	C1&C2&~D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0440	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.86	0.93	1.01	1.33
0.38	0.87	0.95	1.03	1.34
1.00	0.94	1.01	1.10	1.41
3.00	1.19	1.27	1.35	1.66

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->QN	C1&C2&~D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0177	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.63	0.71	0.78	1.02
0.38	0.71	0.79	0.86	1.10
1.00	0.82	0.90	0.97	1.21
3.00	1.04	1.11	1.19	1.43

LS1P | LS1P | 11/14

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->QN	~C1&C2&D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0440	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.94	1.02	1.10	1.42
0.38	0.96	1.03	1.12	1.43
1.00	1.03	1.10	1.18	1.50
3.00	1.28	1.36	1.44	1.76

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->QN	~C1&C2&D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0177	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.65	0.73	0.80	1.04
0.38	0.73	0.81	0.88	1.12
1.00	0.84	0.92	0.99	1.23
3.00	1.07	1.15	1.22	1.46

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->QN	~C1&C2&~D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0440	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.74	0.81	0.90	1.21
0.38	0.76	0.83	0.92	1.23
1.00	0.83	0.90	0.99	1.30
3.00	1.06	1.13	1.21	1.53

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->QN	~C1&C2&~D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0177	0.13

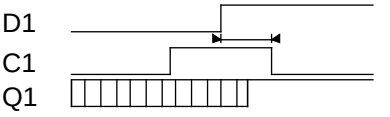
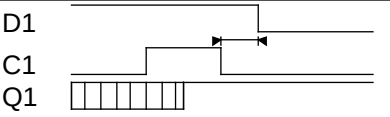
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.63	0.71	0.78	1.02
0.38	0.71	0.79	0.86	1.10
1.00	0.82	0.90	0.97	1.21
3.00	1.05	1.13	1.20	1.45

LS1P	LS1P	12/14

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D1	C1	~C2

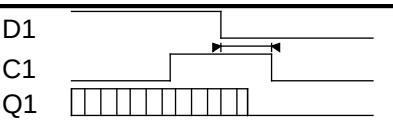
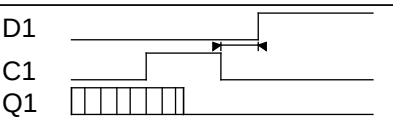
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.620	0.591	0.541	0.382
0.38	0.643	0.611	0.557	0.385
1.00	0.680	0.644	0.584	0.389
3.00	0.802	0.752	0.670	0.405

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.129	0.083	0.006	-0.243
0.38	0.071	0.026	-0.050	-0.294
1.00	-0.026	-0.070	-0.143	-0.380
3.00	-0.340	-0.379	-0.445	-0.657

TIMING CONDITION

DATA	CLOCK	CONDITION
D1	C1	~C2

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.632	0.671	0.735	0.944
0.38	0.692	0.730	0.794	0.999
1.00	0.793	0.830	0.891	1.090
3.00	1.118	1.151	1.206	1.384

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.200	0.229	0.279	0.438
0.38	0.181	0.214	0.269	0.447
1.00	0.149	0.188	0.253	0.462
3.00	0.048	0.105	0.200	0.509

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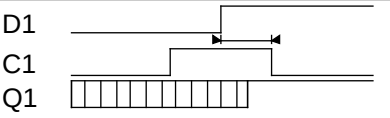
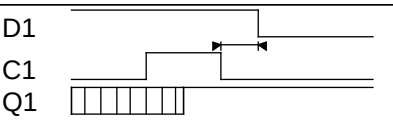
CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D2	C2	~C1

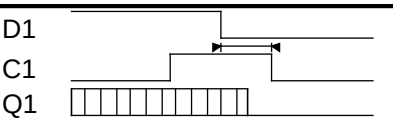
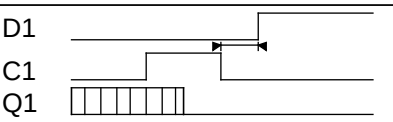
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.626	0.583	0.512	0.282
0.38	0.665	0.621	0.547	0.308
1.00	0.731	0.684	0.605	0.352
3.00	0.942	0.887	0.794	0.493

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.136	0.096	0.028	-0.189
0.38	0.084	0.045	-0.020	-0.231
1.00	-0.002	-0.039	-0.101	-0.301
3.00	-0.281	-0.311	-0.363	-0.528

TIMING CONDITION

DATA	CLOCK	CONDITION
D2	C2	~C1

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

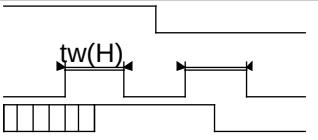
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.639	0.672	0.729	0.910
0.38	0.693	0.726	0.780	0.956
1.00	0.784	0.815	0.867	1.033
3.00	1.077	1.103	1.145	1.284

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.207	0.249	0.320	0.549
0.38	0.171	0.215	0.290	0.531
1.00	0.110	0.158	0.239	0.501
3.00	-0.087	-0.026	0.075	0.404

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

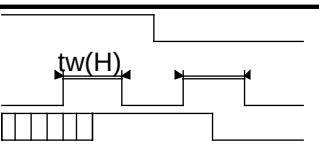
CLOCK	CONDITION
C1	---

ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.980

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
C2	---

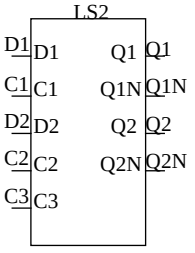
ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	1.000

LS2	LS2	1/27

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
LS2	D-TYPE TRANSPARENT LATCH with SCAN TEST INPUT	11	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT					OUTPUT			
D1	C1	D2	C2	C3	Q1	Q1N	Q2	Q2N
L	H	X	L	-	L	H	-	-
H	H	X	L	-	H	L	-	-
X	L	L	H	-	L	H	-	-
X	L	H	H	-	H	L	-	-
X	L	X	L	-	HOLD	HOLD	-	-
H	H	X	H	-	H	L	-	-
X	H	H	H	-	H	L	-	-
L	H	L	H	-	L	H	-	-
-	-	-	-	H	-	-	Q1	Q1N
-	-	-	-	L	-	-	HOLD	HOLD

Verilog-HDL DESCRIPTION

```
LS2  inst(Q1,Q1N,Q2,Q2N,D1,C1,D2,
C2,C3);
```

VHDL DESCRIPTION

```
inst:LS2
   port   map(Q1,Q1N,Q2,Q2N,D1,
C1,D2,C2,C3);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q1,Q1N,Q2,Q2N
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D1	0.98
C1	2.00
D2,C3	0.99
C2	1.97

OUTPUT DRIVE (LU)

PIN NAME	Q1	Q1N	Q2	Q2N
DRIVE	40.9	49.4	50.2	42.1

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LS2 LS2 2/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q1	C2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0987	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.60	0.80	1.52
0.38	0.47	0.65	0.85	1.57
1.00	0.55	0.73	0.92	1.64
3.00	0.69	0.88	1.07	1.79

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q1	C2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0438	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.71	0.91	1.10	1.68
0.38	0.70	0.90	1.09	1.68
1.00	0.72	0.92	1.11	1.69
3.00	0.86	1.07	1.26	1.85

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q1	~C2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0987	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.67	0.86	1.58
0.38	0.55	0.73	0.93	1.65
1.00	0.63	0.81	1.01	1.73
3.00	0.80	0.99	1.18	1.91

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q1	~C2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0438	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.38	0.55	0.72	1.28
0.38	0.46	0.63	0.80	1.35
1.00	0.53	0.70	0.87	1.42
3.00	0.64	0.81	0.98	1.52

LS2 LS2 3/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q1N	C2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0845	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.05	1.20	1.37	1.99
0.38	1.05	1.19	1.36	1.98
1.00	1.07	1.21	1.38	2.00
3.00	1.22	1.36	1.53	2.15

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q1N	C2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0346	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.74	0.89	1.03	1.49
0.38	0.79	0.94	1.08	1.54
1.00	0.87	1.01	1.15	1.62
3.00	1.02	1.17	1.31	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q1N	~C2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0845	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.67	0.82	0.99	1.61
0.38	0.75	0.90	1.07	1.69
1.00	0.82	0.97	1.14	1.76
3.00	0.93	1.07	1.24	1.86

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q1N	~C2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0346	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.80	0.95	1.09	1.55
0.38	0.87	1.02	1.15	1.62
1.00	0.95	1.09	1.23	1.70
3.00	1.13	1.28	1.42	1.88

LS2 LS2 4/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q2	C2&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0860	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.98	1.11	1.27	1.88
0.38	1.03	1.16	1.32	1.93
1.00	1.11	1.24	1.40	2.01
3.00	1.26	1.40	1.55	2.16

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q2	C2&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0343	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.29	1.40	1.52	1.95
0.38	1.28	1.40	1.52	1.94
1.00	1.30	1.42	1.53	1.96
3.00	1.45	1.57	1.68	2.11

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q2	~C2&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0860	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.04	1.17	1.33	1.94
0.38	1.11	1.24	1.40	2.01
1.00	1.19	1.32	1.48	2.09
3.00	1.37	1.50	1.66	2.27

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q2	~C2&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0343	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.91	1.03	1.14	1.57
0.38	0.99	1.10	1.22	1.65
1.00	1.06	1.18	1.29	1.72
3.00	1.17	1.28	1.40	1.82

LS2 LS2 5/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q2N	C2&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0981	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.14	1.31	1.50	2.20
0.38	1.13	1.30	1.49	2.19
1.00	1.15	1.32	1.51	2.21
3.00	1.30	1.47	1.66	2.36

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q2N	C2&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0424	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.82	0.99	1.16	1.70
0.38	0.87	1.05	1.21	1.75
1.00	0.95	1.12	1.29	1.83
3.00	1.10	1.28	1.44	1.99

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q2N	~C2&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0981	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.76	0.93	1.12	1.82
0.38	0.84	1.01	1.20	1.90
1.00	0.91	1.08	1.27	1.97
3.00	1.01	1.18	1.37	2.08

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q2N	~C2&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0424	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.88	1.06	1.22	1.76
0.38	0.95	1.12	1.29	1.83
1.00	1.03	1.20	1.37	1.91
3.00	1.21	1.38	1.55	2.09

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LS2 LS2 6/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q2	C1&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0860	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.97	1.11	1.27	1.87
0.38	1.03	1.17	1.32	1.93
1.00	1.11	1.24	1.40	2.01
3.00	1.24	1.38	1.53	2.14

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q2	C1&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0343	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.22	1.33	1.45	1.88
0.38	1.23	1.34	1.46	1.88
1.00	1.30	1.42	1.53	1.96
3.00	1.57	1.68	1.80	2.22

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q2	~C1&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0860	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.04	1.17	1.33	1.94
0.38	1.11	1.24	1.40	2.01
1.00	1.18	1.31	1.47	2.08
3.00	1.33	1.47	1.62	2.23

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q2	~C1&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0343	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.91	1.02	1.14	1.56
0.38	0.98	1.10	1.21	1.64
1.00	1.04	1.16	1.28	1.70
3.00	1.11	1.22	1.34	1.77

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q2N	C1&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0981	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.07	1.24	1.43	2.13
0.38	1.07	1.25	1.44	2.14
1.00	1.15	1.32	1.51	2.21
3.00	1.41	1.58	1.77	2.48

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q2N	C1&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0424	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.82	0.99	1.15	1.70
0.38	0.87	1.05	1.21	1.76
1.00	0.95	1.12	1.29	1.83
3.00	1.08	1.26	1.42	1.97

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q2N	~C1&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0981	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.75	0.92	1.11	1.82
0.38	0.83	1.00	1.19	1.90
1.00	0.89	1.06	1.25	1.96
3.00	0.96	1.13	1.32	2.02

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q2N	~C1&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0424	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.88	1.05	1.22	1.76
0.38	0.95	1.13	1.29	1.83
1.00	1.02	1.20	1.36	1.90
3.00	1.17	1.35	1.51	2.06

LS2 LS2 8/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q1	C1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0987	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.60	0.80	1.52
0.38	0.48	0.66	0.86	1.58
1.00	0.55	0.73	0.93	1.65
3.00	0.68	0.86	1.06	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q1	C1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0438	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.64	0.84	1.03	1.61
0.38	0.66	0.86	1.05	1.63
1.00	0.73	0.93	1.12	1.70
3.00	0.99	1.19	1.38	1.97

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q1	~C1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0987	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.66	0.86	1.58
0.38	0.55	0.73	0.93	1.65
1.00	0.62	0.80	1.00	1.72
3.00	0.76	0.95	1.15	1.88

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q1	~C1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0438	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.55	0.72	1.27
0.38	0.45	0.63	0.79	1.34
1.00	0.51	0.69	0.85	1.40
3.00	0.58	0.75	0.92	1.47

LS2 LS2 9/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q1N	C1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0845	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.99	1.14	1.31	1.93
0.38	1.00	1.15	1.32	1.94
1.00	1.08	1.23	1.39	2.01
3.00	1.35	1.49	1.66	2.28

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q1N	C1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0346	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.74	0.89	1.03	1.50
0.38	0.80	0.95	1.09	1.55
1.00	0.87	1.02	1.16	1.63
3.00	1.01	1.16	1.30	1.77

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q1N	~C1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0845	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.67	0.82	0.98	1.61
0.38	0.75	0.90	1.06	1.68
1.00	0.81	0.96	1.12	1.74
3.00	0.87	1.02	1.19	1.81

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q1N	~C1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0346	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.80	0.95	1.09	1.56
0.38	0.87	1.02	1.16	1.63
1.00	0.94	1.09	1.23	1.70
3.00	1.10	1.25	1.39	1.85

LS2 LS2 10/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C3->Q2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0860	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.50	0.63	0.79	1.40
0.38	0.57	0.70	0.86	1.47
1.00	0.63	0.77	0.93	1.54
3.00	0.75	0.89	1.05	1.65

PATH CONDITION

PATH	CONDITION	FUNCTION
C3->Q2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0343	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.56	0.67	0.79	1.21
0.38	0.63	0.75	0.86	1.29
1.00	0.69	0.81	0.92	1.35
3.00	0.80	0.91	1.03	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
C3->Q2N	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0981	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.59	0.77	1.47
0.38	0.49	0.66	0.84	1.55
1.00	0.55	0.72	0.91	1.61
3.00	0.65	0.82	1.01	1.71

PATH CONDITION

PATH	CONDITION	FUNCTION
C3->Q2N	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0424	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.51	0.66	1.19
0.38	0.43	0.58	0.74	1.26
1.00	0.49	0.65	0.80	1.33
3.00	0.61	0.77	0.92	1.45

LS2 LS2 11/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q1	C1&C2&~D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0987	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.59	0.79	1.51
0.38	0.49	0.67	0.86	1.58
1.00	0.60	0.78	0.97	1.69
3.00	0.82	1.00	1.20	1.91

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q1	C1&C2&~D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0438	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.62	0.82	1.00	1.58
0.38	0.62	0.82	1.00	1.58
1.00	0.64	0.83	1.02	1.59
3.00	0.75	0.95	1.13	1.71

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q1	C1&~C2&D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0987	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.43	0.61	0.81	1.53
0.38	0.51	0.69	0.88	1.60
1.00	0.62	0.80	1.00	1.72
3.00	0.86	1.04	1.23	1.95

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q1	C1&~C2&D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0438	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.68	0.88	1.07	1.65
0.38	0.68	0.88	1.07	1.65
1.00	0.70	0.89	1.08	1.66
3.00	0.80	1.01	1.20	1.78

LS2 LS2 12/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q1	C1&~C2&~D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0987	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.60	0.80	1.52
0.38	0.50	0.68	0.88	1.59
1.00	0.62	0.80	0.99	1.71
3.00	0.86	1.04	1.23	1.95

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q1	C1&~C2&~D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0438	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.71	0.88	1.44
0.38	0.53	0.71	0.89	1.45
1.00	0.56	0.75	0.92	1.48
3.00	0.68	0.87	1.05	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q1N	C1&C2&~D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0845	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.96	1.11	1.27	1.89
0.38	0.96	1.10	1.27	1.89
1.00	0.97	1.12	1.29	1.91
3.00	1.09	1.24	1.41	2.03

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q1N	C1&C2&~D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0346	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.73	0.87	1.01	1.48
0.38	0.80	0.95	1.09	1.56
1.00	0.92	1.06	1.20	1.67
3.00	1.15	1.29	1.44	1.90

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q1N	C1&~C2&D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0845	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.03	1.17	1.34	1.96
0.38	1.02	1.17	1.34	1.96
1.00	1.04	1.19	1.35	1.97
3.00	1.16	1.30	1.47	2.09

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q1N	C1&~C2&D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0346	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.75	0.89	1.03	1.50
0.38	0.82	0.97	1.11	1.58
1.00	0.94	1.09	1.23	1.69
3.00	1.18	1.33	1.47	1.94

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q1N	C1&~C2&~D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0845	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.83	0.98	1.15	1.77
0.38	0.84	0.99	1.16	1.78
1.00	0.88	1.02	1.19	1.81
3.00	1.01	1.16	1.33	1.95

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q1N	C1&~C2&~D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0346	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.74	0.89	1.03	1.49
0.38	0.82	0.96	1.10	1.57
1.00	0.93	1.08	1.22	1.69
3.00	1.18	1.33	1.47	1.94

LS2 LS2 14/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q2	C1&C2&~D2&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0860	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.97	1.10	1.26	1.87
0.38	1.04	1.18	1.33	1.94
1.00	1.15	1.29	1.45	2.05
3.00	1.39	1.52	1.68	2.29

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q2	C1&C2&~D2&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0343	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.20	1.31	1.43	1.85
0.38	1.19	1.31	1.42	1.85
1.00	1.21	1.32	1.44	1.87
3.00	1.33	1.44	1.56	1.99

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q2	C1&~C2&D2&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0860	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.99	1.12	1.28	1.89
0.38	1.06	1.20	1.35	1.96
1.00	1.18	1.31	1.47	2.08
3.00	1.42	1.56	1.72	2.32

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q2	C1&~C2&D2&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0343	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.26	1.38	1.49	1.92
0.38	1.26	1.38	1.49	1.92
1.00	1.28	1.39	1.51	1.93
3.00	1.39	1.51	1.62	2.05

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q2	C1&~C2&~D2&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0860	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.98	1.11	1.27	1.88
0.38	1.05	1.19	1.35	1.95
1.00	1.17	1.31	1.46	2.07
3.00	1.42	1.56	1.71	2.32

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q2	C1&~C2&~D2&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0343	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.07	1.19	1.30	1.73
0.38	1.08	1.19	1.31	1.74
1.00	1.11	1.23	1.35	1.77
3.00	1.25	1.36	1.48	1.90

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q2N	C1&C2&~D2&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0981	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.04	1.21	1.40	2.11
0.38	1.04	1.21	1.40	2.10
1.00	1.06	1.23	1.42	2.12
3.00	1.18	1.35	1.54	2.24

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q2N	C1&C2&~D2&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0424	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.81	0.98	1.15	1.69
0.38	0.89	1.06	1.22	1.77
1.00	1.00	1.17	1.33	1.88
3.00	1.23	1.40	1.57	2.11

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q2N	C1&~C2&D2&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0981	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.11	1.28	1.47	2.17
0.38	1.11	1.28	1.47	2.17
1.00	1.12	1.29	1.48	2.19
3.00	1.24	1.41	1.60	2.30

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q2N	C1&~C2&D2&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0424	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.83	1.00	1.17	1.71
0.38	0.91	1.08	1.24	1.79
1.00	1.02	1.20	1.36	1.90
3.00	1.26	1.44	1.60	2.15

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q2N	C1&~C2&~D2&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0981	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.92	1.09	1.28	1.98
0.38	0.93	1.10	1.29	1.99
1.00	0.96	1.13	1.32	2.03
3.00	1.09	1.27	1.45	2.16

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q2N	C1&~C2&~D2&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0424	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.82	0.99	1.16	1.70
0.38	0.90	1.07	1.23	1.78
1.00	1.01	1.19	1.35	1.90
3.00	1.26	1.44	1.60	2.15

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q1	C1&C2&~D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0987	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.40	0.59	0.78	1.50
0.38	0.48	0.66	0.86	1.58
1.00	0.58	0.76	0.96	1.68
3.00	0.77	0.95	1.15	1.87

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q1	C1&C2&~D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0438	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.58	0.78	0.96	1.54
0.38	0.60	0.79	0.98	1.55
1.00	0.67	0.86	1.04	1.62
3.00	0.90	1.10	1.28	1.87

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q1	~C1&C2&D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0987	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.60	0.80	1.53
0.38	0.50	0.68	0.88	1.61
1.00	0.61	0.79	0.99	1.71
3.00	0.80	0.98	1.18	1.90

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q1	~C1&C2&D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0438	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.66	0.86	1.05	1.63
0.38	0.67	0.88	1.06	1.65
1.00	0.74	0.94	1.13	1.72
3.00	0.99	1.19	1.38	1.97

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q1	~C1&C2&~D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0987	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.40	0.59	0.78	1.50
0.38	0.48	0.66	0.86	1.58
1.00	0.58	0.77	0.96	1.68
3.00	0.79	0.97	1.17	1.89

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q1	~C1&C2&~D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0438	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.50	0.68	0.85	1.41
0.38	0.52	0.70	0.88	1.43
1.00	0.59	0.77	0.95	1.51
3.00	0.79	0.98	1.15	1.72

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q1N	C1&C2&~D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0845	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.92	1.06	1.23	1.85
0.38	0.93	1.08	1.25	1.87
1.00	1.00	1.15	1.32	1.94
3.00	1.25	1.39	1.56	2.18

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q1N	C1&C2&~D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0346	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.72	0.87	1.01	1.48
0.38	0.80	0.95	1.09	1.56
1.00	0.90	1.05	1.19	1.66
3.00	1.10	1.25	1.39	1.85

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q1N	~C1&C2&D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0845	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.01	1.15	1.32	1.94
0.38	1.02	1.17	1.34	1.96
1.00	1.09	1.24	1.40	2.02
3.00	1.34	1.49	1.66	2.28

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q1N	~C1&C2&D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0346	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.75	0.89	1.03	1.50
0.38	0.83	0.97	1.11	1.58
1.00	0.93	1.08	1.22	1.69
3.00	1.13	1.28	1.42	1.89

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q1N	~C1&C2&~D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0845	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.81	0.96	1.12	1.74
0.38	0.83	0.98	1.15	1.77
1.00	0.90	1.05	1.22	1.84
3.00	1.12	1.26	1.43	2.05

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q1N	~C1&C2&~D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0346	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.72	0.87	1.01	1.48
0.38	0.80	0.95	1.09	1.56
1.00	0.91	1.05	1.19	1.66
3.00	1.12	1.27	1.41	1.88

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q2	C2&C1&~D1&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0860	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.96	1.10	1.25	1.86
0.38	1.04	1.18	1.33	1.94
1.00	1.14	1.28	1.43	2.04
3.00	1.34	1.47	1.63	2.24

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q2	C2&C1&~D1&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0343	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.15	1.27	1.38	1.81
0.38	1.17	1.28	1.40	1.82
1.00	1.24	1.35	1.47	1.89
3.00	1.48	1.60	1.71	2.14

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q2	C2&~C1&D1&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0860	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.98	1.12	1.28	1.88
0.38	1.06	1.20	1.36	1.96
1.00	1.17	1.30	1.46	2.07
3.00	1.37	1.51	1.67	2.28

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q2	C2&~C1&D1&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0343	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.24	1.36	1.47	1.90
0.38	1.26	1.37	1.49	1.91
1.00	1.33	1.44	1.56	1.98
3.00	1.58	1.69	1.81	2.24

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q2	C2&~C1&~D1&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0860	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.96	1.10	1.25	1.86
0.38	1.04	1.18	1.33	1.94
1.00	1.14	1.28	1.44	2.04
3.00	1.36	1.49	1.65	2.26

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q2	C2&~C1&~D1&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0343	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.05	1.16	1.28	1.70
0.38	1.07	1.18	1.30	1.72
1.00	1.14	1.25	1.37	1.79
3.00	1.35	1.47	1.58	2.01

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q2N	C2&C1&~D1&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0981	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.00	1.17	1.36	2.06
0.38	1.01	1.19	1.38	2.08
1.00	1.08	1.26	1.45	2.15
3.00	1.33	1.50	1.69	2.39

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q2N	C2&C1&~D1&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0424	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.81	0.98	1.14	1.69
0.38	0.88	1.06	1.22	1.77
1.00	0.99	1.16	1.32	1.87
3.00	1.18	1.36	1.52	2.06

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q2N	C2&~C1&D1&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0981	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.09	1.26	1.45	2.15
0.38	1.10	1.27	1.46	2.17
1.00	1.17	1.34	1.53	2.24
3.00	1.42	1.60	1.79	2.49

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q2N	C2&~C1&D1&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0424	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.83	1.00	1.16	1.71
0.38	0.91	1.08	1.25	1.79
1.00	1.01	1.19	1.35	1.89
3.00	1.22	1.39	1.56	2.10

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q2N	C2&~C1&~D1&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0981	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.89	1.07	1.26	1.96
0.38	0.92	1.09	1.28	1.98
1.00	0.99	1.16	1.35	2.05
3.00	1.20	1.37	1.56	2.26

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q2N	C2&~C1&~D1&C3	FALL

SLEW FACTOR

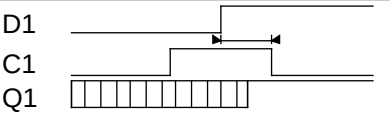
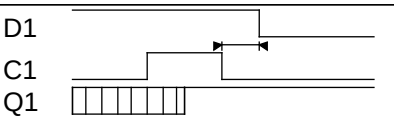
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0424	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.81	0.98	1.14	1.69
0.38	0.88	1.06	1.22	1.77
1.00	0.99	1.16	1.32	1.87
3.00	1.20	1.38	1.54	2.08

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D1	C1	~C2

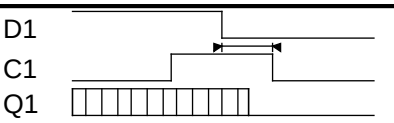
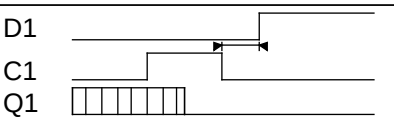
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.654	0.626	0.578	0.422
0.38	0.677	0.646	0.594	0.427
1.00	0.715	0.680	0.623	0.436
3.00	0.837	0.791	0.713	0.464

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.165	0.121	0.046	-0.194
0.38	0.109	0.065	-0.008	-0.244
1.00	0.015	-0.027	-0.098	-0.328
3.00	-0.287	-0.326	-0.390	-0.599

TIMING CONDITION

DATA	CLOCK	CONDITION
D1	C1	~C2

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

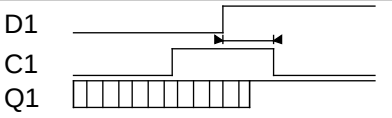
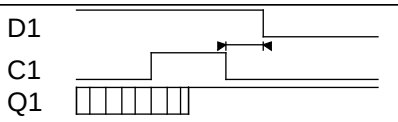
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.639	0.672	0.729	0.910
0.38	0.697	0.730	0.785	0.962
1.00	0.794	0.825	0.879	1.051
3.00	1.106	1.135	1.182	1.336

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.223	0.252	0.300	0.457
0.38	0.205	0.237	0.292	0.468
1.00	0.174	0.213	0.278	0.488
3.00	0.077	0.135	0.233	0.550

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D1	C3	C1&~C2

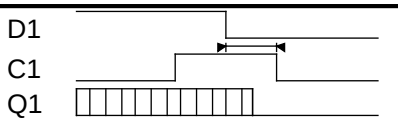
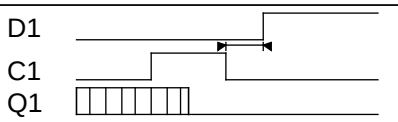
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	1.111	1.079	1.025	0.851
0.38	1.127	1.094	1.040	0.867
1.00	1.152	1.120	1.066	0.893
3.00	1.235	1.203	1.150	0.979

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.281	-0.265	-0.237	-0.147
0.38	-0.334	-0.318	-0.290	-0.200
1.00	-0.423	-0.406	-0.379	-0.289
3.00	-0.709	-0.692	-0.665	-0.575

TIMING CONDITION

DATA	CLOCK	CONDITION
D1	C3	C1&~C2

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

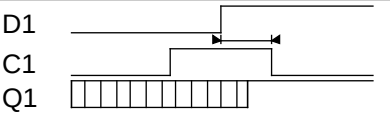
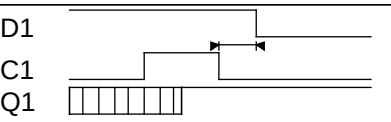
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.937	0.921	0.893	0.804
0.38	0.990	0.973	0.946	0.857
1.00	1.079	1.062	1.034	0.945
3.00	1.364	1.348	1.320	1.231

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.457	-0.424	-0.369	-0.193
0.38	-0.472	-0.439	-0.385	-0.209
1.00	-0.497	-0.465	-0.411	-0.236
3.00	-0.580	-0.548	-0.495	-0.324

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D2	C2	~C1

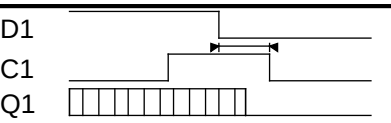
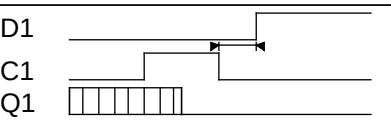
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.650	0.609	0.541	0.322
0.38	0.689	0.647	0.576	0.349
1.00	0.754	0.710	0.635	0.392
3.00	0.966	0.913	0.823	0.534

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.177	0.138	0.073	-0.135
0.38	0.127	0.090	0.027	-0.174
1.00	0.045	0.009	-0.050	-0.240
3.00	-0.222	-0.251	-0.298	-0.452

TIMING CONDITION

DATA	CLOCK	CONDITION
D2	C2	~C1

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

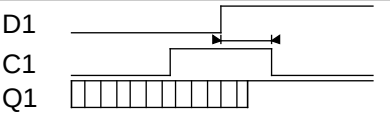
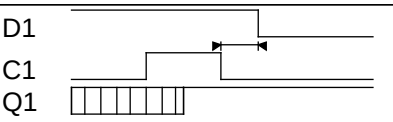
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.643	0.670	0.716	0.863
0.38	0.695	0.721	0.765	0.907
1.00	0.781	0.806	0.847	0.981
3.00	1.060	1.079	1.112	1.219

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.230	0.271	0.342	0.568
0.38	0.195	0.239	0.314	0.554
1.00	0.136	0.185	0.267	0.531
3.00	-0.052	0.011	0.116	0.456

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D2	C3	C2&~C1

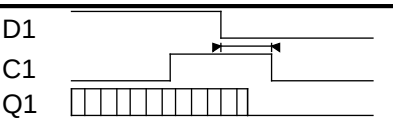
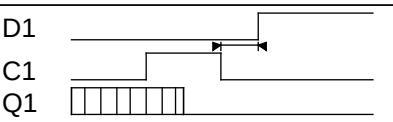
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	1.052	1.021	0.968	0.797
0.38	1.094	1.062	1.009	0.838
1.00	1.163	1.132	1.079	0.908
3.00	1.388	1.356	1.303	1.132

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.281	-0.264	-0.236	-0.143
0.38	-0.328	-0.311	-0.282	-0.190
1.00	-0.405	-0.389	-0.360	-0.269
3.00	-0.656	-0.640	-0.612	-0.523

TIMING CONDITION

DATA	CLOCK	CONDITION
D2	C3	C2&~C1

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.937	0.921	0.893	0.804
0.38	0.983	0.967	0.939	0.850
1.00	1.061	1.045	1.017	0.928
3.00	1.312	1.295	1.267	1.178

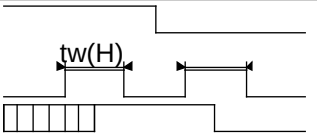
HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.398	-0.366	-0.311	-0.134
0.38	-0.440	-0.407	-0.352	-0.177
1.00	-0.509	-0.476	-0.422	-0.247
3.00	-0.732	-0.700	-0.647	-0.475

LS2	LS2	27/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

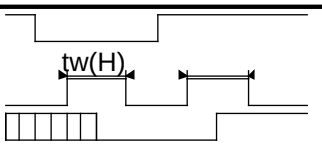
CLOCK	CONDITION
C1	---

ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.980

MINIMUM PULSE WIDTH CONDITION

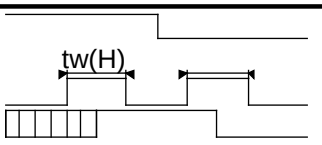
CLOCK	CONDITION
C3	---

ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
C2	---

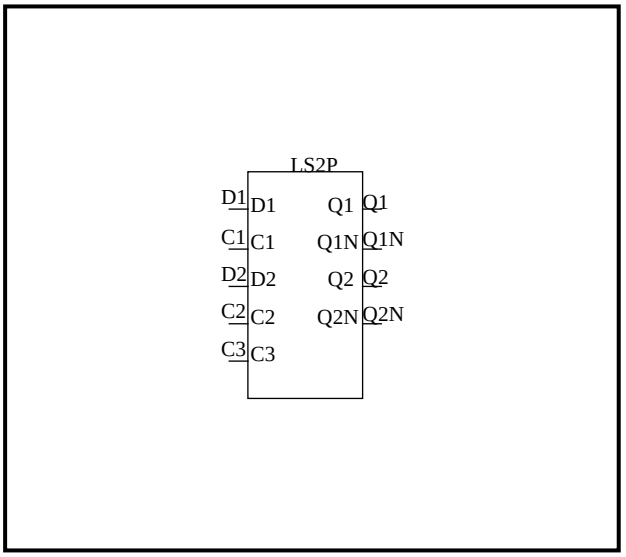
ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	1.000

LS2P	LS2P	1/27

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
LS2P	D-TYPE TRANSPARENT LATCH with SCAN TEST INPUT	13	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT					OUTPUT			
D1	C1	D2	C2	C3	Q1	Q1N	Q2	Q2N
L	H	X	L	-	L	H	-	-
H	H	X	L	-	H	L	-	-
X	L	L	H	-	L	H	-	-
X	L	H	H	-	H	L	-	-
X	L	X	L	-	HOLD	HOLD	-	-
H	H	X	H	-	H	L	-	-
X	H	H	H	-	H	L	-	-
L	H	L	H	-	L	H	-	-
-	-	-	-	H	-	-	Q1	Q1N
-	-	-	-	L	-	-	HOLD	HOLD

Verilog-HDL DESCRIPTION

```
LS2P  inst(Q1,Q1N,Q2,Q2N,D1,C1,D2,
C2,C3);
```

VHDL DESCRIPTION

```
inst:LS2P
   port   map(Q1,Q1N,Q2,Q2N,D1,
C1,D2,C2,C3);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q1,Q1N,Q2,Q2N
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D1	0.98
C1	2.00
D2	0.99
C2	1.97
C3	1.01

OUTPUT DRIVE (LU)

PIN NAME	Q1	Q1N	Q2	Q2N
DRIVE	73.2	88.8	97.9	74.4

Rev.1.01.10

LS2P | LS2P | 2/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q1	C2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0540	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.51	0.62	1.01
0.38	0.47	0.56	0.67	1.06
1.00	0.55	0.64	0.75	1.14
3.00	0.71	0.80	0.91	1.30

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q1	C2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0274	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.71	0.83	0.95	1.33
0.38	0.70	0.83	0.95	1.33
1.00	0.72	0.85	0.97	1.35
3.00	0.86	0.99	1.11	1.49

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q1	~C2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0540	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.57	0.68	1.07
0.38	0.55	0.64	0.75	1.14
1.00	0.63	0.72	0.83	1.22
3.00	0.81	0.90	1.01	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q1	~C2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0274	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.47	0.57	0.92
0.38	0.44	0.55	0.65	1.00
1.00	0.51	0.62	0.72	1.07
3.00	0.62	0.72	0.83	1.17

LS2P | LS2P | 3/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q1N	C2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0460	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.19	1.28	1.38	1.73
0.38	1.19	1.28	1.37	1.73
1.00	1.21	1.29	1.39	1.74
3.00	1.36	1.44	1.54	1.89

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q1N	C2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0200	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.83	0.94	1.04	1.34
0.38	0.88	0.99	1.09	1.39
1.00	0.96	1.07	1.17	1.47
3.00	1.13	1.24	1.34	1.64

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q1N	~C2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0460	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.77	0.86	0.95	1.31
0.38	0.85	0.94	1.03	1.39
1.00	0.92	1.01	1.10	1.46
3.00	1.02	1.10	1.20	1.56

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q1N	~C2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0200	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.89	1.00	1.10	1.40
0.38	0.96	1.07	1.16	1.47
1.00	1.04	1.15	1.24	1.55
3.00	1.23	1.34	1.44	1.74

Rev.1.01.10

LS2P | LS2P | 4/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q2	C2&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0441	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.17	1.24	1.32	1.63
0.38	1.22	1.29	1.37	1.69
1.00	1.30	1.37	1.45	1.77
3.00	1.47	1.54	1.62	1.94

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q2	C2&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0176	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.52	1.59	1.66	1.90
0.38	1.51	1.58	1.66	1.90
1.00	1.53	1.60	1.67	1.92
3.00	1.68	1.75	1.82	2.07

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q2	~C2&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0441	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.22	1.30	1.38	1.69
0.38	1.29	1.36	1.45	1.76
1.00	1.37	1.44	1.53	1.84
3.00	1.57	1.64	1.72	2.04

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q2	~C2&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0176	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.09	1.17	1.24	1.48
0.38	1.17	1.24	1.32	1.56
1.00	1.24	1.31	1.39	1.63
3.00	1.34	1.41	1.49	1.73

Rev.1.01.10

LS2P | LS2P | 5/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q2N	C2&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0542	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.29	1.38	1.49	1.87
0.38	1.28	1.37	1.48	1.87
1.00	1.30	1.39	1.50	1.89
3.00	1.45	1.54	1.65	2.04

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q2N	C2&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0264	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.92	1.03	1.15	1.50
0.38	0.97	1.09	1.20	1.55
1.00	1.05	1.16	1.28	1.63
3.00	1.22	1.34	1.45	1.80

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q2N	~C2&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0542	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.86	0.96	1.07	1.45
0.38	0.94	1.04	1.14	1.53
1.00	1.01	1.11	1.21	1.60
3.00	1.11	1.21	1.31	1.70

PATH CONDITION

PATH	CONDITION	FUNCTION
C1->Q2N	~C2&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0264	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.98	1.09	1.20	1.56
0.38	1.05	1.16	1.27	1.63
1.00	1.13	1.24	1.35	1.71
3.00	1.32	1.43	1.55	1.90

Rev.1.01.10

LS2P | LS2P | 6/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q2	C1&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0441	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.17	1.24	1.33	1.64
0.38	1.23	1.30	1.38	1.70
1.00	1.30	1.38	1.46	1.77
3.00	1.46	1.53	1.61	1.93

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q2	C1&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0176	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.44	1.51	1.59	1.83
0.38	1.45	1.52	1.60	1.84
1.00	1.52	1.59	1.67	1.91
3.00	1.79	1.87	1.94	2.18

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q2	~C1&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0441	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.23	1.30	1.39	1.70
0.38	1.30	1.38	1.46	1.77
1.00	1.37	1.45	1.53	1.84
3.00	1.54	1.61	1.70	2.01

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q2	~C1&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0176	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.09	1.17	1.24	1.48
0.38	1.17	1.24	1.32	1.56
1.00	1.23	1.30	1.37	1.62
3.00	1.29	1.37	1.44	1.68

LS2P | LS2P | 7/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q2N	C1&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0542	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.21	1.31	1.41	1.80
0.38	1.22	1.31	1.42	1.81
1.00	1.29	1.38	1.49	1.88
3.00	1.56	1.66	1.76	2.15

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q2N	C1&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0264	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.92	1.04	1.15	1.50
0.38	0.98	1.10	1.21	1.56
1.00	1.06	1.17	1.28	1.64
3.00	1.21	1.33	1.44	1.79

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q2N	~C1&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0542	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.86	0.96	1.07	1.45
0.38	0.94	1.04	1.14	1.53
1.00	1.00	1.10	1.20	1.59
3.00	1.06	1.16	1.26	1.65

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q2N	~C1&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0264	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.98	1.10	1.21	1.56
0.38	1.05	1.17	1.28	1.64
1.00	1.13	1.24	1.35	1.71
3.00	1.29	1.41	1.52	1.87

LS2P | LS2P | 8/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q1	C1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0540	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.51	0.62	1.01
0.38	0.47	0.57	0.68	1.07
1.00	0.55	0.65	0.75	1.14
3.00	0.69	0.79	0.89	1.29

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q1	C1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0274	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.64	0.77	0.89	1.27
0.38	0.66	0.78	0.90	1.28
1.00	0.73	0.85	0.97	1.35
3.00	0.99	1.12	1.24	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q1	~C1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0540	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.57	0.68	1.07
0.38	0.55	0.64	0.75	1.14
1.00	0.62	0.71	0.82	1.21
3.00	0.77	0.87	0.98	1.37

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q1	~C1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0274	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.46	0.57	0.92
0.38	0.43	0.54	0.65	1.00
1.00	0.49	0.60	0.71	1.06
3.00	0.56	0.67	0.77	1.12

LS2P | LS2P | 9/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q1N	C1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0460	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.12	1.21	1.31	1.66
0.38	1.14	1.23	1.32	1.68
1.00	1.21	1.30	1.39	1.75
3.00	1.48	1.57	1.67	2.02

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q1N	C1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0200	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.83	0.94	1.04	1.35
0.38	0.89	1.00	1.10	1.40
1.00	0.97	1.08	1.18	1.48
3.00	1.12	1.23	1.33	1.64

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q1N	~C1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0460	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.77	0.86	0.96	1.31
0.38	0.85	0.94	1.03	1.39
1.00	0.90	0.99	1.09	1.45
3.00	0.97	1.06	1.15	1.51

PATH CONDITION

PATH	CONDITION	FUNCTION
C2->Q1N	~C1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0200	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.89	1.00	1.10	1.41
0.38	0.96	1.07	1.17	1.48
1.00	1.03	1.15	1.24	1.55
3.00	1.20	1.31	1.41	1.72

LS2P | LS2P | 10/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C3->Q2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0441	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.54	0.61	0.70	1.01
0.38	0.61	0.69	0.77	1.09
1.00	0.68	0.75	0.84	1.15
3.00	0.80	0.88	0.96	1.28

PATH CONDITION

PATH	CONDITION	FUNCTION
C3->Q2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0176	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.61	0.68	0.75	0.99
0.38	0.68	0.75	0.83	1.07
1.00	0.74	0.82	0.89	1.13
3.00	0.85	0.92	0.99	1.23

PATH CONDITION

PATH	CONDITION	FUNCTION
C3->Q2N	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0542	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.40	0.49	0.59	0.98
0.38	0.47	0.56	0.67	1.05
1.00	0.53	0.62	0.73	1.11
3.00	0.64	0.73	0.83	1.22

PATH CONDITION

PATH	CONDITION	FUNCTION
C3->Q2N	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0264	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.44	0.54	0.87
0.38	0.41	0.51	0.61	0.94
1.00	0.48	0.57	0.68	1.01
3.00	0.60	0.70	0.80	1.13

LS2P | LS2P | 11/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q1	C1&C2&~D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0540	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.50	0.61	1.00
0.38	0.49	0.58	0.68	1.07
1.00	0.60	0.69	0.80	1.19
3.00	0.84	0.93	1.04	1.43

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q1	C1&C2&~D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0274	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.63	0.75	0.86	1.24
0.38	0.63	0.75	0.86	1.23
1.00	0.64	0.76	0.88	1.25
3.00	0.75	0.87	0.99	1.37

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q1	C1&~C2&D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0540	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.52	0.62	1.02
0.38	0.50	0.60	0.70	1.09
1.00	0.62	0.71	0.82	1.21
3.00	0.87	0.97	1.07	1.46

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q1	C1&~C2&D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0274	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.68	0.81	0.93	1.30
0.38	0.69	0.81	0.93	1.30
1.00	0.70	0.82	0.94	1.32
3.00	0.81	0.93	1.05	1.43

LS2P | LS2P | 12/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q1	C1&~C2&~D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0540	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.51	0.62	1.01
0.38	0.50	0.59	0.70	1.08
1.00	0.62	0.71	0.81	1.20
3.00	0.88	0.97	1.07	1.46

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q1	C1&~C2&~D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0274	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.63	0.74	1.09
0.38	0.52	0.63	0.74	1.10
1.00	0.56	0.67	0.78	1.14
3.00	0.68	0.79	0.91	1.27

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q1N	C1&C2&~D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0460	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.09	1.18	1.28	1.63
0.38	1.09	1.18	1.28	1.63
1.00	1.11	1.20	1.29	1.65
3.00	1.23	1.32	1.41	1.77

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q1N	C1&C2&~D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0200	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.82	0.93	1.03	1.33
0.38	0.89	1.00	1.10	1.40
1.00	1.01	1.12	1.22	1.52
3.00	1.26	1.37	1.47	1.77

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q1N	C1&~C2&D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0460	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.16	1.25	1.35	1.70
0.38	1.16	1.25	1.35	1.70
1.00	1.17	1.26	1.36	1.71
3.00	1.29	1.38	1.48	1.83

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q1N	C1&~C2&D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0200	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.84	0.95	1.05	1.35
0.38	0.91	1.02	1.12	1.43
1.00	1.03	1.14	1.24	1.54
3.00	1.30	1.41	1.50	1.81

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q1N	C1&~C2&~D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0460	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.94	1.03	1.13	1.48
0.38	0.95	1.04	1.14	1.49
1.00	0.99	1.07	1.17	1.53
3.00	1.13	1.22	1.31	1.67

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q1N	C1&~C2&~D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0200	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.83	0.94	1.04	1.34
0.38	0.91	1.02	1.11	1.42
1.00	1.03	1.14	1.23	1.54
3.00	1.29	1.40	1.50	1.80

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q2	C1&C2&~D2&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0441	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.15	1.23	1.31	1.62
0.38	1.23	1.30	1.39	1.70
1.00	1.35	1.42	1.50	1.82
3.00	1.60	1.67	1.75	2.07

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q2	C1&C2&~D2&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0176	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.41	1.49	1.56	1.80
0.38	1.41	1.49	1.56	1.80
1.00	1.43	1.50	1.58	1.82
3.00	1.55	1.62	1.70	1.94

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q2	C1&~C2&D2&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0441	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.18	1.25	1.33	1.64
0.38	1.25	1.32	1.41	1.72
1.00	1.37	1.44	1.53	1.84
3.00	1.63	1.71	1.79	2.10

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q2	C1&~C2&D2&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0176	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.48	1.56	1.63	1.87
0.38	1.48	1.56	1.63	1.87
1.00	1.50	1.57	1.64	1.88
3.00	1.61	1.69	1.76	2.00

LS2P | LS2P | 15/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q2	C1&~C2&~D2&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0441	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.16	1.24	1.32	1.63
0.38	1.24	1.32	1.40	1.71
1.00	1.36	1.43	1.52	1.83
3.00	1.63	1.70	1.79	2.10

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q2	C1&~C2&~D2&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0176	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.27	1.34	1.41	1.65
0.38	1.27	1.35	1.42	1.66
1.00	1.31	1.38	1.46	1.70
3.00	1.45	1.52	1.60	1.84

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q2N	C1&C2&~D2&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0542	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.19	1.28	1.39	1.78
0.38	1.18	1.28	1.39	1.77
1.00	1.20	1.30	1.40	1.79
3.00	1.32	1.42	1.52	1.91

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q2N	C1&C2&~D2&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0264	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.91	1.02	1.14	1.49
0.38	0.98	1.10	1.21	1.56
1.00	1.10	1.21	1.33	1.68
3.00	1.35	1.47	1.58	1.93

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q2N	C1&~C2&D2&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0542	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.25	1.35	1.45	1.84
0.38	1.25	1.35	1.45	1.84
1.00	1.27	1.36	1.47	1.86
3.00	1.38	1.48	1.58	1.97

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q2N	C1&~C2&D2&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0264	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.93	1.04	1.16	1.51
0.38	1.00	1.12	1.23	1.58
1.00	1.12	1.24	1.35	1.70
3.00	1.39	1.50	1.61	1.97

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q2N	C1&~C2&~D2&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0542	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.04	1.13	1.24	1.63
0.38	1.05	1.14	1.25	1.64
1.00	1.08	1.18	1.28	1.67
3.00	1.22	1.32	1.42	1.81

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Q2N	C1&~C2&~D2&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0264	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.92	1.03	1.15	1.50
0.38	1.00	1.11	1.22	1.58
1.00	1.12	1.23	1.34	1.70
3.00	1.38	1.50	1.61	1.96

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q1	C1&C2&~D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0540	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.40	0.50	0.60	1.00
0.38	0.48	0.58	0.68	1.08
1.00	0.59	0.68	0.79	1.18
3.00	0.79	0.89	0.99	1.39

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q1	C1&C2&~D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0274	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.59	0.71	0.82	1.19
0.38	0.60	0.72	0.84	1.21
1.00	0.67	0.79	0.91	1.28
3.00	0.91	1.03	1.15	1.52

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q1	~C1&C2&D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0540	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.51	0.62	1.02
0.38	0.50	0.60	0.70	1.10
1.00	0.61	0.70	0.81	1.20
3.00	0.82	0.92	1.03	1.42

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q1	~C1&C2&D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0274	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.66	0.79	0.91	1.29
0.38	0.68	0.80	0.92	1.30
1.00	0.74	0.87	0.99	1.37
3.00	0.99	1.12	1.24	1.62

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q1	~C1&C2&~D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0540	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.40	0.50	0.60	1.00
0.38	0.48	0.58	0.68	1.07
1.00	0.59	0.68	0.79	1.18
3.00	0.81	0.91	1.01	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q1	~C1&C2&~D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1	0.0274	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.60	0.71	1.07
0.38	0.51	0.63	0.74	1.09
1.00	0.58	0.70	0.81	1.16
3.00	0.79	0.91	1.02	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q1N	C1&C2&~D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0460	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.05	1.14	1.24	1.59
0.38	1.07	1.16	1.25	1.61
1.00	1.13	1.22	1.32	1.67
3.00	1.39	1.48	1.57	1.93

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q1N	C1&C2&~D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0200	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.82	0.93	1.03	1.33
0.38	0.90	1.01	1.11	1.41
1.00	1.01	1.12	1.21	1.52
3.00	1.22	1.33	1.43	1.74

LS2P | LS2P | 19/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q1N	~C1&C2&D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0460	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.15	1.24	1.33	1.69
0.38	1.16	1.25	1.35	1.70
1.00	1.23	1.32	1.41	1.77
3.00	1.49	1.58	1.67	2.03

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q1N	~C1&C2&D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0200	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.84	0.95	1.05	1.35
0.38	0.92	1.03	1.13	1.44
1.00	1.03	1.14	1.24	1.54
3.00	1.26	1.37	1.47	1.77

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q1N	~C1&C2&~D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0460	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.92	1.01	1.11	1.46
0.38	0.94	1.03	1.13	1.48
1.00	1.01	1.10	1.20	1.55
3.00	1.24	1.33	1.43	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q1N	~C1&C2&~D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q1N	0.0200	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.82	0.93	1.03	1.33
0.38	0.90	1.01	1.11	1.41
1.00	1.01	1.12	1.22	1.52
3.00	1.24	1.35	1.45	1.75

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q2	C2&C1&~D1&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0441	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.16	1.23	1.31	1.63
0.38	1.24	1.31	1.39	1.71
1.00	1.34	1.42	1.50	1.81
3.00	1.56	1.63	1.72	2.03

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q2	C2&C1&~D1&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0176	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.37	1.45	1.52	1.76
0.38	1.39	1.46	1.54	1.78
1.00	1.46	1.53	1.60	1.85
3.00	1.71	1.78	1.86	2.10

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q2	C2&~C1&D1&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0441	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.18	1.25	1.34	1.65
0.38	1.26	1.33	1.42	1.73
1.00	1.37	1.44	1.53	1.84
3.00	1.60	1.67	1.75	2.07

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q2	C2&~C1&D1&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0176	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.47	1.54	1.62	1.86
0.38	1.48	1.56	1.63	1.87
1.00	1.55	1.62	1.70	1.94
3.00	1.81	1.88	1.96	2.20

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q2	C2&~C1&~D1&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0441	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.16	1.23	1.31	1.63
0.38	1.24	1.31	1.39	1.71
1.00	1.35	1.42	1.50	1.81
3.00	1.58	1.65	1.74	2.05

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q2	C2&~C1&~D1&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2	0.0176	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.25	1.32	1.39	1.63
0.38	1.27	1.34	1.41	1.66
1.00	1.34	1.41	1.48	1.73
3.00	1.56	1.64	1.71	1.95

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q2N	C2&C1&~D1&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0542	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.14	1.24	1.34	1.73
0.38	1.16	1.25	1.36	1.75
1.00	1.23	1.32	1.43	1.82
3.00	1.48	1.58	1.68	2.07

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q2N	C2&C1&~D1&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0264	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.91	1.03	1.14	1.49
0.38	0.99	1.11	1.22	1.57
1.00	1.10	1.21	1.32	1.68
3.00	1.31	1.43	1.54	1.89

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q2N	C2&~C1&D1&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0542	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.24	1.33	1.44	1.83
0.38	1.25	1.35	1.46	1.84
1.00	1.32	1.41	1.52	1.91
3.00	1.58	1.67	1.78	2.17

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q2N	C2&~C1&D1&C3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0264	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.93	1.05	1.16	1.51
0.38	1.01	1.13	1.24	1.59
1.00	1.12	1.24	1.35	1.70
3.00	1.35	1.46	1.58	1.93

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q2N	C2&~C1&~D1&C3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0542	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.02	1.11	1.22	1.61
0.38	1.04	1.13	1.24	1.63
1.00	1.11	1.20	1.31	1.70
3.00	1.33	1.43	1.53	1.92

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Q2N	C2&~C1&~D1&C3	FALL

SLEW FACTOR

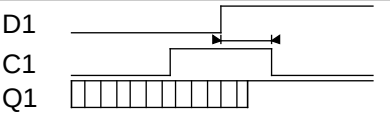
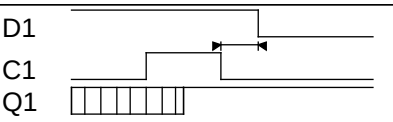
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q2N	0.0264	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.91	1.03	1.14	1.49
0.38	0.99	1.11	1.22	1.57
1.00	1.10	1.21	1.33	1.68
3.00	1.33	1.45	1.56	1.91

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D1	C1	~C2

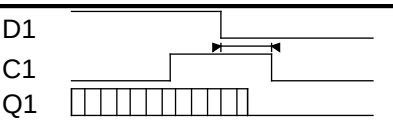
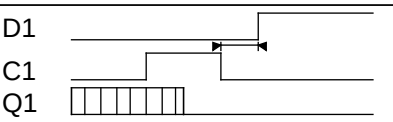
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.749	0.720	0.670	0.511
0.38	0.773	0.741	0.689	0.520
1.00	0.811	0.777	0.720	0.536
3.00	0.937	0.894	0.821	0.586

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.129	0.083	0.006	-0.243
0.38	0.071	0.026	-0.050	-0.294
1.00	-0.026	-0.070	-0.143	-0.380
3.00	-0.340	-0.379	-0.445	-0.657

TIMING CONDITION

DATA	CLOCK	CONDITION
D1	C1	~C2

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.732	0.763	0.816	0.985
0.38	0.792	0.823	0.874	1.041
1.00	0.893	0.923	0.973	1.134
3.00	1.218	1.245	1.290	1.436

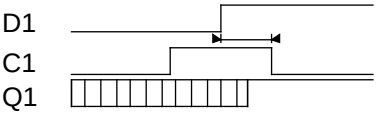
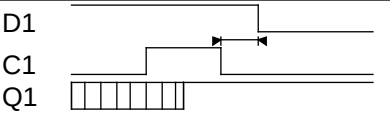
HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.207	0.237	0.286	0.446
0.38	0.188	0.221	0.276	0.454
1.00	0.156	0.195	0.259	0.468
3.00	0.053	0.110	0.206	0.515

LS2P	LS2P	24/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D1	C3	C1&~C2

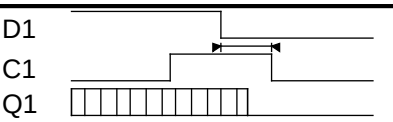
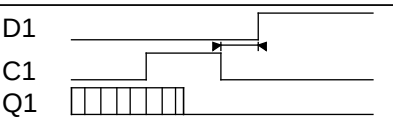
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	1.340	1.309	1.258	1.091
0.38	1.356	1.325	1.273	1.107
1.00	1.381	1.351	1.299	1.133
3.00	1.464	1.434	1.383	1.219

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.474	-0.456	-0.426	-0.330
0.38	-0.529	-0.512	-0.482	-0.386
1.00	-0.623	-0.605	-0.575	-0.479
3.00	-0.925	-0.907	-0.877	-0.780

TIMING CONDITION

DATA	CLOCK	CONDITION
D1	C3	C1&~C2

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	1.131	1.113	1.083	0.985
0.38	1.187	1.169	1.138	1.041
1.00	1.280	1.262	1.232	1.134
3.00	1.581	1.563	1.533	1.436

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.684	-0.653	-0.601	-0.433
0.38	-0.699	-0.668	-0.617	-0.450
1.00	-0.725	-0.694	-0.643	-0.477
3.00	-0.808	-0.778	-0.727	-0.564

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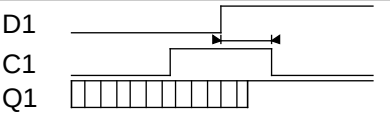
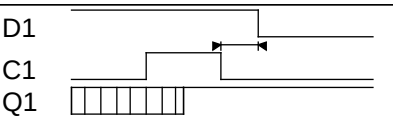
CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D2	C2	~C1

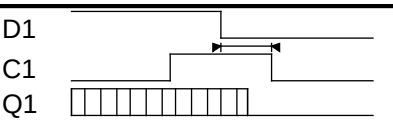
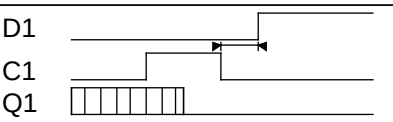
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.754	0.712	0.642	0.415
0.38	0.794	0.751	0.679	0.446
1.00	0.861	0.816	0.740	0.497
3.00	1.077	1.026	0.940	0.663

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.136	0.096	0.028	-0.189
0.38	0.084	0.045	-0.020	-0.231
1.00	-0.002	-0.039	-0.101	-0.301
3.00	-0.281	-0.311	-0.363	-0.528

TIMING CONDITION

DATA	CLOCK	CONDITION
D2	C2	~C1

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

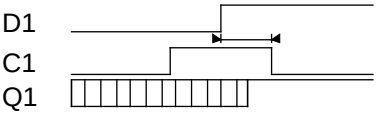
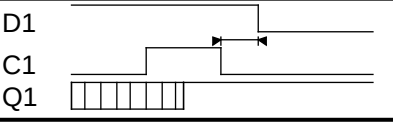
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.750	0.774	0.815	0.944
0.38	0.804	0.827	0.866	0.993
1.00	0.893	0.916	0.953	1.074
3.00	1.182	1.201	1.233	1.336

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.207	0.249	0.320	0.549
0.38	0.171	0.216	0.291	0.532
1.00	0.111	0.160	0.241	0.503
3.00	-0.082	-0.021	0.081	0.409

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D2	C3	C2&~C1

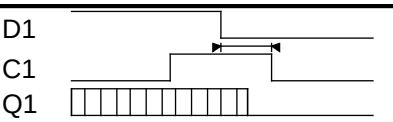
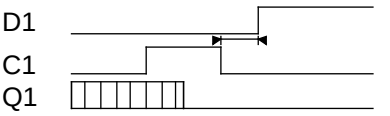
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	1.281	1.250	1.199	1.032
0.38	1.323	1.293	1.241	1.075
1.00	1.394	1.363	1.312	1.146
3.00	1.622	1.592	1.541	1.377

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.481	-0.463	-0.433	-0.335
0.38	-0.531	-0.513	-0.483	-0.385
1.00	-0.615	-0.596	-0.566	-0.469
3.00	-0.884	-0.866	-0.836	-0.739

TIMING CONDITION

DATA	CLOCK	CONDITION
D2	C3	C2&~C1

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	1.136	1.118	1.088	0.992
0.38	1.186	1.168	1.138	1.042
1.00	1.269	1.252	1.222	1.126
3.00	1.540	1.522	1.492	1.395

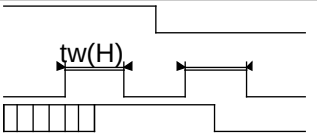
HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.627	-0.595	-0.543	-0.375
0.38	-0.669	-0.638	-0.585	-0.418
1.00	-0.739	-0.708	-0.656	-0.490
3.00	-0.966	-0.936	-0.885	-0.722

LS2P	LS2P	27/27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

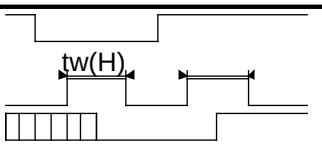
CLOCK	CONDITION
C1	---

ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	1.070

MINIMUM PULSE WIDTH CONDITION

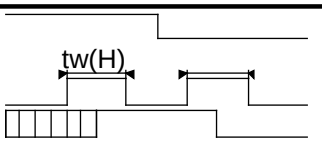
CLOCK	CONDITION
C3	---

ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
C2	---

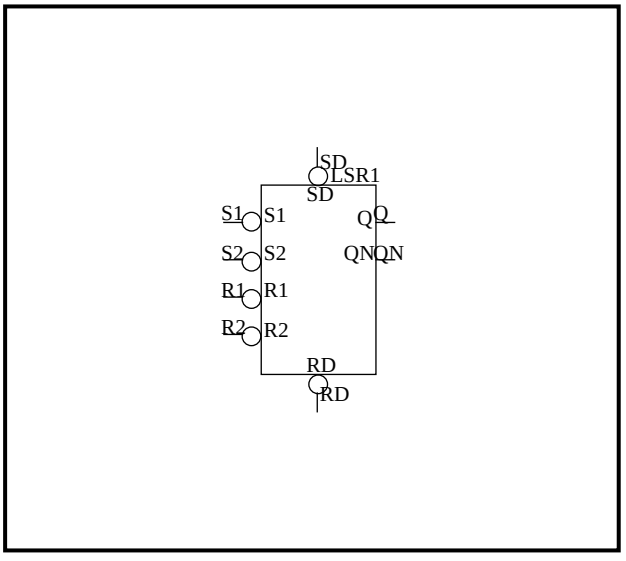
ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	1.100

LSR1	LSR1	1/6

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
LSR1	SR-LATCH with SEPARATE GATE SD and RD	4	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT	
SD	RD	S1+S2	R1+R2	Q	QN
L	H	X	H	H	L
H	L	H	X	L	H
H	H	L	H	H	L
H	H	H	L	L	H
H	H	H	H	HOLD	
ALL OTHER COMBINATIONS				H*	H*

*:Inhibit from changing directly to HOLD

Verilog-HDL DESCRIPTION

```
LSR1  inst(Q,QN,S1,S2,SD,R1,R2,RD);
```

VHDL DESCRIPTION

```
inst:LSR1
   port   map(Q,QN,S1,S2,SD,R1,
              R2,RD);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
S1	1.08
S2,R2	1.05
SD,RD	0.98
R1	0.99

OUTPUT DRIVE (LU)

PIN NAME	Q,QN
DRIVE	19.7

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LSR1 LSR1 2/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QN->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0837	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.44	0.68	1.61
0.38	0.30	0.49	0.72	1.65
1.00	0.35	0.55	0.79	1.72
3.00	0.48	0.72	0.98	1.95

PATH CONDITION

PATH	CONDITION	FUNCTION
R1->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.1784	0.44

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.50	0.81	2.05
0.38	0.27	0.52	0.83	2.07
1.00	0.31	0.57	0.88	2.11
3.00	0.39	0.70	1.03	2.28

PATH CONDITION

PATH	CONDITION	FUNCTION
QN->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0837	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.44	0.68	1.61
0.38	0.30	0.49	0.72	1.65
1.00	0.35	0.55	0.79	1.72
3.00	0.48	0.72	0.98	1.95

PATH CONDITION

PATH	CONDITION	FUNCTION
R2->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.1784	0.44

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.53	0.84	2.07
0.38	0.28	0.53	0.85	2.09
1.00	0.28	0.54	0.85	2.08
3.00	0.28	0.56	0.88	2.11

LSR1 LSR1 3/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QN->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0837	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.44	0.68	1.61
0.38	0.30	0.49	0.72	1.65
1.00	0.35	0.55	0.79	1.72
3.00	0.48	0.72	0.98	1.95

PATH CONDITION

PATH	CONDITION	FUNCTION
RD->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.1784	0.44

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.33	0.50	1.16
0.38	0.22	0.36	0.52	1.19
1.00	0.26	0.41	0.58	1.24
3.00	0.30	0.49	0.70	1.42

PATH CONDITION

PATH	CONDITION	FUNCTION
S1->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.1785	0.43

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.50	0.81	2.05
0.38	0.27	0.52	0.83	2.07
1.00	0.31	0.57	0.88	2.11
3.00	0.39	0.70	1.03	2.28

PATH CONDITION

PATH	CONDITION	FUNCTION
Q->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0837	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.44	0.68	1.61
0.38	0.30	0.49	0.72	1.65
1.00	0.35	0.55	0.79	1.72
3.00	0.48	0.72	0.98	1.95

LSR1 LSR1 4/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
S2->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.1785	0.43

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.53	0.83	2.07
0.38	0.28	0.53	0.84	2.08
1.00	0.28	0.53	0.85	2.08
3.00	0.27	0.55	0.88	2.11

PATH CONDITION

PATH	CONDITION	FUNCTION
Q->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0837	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.44	0.68	1.61
0.38	0.30	0.49	0.72	1.65
1.00	0.35	0.55	0.79	1.72
3.00	0.48	0.72	0.98	1.95

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.1785	0.43

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.33	0.50	1.16
0.38	0.22	0.36	0.52	1.19
1.00	0.26	0.41	0.58	1.24
3.00	0.30	0.49	0.70	1.42

PATH CONDITION

PATH	CONDITION	FUNCTION
Q->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0837	0.29

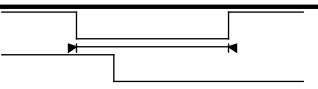
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.44	0.68	1.61
0.38	0.30	0.49	0.72	1.65
1.00	0.35	0.55	0.79	1.72
3.00	0.48	0.72	0.98	1.95

LSR1	LSR1	5/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

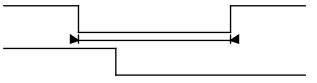
CLOCK	CONDITION
R1	RD&SD&(S1 S2)&~R2

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.710

MINIMUM PULSE WIDTH CONDITION

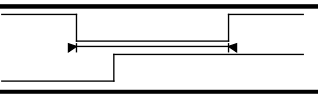
CLOCK	CONDITION
R2	RD&SD&(S1 S2)&~R1

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.690

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
S1	RD&SD&(R1 R2)&~S2

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.710

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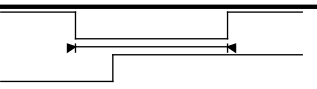
CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
S2	RD&SD&(R1 R2)&~S1

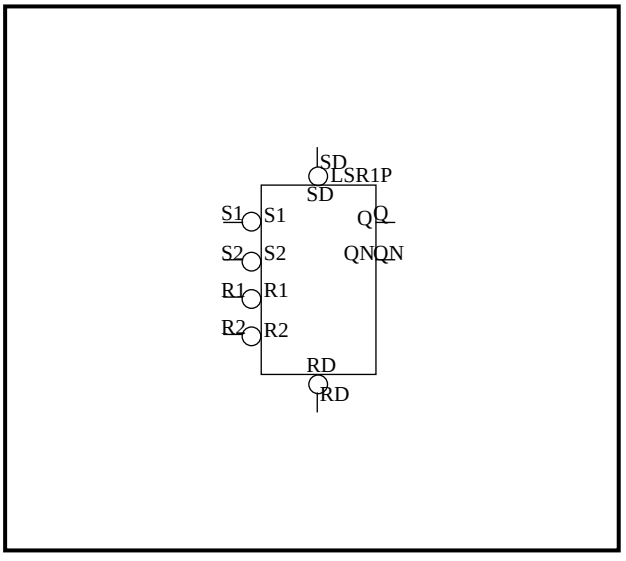
ITEM	WAVE_FORM
NEGLIMIT	S1 Q 

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.690

LSR1P	LSR1P	1/6

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
LSR1P	SR-LATCH with SEPARATE GATE SD and RD	8	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT	
SD	RD	S1+S2	R1+R2	Q	QN
L	H	X	H	H	L
H	L	H	X	L	H
H	H	L	H	H	L
H	H	H	L	L	H
H	H	H	H	HOLD	
ALL OTHER COMBINATIONS				H*	H*

*:Inhibit from changing directly to HOLD

Verilog-HDL DESCRIPTION

```
LSR1P  inst(Q,QN,S1,S2,SD,R1,R2,RD);
```

VHDL DESCRIPTION

```
inst:LSR1P
   port   map(Q,QN,S1,S2,SD,R1,
              R2,RD);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
S1,R1	2.02
S2,R2	2.20
SD,RD	2.11

OUTPUT DRIVE (LU)

PIN NAME	Q,QN
DRIVE	42.4

Rev.1.01.10

LSR1P | LSR1P | 2/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QN->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0384	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.31	0.42	0.85
0.38	0.26	0.35	0.46	0.90
1.00	0.31	0.41	0.52	0.96
3.00	0.42	0.54	0.67	1.16

PATH CONDITION

PATH	CONDITION	FUNCTION
R1->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0874	0.45

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.35	0.50	1.11
0.38	0.24	0.37	0.52	1.13
1.00	0.28	0.41	0.57	1.18
3.00	0.37	0.53	0.71	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION
QN->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0384	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.31	0.42	0.85
0.38	0.26	0.35	0.46	0.90
1.00	0.31	0.41	0.52	0.96
3.00	0.42	0.54	0.67	1.16

PATH CONDITION

PATH	CONDITION	FUNCTION
R2->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0874	0.45

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.38	0.53	1.14
0.38	0.25	0.38	0.53	1.15
1.00	0.25	0.38	0.54	1.15
3.00	0.25	0.40	0.57	1.19

LSR1P | LSR1P | 3/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QN->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0384	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.31	0.42	0.85
0.38	0.26	0.35	0.46	0.90
1.00	0.31	0.41	0.52	0.96
3.00	0.42	0.54	0.67	1.16

PATH CONDITION

PATH	CONDITION	FUNCTION
RD->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0874	0.45

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.25	0.33	0.67
0.38	0.21	0.28	0.36	0.69
1.00	0.24	0.32	0.41	0.75
3.00	0.29	0.39	0.51	0.90

PATH CONDITION

PATH	CONDITION	FUNCTION
S1->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0874	0.45

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.35	0.50	1.11
0.38	0.24	0.37	0.52	1.13
1.00	0.28	0.41	0.57	1.18
3.00	0.37	0.53	0.71	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION
Q->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0384	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.31	0.42	0.85
0.38	0.26	0.35	0.46	0.90
1.00	0.31	0.41	0.52	0.96
3.00	0.42	0.54	0.67	1.16

LSR1P | LSR1P | 4/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
S2->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0874	0.45

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.38	0.53	1.14
0.38	0.25	0.38	0.53	1.15
1.00	0.25	0.38	0.54	1.15
3.00	0.25	0.40	0.57	1.19

PATH CONDITION

PATH	CONDITION	FUNCTION
Q->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0384	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.31	0.42	0.85
0.38	0.26	0.35	0.46	0.90
1.00	0.31	0.41	0.52	0.96
3.00	0.42	0.54	0.67	1.16

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0874	0.45

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.25	0.33	0.67
0.38	0.21	0.28	0.36	0.69
1.00	0.24	0.32	0.41	0.75
3.00	0.29	0.39	0.51	0.90

PATH CONDITION

PATH	CONDITION	FUNCTION
Q->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0384	0.29

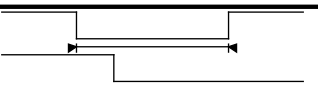
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.31	0.42	0.85
0.38	0.26	0.35	0.46	0.90
1.00	0.31	0.41	0.52	0.96
3.00	0.42	0.54	0.67	1.16

LSR1P	LSR1P	5/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

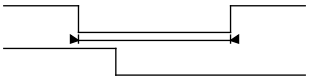
CLOCK	CONDITION
R1	RD&SD&(S1 S2)&~R2

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.710

MINIMUM PULSE WIDTH CONDITION

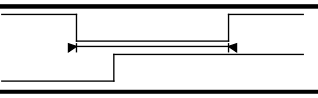
CLOCK	CONDITION
R2	RD&SD&(S1 S2)&~R1

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.690

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
S1	RD&SD&(R1 R2)&~S2

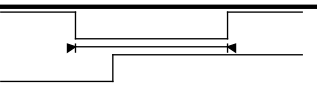
ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.710

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
S2	RD&SD&(R1 R2)&~S1

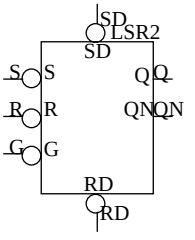
ITEM	WAVE_FORM
NEGLIMIT	S1  Q

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.690

LSR2	LSR2	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
LSR2	SR-LATCH with COMMON GATE SD and RD	4	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT	
SD	RD	G+S	G+R	Q	QN
L	H	X	H	H	L
H	L	H	X	L	H
H	H	L	H	H	L
H	H	H	L	L	H
H	H	H	H	HOLD	
ALL OTHER COMBINATIONS				H*	H*

*:Inhibit from changing directly to HOLD

Verilog-HDL DESCRIPTION

```
LSR2 inst(Q,QN,S,R,G,SD,RD);
```

VHDL DESCRIPTION

```
inst:LSR2
  port map(Q,QN,S,R,G,SD,RD);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
S	1.02
R	1.03
G	2.11
SD	1.06
RD	0.99

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	18.3	18.2

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LSR2 LSR2 2/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.1784	0.44

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.51	0.82	2.05
0.38	0.27	0.53	0.84	2.08
1.00	0.31	0.57	0.88	2.11
3.00	0.40	0.70	1.03	2.28

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.1003	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.44	0.72	1.80
0.38	0.29	0.52	0.80	1.89
1.00	0.38	0.64	0.94	2.04
3.00	0.55	0.90	1.26	2.47

PATH CONDITION

PATH	CONDITION	FUNCTION
G->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.1784	0.44

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.50	0.81	2.05
0.38	0.27	0.52	0.84	2.07
1.00	0.31	0.57	0.88	2.11
3.00	0.40	0.70	1.03	2.28

PATH CONDITION

PATH	CONDITION	FUNCTION
G->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.1003	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.44	0.71	1.80
0.38	0.29	0.52	0.80	1.89
1.00	0.38	0.64	0.94	2.04
3.00	0.55	0.90	1.26	2.47

LSR2 LSR2 3/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QN->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.1003	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.44	0.68	1.61
0.38	0.30	0.49	0.72	1.66
1.00	0.35	0.55	0.79	1.72
3.00	0.47	0.71	0.98	1.94

PATH CONDITION

PATH	CONDITION	FUNCTION
R->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.1784	0.44

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.53	0.84	2.07
0.38	0.28	0.54	0.85	2.09
1.00	0.28	0.54	0.85	2.08
3.00	0.28	0.56	0.88	2.11

PATH CONDITION

PATH	CONDITION	FUNCTION
QN->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.1003	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.44	0.68	1.61
0.38	0.30	0.49	0.72	1.66
1.00	0.35	0.55	0.79	1.72
3.00	0.47	0.71	0.98	1.94

PATH CONDITION

PATH	CONDITION	FUNCTION
RD->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.1784	0.44

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.34	0.51	1.20
0.38	0.23	0.37	0.54	1.22
1.00	0.25	0.41	0.59	1.28
3.00	0.28	0.48	0.70	1.45

LSR2 LSR2 4/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.1784	0.44

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.53	0.84	2.07
0.38	0.28	0.53	0.84	2.09
1.00	0.28	0.53	0.85	2.08
3.00	0.28	0.56	0.88	2.11

PATH CONDITION

PATH	CONDITION	FUNCTION
Q->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.1003	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.44	0.68	1.61
0.38	0.30	0.49	0.72	1.65
1.00	0.35	0.55	0.79	1.72
3.00	0.47	0.71	0.97	1.94

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.1784	0.44

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.34	0.51	1.20
0.38	0.23	0.37	0.54	1.22
1.00	0.26	0.41	0.59	1.28
3.00	0.28	0.48	0.70	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
Q->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.1003	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.44	0.68	1.61
0.38	0.30	0.49	0.72	1.65
1.00	0.35	0.55	0.79	1.72
3.00	0.47	0.71	0.97	1.94

LSR2	LSR2	5/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

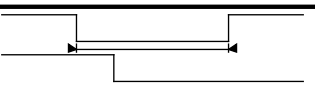
CLOCK	CONDITION
G	RD&SD

ITEM	WAVE_FORM
NEGLIMIT	G  tw(L)

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.730

MINIMUM PULSE WIDTH CONDITION

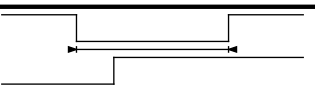
CLOCK	CONDITION
R	RD&SD&S&~G

ITEM	WAVE_FORM
NEGLIMIT	R  Q

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.720

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
S	RD&SD&R&~G

ITEM	WAVE_FORM
NEGLIMIT	S  Q

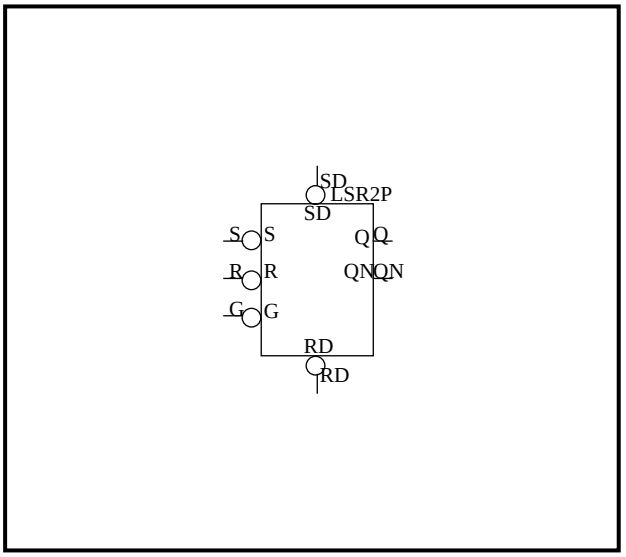
NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.720

Rev.1.01.10

LSR2P	LSR2P	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
LSR2P	SR-LATCH with COMMON GATE SD and RD	8	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT	
SD	RD	G+S	G+R	Q	QN
L	H	X	H	H	L
H	L	H	X	L	H
H	H	L	H	H	L
H	H	H	L	L	H
H	H	H	H	HOLD	
ALL OTHER COMBINATIONS				H*	H*

*:Inhibit from changing directly to HOLD

Verilog-HDL DESCRIPTION

```
LSR2P  inst(Q,QN,S,R,G,SD,RD);
```

VHDL DESCRIPTION

```
inst:LSR2P
   port   map(Q,QN,S,R,G,SD,RD);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
S,R	2.02
G	4.53
SD,RD	2.12

OUTPUT DRIVE (LU)

PIN NAME	Q,QN
DRIVE	38.4

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LSR2P | LSR2P | 2/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0874	0.45

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.35	0.51	1.12
0.38	0.25	0.37	0.53	1.14
1.00	0.29	0.42	0.58	1.18
3.00	0.37	0.53	0.71	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0468	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.29	0.42	0.94
0.38	0.26	0.37	0.50	1.03
1.00	0.34	0.48	0.62	1.17
3.00	0.48	0.67	0.87	1.53

PATH CONDITION

PATH	CONDITION	FUNCTION
G->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0875	0.45

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.35	0.51	1.12
0.38	0.25	0.37	0.53	1.14
1.00	0.29	0.42	0.58	1.18
3.00	0.37	0.53	0.71	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION
G->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0468	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.29	0.42	0.94
0.38	0.26	0.37	0.50	1.03
1.00	0.34	0.48	0.62	1.17
3.00	0.48	0.67	0.87	1.53

LSR2P | LSR2P | 3/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QN->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0468	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.31	0.42	0.85
0.38	0.26	0.35	0.46	0.90
1.00	0.31	0.41	0.52	0.96
3.00	0.42	0.54	0.68	1.16

PATH CONDITION

PATH	CONDITION	FUNCTION
R->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0875	0.45

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.37	0.53	1.14
0.38	0.25	0.38	0.53	1.15
1.00	0.25	0.38	0.54	1.15
3.00	0.25	0.40	0.57	1.19

PATH CONDITION

PATH	CONDITION	FUNCTION
QN->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0468	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.31	0.42	0.85
0.38	0.26	0.35	0.46	0.90
1.00	0.31	0.41	0.52	0.96
3.00	0.42	0.54	0.68	1.16

PATH CONDITION

PATH	CONDITION	FUNCTION
RD->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0875	0.45

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.25	0.33	0.67
0.38	0.21	0.28	0.36	0.69
1.00	0.24	0.31	0.41	0.75
3.00	0.27	0.37	0.49	0.88

LSR2P | LSR2P | 4/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0874	0.45

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.37	0.53	1.14
0.38	0.25	0.38	0.53	1.15
1.00	0.25	0.38	0.54	1.15
3.00	0.25	0.40	0.57	1.19

PATH CONDITION

PATH	CONDITION	FUNCTION
Q->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0468	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.31	0.42	0.85
0.38	0.26	0.35	0.46	0.90
1.00	0.31	0.41	0.52	0.96
3.00	0.42	0.54	0.67	1.16

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0874	0.45

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.25	0.33	0.67
0.38	0.21	0.28	0.36	0.69
1.00	0.24	0.31	0.41	0.75
3.00	0.27	0.37	0.49	0.88

PATH CONDITION

PATH	CONDITION	FUNCTION
Q->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0468	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.31	0.42	0.85
0.38	0.26	0.35	0.46	0.90
1.00	0.31	0.41	0.52	0.96
3.00	0.42	0.54	0.67	1.16

LSR2P	LSR2P	5/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

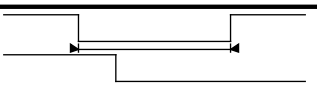
CLOCK	CONDITION
G	RD&SD

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.730

MINIMUM PULSE WIDTH CONDITION

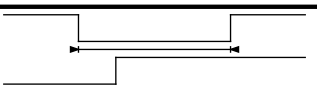
CLOCK	CONDITION
R	RD&SD&S&~G

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.720

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
S	RD&SD&R&~G

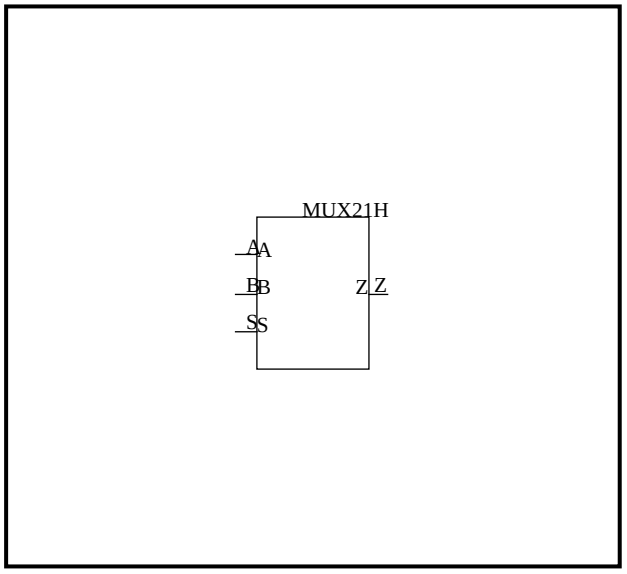
ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.720

MUX21H	MUX21H	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
MUX21H	2 TO 1 MULTIPLEXER	4	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
S	A	B	Z
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

Verilog-HDL DESCRIPTION

```
MUX21H  inst(Z,A,B,S);
```

VHDL DESCRIPTION

```
inst:MUX21H
   port   map(Z,A,B,S);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A,B	0.99
S	1.98

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	64.4

Rev.1.01.10

MUX21H | MUX21H | 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0545	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.29	0.39	0.76
0.38	0.28	0.37	0.46	0.84
1.00	0.35	0.44	0.54	0.91
3.00	0.47	0.57	0.67	1.05

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0395	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.44	0.57	1.05
0.38	0.34	0.47	0.61	1.09
1.00	0.42	0.55	0.68	1.16
3.00	0.58	0.71	0.85	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0545	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.29	0.39	0.77
0.38	0.28	0.37	0.47	0.84
1.00	0.35	0.44	0.55	0.92
3.00	0.48	0.57	0.68	1.06

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0395	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.46	0.60	1.08
0.38	0.37	0.50	0.63	1.12
1.00	0.44	0.57	0.71	1.19
3.00	0.61	0.74	0.88	1.37

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MUX21H | MUX21H | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z	~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0545	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.34	0.44	0.81
0.38	0.29	0.38	0.47	0.85
1.00	0.35	0.44	0.54	0.91
3.00	0.49	0.58	0.67	1.05

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z	~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0395	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.38	0.52	1.00
0.38	0.33	0.46	0.59	1.08
1.00	0.44	0.56	0.70	1.18
3.00	0.53	0.66	0.79	1.27

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z	A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0545	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.25	0.35	0.72
0.38	0.24	0.33	0.43	0.80
1.00	0.30	0.39	0.49	0.87
3.00	0.41	0.50	0.61	0.99

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z	A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0395	0.13

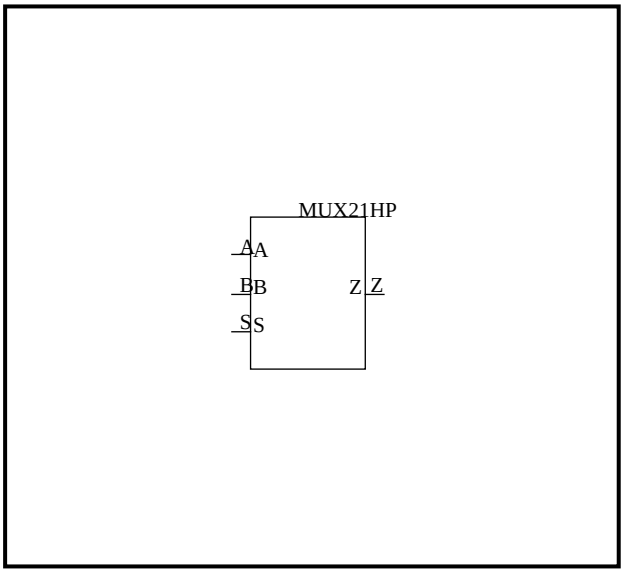
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.38	0.52	0.99
0.38	0.29	0.41	0.55	1.02
1.00	0.35	0.48	0.61	1.09
3.00	0.51	0.64	0.78	1.26

Rev.1.01.10

MUX21HP	MUX21HP	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
MUX21HP	2 TO 1 MULTIPLEXER	5	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
S	A	B	Z
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

Verilog-HDL DESCRIPTION

```
MUX21HP  inst(Z,A,B,S);
```

VHDL DESCRIPTION

```
inst:MUX21HP
   port   map(Z,A,B,S);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A,B	0.99
S	1.98

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	117.5

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0266	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.29	0.35	0.56
0.38	0.32	0.37	0.43	0.63
1.00	0.40	0.46	0.52	0.72
3.00	0.57	0.62	0.68	0.89

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0245	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.38	0.47	0.56	0.88
0.38	0.42	0.50	0.59	0.91
1.00	0.49	0.58	0.67	0.99
3.00	0.68	0.77	0.86	1.17

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0266	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.28	0.34	0.55
0.38	0.31	0.36	0.42	0.62
1.00	0.39	0.44	0.50	0.71
3.00	0.54	0.59	0.65	0.86

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0245	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.39	0.48	0.57	0.89
0.38	0.43	0.51	0.61	0.92
1.00	0.50	0.59	0.68	1.00
3.00	0.70	0.78	0.88	1.19

MUX21HP | MUX21HP | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z	~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0266	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.33	0.39	0.59
0.38	0.31	0.37	0.43	0.63
1.00	0.38	0.43	0.49	0.69
3.00	0.52	0.57	0.63	0.83

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z	~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0245	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.39	0.48	0.80
0.38	0.37	0.46	0.55	0.87
1.00	0.51	0.60	0.69	1.00
3.00	0.64	0.72	0.81	1.12

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z	A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0266	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.24	0.30	0.50
0.38	0.27	0.32	0.38	0.58
1.00	0.35	0.41	0.47	0.67
3.00	0.50	0.56	0.62	0.83

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z	A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0245	0.17

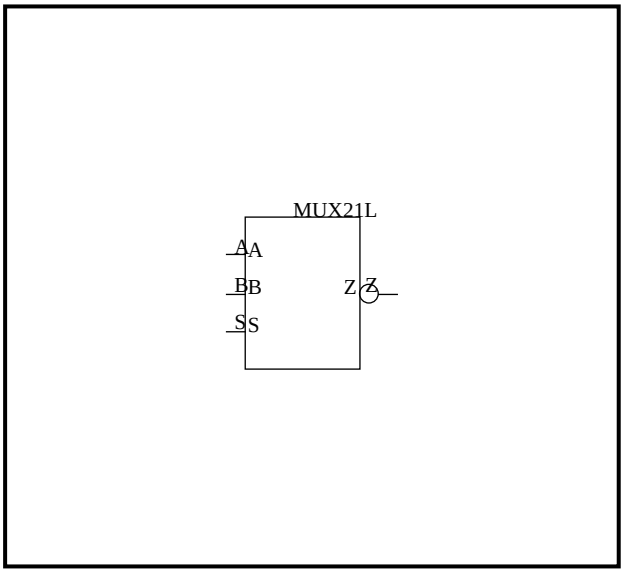
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.40	0.49	0.81
0.38	0.34	0.43	0.52	0.83
1.00	0.41	0.49	0.59	0.90
3.00	0.58	0.66	0.76	1.07

Rev.1.01.10

MUX21L	MUX21L	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
MUX21L	2 TO 1 INVERTING MULTIPLEXER	3	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
S	A	B	Z
L	L	X	H
L	H	X	L
H	X	L	H
H	X	H	L

Verilog-HDL DESCRIPTION

```
MUX21L  inst(Z,A,B,S);
```

VHDL DESCRIPTION

```
inst:MUX21L
   port   map(Z,A,B,S);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	3.85
B	3.84
S	2.00

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	67.2

Rev.1.01.10

MUX21L | MUX21L | 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0471	0.06

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.18	0.27	0.59
0.38	0.11	0.19	0.28	0.61
1.00	0.10	0.20	0.31	0.66
3.00	0.04	0.18	0.32	0.75

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0347	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.21	0.32	0.73
0.38	0.17	0.28	0.39	0.81
1.00	0.24	0.38	0.51	0.95
3.00	0.38	0.58	0.77	1.33

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0471	0.06

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.17	0.26	0.58
0.38	0.11	0.19	0.27	0.60
1.00	0.10	0.20	0.30	0.65
3.00	0.04	0.18	0.32	0.75

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0347	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.23	0.34	0.75
0.38	0.18	0.29	0.40	0.82
1.00	0.24	0.38	0.52	0.95
3.00	0.38	0.58	0.77	1.34

MUX21L | MUX21L | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z	~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0471	0.06

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.18	0.27	0.59
0.38	0.18	0.25	0.33	0.66
1.00	0.23	0.30	0.39	0.72
3.00	0.30	0.38	0.47	0.81

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z	~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0347	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.29	0.40	0.81
0.38	0.23	0.32	0.43	0.84
1.00	0.29	0.39	0.49	0.90
3.00	0.42	0.53	0.64	1.05

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z	A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0471	0.06

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.28	0.37	0.70
0.38	0.25	0.32	0.40	0.73
1.00	0.31	0.38	0.46	0.79
3.00	0.43	0.50	0.58	0.91

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z	A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0347	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.28	0.39	0.80
0.38	0.27	0.37	0.48	0.89
1.00	0.35	0.45	0.56	0.97
3.00	0.46	0.56	0.67	1.08

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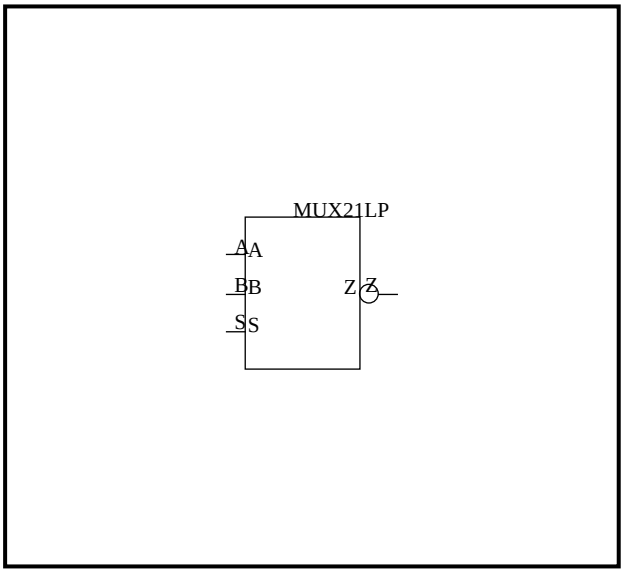
MUX21LP	MUX21LP	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
MUX21LP	2 TO 1 INVERTING MULTIPLEXER	4	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
S	A	B	Z
L	L	X	H
L	H	X	L
H	X	L	H
H	X	H	L

Verilog-HDL DESCRIPTION

```
MUX21LP  inst(Z,A,B,S);
```

VHDL DESCRIPTION

```
inst:MUX21LP
   port   map(Z,A,B,S);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	5.25
B	5.24
S	2.00

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	112.2

Rev.1.01.10

MUX21LP | MUX21LP | 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0224	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.16	0.21	0.37
0.38	0.12	0.17	0.22	0.38
1.00	0.11	0.17	0.22	0.41
3.00	0.02	0.10	0.19	0.44

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0185	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.19	0.26	0.49
0.38	0.18	0.25	0.32	0.55
1.00	0.24	0.33	0.41	0.68
3.00	0.40	0.51	0.63	0.99

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0224	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.15	0.19	0.36
0.38	0.12	0.16	0.21	0.37
1.00	0.10	0.16	0.22	0.41
3.00	0.02	0.10	0.18	0.44

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0185	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.21	0.28	0.51
0.38	0.19	0.26	0.33	0.56
1.00	0.25	0.33	0.42	0.68
3.00	0.39	0.51	0.63	0.99

MUX21LP | MUX21LP | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z	~A&B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0224	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.16	0.21	0.37
0.38	0.20	0.24	0.29	0.45
1.00	0.27	0.31	0.36	0.52
3.00	0.37	0.42	0.47	0.65

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z	~A&B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0185	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.28	0.35	0.58
0.38	0.25	0.32	0.38	0.61
1.00	0.32	0.38	0.45	0.68
3.00	0.47	0.54	0.61	0.85

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z	A&~B	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0224	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.26	0.31	0.47
0.38	0.26	0.30	0.35	0.51
1.00	0.32	0.36	0.41	0.57
3.00	0.44	0.49	0.53	0.70

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z	A&~B	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0185	0.10

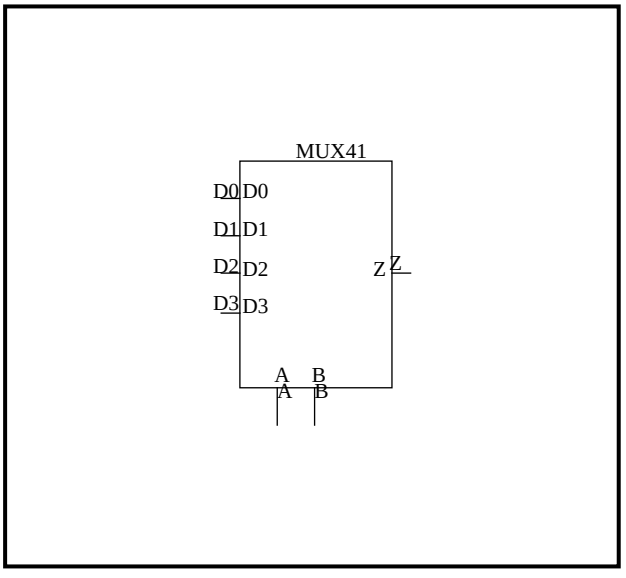
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.25	0.32	0.55
0.38	0.28	0.34	0.41	0.65
1.00	0.39	0.45	0.52	0.75
3.00	0.50	0.57	0.63	0.87

Rev.1.01.10

MUX41	MUX41	1/7

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
MUX41	4 TO 1 MULTIPLEXER	6	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
B	A	Z
L	L	D0
L	H	D1
H	L	D2
H	H	D3

Verilog-HDL DESCRIPTION

```
MUX41  inst(Z,D0,D1,D2,D3,A,B);
```

VHDL DESCRIPTION

```
inst:MUX41
   port   map(Z,D0,D1,D2,D3,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D0	3.50
D1	3.58
D2	3.35
D3	3.41
A	3.08
B	2.06

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	42.2

Rev.1.01.10

MUX41 MUX41 2/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~D2&D3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0999	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.39	0.55	0.73	1.41
0.38	0.43	0.58	0.76	1.45
1.00	0.48	0.64	0.81	1.50
3.00	0.60	0.76	0.94	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~D2&D3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0425	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.39	0.53	0.67	1.19
0.38	0.45	0.59	0.74	1.25
1.00	0.50	0.64	0.79	1.30
3.00	0.59	0.73	0.88	1.39

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&D2&~D3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0999	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.56	0.74	1.43
0.38	0.50	0.66	0.83	1.52
1.00	0.60	0.75	0.93	1.62
3.00	0.72	0.88	1.06	1.74

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&D2&~D3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0425	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.67	0.81	1.32
0.38	0.56	0.70	0.84	1.35
1.00	0.63	0.77	0.91	1.42
3.00	0.77	0.91	1.05	1.56

MUX41 MUX41 3/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&~D0&D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0999	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.40	0.55	0.73	1.41
0.38	0.43	0.58	0.76	1.44
1.00	0.49	0.64	0.81	1.50
3.00	0.61	0.76	0.94	1.63

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&~D0&D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0425	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.38	0.52	0.66	1.17
0.38	0.45	0.58	0.73	1.24
1.00	0.50	0.64	0.78	1.29
3.00	0.59	0.73	0.88	1.39

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&D0&~D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0999	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.56	0.74	1.42
0.38	0.50	0.65	0.83	1.52
1.00	0.60	0.75	0.93	1.61
3.00	0.73	0.88	1.06	1.74

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&D0&~D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0425	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.66	0.80	1.31
0.38	0.55	0.69	0.83	1.34
1.00	0.62	0.76	0.90	1.41
3.00	0.76	0.90	1.04	1.55

MUX41 MUX41 4/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~D1&D3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0999	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.45	0.63	1.32
0.38	0.33	0.48	0.66	1.35
1.00	0.39	0.54	0.72	1.40
3.00	0.52	0.67	0.84	1.52

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~D1&D3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0425	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.37	0.51	1.02
0.38	0.31	0.45	0.59	1.10
1.00	0.42	0.55	0.69	1.20
3.00	0.53	0.66	0.80	1.31

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&D1&~D3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0999	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.35	0.52	1.21
0.38	0.28	0.43	0.60	1.29
1.00	0.35	0.50	0.67	1.36
3.00	0.47	0.62	0.80	1.48

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&D1&~D3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0425	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.37	0.51	1.01
0.38	0.27	0.40	0.54	1.04
1.00	0.33	0.46	0.60	1.11
3.00	0.47	0.61	0.75	1.26

MUX41 MUX41 5/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&~D0&D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0999	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.45	0.63	1.32
0.38	0.33	0.48	0.66	1.35
1.00	0.39	0.54	0.72	1.40
3.00	0.52	0.67	0.84	1.52

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&~D0&D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0425	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.37	0.51	1.02
0.38	0.31	0.45	0.59	1.10
1.00	0.42	0.55	0.69	1.20
3.00	0.53	0.66	0.80	1.31

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&D0&~D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0999	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.35	0.52	1.21
0.38	0.28	0.43	0.60	1.29
1.00	0.35	0.50	0.67	1.36
3.00	0.47	0.62	0.80	1.48

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&D0&~D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0425	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.37	0.51	1.01
0.38	0.27	0.40	0.54	1.04
1.00	0.33	0.46	0.60	1.11
3.00	0.47	0.61	0.75	1.26

MUX41 MUX41 6/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D0->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0999	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.47	0.65	1.34
0.38	0.39	0.54	0.71	1.40
1.00	0.46	0.61	0.79	1.48
3.00	0.61	0.76	0.94	1.63

PATH CONDITION

PATH	CONDITION	FUNCTION
D0->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0425	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.50	0.64	1.15
0.38	0.38	0.52	0.66	1.17
1.00	0.44	0.58	0.73	1.24
3.00	0.59	0.74	0.89	1.41

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0999	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.49	0.66	1.35
0.38	0.39	0.54	0.72	1.41
1.00	0.47	0.62	0.80	1.48
3.00	0.61	0.76	0.94	1.63

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0425	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.49	0.64	1.14
0.38	0.38	0.52	0.66	1.17
1.00	0.44	0.58	0.73	1.24
3.00	0.59	0.74	0.89	1.41

MUX41 MUX41 7/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0999	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.48	0.65	1.34
0.38	0.39	0.54	0.72	1.41
1.00	0.46	0.62	0.80	1.49
3.00	0.61	0.76	0.94	1.64

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0425	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.50	0.65	1.16
0.38	0.38	0.52	0.67	1.18
1.00	0.45	0.59	0.73	1.25
3.00	0.59	0.74	0.89	1.42

PATH CONDITION

PATH	CONDITION	FUNCTION
D3->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0999	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.49	0.66	1.35
0.38	0.39	0.54	0.72	1.41
1.00	0.47	0.62	0.80	1.49
3.00	0.61	0.76	0.94	1.64

PATH CONDITION

PATH	CONDITION	FUNCTION
D3->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0425	0.13

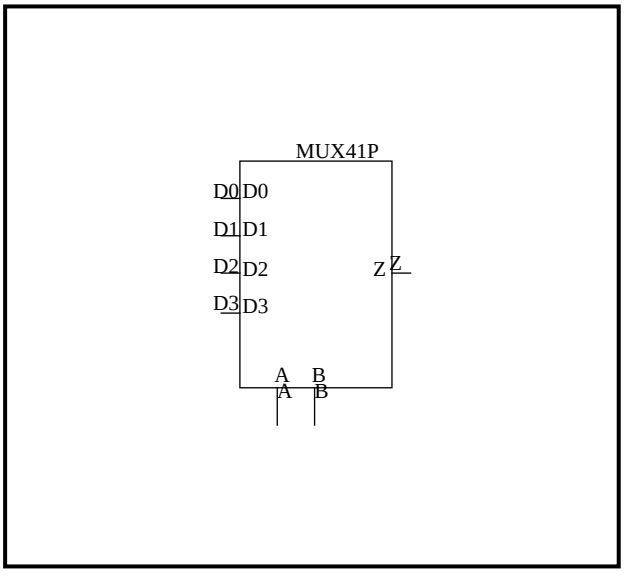
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.50	0.64	1.16
0.38	0.38	0.52	0.67	1.18
1.00	0.44	0.59	0.73	1.24
3.00	0.59	0.74	0.89	1.41

Rev.1.01.10

MUX41P	MUX41P	1/7

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
MUX41P	4 TO 1 MULTIPLEXER	7	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
B	A	Z
L	L	D0
L	H	D1
H	L	D2
H	H	D3

Verilog-HDL DESCRIPTION

```
MUX41P  inst(Z,D0,D1,D2,D3,A,B);
```

VHDL DESCRIPTION

```
inst:MUX41P
   port   map(Z,D0,D1,D2,D3,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D0	3.50
D1	3.58
D2	3.35
D3	3.41
A	3.08
B	2.06

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	94.9

Rev.1.01.10

MUX41P MUX41P 2/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~D2&D3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0439	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.39	0.46	0.55	0.87
0.38	0.42	0.50	0.58	0.90
1.00	0.47	0.55	0.64	0.96
3.00	0.60	0.67	0.76	1.08

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&~D2&D3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0199	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.38	0.47	0.55	0.81
0.38	0.44	0.53	0.61	0.88
1.00	0.49	0.58	0.66	0.93
3.00	0.58	0.67	0.75	1.02

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&D2&~D3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0439	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.40	0.48	0.57	0.89
0.38	0.49	0.57	0.66	0.98
1.00	0.59	0.67	0.75	1.07
3.00	0.72	0.79	0.88	1.20

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	B&D2&~D3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0199	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.60	0.68	0.95
0.38	0.55	0.63	0.72	0.98
1.00	0.62	0.70	0.79	1.05
3.00	0.76	0.84	0.93	1.19

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&~D0&D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0439	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.39	0.46	0.55	0.87
0.38	0.42	0.50	0.58	0.90
1.00	0.48	0.55	0.64	0.96
3.00	0.60	0.68	0.77	1.08

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&~D0&D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0199	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.45	0.54	0.80
0.38	0.44	0.52	0.60	0.86
1.00	0.49	0.57	0.65	0.92
3.00	0.59	0.67	0.75	1.01

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&D0&~D1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0439	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.40	0.48	0.56	0.88
0.38	0.49	0.57	0.65	0.97
1.00	0.59	0.66	0.75	1.07
3.00	0.72	0.79	0.88	1.20

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	~B&D0&~D1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0199	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.59	0.67	0.93
0.38	0.54	0.62	0.71	0.97
1.00	0.61	0.69	0.78	1.04
3.00	0.75	0.84	0.92	1.18

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~D1&D3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0439	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.35	0.44	0.76
0.38	0.31	0.39	0.47	0.79
1.00	0.37	0.45	0.53	0.85
3.00	0.49	0.57	0.65	0.97

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&~D1&D3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0199	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.29	0.37	0.63
0.38	0.28	0.37	0.45	0.71
1.00	0.41	0.49	0.57	0.83
3.00	0.53	0.61	0.69	0.95

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&D1&~D3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0439	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.28	0.37	0.69
0.38	0.29	0.36	0.45	0.77
1.00	0.37	0.45	0.53	0.85
3.00	0.53	0.61	0.69	1.01

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	A&D1&~D3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0199	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.31	0.39	0.64
0.38	0.26	0.34	0.42	0.67
1.00	0.32	0.40	0.48	0.74
3.00	0.46	0.55	0.63	0.90

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&~D0&D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0439	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.35	0.44	0.76
0.38	0.31	0.39	0.47	0.79
1.00	0.37	0.45	0.53	0.85
3.00	0.49	0.57	0.65	0.97

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&~D0&D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0199	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.29	0.37	0.63
0.38	0.28	0.37	0.45	0.71
1.00	0.41	0.49	0.57	0.83
3.00	0.53	0.61	0.69	0.95

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&D0&~D2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0439	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.28	0.37	0.69
0.38	0.29	0.36	0.45	0.77
1.00	0.37	0.45	0.53	0.85
3.00	0.53	0.61	0.69	1.01

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	~A&D0&~D2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0199	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.31	0.39	0.64
0.38	0.26	0.34	0.42	0.67
1.00	0.32	0.40	0.48	0.74
3.00	0.46	0.55	0.63	0.90

MUX41P | MUX41P | 6/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D0->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0439	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.39	0.47	0.79
0.38	0.38	0.45	0.54	0.86
1.00	0.46	0.54	0.63	0.94
3.00	0.63	0.71	0.79	1.11

PATH CONDITION

PATH	CONDITION	FUNCTION
D0->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0199	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.43	0.51	0.78
0.38	0.37	0.45	0.53	0.79
1.00	0.44	0.52	0.60	0.86
3.00	0.60	0.69	0.77	1.04

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0439	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.40	0.49	0.80
0.38	0.38	0.46	0.55	0.86
1.00	0.47	0.54	0.63	0.95
3.00	0.63	0.71	0.79	1.12

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0199	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.43	0.51	0.77
0.38	0.37	0.45	0.53	0.79
1.00	0.44	0.52	0.60	0.86
3.00	0.60	0.69	0.77	1.04

MUX41P | MUX41P | 7/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0439	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.39	0.48	0.80
0.38	0.38	0.46	0.54	0.86
1.00	0.47	0.54	0.63	0.95
3.00	0.63	0.71	0.80	1.12

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0199	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.44	0.52	0.79
0.38	0.38	0.46	0.54	0.81
1.00	0.44	0.52	0.61	0.87
3.00	0.60	0.69	0.77	1.05

PATH CONDITION

PATH	CONDITION	FUNCTION
D3->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0439	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.40	0.49	0.81
0.38	0.38	0.46	0.55	0.87
1.00	0.47	0.54	0.63	0.95
3.00	0.63	0.71	0.80	1.12

PATH CONDITION

PATH	CONDITION	FUNCTION
D3->Z	---	FALL

SLEW FACTOR

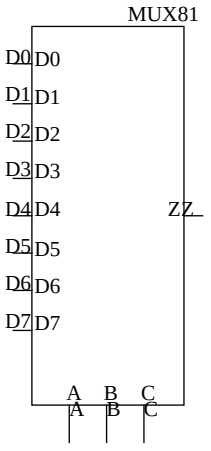
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0199	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.43	0.52	0.78
0.38	0.37	0.46	0.54	0.80
1.00	0.44	0.52	0.61	0.87
3.00	0.60	0.69	0.77	1.05

MUX81	MUX81	1/17

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
MUX81	8 TO 1 MULTIPLEXER	15	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
C	B	A	Z
L	L	L	D0
L	L	H	D1
L	H	L	D2
L	H	H	D3
H	L	L	D4
H	L	H	D5
H	H	L	D6
H	H	H	D7

Verilog-HDL DESCRIPTION

```
MUX81  inst(Z,D0,D1,D2,D3,D4,D5,
            D6,D7,A,B,C);
```

VHDL DESCRIPTION

```
inst:MUX81
   port   map(Z,D0,D1,D2,D3,D4,
              D5,D6,D7,A,B,C);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D0	3.46
D1,D7	3.42
D2	3.30
D3	3.39
D4	3.40
D5	3.49
D6	3.36
A	0.99
B	3.24
C	2.11

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	46.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(B&C)&(~D6&D7)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.81	0.95	1.12	1.75
0.38	0.84	0.99	1.15	1.78
1.00	0.92	1.06	1.23	1.86
3.00	1.08	1.23	1.39	2.03

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(B&C)&(~D6&D7)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.80	0.95	1.10	1.60
0.38	0.89	1.04	1.19	1.68
1.00	0.98	1.14	1.29	1.78
3.00	1.16	1.32	1.47	1.96

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(B&C)&(D6&~D7)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.65	0.79	0.96	1.59
0.38	0.74	0.88	1.05	1.68
1.00	0.85	0.99	1.16	1.79
3.00	1.06	1.21	1.37	2.01

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(B&C)&(D6&~D7)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.74	0.89	1.04	1.53
0.38	0.77	0.92	1.07	1.56
1.00	0.85	1.00	1.15	1.64
3.00	1.03	1.18	1.33	1.83

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(B&~C)&(~D2&D3)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.86	1.00	1.17	1.81
0.38	0.89	1.04	1.20	1.84
1.00	0.96	1.11	1.28	1.91
3.00	1.13	1.28	1.44	2.08

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(B&~C)&(~D2&D3)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.86	1.02	1.17	1.67
0.38	0.95	1.10	1.26	1.76
1.00	1.04	1.20	1.35	1.86
3.00	1.22	1.38	1.53	2.04

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(B&~C)&(D2&~D3)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.69	0.84	1.01	1.65
0.38	0.78	0.93	1.10	1.73
1.00	0.90	1.04	1.21	1.85
3.00	1.11	1.26	1.42	2.06

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(B&~C)&(D2&~D3)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.80	0.96	1.11	1.61
0.38	0.83	0.99	1.14	1.64
1.00	0.91	1.07	1.22	1.72
3.00	1.09	1.25	1.40	1.91

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(~B&C)&(~D4&D5)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.84	0.99	1.16	1.79
0.38	0.88	1.02	1.19	1.82
1.00	0.95	1.10	1.27	1.90
3.00	1.12	1.26	1.43	2.07

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(~B&C)&(~D4&D5)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.81	0.97	1.12	1.61
0.38	0.90	1.05	1.20	1.70
1.00	1.00	1.15	1.30	1.80
3.00	1.18	1.33	1.48	1.98

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(~B&C)&(D4&~D5)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.68	0.83	0.99	1.63
0.38	0.77	0.92	1.08	1.72
1.00	0.88	1.03	1.19	1.83
3.00	1.09	1.24	1.40	2.04

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(~B&C)&(D4&~D5)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.76	0.92	1.07	1.56
0.38	0.79	0.95	1.10	1.60
1.00	0.87	1.03	1.18	1.68
3.00	1.06	1.22	1.37	1.86

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(~B&~C)&(~D0&D1)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.86	1.01	1.17	1.81
0.38	0.89	1.04	1.21	1.84
1.00	0.97	1.11	1.28	1.92
3.00	1.13	1.28	1.45	2.08

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(~B&~C)&(~D0&D1)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.85	1.01	1.16	1.66
0.38	0.94	1.09	1.25	1.75
1.00	1.03	1.19	1.34	1.84
3.00	1.21	1.37	1.52	2.02

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(~B&~C)&(D0&~D1)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.71	0.86	1.02	1.66
0.38	0.80	0.94	1.11	1.75
1.00	0.91	1.06	1.22	1.86
3.00	1.12	1.27	1.44	2.07

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(~B&~C)&(D0&~D1)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.78	0.93	1.09	1.59
0.38	0.81	0.96	1.12	1.62
1.00	0.89	1.04	1.20	1.70
3.00	1.07	1.23	1.38	1.88

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(A&C)&(~D5&D7)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.44	0.59	0.76	1.39
0.38	0.48	0.62	0.79	1.42
1.00	0.55	0.69	0.86	1.49
3.00	0.69	0.84	1.00	1.64

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(A&C)&(~D5&D7)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.48	0.63	1.13
0.38	0.41	0.56	0.71	1.21
1.00	0.55	0.70	0.85	1.35
3.00	0.71	0.87	1.02	1.51

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(A&C)&(D5&~D7)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.46	0.63	1.26
0.38	0.40	0.54	0.71	1.34
1.00	0.49	0.64	0.80	1.44
3.00	0.66	0.81	0.97	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(A&C)&(D5&~D7)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.51	0.66	1.16
0.38	0.39	0.54	0.69	1.19
1.00	0.46	0.61	0.76	1.26
3.00	0.62	0.78	0.93	1.44

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(A&~C)&(~D1&D3)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.44	0.59	0.76	1.39
0.38	0.47	0.62	0.79	1.42
1.00	0.54	0.69	0.86	1.49
3.00	0.69	0.83	1.00	1.63

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(A&~C)&(~D1&D3)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.48	0.63	1.13
0.38	0.40	0.56	0.71	1.21
1.00	0.55	0.70	0.85	1.35
3.00	0.71	0.87	1.02	1.52

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(A&~C)&(D1&~D3)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.47	0.64	1.27
0.38	0.40	0.55	0.72	1.35
1.00	0.49	0.64	0.81	1.45
3.00	0.67	0.82	0.99	1.63

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(A&~C)&(D1&~D3)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.50	0.65	1.15
0.38	0.38	0.53	0.68	1.18
1.00	0.45	0.60	0.75	1.25
3.00	0.61	0.77	0.92	1.43

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(~A&C)&(~D4&D6)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.44	0.59	0.76	1.39
0.38	0.48	0.62	0.79	1.42
1.00	0.55	0.69	0.86	1.49
3.00	0.69	0.84	1.00	1.64

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(~A&C)&(~D4&D6)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.48	0.63	1.13
0.38	0.41	0.56	0.71	1.21
1.00	0.55	0.70	0.85	1.35
3.00	0.71	0.87	1.02	1.51

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(~A&C)&(D4&~D6)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.46	0.63	1.26
0.38	0.40	0.54	0.71	1.34
1.00	0.49	0.64	0.80	1.44
3.00	0.66	0.81	0.97	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(~A&C)&(D4&~D6)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.51	0.66	1.16
0.38	0.39	0.54	0.69	1.19
1.00	0.46	0.61	0.76	1.26
3.00	0.62	0.78	0.93	1.44

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(~A&~C)&(~D0&D2)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.44	0.59	0.76	1.39
0.38	0.47	0.62	0.79	1.42
1.00	0.54	0.69	0.86	1.49
3.00	0.69	0.83	1.00	1.63

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(~A&~C)&(~D0&D2)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.48	0.63	1.13
0.38	0.40	0.56	0.71	1.21
1.00	0.55	0.70	0.85	1.35
3.00	0.71	0.87	1.02	1.52

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(~A&~C)&(D0&~D2)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.47	0.64	1.27
0.38	0.40	0.55	0.72	1.35
1.00	0.49	0.64	0.81	1.45
3.00	0.67	0.82	0.99	1.63

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(~A&~C)&(D0&~D2)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.50	0.65	1.15
0.38	0.38	0.53	0.68	1.18
1.00	0.45	0.60	0.75	1.25
3.00	0.61	0.77	0.92	1.43

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(A&B)&(~D3&D7)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.46	0.63	1.26
0.38	0.34	0.49	0.66	1.30
1.00	0.40	0.55	0.72	1.35
3.00	0.51	0.66	0.83	1.46

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(A&B)&(~D3&D7)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.36	0.50	0.99
0.38	0.30	0.45	0.59	1.08
1.00	0.43	0.57	0.70	1.19
3.00	0.54	0.68	0.82	1.29

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(A&B)&(D3&~D7)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.35	0.52	1.15
0.38	0.29	0.43	0.60	1.23
1.00	0.36	0.50	0.67	1.31
3.00	0.47	0.61	0.78	1.42

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(A&B)&(D3&~D7)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.37	0.52	1.00
0.38	0.27	0.41	0.55	1.04
1.00	0.34	0.47	0.62	1.10
3.00	0.49	0.63	0.78	1.27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(A&~B)&(~D1&D5)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.45	0.62	1.26
0.38	0.34	0.49	0.65	1.29
1.00	0.39	0.54	0.71	1.34
3.00	0.51	0.65	0.82	1.46

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(A&~B)&(~D1&D5)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.36	0.51	1.00
0.38	0.30	0.45	0.59	1.08
1.00	0.43	0.57	0.71	1.19
3.00	0.54	0.68	0.82	1.30

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(A&~B)&(D1&~D5)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.35	0.52	1.15
0.38	0.28	0.43	0.60	1.23
1.00	0.36	0.50	0.67	1.31
3.00	0.47	0.62	0.78	1.43

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(A&~B)&(D1&~D5)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.37	0.51	1.00
0.38	0.27	0.41	0.55	1.03
1.00	0.34	0.47	0.61	1.10
3.00	0.49	0.63	0.77	1.26

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(~A&B)&(~D2&D6)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.46	0.63	1.26
0.38	0.34	0.49	0.66	1.30
1.00	0.40	0.55	0.72	1.35
3.00	0.51	0.66	0.83	1.46

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(~A&B)&(~D2&D6)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.36	0.50	0.99
0.38	0.30	0.45	0.59	1.08
1.00	0.43	0.57	0.70	1.19
3.00	0.54	0.68	0.82	1.29

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(~A&B)&(D2&~D6)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.35	0.52	1.15
0.38	0.29	0.43	0.60	1.23
1.00	0.36	0.50	0.67	1.31
3.00	0.47	0.61	0.78	1.42

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(~A&B)&(D2&~D6)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.37	0.52	1.00
0.38	0.27	0.41	0.55	1.04
1.00	0.34	0.47	0.62	1.10
3.00	0.49	0.63	0.78	1.27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(~A&~B)&(~D0&D4)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.45	0.62	1.26
0.38	0.34	0.49	0.65	1.29
1.00	0.39	0.54	0.71	1.34
3.00	0.51	0.65	0.82	1.46

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(~A&~B)&(~D0&D4)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.36	0.51	1.00
0.38	0.30	0.45	0.59	1.08
1.00	0.43	0.57	0.71	1.19
3.00	0.54	0.68	0.82	1.30

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(~A&~B)&(D0&~D4)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.35	0.52	1.15
0.38	0.28	0.43	0.60	1.23
1.00	0.36	0.50	0.67	1.31
3.00	0.47	0.62	0.78	1.43

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(~A&~B)&(D0&~D4)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.37	0.51	1.00
0.38	0.27	0.41	0.55	1.03
1.00	0.34	0.47	0.61	1.10
3.00	0.49	0.63	0.77	1.26

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D0->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.60	0.77	1.40
0.38	0.51	0.66	0.83	1.46
1.00	0.60	0.75	0.92	1.55
3.00	0.79	0.94	1.11	1.75

PATH CONDITION

PATH	CONDITION	FUNCTION
D0->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.63	0.79	1.29
0.38	0.50	0.65	0.81	1.31
1.00	0.57	0.72	0.88	1.38
3.00	0.74	0.90	1.06	1.57

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.60	0.77	1.40
0.38	0.52	0.67	0.83	1.47
1.00	0.61	0.76	0.92	1.56
3.00	0.80	0.95	1.11	1.75

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.64	0.79	1.29
0.38	0.51	0.66	0.81	1.32
1.00	0.57	0.73	0.88	1.38
3.00	0.75	0.91	1.07	1.58

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.60	0.77	1.40
0.38	0.52	0.66	0.83	1.47
1.00	0.61	0.76	0.92	1.56
3.00	0.80	0.94	1.11	1.75

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.64	0.79	1.30
0.38	0.51	0.66	0.82	1.32
1.00	0.57	0.73	0.89	1.39
3.00	0.75	0.91	1.07	1.58

PATH CONDITION

PATH	CONDITION	FUNCTION
D3->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.60	0.77	1.40
0.38	0.51	0.66	0.83	1.47
1.00	0.61	0.75	0.92	1.56
3.00	0.79	0.94	1.11	1.75

PATH CONDITION

PATH	CONDITION	FUNCTION
D3->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.64	0.79	1.30
0.38	0.50	0.66	0.82	1.32
1.00	0.57	0.73	0.89	1.39
3.00	0.75	0.91	1.07	1.58

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D4->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.44	0.59	0.76	1.39
0.38	0.50	0.65	0.82	1.45
1.00	0.59	0.74	0.90	1.54
3.00	0.77	0.92	1.09	1.72

PATH CONDITION

PATH	CONDITION	FUNCTION
D4->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.47	0.62	0.77	1.27
0.38	0.49	0.64	0.80	1.29
1.00	0.56	0.71	0.86	1.36
3.00	0.73	0.89	1.04	1.55

PATH CONDITION

PATH	CONDITION	FUNCTION
D5->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.44	0.58	0.75	1.38
0.38	0.50	0.64	0.81	1.44
1.00	0.59	0.73	0.90	1.53
3.00	0.76	0.91	1.08	1.72

PATH CONDITION

PATH	CONDITION	FUNCTION
D5->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.62	0.77	1.26
0.38	0.48	0.64	0.79	1.29
1.00	0.55	0.71	0.86	1.36
3.00	0.72	0.88	1.04	1.54

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D6->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.56	0.73	1.36
0.38	0.48	0.62	0.79	1.42
1.00	0.56	0.71	0.87	1.51
3.00	0.73	0.88	1.05	1.68

PATH CONDITION

PATH	CONDITION	FUNCTION
D6->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.44	0.59	0.74	1.24
0.38	0.47	0.62	0.77	1.26
1.00	0.53	0.69	0.84	1.33
3.00	0.70	0.86	1.01	1.51

PATH CONDITION

PATH	CONDITION	FUNCTION
D7->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0891	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.56	0.73	1.36
0.38	0.48	0.62	0.79	1.42
1.00	0.56	0.71	0.87	1.51
3.00	0.73	0.88	1.05	1.68

PATH CONDITION

PATH	CONDITION	FUNCTION
D7->Z	---	FALL

SLEW FACTOR

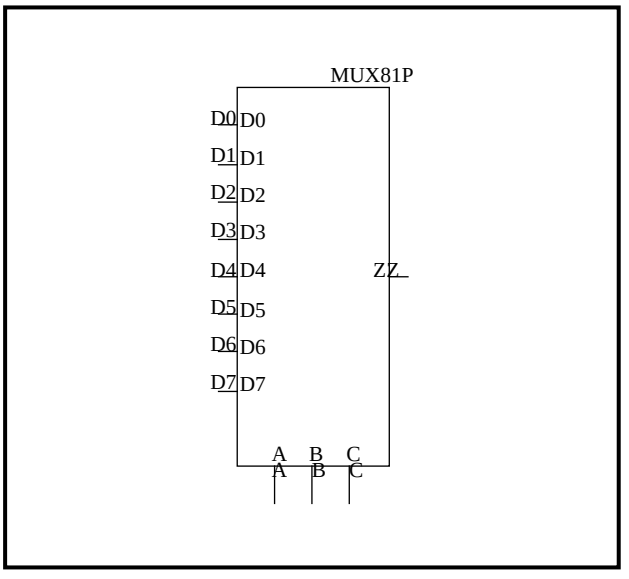
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0391	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.44	0.59	0.74	1.24
0.38	0.47	0.62	0.77	1.26
1.00	0.53	0.69	0.84	1.33
3.00	0.69	0.85	1.01	1.51

MUX81P	MUX81P	1/17

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
MUX81P	8 TO 1 MULTIPLEXER	15	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
C	B	A	Z
L	L	L	D0
L	L	H	D1
L	H	L	D2
L	H	H	D3
H	L	L	D4
H	L	H	D5
H	H	L	D6
H	H	H	D7

Verilog-HDL DESCRIPTION

```
MUX81P  inst(Z,D0,D1,D2,D3,D4,D5,
             D6,D7,A,B,C);
```

VHDL DESCRIPTION

```
inst:MUX81P
   port   map(Z,D0,D1,D2,D3,D4,
              D5,D6,D7,A,B,C);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D0	3.46
D1,D7	3.42
D2	3.30
D3	3.39
D4	3.40
D5	3.49
D6	3.36
A	0.99
B	3.24
C	2.11

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	88.9

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(B&C)&(~D6&D7)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.83	0.91	1.00	1.33
0.38	0.86	0.94	1.03	1.36
1.00	0.93	1.02	1.11	1.44
3.00	1.10	1.18	1.27	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(B&C)&(~D6&D7)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.80	0.90	1.00	1.30
0.38	0.89	0.99	1.09	1.39
1.00	0.99	1.09	1.18	1.48
3.00	1.17	1.27	1.36	1.66

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(B&C)&(D6&~D7)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.67	0.75	0.84	1.17
0.38	0.75	0.84	0.93	1.26
1.00	0.87	0.95	1.04	1.37
3.00	1.08	1.16	1.25	1.59

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(B&C)&(D6&~D7)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.74	0.84	0.94	1.24
0.38	0.77	0.87	0.97	1.27
1.00	0.85	0.95	1.05	1.35
3.00	1.04	1.13	1.23	1.53

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(B&~C)&(~D2&D3)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.88	0.96	1.05	1.39
0.38	0.91	0.99	1.08	1.42
1.00	0.98	1.07	1.16	1.50
3.00	1.15	1.23	1.32	1.66

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(B&~C)&(~D2&D3)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.87	0.97	1.07	1.37
0.38	0.95	1.05	1.15	1.46
1.00	1.05	1.15	1.25	1.56
3.00	1.23	1.33	1.43	1.74

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(B&~C)&(D2&~D3)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.71	0.80	0.89	1.23
0.38	0.80	0.89	0.98	1.31
1.00	0.92	1.00	1.09	1.43
3.00	1.13	1.21	1.30	1.64

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(B&~C)&(D2&~D3)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.81	0.91	1.00	1.31
0.38	0.84	0.94	1.04	1.34
1.00	0.92	1.02	1.12	1.42
3.00	1.10	1.20	1.30	1.61

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(~B&C)&(~D4&D5)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.86	0.95	1.04	1.37
0.38	0.90	0.98	1.07	1.40
1.00	0.97	1.05	1.15	1.48
3.00	1.14	1.22	1.31	1.65

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(~B&C)&(~D4&D5)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.82	0.92	1.01	1.32
0.38	0.91	1.00	1.10	1.40
1.00	1.00	1.10	1.20	1.50
3.00	1.18	1.28	1.38	1.68

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(~B&C)&(D4&~D5)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.70	0.78	0.87	1.21
0.38	0.79	0.87	0.96	1.30
1.00	0.90	0.98	1.07	1.41
3.00	1.11	1.19	1.28	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(~B&C)&(D4&~D5)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.77	0.87	0.96	1.27
0.38	0.80	0.90	1.00	1.30
1.00	0.88	0.98	1.08	1.38
3.00	1.07	1.17	1.26	1.57

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(~B&~C)&(~D0&D1)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.88	0.96	1.05	1.39
0.38	0.91	0.99	1.09	1.42
1.00	0.99	1.07	1.16	1.50
3.00	1.15	1.23	1.33	1.66

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(~B&~C)&(~D0&D1)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.86	0.96	1.05	1.36
0.38	0.94	1.04	1.14	1.45
1.00	1.04	1.14	1.24	1.54
3.00	1.22	1.32	1.42	1.72

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(~B&~C)&(D0&~D1)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.73	0.81	0.90	1.24
0.38	0.82	0.90	0.99	1.33
1.00	0.93	1.01	1.10	1.44
3.00	1.14	1.23	1.32	1.65

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	(~B&~C)&(D0&~D1)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.79	0.88	0.98	1.29
0.38	0.82	0.92	1.01	1.32
1.00	0.90	0.99	1.09	1.40
3.00	1.08	1.18	1.27	1.58

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(A&C)&(~D5&D7)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.55	0.64	0.97
0.38	0.49	0.58	0.67	1.00
1.00	0.56	0.65	0.74	1.07
3.00	0.71	0.79	0.88	1.21

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(A&C)&(~D5&D7)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.43	0.53	0.83
0.38	0.41	0.51	0.61	0.91
1.00	0.55	0.65	0.75	1.05
3.00	0.73	0.83	0.93	1.23

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(A&C)&(D5&~D7)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.42	0.51	0.84
0.38	0.42	0.50	0.59	0.92
1.00	0.51	0.60	0.69	1.02
3.00	0.71	0.79	0.88	1.21

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(A&C)&(D5&~D7)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.46	0.56	0.86
0.38	0.40	0.49	0.59	0.89
1.00	0.46	0.56	0.66	0.96
3.00	0.62	0.73	0.82	1.13

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(A&~C)&(~D1&D3)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.54	0.64	0.97
0.38	0.49	0.57	0.67	1.00
1.00	0.56	0.64	0.73	1.07
3.00	0.70	0.79	0.88	1.21

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(A&~C)&(~D1&D3)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.43	0.52	0.83
0.38	0.40	0.50	0.60	0.91
1.00	0.55	0.65	0.74	1.05
3.00	0.74	0.84	0.93	1.24

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(A&~C)&(D1&~D3)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.42	0.52	0.85
0.38	0.42	0.51	0.60	0.93
1.00	0.52	0.61	0.70	1.03
3.00	0.72	0.81	0.90	1.24

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(A&~C)&(D1&~D3)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.45	0.55	0.85
0.38	0.38	0.48	0.58	0.88
1.00	0.45	0.55	0.64	0.95
3.00	0.61	0.71	0.81	1.12

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(~A&C)&(~D4&D6)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.55	0.64	0.97
0.38	0.49	0.58	0.67	1.00
1.00	0.56	0.65	0.74	1.07
3.00	0.71	0.79	0.88	1.21

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(~A&C)&(~D4&D6)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.43	0.53	0.83
0.38	0.41	0.51	0.61	0.91
1.00	0.55	0.65	0.75	1.05
3.00	0.73	0.83	0.93	1.23

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(~A&C)&(D4&~D6)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.42	0.51	0.84
0.38	0.42	0.50	0.59	0.92
1.00	0.51	0.60	0.69	1.02
3.00	0.71	0.79	0.88	1.21

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(~A&C)&(D4&~D6)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.46	0.56	0.86
0.38	0.40	0.49	0.59	0.89
1.00	0.46	0.56	0.66	0.96
3.00	0.62	0.73	0.82	1.13

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(~A&~C)&(~D0&D2)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.54	0.64	0.97
0.38	0.49	0.57	0.67	1.00
1.00	0.56	0.64	0.73	1.07
3.00	0.70	0.79	0.88	1.21

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(~A&~C)&(~D0&D2)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.43	0.52	0.83
0.38	0.40	0.50	0.60	0.91
1.00	0.55	0.65	0.74	1.05
3.00	0.74	0.84	0.93	1.24

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(~A&~C)&(D0&~D2)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.42	0.52	0.85
0.38	0.42	0.51	0.60	0.93
1.00	0.52	0.61	0.70	1.03
3.00	0.72	0.81	0.90	1.24

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	(~A&~C)&(D0&~D2)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.45	0.55	0.85
0.38	0.38	0.48	0.58	0.88
1.00	0.45	0.55	0.64	0.95
3.00	0.61	0.71	0.81	1.12

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(A&B)&(~D3&D7)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.41	0.50	0.84
0.38	0.36	0.44	0.54	0.87
1.00	0.42	0.50	0.59	0.93
3.00	0.53	0.62	0.71	1.05

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(A&B)&(~D3&D7)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.30	0.40	0.70
0.38	0.30	0.39	0.49	0.78
1.00	0.44	0.54	0.63	0.92
3.00	0.59	0.68	0.77	1.06

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(A&B)&(D3&~D7)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.31	0.40	0.74
0.38	0.31	0.39	0.49	0.82
1.00	0.40	0.48	0.57	0.91
3.00	0.56	0.64	0.73	1.06

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(A&B)&(D3&~D7)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.33	0.42	0.72
0.38	0.28	0.37	0.46	0.75
1.00	0.34	0.43	0.52	0.82
3.00	0.50	0.59	0.69	0.99

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(A&~B)&(~D1&D5)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.40	0.50	0.83
0.38	0.35	0.44	0.53	0.86
1.00	0.41	0.49	0.58	0.92
3.00	0.53	0.61	0.70	1.04

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(A&~B)&(~D1&D5)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.31	0.40	0.70
0.38	0.30	0.39	0.49	0.79
1.00	0.45	0.54	0.63	0.92
3.00	0.60	0.69	0.77	1.06

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(A&~B)&(D1&~D5)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.31	0.40	0.74
0.38	0.31	0.39	0.48	0.82
1.00	0.40	0.48	0.57	0.91
3.00	0.56	0.64	0.73	1.06

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(A&~B)&(D1&~D5)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.33	0.42	0.72
0.38	0.27	0.36	0.46	0.75
1.00	0.34	0.43	0.52	0.82
3.00	0.49	0.59	0.68	0.98

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(~A&B)&(~D2&D6)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.41	0.50	0.84
0.38	0.36	0.44	0.54	0.87
1.00	0.42	0.50	0.59	0.93
3.00	0.53	0.62	0.71	1.05

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(~A&B)&(~D2&D6)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.30	0.40	0.70
0.38	0.30	0.39	0.48	0.78
1.00	0.44	0.54	0.63	0.92
3.00	0.59	0.68	0.77	1.06

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(~A&B)&(D2&~D6)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.31	0.40	0.74
0.38	0.31	0.39	0.49	0.82
1.00	0.40	0.48	0.57	0.91
3.00	0.56	0.64	0.73	1.06

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(~A&B)&(D2&~D6)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.33	0.42	0.72
0.38	0.28	0.37	0.46	0.75
1.00	0.34	0.43	0.52	0.82
3.00	0.50	0.59	0.69	0.99

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(~A&~B)&(~D0&D4)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.40	0.50	0.83
0.38	0.35	0.44	0.53	0.86
1.00	0.41	0.49	0.58	0.92
3.00	0.53	0.61	0.70	1.04

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(~A&~B)&(~D0&D4)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.31	0.40	0.70
0.38	0.30	0.39	0.49	0.79
1.00	0.45	0.54	0.63	0.92
3.00	0.60	0.69	0.77	1.06

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(~A&~B)&(D0&~D4)	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.31	0.40	0.74
0.38	0.31	0.39	0.48	0.82
1.00	0.40	0.48	0.57	0.91
3.00	0.56	0.64	0.73	1.06

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	(~A&~B)&(D0&~D4)	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.33	0.42	0.72
0.38	0.27	0.36	0.46	0.75
1.00	0.34	0.43	0.52	0.82
3.00	0.49	0.59	0.68	0.98

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D0->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.47	0.55	0.64	0.98
0.38	0.53	0.62	0.71	1.04
1.00	0.63	0.71	0.80	1.13
3.00	0.82	0.91	1.00	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
D0->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.58	0.68	0.99
0.38	0.50	0.60	0.70	1.01
1.00	0.57	0.67	0.77	1.08
3.00	0.76	0.86	0.96	1.27

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.47	0.56	0.65	0.98
0.38	0.54	0.62	0.71	1.05
1.00	0.63	0.71	0.81	1.14
3.00	0.83	0.91	1.01	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
D1->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.59	0.69	0.99
0.38	0.51	0.61	0.71	1.01
1.00	0.58	0.68	0.78	1.08
3.00	0.76	0.86	0.97	1.28

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.47	0.56	0.65	0.98
0.38	0.54	0.62	0.71	1.05
1.00	0.63	0.71	0.81	1.14
3.00	0.83	0.91	1.00	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
D2->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.59	0.69	1.00
0.38	0.51	0.61	0.71	1.02
1.00	0.58	0.68	0.78	1.09
3.00	0.76	0.86	0.97	1.28

PATH CONDITION

PATH	CONDITION	FUNCTION
D3->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.47	0.55	0.65	0.98
0.38	0.53	0.62	0.71	1.05
1.00	0.63	0.71	0.80	1.14
3.00	0.83	0.91	1.00	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
D3->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.59	0.69	1.00
0.38	0.51	0.61	0.71	1.02
1.00	0.58	0.68	0.78	1.09
3.00	0.76	0.86	0.96	1.28

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D4->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.54	0.63	0.97
0.38	0.52	0.60	0.70	1.03
1.00	0.61	0.69	0.79	1.12
3.00	0.80	0.88	0.98	1.31

PATH CONDITION

PATH	CONDITION	FUNCTION
D4->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.47	0.57	0.67	0.97
0.38	0.50	0.59	0.69	1.00
1.00	0.57	0.66	0.76	1.06
3.00	0.74	0.84	0.94	1.25

PATH CONDITION

PATH	CONDITION	FUNCTION
D5->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.54	0.63	0.96
0.38	0.52	0.60	0.69	1.02
1.00	0.61	0.69	0.78	1.11
3.00	0.80	0.88	0.97	1.31

PATH CONDITION

PATH	CONDITION	FUNCTION
D5->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.47	0.57	0.66	0.97
0.38	0.49	0.59	0.69	0.99
1.00	0.56	0.66	0.75	1.06
3.00	0.73	0.84	0.94	1.25

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
D6->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.43	0.52	0.61	0.94
0.38	0.50	0.58	0.67	1.00
1.00	0.58	0.66	0.76	1.09
3.00	0.76	0.85	0.94	1.27

PATH CONDITION

PATH	CONDITION	FUNCTION
D6->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.54	0.64	0.94
0.38	0.47	0.57	0.67	0.97
1.00	0.54	0.64	0.73	1.04
3.00	0.71	0.81	0.91	1.22

PATH CONDITION

PATH	CONDITION	FUNCTION
D7->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0444	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.43	0.51	0.61	0.94
0.38	0.49	0.58	0.67	1.00
1.00	0.58	0.66	0.75	1.09
3.00	0.76	0.84	0.94	1.27

PATH CONDITION

PATH	CONDITION	FUNCTION
D7->Z	---	FALL

SLEW FACTOR

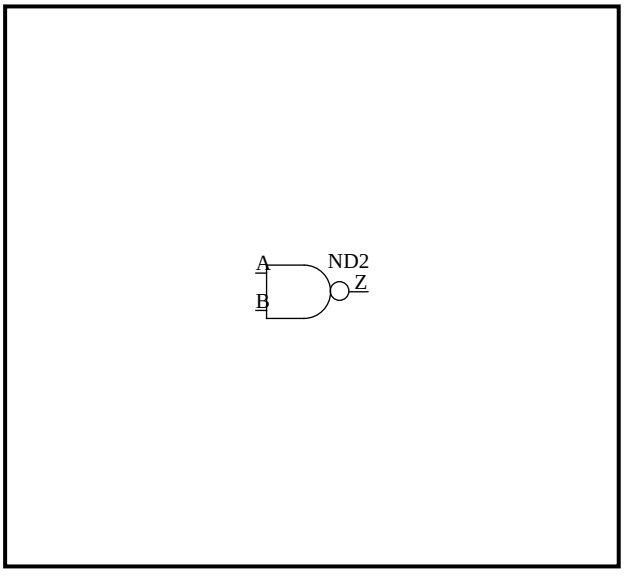
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0227	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.54	0.64	0.94
0.38	0.47	0.57	0.66	0.97
1.00	0.54	0.64	0.73	1.04
3.00	0.71	0.81	0.91	1.22

ND2	ND2	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
ND2	2-INPUT NAND	1	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
A	B	Z
L	L	H
L	H	H
H	L	H
H	H	L

Verilog-HDL DESCRIPTION

```
ND2  inst(Z,A,B);
```

VHDL DESCRIPTION

```
inst:ND2
   port   map(Z,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A,B	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	34.3

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ND2 ND2 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0997	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.09
0.38	0.11	0.26	0.43	1.12
1.00	0.13	0.30	0.49	1.17
3.00	0.15	0.37	0.60	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0654	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.79

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0997	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.26	0.43	1.11
0.38	0.14	0.28	0.45	1.14
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

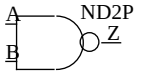
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0654	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.44	1.18
0.38	0.15	0.31	0.50	1.24
1.00	0.20	0.38	0.58	1.33
3.00	0.26	0.52	0.78	1.61

ND2P	ND2P	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
ND2P	2-INPUT NAND	2	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
A	B	Z
L	L	H
L	H	H
H	L	H
H	H	L

Verilog-HDL DESCRIPTION

```
ND2P  inst(Z,A,B);
```

VHDL DESCRIPTION

```
inst:ND2P
   port   map(Z,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	2.06
B	2.07

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	66.3

Rev.1.01.10

ND2P | ND2P | 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0492	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.08	0.15	0.23	0.57
0.38	0.09	0.17	0.26	0.60
1.00	0.11	0.20	0.30	0.66
3.00	0.11	0.24	0.37	0.80

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0316	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.07	0.15	0.24	0.61
0.38	0.13	0.22	0.32	0.69
1.00	0.18	0.30	0.42	0.83
3.00	0.27	0.45	0.62	1.15

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0492	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.17	0.25	0.60
0.38	0.11	0.19	0.28	0.62
1.00	0.14	0.23	0.33	0.68
3.00	0.20	0.31	0.43	0.83

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

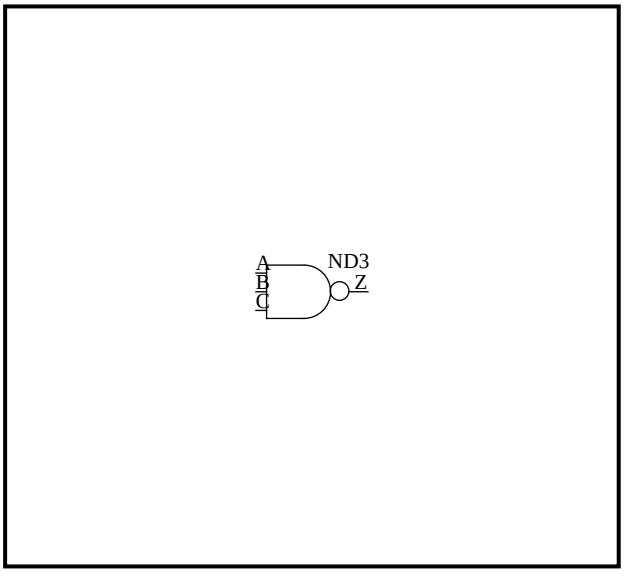
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0316	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.16	0.25	0.62
0.38	0.13	0.21	0.31	0.68
1.00	0.16	0.27	0.38	0.77
3.00	0.22	0.37	0.52	1.00

ND3	ND3	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
ND3	3-INPUT NAND	2	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
A	B	C	Z
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
ND3  inst(Z,A,B,C);
```

VHDL DESCRIPTION

```
inst:ND3
   port   map(Z,A,B,C);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.07
B	1.03
C	0.99

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	29.1

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ND3 ND3 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0999	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.24	0.41	1.10
0.38	0.12	0.27	0.44	1.13
1.00	0.13	0.31	0.49	1.18
3.00	0.10	0.34	0.57	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0932	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.36	0.62	1.67
0.38	0.22	0.44	0.70	1.75
1.00	0.30	0.56	0.83	1.89
3.00	0.49	0.83	1.17	2.32

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0999	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.26	0.43	1.12
0.38	0.15	0.29	0.46	1.15
1.00	0.17	0.33	0.52	1.20
3.00	0.17	0.38	0.61	1.37

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0932	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.38	0.65	1.70
0.38	0.22	0.44	0.70	1.76
1.00	0.29	0.53	0.80	1.86
3.00	0.46	0.76	1.08	2.19

ND3 ND3 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0999	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.27	0.44	1.07
0.38	0.16	0.30	0.46	1.10
1.00	0.19	0.34	0.51	1.15
3.00	0.22	0.42	0.62	1.33

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

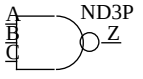
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0932	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.40	0.66	1.71
0.38	0.22	0.43	0.70	1.75
1.00	0.26	0.48	0.74	1.79
3.00	0.34	0.60	0.88	1.95

ND3P	ND3P	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
ND3P	3-INPUT NAND	3	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
A	B	C	Z
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
ND3P  inst(Z,A,B,C);
```

VHDL DESCRIPTION

```
inst:ND3P
   port   map(Z,A,B,C);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	2.10
B	2.02
C	1.96

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	51.7

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ND3P | ND3P | 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0568	0.32

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.16	0.24	0.58
0.38	0.10	0.18	0.27	0.61
1.00	0.11	0.20	0.31	0.67
3.00	0.05	0.19	0.33	0.78

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0480	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.24	0.37	0.92
0.38	0.19	0.31	0.45	1.00
1.00	0.26	0.41	0.57	1.14
3.00	0.45	0.65	0.85	1.52

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0568	0.32

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.18	0.26	0.60
0.38	0.13	0.20	0.29	0.63
1.00	0.14	0.23	0.33	0.69
3.00	0.12	0.25	0.38	0.81

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0480	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.26	0.40	0.95
0.38	0.20	0.31	0.45	1.01
1.00	0.27	0.40	0.55	1.11
3.00	0.43	0.60	0.79	1.42

ND3P | ND3P | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0568	0.32

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.24	0.34	0.73
0.38	0.17	0.26	0.36	0.75
1.00	0.21	0.30	0.41	0.80
3.00	0.26	0.38	0.51	0.96

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

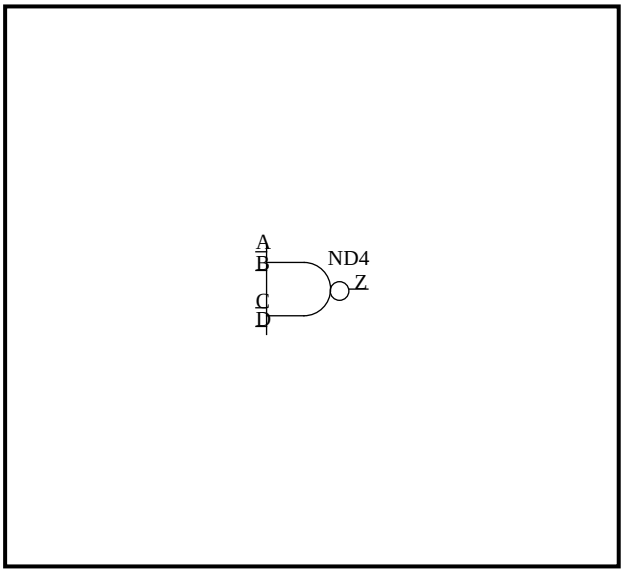
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0480	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.28	0.41	0.96
0.38	0.20	0.31	0.45	1.00
1.00	0.24	0.36	0.50	1.05
3.00	0.30	0.45	0.62	1.20

ND4	ND4	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
ND4	4-INPUT NAND	2	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT
A	B	C	D	Z
H	H	H	H	L
ALL OTHER COMBINATIONS				H

Verilog-HDL DESCRIPTION

```
ND4  inst(Z,A,B,C,D);
```

VHDL DESCRIPTION

```
inst:ND4
   port   map(Z,A,B,C,D);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.07
B	1.04
C	0.98
D	1.00

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	25.1

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ND4 ND4 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0999	0.35

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.24	0.41	1.10
0.38	0.13	0.27	0.45	1.13
1.00	0.13	0.31	0.50	1.18
3.00	0.06	0.30	0.55	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1205	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.46	0.80	2.15
0.38	0.26	0.53	0.87	2.22
1.00	0.35	0.66	1.01	2.36
3.00	0.59	0.97	1.38	2.79

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0999	0.35

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.26	0.44	1.12
0.38	0.15	0.29	0.47	1.15
1.00	0.16	0.33	0.52	1.20
3.00	0.12	0.35	0.58	1.36

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1205	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.49	0.83	2.18
0.38	0.27	0.55	0.89	2.24
1.00	0.36	0.65	0.99	2.35
3.00	0.58	0.93	1.31	2.70

ND4 | ND4 | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0999	0.35

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.30	0.47	1.16
0.38	0.18	0.32	0.49	1.18
1.00	0.20	0.36	0.55	1.23
3.00	0.19	0.41	0.63	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1205	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.53	0.86	2.22
0.38	0.29	0.57	0.91	2.26
1.00	0.35	0.62	0.96	2.32
3.00	0.50	0.81	1.17	2.52

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0999	0.35

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.31	0.49	1.18
0.38	0.19	0.34	0.51	1.20
1.00	0.21	0.38	0.57	1.25
3.00	0.22	0.43	0.66	1.42

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	FALL

SLEW FACTOR

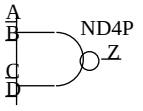
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1205	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.54	0.88	2.23
0.38	0.29	0.57	0.91	2.26
1.00	0.33	0.61	0.95	2.30
3.00	0.44	0.74	1.08	2.42

ND4P	ND4P	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
ND4P	4-INPUT NAND	4	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT
A	B	C	D	Z
H	H	H	H	L
ALL OTHER COMBINATIONS				H

Verilog-HDL DESCRIPTION

```
ND4P  inst(Z,A,B,C,D);
```

VHDL DESCRIPTION

```
inst:ND4P
   port   map(Z,A,B,C,D);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	2.15
B	2.12
C	2.05
D	1.98

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	47.9

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ND4P | ND4P | 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0498	0.35

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.16	0.24	0.58
0.38	0.11	0.19	0.28	0.62
1.00	0.10	0.20	0.31	0.67
3.00	0.00	0.15	0.29	0.76

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0645	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.31	0.49	1.22
0.38	0.23	0.38	0.57	1.29
1.00	0.32	0.50	0.70	1.43
3.00	0.57	0.79	1.02	1.84

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0498	0.35

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.18	0.27	0.61
0.38	0.13	0.21	0.30	0.64
1.00	0.14	0.23	0.33	0.69
3.00	0.06	0.20	0.34	0.79

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0645	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.35	0.53	1.26
0.38	0.26	0.40	0.59	1.31
1.00	0.34	0.51	0.69	1.42
3.00	0.57	0.77	0.99	1.77

ND4P | ND4P | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0498	0.35

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.21	0.30	0.64
0.38	0.16	0.23	0.32	0.67
1.00	0.17	0.26	0.36	0.72
3.00	0.14	0.26	0.40	0.83

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0645	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.38	0.56	1.29
0.38	0.27	0.42	0.60	1.33
1.00	0.32	0.47	0.65	1.38
3.00	0.47	0.64	0.83	1.57

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0498	0.35

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.22	0.31	0.66
0.38	0.17	0.25	0.34	0.68
1.00	0.18	0.28	0.38	0.74
3.00	0.17	0.29	0.42	0.86

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	FALL

SLEW FACTOR

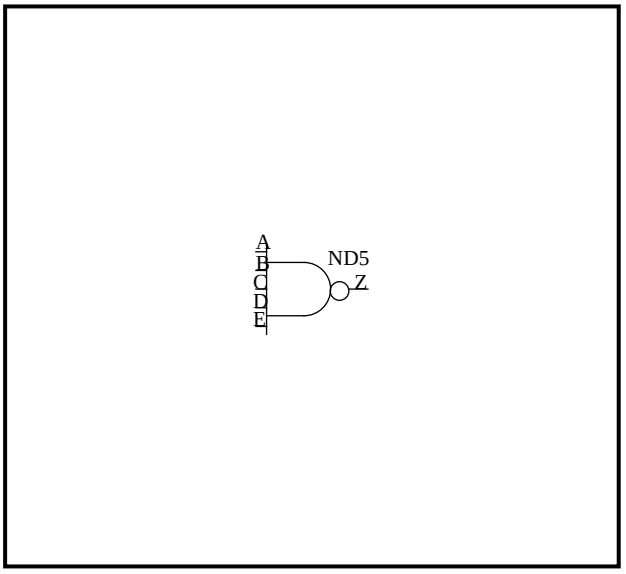
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0645	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.39	0.57	1.30
0.38	0.27	0.42	0.61	1.33
1.00	0.31	0.46	0.64	1.36
3.00	0.41	0.58	0.76	1.48

ND5	ND5	1/4

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
ND5	5-INPUT NAND	4	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT					OUTPUT
A	B	C	D	E	Z
H	H	H	H	H	L
ALL OTHER COMBINATIONS					H

Verilog-HDL DESCRIPTION

```
ND5  inst(Z,A,B,C,D,E);
```

VHDL DESCRIPTION

```
inst:ND5
   port   map(Z,A,B,C,D,E);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.04
B	0.99
C	0.98
D	1.05
E	1.09

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	44.4

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ND5 | ND5 | 2/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0966	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.43	0.60	1.26
0.38	0.32	0.46	0.63	1.29
1.00	0.35	0.49	0.66	1.32
3.00	0.37	0.51	0.67	1.33

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0396	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.54	0.66	1.14
0.38	0.49	0.61	0.74	1.21
1.00	0.59	0.71	0.84	1.31
3.00	0.84	0.96	1.09	1.57

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0966	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.46	0.63	1.29
0.38	0.35	0.49	0.65	1.32
1.00	0.39	0.53	0.70	1.36
3.00	0.45	0.59	0.76	1.42

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0396	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.44	0.56	0.69	1.16
0.38	0.50	0.62	0.75	1.22
1.00	0.59	0.71	0.84	1.31
3.00	0.82	0.94	1.07	1.54

ND5 | ND5 | 3/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0966	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.51	0.68	1.35
0.38	0.39	0.53	0.70	1.37
1.00	0.45	0.59	0.76	1.43
3.00	0.58	0.72	0.89	1.56

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0396	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.58	0.71	1.18
0.38	0.50	0.62	0.75	1.22
1.00	0.55	0.67	0.80	1.27
3.00	0.69	0.81	0.94	1.41

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0966	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.42	0.59	1.26
0.38	0.31	0.45	0.62	1.29
1.00	0.35	0.49	0.66	1.33
3.00	0.42	0.56	0.73	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0396	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.48	0.61	1.08
0.38	0.42	0.54	0.67	1.14
1.00	0.49	0.61	0.73	1.21
3.00	0.63	0.75	0.88	1.36

ND5 ND5 4/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0966	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.45	0.62	1.29
0.38	0.34	0.48	0.65	1.32
1.00	0.40	0.54	0.71	1.37
3.00	0.52	0.66	0.83	1.50

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	FALL

SLEW FACTOR

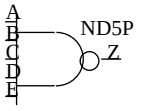
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0396	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.49	0.62	1.09
0.38	0.42	0.54	0.66	1.14
1.00	0.47	0.59	0.71	1.19
3.00	0.57	0.69	0.81	1.29

ND5P	ND5P	1/4

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
ND5P	5-INPUT NAND	5	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT					OUTPUT
A	B	C	D	E	Z
H	H	H	H	H	L
ALL OTHER COMBINATIONS					H

Verilog-HDL DESCRIPTION

```
ND5P  inst(Z,A,B,C,D,E);
```

VHDL DESCRIPTION

```
inst:ND5P
   port   map(Z,A,B,C,D,E);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A,C	0.99
B	1.04
D	1.02
E	1.06

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	81.4

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ND5P | ND5P | 2/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0550	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.37	0.46	0.83
0.38	0.31	0.40	0.49	0.86
1.00	0.35	0.43	0.53	0.89
3.00	0.38	0.46	0.55	0.92

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0193	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.53	0.61	0.87
0.38	0.52	0.60	0.68	0.94
1.00	0.62	0.70	0.77	1.04
3.00	0.87	0.94	1.02	1.28

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0550	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.40	0.50	0.86
0.38	0.35	0.43	0.52	0.89
1.00	0.39	0.48	0.57	0.94
3.00	0.46	0.55	0.64	1.01

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0193	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.55	0.63	0.89
0.38	0.53	0.61	0.69	0.95
1.00	0.62	0.70	0.77	1.04
3.00	0.84	0.92	1.00	1.26

Rev.1.01.10

ND5P | ND5P | 3/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0550	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.43	0.52	0.89
0.38	0.37	0.45	0.55	0.92
1.00	0.43	0.51	0.61	0.98
3.00	0.55	0.63	0.73	1.10

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0193	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.57	0.65	0.91
0.38	0.53	0.60	0.68	0.94
1.00	0.58	0.66	0.73	1.00
3.00	0.72	0.80	0.88	1.14

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0550	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.37	0.46	0.83
0.38	0.31	0.40	0.49	0.86
1.00	0.36	0.44	0.54	0.91
3.00	0.45	0.53	0.63	1.00

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0193	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.40	0.48	0.56	0.82
0.38	0.46	0.54	0.62	0.88
1.00	0.53	0.60	0.68	0.94
3.00	0.66	0.74	0.82	1.08

Rev.1.01.10

ND5P | ND5P | 4/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0550	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.39	0.48	0.85
0.38	0.34	0.42	0.51	0.88
1.00	0.40	0.48	0.57	0.94
3.00	0.52	0.60	0.70	1.07

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0193	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.49	0.57	0.83
0.38	0.46	0.53	0.61	0.87
1.00	0.50	0.58	0.66	0.92
3.00	0.60	0.68	0.76	1.02

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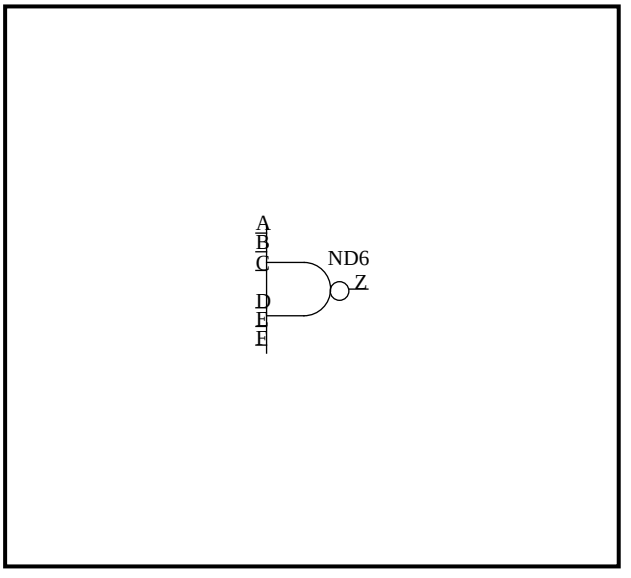
ND6	ND6	1/4

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
ND6	6-INPUT NAND	5	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT						OUTPUT
A	B	C	D	E	F	Z
H	H	H	H	H	H	L
ALL OTHER COMBINATIONS						H

Verilog-HDL DESCRIPTION

```
ND6  inst(Z,A,B,C,D,E,F);
```

VHDL DESCRIPTION

```
inst:ND6
   port   map(Z,A,B,C,D,E,F);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.10
B,D	1.03
C,E,F	0.99

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	43.1

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ND6 ND6 2/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1005	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.43	0.60	1.29
0.38	0.32	0.46	0.63	1.32
1.00	0.35	0.49	0.67	1.35
3.00	0.37	0.52	0.69	1.37

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0395	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.53	0.66	1.13
0.38	0.48	0.60	0.73	1.20
1.00	0.58	0.70	0.82	1.30
3.00	0.82	0.94	1.07	1.54

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1005	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.46	0.63	1.32
0.38	0.35	0.49	0.66	1.35
1.00	0.39	0.54	0.71	1.39
3.00	0.46	0.60	0.77	1.46

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0395	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.43	0.55	0.68	1.15
0.38	0.49	0.61	0.74	1.21
1.00	0.57	0.69	0.82	1.30
3.00	0.79	0.91	1.04	1.52

ND6 ND6 3/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1005	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.48	0.66	1.34
0.38	0.37	0.51	0.68	1.37
1.00	0.43	0.57	0.74	1.43
3.00	0.55	0.69	0.86	1.55

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0395	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.57	0.69	1.17
0.38	0.48	0.60	0.73	1.20
1.00	0.53	0.65	0.78	1.26
3.00	0.66	0.78	0.91	1.39

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1005	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.45	0.62	1.30
0.38	0.33	0.47	0.65	1.33
1.00	0.36	0.51	0.68	1.36
3.00	0.38	0.53	0.70	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0395	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.54	0.67	1.14
0.38	0.49	0.61	0.74	1.22
1.00	0.59	0.71	0.84	1.31
3.00	0.84	0.96	1.09	1.56

ND6 | ND6 | 4/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1005	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.48	0.65	1.34
0.38	0.36	0.50	0.68	1.36
1.00	0.41	0.55	0.72	1.41
3.00	0.47	0.61	0.78	1.46

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0395	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.57	0.69	1.17
0.38	0.50	0.62	0.75	1.23
1.00	0.59	0.71	0.84	1.31
3.00	0.81	0.93	1.06	1.53

PATH CONDITION

PATH	CONDITION	FUNCTION
F->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1005	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.38	0.52	0.70	1.38
0.38	0.40	0.55	0.72	1.41
1.00	0.46	0.61	0.79	1.47
3.00	0.60	0.74	0.92	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION
F->Z	---	FALL

SLEW FACTOR

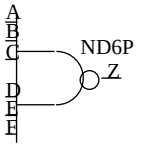
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0395	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.58	0.71	1.19
0.38	0.50	0.62	0.75	1.23
1.00	0.55	0.67	0.80	1.28
3.00	0.68	0.80	0.93	1.40

ND6P	ND6P	1/4

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
ND6P	6-INPUT NAND	5	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT						OUTPUT
A	B	C	D	E	F	Z
H	H	H	H	H	H	L
ALL OTHER COMBINATIONS						H

Verilog-HDL DESCRIPTION

```
ND6P  inst(Z,A,B,C,D,E,F);
```

VHDL DESCRIPTION

```
inst:ND6P
   port   map(Z,A,B,C,D,E,F);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A,B,E,F	0.98
C	0.97
D	0.99

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	95.3

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ND6P | ND6P | 2/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0452	0.06

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.32	0.40	0.72
0.38	0.28	0.35	0.43	0.75
1.00	0.32	0.39	0.47	0.78
3.00	0.34	0.41	0.49	0.81

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0185	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.43	0.50	0.58	0.83
0.38	0.50	0.58	0.65	0.90
1.00	0.60	0.68	0.75	1.00
3.00	0.85	0.93	1.00	1.25

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0452	0.06

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.37	0.45	0.76
0.38	0.33	0.39	0.48	0.79
1.00	0.38	0.45	0.53	0.84
3.00	0.46	0.53	0.61	0.92

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0185	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.53	0.60	0.85
0.38	0.51	0.58	0.66	0.91
1.00	0.59	0.67	0.74	0.99
3.00	0.80	0.88	0.95	1.20

ND6P | ND6P | 3/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0452	0.06

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.40	0.48	0.80
0.38	0.36	0.43	0.51	0.82
1.00	0.43	0.50	0.58	0.89
3.00	0.57	0.64	0.72	1.03

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0185	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.47	0.54	0.62	0.86
0.38	0.51	0.58	0.65	0.90
1.00	0.56	0.63	0.71	0.95
3.00	0.68	0.76	0.83	1.08

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0452	0.06

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.34	0.42	0.74
0.38	0.30	0.37	0.45	0.77
1.00	0.34	0.40	0.49	0.80
3.00	0.37	0.44	0.52	0.83

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0185	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.44	0.51	0.58	0.83
0.38	0.51	0.58	0.66	0.91
1.00	0.60	0.67	0.75	1.00
3.00	0.83	0.90	0.98	1.23

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ND6P | ND6P | 4/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0452	0.06

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.37	0.45	0.77
0.38	0.33	0.40	0.48	0.80
1.00	0.38	0.45	0.53	0.85
3.00	0.46	0.53	0.61	0.92

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0185	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.53	0.61	0.86
0.38	0.51	0.59	0.66	0.91
1.00	0.59	0.67	0.74	0.99
3.00	0.79	0.87	0.94	1.19

PATH CONDITION

PATH	CONDITION	FUNCTION
F->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0452	0.06

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.41	0.49	0.81
0.38	0.37	0.44	0.52	0.83
1.00	0.43	0.50	0.58	0.90
3.00	0.58	0.65	0.73	1.04

PATH CONDITION

PATH	CONDITION	FUNCTION
F->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0185	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.55	0.62	0.87
0.38	0.51	0.58	0.66	0.91
1.00	0.56	0.63	0.70	0.95
3.00	0.66	0.73	0.81	1.06

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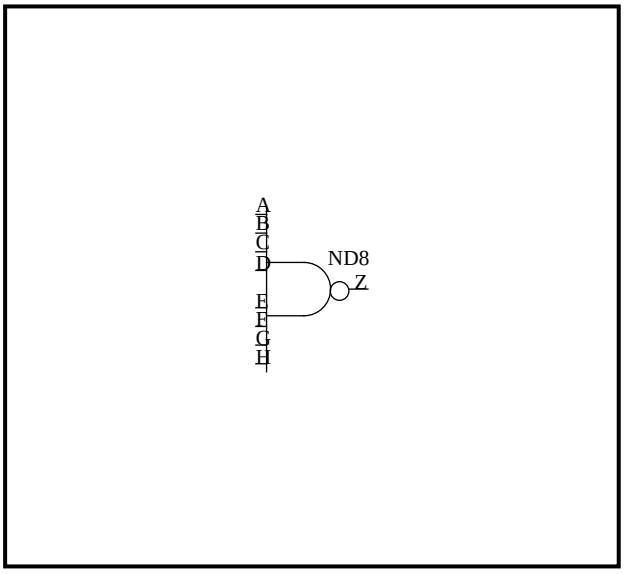
ND8	ND8	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
ND8	8-INPUT NAND	6	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT								OUTPUT
A	B	C	D	E	F	G	H	Z
H	H	H	H	H	H	H	H	L
ALL OTHER COMBINATIONS								H

Verilog-HDL DESCRIPTION

```
ND8  inst(Z,A,B,C,D,E,F,G,H);
```

VHDL DESCRIPTION

```
inst:ND8
   port   map(Z,A,B,C,D,E,F,G,H);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.09
B,F,H	1.03
C,G	0.98
D	1.07
E	1.00

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	45.4

Rev.1.01.10

ND8 ND8 2/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0942	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.42	0.58	1.22
0.38	0.31	0.45	0.61	1.25
1.00	0.34	0.47	0.64	1.28
3.00	0.34	0.47	0.63	1.27

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0392	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.43	0.55	0.67	1.14
0.38	0.50	0.62	0.74	1.21
1.00	0.61	0.72	0.85	1.32
3.00	0.89	1.01	1.14	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0942	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.45	0.61	1.25
0.38	0.34	0.48	0.64	1.28
1.00	0.38	0.52	0.68	1.32
3.00	0.42	0.55	0.71	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0392	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.58	0.70	1.17
0.38	0.52	0.64	0.76	1.23
1.00	0.62	0.73	0.86	1.32
3.00	0.88	1.00	1.12	1.59

ND8 | ND8 | 3/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0942	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.49	0.65	1.29
0.38	0.38	0.51	0.67	1.31
1.00	0.43	0.57	0.73	1.37
3.00	0.53	0.66	0.82	1.46

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0392	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.61	0.73	1.20
0.38	0.53	0.65	0.77	1.24
1.00	0.60	0.71	0.84	1.30
3.00	0.79	0.91	1.03	1.50

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0942	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.51	0.67	1.31
0.38	0.39	0.53	0.69	1.33
1.00	0.46	0.59	0.75	1.39
3.00	0.59	0.72	0.88	1.52

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0392	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.50	0.62	0.74	1.21
0.38	0.53	0.65	0.77	1.24
1.00	0.58	0.69	0.82	1.29
3.00	0.71	0.83	0.95	1.42

ND8 | ND8 | 4/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0942	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.43	0.59	1.23
0.38	0.32	0.46	0.62	1.26
1.00	0.35	0.49	0.65	1.29
3.00	0.35	0.48	0.65	1.29

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0392	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.54	0.67	1.13
0.38	0.50	0.62	0.74	1.21
1.00	0.60	0.72	0.85	1.31
3.00	0.89	1.00	1.13	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION
F->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0942	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.46	0.62	1.26
0.38	0.35	0.49	0.65	1.29
1.00	0.39	0.53	0.69	1.33
3.00	0.43	0.57	0.73	1.37

PATH CONDITION

PATH	CONDITION	FUNCTION
F->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0392	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.57	0.70	1.17
0.38	0.51	0.63	0.76	1.22
1.00	0.61	0.73	0.85	1.32
3.00	0.87	0.99	1.11	1.58

ND8 | ND8 | 5/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0942	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.50	0.66	1.30
0.38	0.39	0.52	0.68	1.32
1.00	0.45	0.58	0.74	1.38
3.00	0.55	0.68	0.84	1.48

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0392	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.60	0.73	1.19
0.38	0.53	0.64	0.77	1.23
1.00	0.59	0.70	0.83	1.30
3.00	0.77	0.89	1.01	1.48

PATH CONDITION

PATH	CONDITION	FUNCTION
H->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0942	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.50	0.66	1.30
0.38	0.39	0.52	0.68	1.32
1.00	0.45	0.58	0.74	1.38
3.00	0.57	0.70	0.86	1.50

PATH CONDITION

PATH	CONDITION	FUNCTION
H->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0392	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.50	0.61	0.74	1.20
0.38	0.53	0.64	0.77	1.23
1.00	0.57	0.69	0.81	1.28
3.00	0.70	0.82	0.94	1.41

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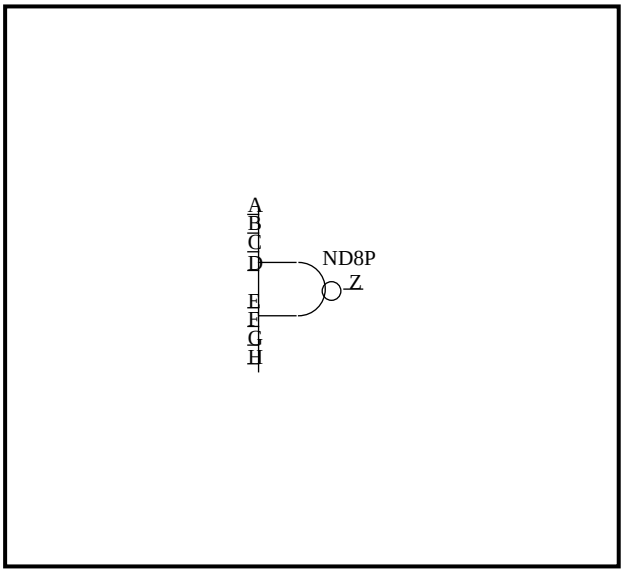
ND8P	ND8P	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
ND8P	8-INPUT NAND	6	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT								OUTPUT
A	B	C	D	E	F	G	H	Z
H	H	H	H	H	H	H	H	L
ALL OTHER COMBINATIONS								H

Verilog-HDL DESCRIPTION

```
ND8P  inst(Z,A,B,C,D,E,F,G,H);
```

VHDL DESCRIPTION

```
inst:ND8P
   port   map(Z,A,B,C,D,E,F,G,H);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	0.99
B,D,F	1.03
C	0.98
E	1.04
G	1.05
H	1.00

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	77.2

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ND8P | ND8P | 2/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0549	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.37	0.46	0.83
0.38	0.32	0.40	0.49	0.86
1.00	0.35	0.43	0.52	0.89
3.00	0.35	0.43	0.53	0.90

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0234	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.56	0.65	0.94
0.38	0.55	0.63	0.72	1.02
1.00	0.66	0.74	0.83	1.13
3.00	0.95	1.03	1.12	1.42

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0549	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.40	0.49	0.86
0.38	0.35	0.43	0.52	0.89
1.00	0.39	0.47	0.57	0.94
3.00	0.43	0.51	0.61	0.98

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0234	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.59	0.68	0.98
0.38	0.57	0.65	0.74	1.04
1.00	0.67	0.75	0.84	1.13
3.00	0.93	1.02	1.10	1.40

ND8P | ND8P | 3/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0549	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.44	0.54	0.91
0.38	0.39	0.47	0.56	0.93
1.00	0.44	0.53	0.62	0.99
3.00	0.55	0.63	0.72	1.09

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0234	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.54	0.62	0.71	1.01
0.38	0.58	0.66	0.75	1.05
1.00	0.64	0.73	0.81	1.11
3.00	0.84	0.93	1.01	1.31

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0549	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.44	0.54	0.90
0.38	0.38	0.47	0.56	0.93
1.00	0.45	0.53	0.62	0.99
3.00	0.57	0.65	0.74	1.11

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0234	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.63	0.72	1.02
0.38	0.58	0.66	0.75	1.05
1.00	0.63	0.71	0.80	1.10
3.00	0.77	0.86	0.94	1.24

ND8P | ND8P | 4/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0549	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.36	0.46	0.83
0.38	0.31	0.39	0.49	0.86
1.00	0.34	0.42	0.52	0.88
3.00	0.32	0.40	0.50	0.86

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0234	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.47	0.55	0.64	0.94
0.38	0.54	0.63	0.71	1.01
1.00	0.65	0.74	0.82	1.12
3.00	0.95	1.03	1.12	1.42

PATH CONDITION

PATH	CONDITION	FUNCTION
F->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0549	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.41	0.50	0.87
0.38	0.36	0.44	0.53	0.90
1.00	0.40	0.48	0.57	0.94
3.00	0.44	0.52	0.61	0.98

PATH CONDITION

PATH	CONDITION	FUNCTION
F->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0234	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.50	0.59	0.67	0.97
0.38	0.56	0.64	0.73	1.03
1.00	0.66	0.74	0.83	1.13
3.00	0.92	1.01	1.09	1.39

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ND8P | ND8P | 5/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0549	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.45	0.55	0.92
0.38	0.40	0.48	0.57	0.94
1.00	0.45	0.53	0.63	1.00
3.00	0.55	0.63	0.73	1.09

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0234	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.54	0.62	0.71	1.01
0.38	0.58	0.66	0.75	1.05
1.00	0.64	0.72	0.81	1.11
3.00	0.83	0.92	1.00	1.30

PATH CONDITION

PATH	CONDITION	FUNCTION
H->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0549	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.45	0.54	0.91
0.38	0.39	0.48	0.57	0.94
1.00	0.45	0.54	0.63	1.00
3.00	0.57	0.65	0.75	1.11

PATH CONDITION

PATH	CONDITION	FUNCTION
H->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0234	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.63	0.72	1.02
0.38	0.58	0.66	0.75	1.05
1.00	0.63	0.71	0.79	1.09
3.00	0.77	0.85	0.94	1.24

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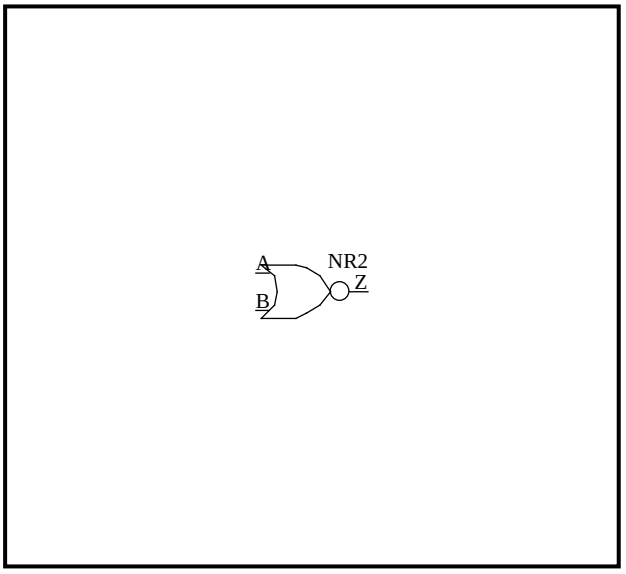
NR2	NR2	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
NR2	2-INPUT NOR	1	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
A	B	Z
L	L	H
L	H	L
H	L	L
H	H	L

Verilog-HDL DESCRIPTION

```
NR2  inst(Z,A,B);
```

VHDL DESCRIPTION

```
inst:NR2
   port   map(Z,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A,B	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	24.8

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NR2 NR2 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1782	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.41	0.72	1.96
0.38	0.18	0.43	0.74	1.97
1.00	0.24	0.49	0.80	2.02
3.00	0.40	0.70	1.02	2.24

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0411	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.06	0.16	0.28	0.76
0.38	0.12	0.24	0.37	0.85
1.00	0.14	0.32	0.48	0.99
3.00	0.13	0.41	0.66	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1782	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.19	0.44	0.75	1.98
0.38	0.18	0.43	0.74	1.98
1.00	0.21	0.46	0.76	1.98
3.00	0.31	0.58	0.88	2.07

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0411	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.07	0.17	0.29	0.77
0.38	0.13	0.25	0.38	0.86
1.00	0.17	0.33	0.49	1.00
3.00	0.18	0.45	0.68	1.36

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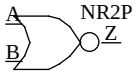
NR2P	NR2P	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
NR2P	2-INPUT NOR	2	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
A	B	Z
L	L	H
L	H	L
H	L	L
H	H	L

Verilog-HDL DESCRIPTION

```
NR2P  inst(Z,A,B);
```

VHDL DESCRIPTION

```
inst:NR2P
   port   map(Z,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A,B	2.07

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	48.8

Rev.1.01.10

NR2P NR2P 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0888	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.26	0.42	1.04
0.38	0.15	0.27	0.43	1.04
1.00	0.21	0.34	0.49	1.10
3.00	0.36	0.52	0.70	1.33

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0193	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.05	0.10	0.16	0.40
0.38	0.10	0.17	0.24	0.49
1.00	0.11	0.22	0.32	0.61
3.00	0.08	0.25	0.41	0.86

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0888	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.28	0.43	1.05
0.38	0.14	0.27	0.43	1.05
1.00	0.17	0.30	0.45	1.06
3.00	0.27	0.41	0.57	1.17

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0193	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.06	0.11	0.17	0.41
0.38	0.11	0.18	0.25	0.49
1.00	0.13	0.23	0.33	0.62
3.00	0.14	0.29	0.44	0.88

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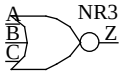
NR3	NR3	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
NR3	3-INPUT NOR	2	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
A	B	C	Z
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	L

Verilog-HDL DESCRIPTION

```
NR3  inst(Z,A,B,C);
```

VHDL DESCRIPTION

```
inst:NR3
   port   map(Z,A,B,C);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.07
B	1.03
C	0.99

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	16.8

Rev.1.01.10

NR3 NR3 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.2674	0.42

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.67	1.14	3.03
0.38	0.29	0.66	1.14	3.03
1.00	0.37	0.73	1.19	3.06
3.00	0.61	1.00	1.45	3.27

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0413	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.07	0.17	0.29	0.77
0.38	0.13	0.25	0.38	0.86
1.00	0.16	0.33	0.49	1.00
3.00	0.13	0.41	0.66	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.2674	0.42

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.72	1.19	3.07
0.38	0.32	0.70	1.17	3.07
1.00	0.36	0.73	1.19	3.07
3.00	0.55	0.92	1.37	3.18

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0413	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.08	0.18	0.30	0.78
0.38	0.15	0.26	0.38	0.87
1.00	0.18	0.34	0.50	1.01
3.00	0.17	0.44	0.68	1.36

NR3 NR3 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.2674	0.42

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.73	1.21	3.09
0.38	0.33	0.71	1.19	3.08
1.00	0.34	0.70	1.16	3.04
3.00	0.47	0.82	1.25	3.04

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

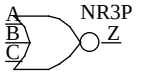
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0413	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.08	0.18	0.29	0.74
0.38	0.14	0.25	0.37	0.83
1.00	0.18	0.34	0.48	0.97
3.00	0.18	0.43	0.66	1.31

NR3P	NR3P	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
NR3P	3-INPUT NOR	3	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
A	B	C	Z
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	L

Verilog-HDL DESCRIPTION

```
NR3P  inst(Z,A,B,C);
```

VHDL DESCRIPTION

```
inst:NR3P
   port   map(Z,A,B,C);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	2.10
B	2.02
C	1.96

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	32.4

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NR3P NR3P 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1381	0.42

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.44	0.69	1.66
0.38	0.25	0.44	0.68	1.66
1.00	0.33	0.52	0.75	1.70
3.00	0.56	0.78	1.02	1.96

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0229	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.06	0.11	0.17	0.41
0.38	0.12	0.18	0.25	0.50
1.00	0.13	0.23	0.33	0.62
3.00	0.08	0.25	0.41	0.86

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1381	0.42

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.49	0.74	1.71
0.38	0.27	0.47	0.72	1.70
1.00	0.32	0.51	0.75	1.71
3.00	0.51	0.72	0.95	1.87

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0229	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.07	0.12	0.18	0.42
0.38	0.13	0.19	0.26	0.51
1.00	0.15	0.25	0.34	0.63
3.00	0.12	0.28	0.44	0.88

Rev.1.01.10

NR3P | NR3P | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1381	0.42

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.52	0.76	1.74
0.38	0.29	0.49	0.74	1.72
1.00	0.30	0.48	0.72	1.69
3.00	0.40	0.60	0.82	1.72

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0229	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.08	0.15	0.22	0.50
0.38	0.15	0.22	0.30	0.58
1.00	0.19	0.29	0.39	0.71
3.00	0.20	0.36	0.52	0.98

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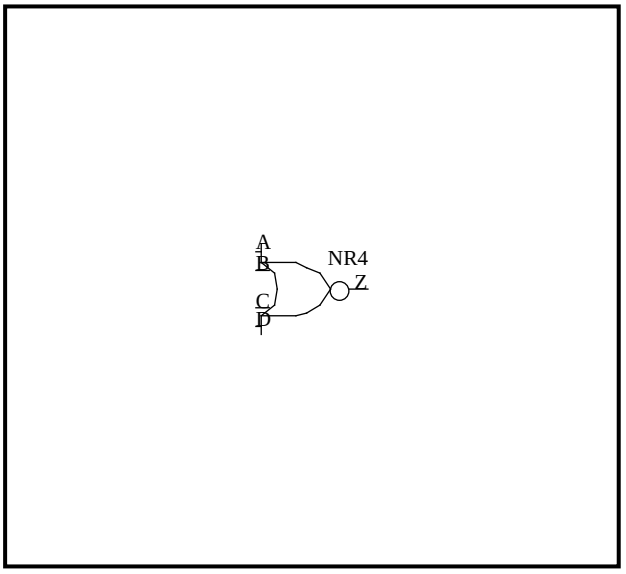
NR4	NR4	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
NR4	4-INPUT NOR	2	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT
A	B	C	D	Z
L	L	L	L	H
ALL OTHER COMBINATIONS				L

Verilog-HDL DESCRIPTION

```
NR4  inst(Z,A,B,C,D);
```

VHDL DESCRIPTION

```
inst:NR4
   port   map(Z,A,B,C,D);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.07
B	1.04
C	0.98
D	1.00

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	12.6

Rev.1.01.10

NR4 NR4 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.3546	0.60

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.37	0.87	1.50	4.00
0.38	0.36	0.86	1.49	4.00
1.00	0.45	0.93	1.54	4.03
3.00	0.73	1.22	1.82	4.22

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0416	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.07	0.17	0.29	0.76
0.38	0.14	0.25	0.38	0.85
1.00	0.17	0.33	0.49	1.00
3.00	0.12	0.40	0.65	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.3546	0.60

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.95	1.58	4.08
0.38	0.41	0.92	1.56	4.07
1.00	0.46	0.95	1.57	4.07
3.00	0.70	1.18	1.77	4.19

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0416	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.08	0.18	0.30	0.77
0.38	0.15	0.26	0.39	0.86
1.00	0.18	0.35	0.50	1.01
3.00	0.15	0.43	0.67	1.35

NR4 NR4 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.3546	0.60

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	1.01	1.64	4.15
0.38	0.47	0.98	1.62	4.13
1.00	0.47	0.97	1.59	4.10
3.00	0.64	1.11	1.69	4.10

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0416	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.19	0.31	0.79
0.38	0.15	0.27	0.40	0.88
1.00	0.19	0.36	0.51	1.02
3.00	0.18	0.45	0.69	1.37

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.3546	0.60

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	1.03	1.66	4.16
0.38	0.48	1.00	1.63	4.15
1.00	0.46	0.96	1.58	4.09
3.00	0.61	1.07	1.64	4.04

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	FALL

SLEW FACTOR

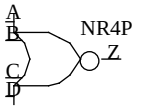
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0416	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.19	0.32	0.80
0.38	0.15	0.27	0.40	0.89
1.00	0.20	0.36	0.52	1.03
3.00	0.19	0.46	0.70	1.38

NR4P	NR4P	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
NR4P	4-INPUT NOR	4	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT
A	B	C	D	Z
L	L	L	L	H
ALL OTHER COMBINATIONS				L

Verilog-HDL DESCRIPTION

```
NR4P  inst(Z,A,B,C,D);
```

VHDL DESCRIPTION

```
inst:NR4P
   port   map(Z,A,B,C,D);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.98
B	2.09
C	2.14
D	2.16

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	23.9

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NR4P NR4P 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1872	0.64

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.58	0.91	2.22
0.38	0.32	0.57	0.90	2.22
1.00	0.41	0.66	0.97	2.26
3.00	0.68	0.95	1.27	2.52

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0184	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.06	0.11	0.16	0.39
0.38	0.12	0.18	0.25	0.48
1.00	0.14	0.23	0.33	0.61
3.00	0.07	0.24	0.40	0.85

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1872	0.64

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.68	1.01	2.32
0.38	0.37	0.64	0.98	2.30
1.00	0.42	0.69	1.01	2.31
3.00	0.67	0.92	1.24	2.49

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0184	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.07	0.12	0.17	0.41
0.38	0.13	0.19	0.26	0.50
1.00	0.16	0.25	0.34	0.62
3.00	0.11	0.27	0.42	0.86

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NR4P NR4P 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1872	0.64

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.74	1.07	2.38
0.38	0.43	0.70	1.03	2.36
1.00	0.43	0.69	1.02	2.32
3.00	0.60	0.85	1.16	2.39

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0184	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.07	0.12	0.18	0.42
0.38	0.14	0.20	0.27	0.51
1.00	0.17	0.26	0.35	0.63
3.00	0.13	0.29	0.45	0.88

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.1872	0.64

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.49	0.76	1.08	2.40
0.38	0.44	0.71	1.05	2.37
1.00	0.42	0.69	1.01	2.32
3.00	0.59	0.83	1.13	2.35

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	FALL

SLEW FACTOR

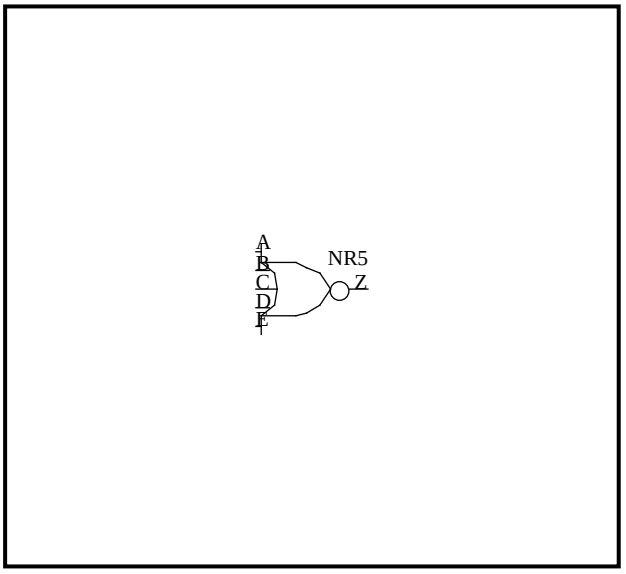
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0184	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.06	0.11	0.17	0.39
0.38	0.12	0.19	0.25	0.47
1.00	0.15	0.24	0.33	0.59
3.00	0.11	0.27	0.42	0.83

NR5	NR5	1/4

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
NR5	5-INPUT NOR	4	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT					OUTPUT
A	B	C	D	E	Z
L	L	L	L	L	H
ALL OTHER COMBINATIONS					L

Verilog-HDL DESCRIPTION

```
NR5  inst(Z,A,B,C,D,E);
```

VHDL DESCRIPTION

```
inst:NR5
   port   map(Z,A,B,C,D,E);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.04
B	0.99
C	0.98
D	1.05
E	1.07

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	44.5

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NR5 NR5 2/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0964	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.70	0.87	1.54
0.38	0.55	0.70	0.87	1.54
1.00	0.64	0.79	0.96	1.63
3.00	0.92	1.06	1.24	1.91

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0401	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.36	0.48	0.95
0.38	0.32	0.43	0.55	1.01
1.00	0.36	0.47	0.59	1.06
3.00	0.37	0.47	0.59	1.06

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0964	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.60	0.75	0.92	1.59
0.38	0.58	0.73	0.90	1.57
1.00	0.64	0.78	0.96	1.63
3.00	0.86	1.01	1.18	1.85

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0401	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.37	0.49	0.96
0.38	0.34	0.44	0.56	1.03
1.00	0.39	0.49	0.61	1.08
3.00	0.42	0.52	0.64	1.11

NR5 NR5 3/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0964	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.63	0.77	0.95	1.62
0.38	0.60	0.75	0.92	1.59
1.00	0.61	0.76	0.93	1.60
3.00	0.78	0.93	1.10	1.77

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0401	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.38	0.51	0.97
0.38	0.35	0.46	0.58	1.04
1.00	0.41	0.52	0.64	1.10
3.00	0.46	0.57	0.70	1.16

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0964	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.38	0.53	0.70	1.37
0.38	0.40	0.54	0.72	1.38
1.00	0.48	0.62	0.79	1.46
3.00	0.68	0.82	0.99	1.66

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0401	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.38	0.50	0.96
0.38	0.33	0.44	0.56	1.03
1.00	0.37	0.48	0.60	1.07
3.00	0.39	0.50	0.63	1.09

NR5 NR5 4/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0964	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.55	0.72	1.39
0.38	0.40	0.54	0.71	1.38
1.00	0.44	0.58	0.76	1.42
3.00	0.58	0.73	0.90	1.57

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0401	0.07

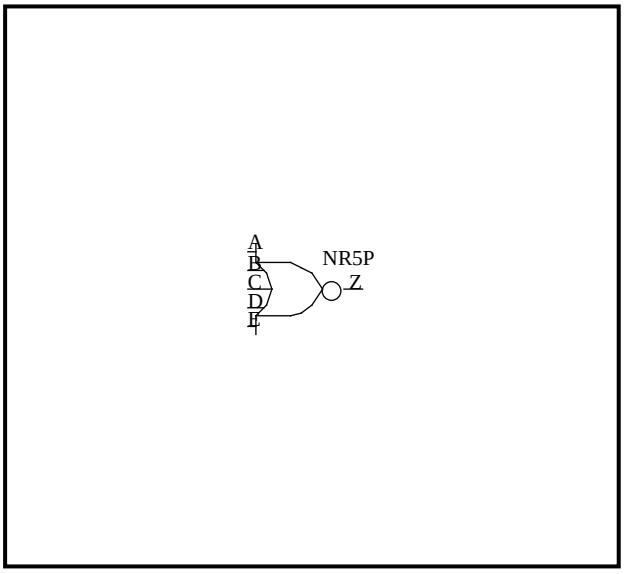
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.39	0.52	0.98
0.38	0.34	0.45	0.58	1.04
1.00	0.39	0.51	0.63	1.09
3.00	0.48	0.59	0.71	1.18

Rev.1.01.10

NR5P	NR5P	1/4

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
NR5P	5-INPUT NOR	5	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT					OUTPUT
A	B	C	D	E	Z
L	L	L	L	L	H
ALL OTHER COMBINATIONS					L

Verilog-HDL DESCRIPTION

```
NR5P  inst(Z,A,B,C,D,E);
```

VHDL DESCRIPTION

```
inst:NR5P
   port   map(Z,A,B,C,D,E);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.07
B	1.04
C	0.99
D	1.01
E	1.02

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	86.2

Rev.1.01.10

NR5P NR5P 2/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0467	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.63	0.72	1.05
0.38	0.55	0.63	0.72	1.05
1.00	0.64	0.72	0.81	1.14
3.00	0.92	0.99	1.08	1.41

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0238	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.35	0.42	0.71
0.38	0.34	0.41	0.49	0.78
1.00	0.38	0.46	0.53	0.82
3.00	0.39	0.46	0.54	0.82

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0467	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.60	0.68	0.77	1.10
0.38	0.58	0.66	0.74	1.08
1.00	0.64	0.71	0.80	1.13
3.00	0.86	0.94	1.02	1.36

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0238	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.36	0.43	0.72
0.38	0.36	0.43	0.51	0.79
1.00	0.41	0.48	0.56	0.84
3.00	0.44	0.51	0.59	0.87

Rev.1.01.10

NR5P NR5P 3/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0467	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.62	0.70	0.79	1.12
0.38	0.59	0.67	0.76	1.09
1.00	0.61	0.69	0.78	1.11
3.00	0.79	0.86	0.95	1.28

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0238	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.36	0.44	0.72
0.38	0.36	0.43	0.51	0.79
1.00	0.41	0.48	0.56	0.84
3.00	0.46	0.53	0.61	0.89

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0467	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.39	0.47	0.56	0.89
0.38	0.41	0.48	0.57	0.90
1.00	0.48	0.56	0.65	0.98
3.00	0.69	0.76	0.85	1.18

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0238	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.36	0.44	0.72
0.38	0.35	0.42	0.50	0.79
1.00	0.38	0.46	0.54	0.83
3.00	0.41	0.49	0.57	0.85

Rev.1.01.10

NR5P | NR5P | 4/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0467	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.48	0.57	0.90
0.38	0.40	0.48	0.57	0.90
1.00	0.45	0.53	0.61	0.94
3.00	0.59	0.66	0.75	1.08

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0238	0.08

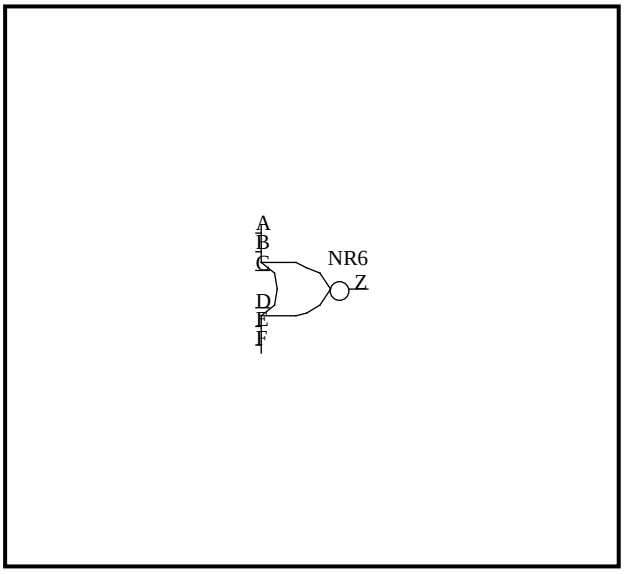
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.37	0.45	0.74
0.38	0.36	0.44	0.52	0.80
1.00	0.41	0.49	0.57	0.85
3.00	0.48	0.56	0.64	0.93

Rev.1.01.10

NR6	NR6	1/4

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
NR6	6-INPUT NOR	5	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT						OUTPUT
A	B	C	D	E	F	Z
L	L	L	L	L	L	H
ALL OTHER COMBINATIONS						L

Verilog-HDL DESCRIPTION

```
NR6  inst(Z,A,B,C,D,E,F);
```

VHDL DESCRIPTION

```
inst:NR6
   port   map(Z,A,B,C,D,E,F);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.04
B,F	0.99
C	0.98
D	1.08
E	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	44.4

Rev.1.01.10

NR6 NR6 2/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0964	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.54	0.69	0.86	1.53
0.38	0.54	0.69	0.86	1.53
1.00	0.64	0.78	0.95	1.62
3.00	0.91	1.06	1.23	1.90

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0402	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.35	0.47	0.93
0.38	0.31	0.42	0.53	1.00
1.00	0.35	0.46	0.58	1.04
3.00	0.36	0.46	0.58	1.04

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0964	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.59	0.74	0.91	1.58
0.38	0.57	0.72	0.89	1.56
1.00	0.63	0.78	0.95	1.62
3.00	0.86	1.00	1.17	1.85

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0402	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.36	0.48	0.94
0.38	0.33	0.43	0.55	1.01
1.00	0.38	0.48	0.60	1.06
3.00	0.41	0.51	0.63	1.09

NR6 NR6 3/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0964	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.62	0.77	0.94	1.61
0.38	0.59	0.74	0.91	1.58
1.00	0.61	0.75	0.92	1.60
3.00	0.78	0.92	1.09	1.76

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0402	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.37	0.49	0.95
0.38	0.34	0.44	0.56	1.03
1.00	0.40	0.50	0.62	1.09
3.00	0.45	0.56	0.68	1.15

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0964	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.65	0.82	1.49
0.38	0.51	0.65	0.82	1.49
1.00	0.60	0.75	0.92	1.59
3.00	0.87	1.01	1.18	1.85

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0402	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.37	0.49	0.95
0.38	0.33	0.44	0.56	1.02
1.00	0.37	0.48	0.60	1.06
3.00	0.38	0.48	0.60	1.07

NR6 NR6 4/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0964	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.56	0.70	0.87	1.54
0.38	0.54	0.68	0.85	1.52
1.00	0.59	0.74	0.91	1.58
3.00	0.81	0.95	1.13	1.79

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0402	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.38	0.50	0.96
0.38	0.34	0.45	0.57	1.03
1.00	0.39	0.50	0.62	1.09
3.00	0.43	0.54	0.66	1.12

PATH CONDITION

PATH	CONDITION	FUNCTION
F->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0964	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.58	0.72	0.89	1.56
0.38	0.55	0.69	0.86	1.53
1.00	0.57	0.71	0.88	1.55
3.00	0.73	0.88	1.05	1.72

PATH CONDITION

PATH	CONDITION	FUNCTION
F->Z	---	FALL

SLEW FACTOR

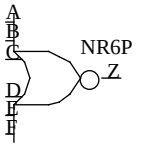
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0402	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.38	0.50	0.96
0.38	0.34	0.45	0.57	1.03
1.00	0.40	0.51	0.63	1.09
3.00	0.45	0.56	0.68	1.14

NR6P	NR6P	1/4

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
NR6P	6-INPUT NOR	5	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT						OUTPUT
A	B	C	D	E	F	Z
L	L	L	L	L	L	H
ALL OTHER COMBINATIONS						L

Verilog-HDL DESCRIPTION

```
NR6P  inst(Z,A,B,C,D,E,F);
```

VHDL DESCRIPTION

```
inst:NR6P
   port   map(Z,A,B,C,D,E,F);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A,C	0.98
B,D,E	0.99
F	0.97

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	96.5

Rev.1.01.10

NR6P NR6P 2/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0448	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.57	0.64	0.72	1.04
0.38	0.57	0.64	0.72	1.04
1.00	0.66	0.74	0.82	1.14
3.00	0.95	1.02	1.11	1.42

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0184	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.32	0.38	0.61
0.38	0.32	0.38	0.45	0.68
1.00	0.36	0.42	0.49	0.72
3.00	0.35	0.41	0.48	0.71

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0448	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.63	0.70	0.78	1.10
0.38	0.61	0.68	0.76	1.08
1.00	0.66	0.74	0.82	1.14
3.00	0.90	0.97	1.05	1.37

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0184	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.33	0.40	0.63
0.38	0.34	0.41	0.47	0.70
1.00	0.40	0.46	0.53	0.76
3.00	0.43	0.49	0.56	0.79

Rev.1.01.10

NR6P NR6P 3/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0448	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.65	0.72	0.81	1.12
0.38	0.62	0.69	0.77	1.09
1.00	0.64	0.71	0.79	1.11
3.00	0.82	0.89	0.98	1.29

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0184	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.33	0.39	0.62
0.38	0.34	0.40	0.47	0.69
1.00	0.39	0.45	0.52	0.75
3.00	0.43	0.49	0.56	0.79

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0448	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.54	0.61	0.70	1.01
0.38	0.54	0.61	0.69	1.01
1.00	0.63	0.70	0.79	1.11
3.00	0.91	0.98	1.07	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0184	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.33	0.40	0.63
0.38	0.33	0.40	0.47	0.70
1.00	0.38	0.44	0.51	0.74
3.00	0.38	0.44	0.51	0.74

NR6P | NR6P | 4/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0448	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.60	0.67	0.75	1.07
0.38	0.57	0.65	0.73	1.05
1.00	0.63	0.70	0.79	1.11
3.00	0.86	0.93	1.02	1.33

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0184	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.34	0.41	0.64
0.38	0.35	0.41	0.48	0.71
1.00	0.40	0.46	0.53	0.76
3.00	0.43	0.49	0.56	0.79

PATH CONDITION

PATH	CONDITION	FUNCTION
F->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0448	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.62	0.69	0.78	1.09
0.38	0.59	0.66	0.74	1.06
1.00	0.60	0.68	0.76	1.08
3.00	0.79	0.86	0.94	1.26

PATH CONDITION

PATH	CONDITION	FUNCTION
F->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0184	0.08

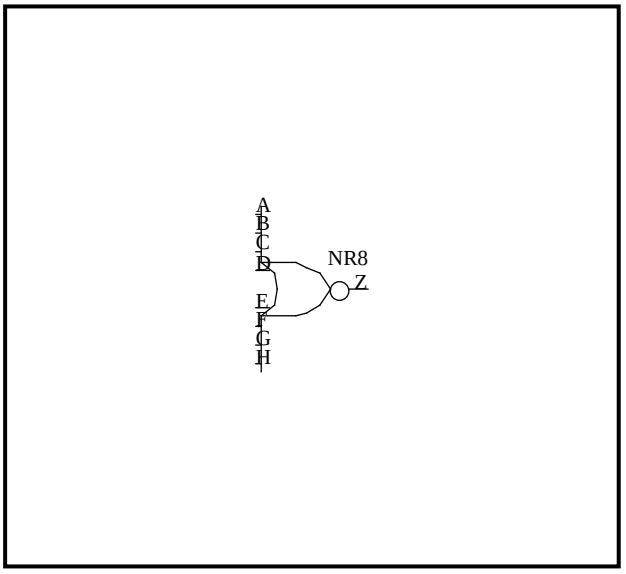
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.33	0.40	0.63
0.38	0.34	0.40	0.47	0.70
1.00	0.39	0.46	0.52	0.75
3.00	0.42	0.49	0.56	0.79

Rev.1.01.10

NR8	NR8	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
NR8	8-INPUT NOR	6	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT								OUTPUT
A	B	C	D	E	F	G	H	Z
L	L	L	L	L	L	L	L	H
ALL OTHER COMBINATIONS								L

Verilog-HDL DESCRIPTION

```
NR8  inst(Z,A,B,C,D,E,F,G,H);
```

VHDL DESCRIPTION

```
inst:NR8
   port   map(Z,A,B,C,D,E,F,G,H);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.12
B,F,H	1.03
C,G	0.98
D,E	1.00

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	47.6

Rev.1.01.10

NR8 NR8 2/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0877	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.61	0.74	0.90	1.51
0.38	0.60	0.73	0.89	1.50
1.00	0.70	0.83	0.99	1.60
3.00	1.00	1.13	1.29	1.91

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0398	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.36	0.47	0.93
0.38	0.32	0.43	0.54	1.00
1.00	0.36	0.47	0.58	1.04
3.00	0.35	0.46	0.58	1.03

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0877	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.69	0.82	0.97	1.59
0.38	0.65	0.79	0.94	1.56
1.00	0.72	0.85	1.00	1.62
3.00	0.96	1.10	1.25	1.87

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0398	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.37	0.48	0.94
0.38	0.34	0.44	0.56	1.01
1.00	0.38	0.49	0.61	1.06
3.00	0.40	0.50	0.62	1.08

Rev.1.01.10

NR8 NR8 3/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0877	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.75	0.88	1.04	1.65
0.38	0.71	0.84	1.00	1.61
1.00	0.72	0.85	1.01	1.62
3.00	0.91	1.04	1.20	1.81

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0398	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.38	0.49	0.95
0.38	0.35	0.45	0.57	1.02
1.00	0.40	0.51	0.62	1.08
3.00	0.44	0.54	0.66	1.12

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0877	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.76	0.89	1.05	1.66
0.38	0.71	0.85	1.00	1.62
1.00	0.70	0.84	0.99	1.61
3.00	0.87	1.01	1.16	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0398	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.38	0.49	0.95
0.38	0.35	0.45	0.57	1.02
1.00	0.40	0.51	0.63	1.08
3.00	0.44	0.55	0.67	1.13

Rev.1.01.10

NR8 NR8 4/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0877	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.60	0.73	0.89	1.51
0.38	0.59	0.73	0.88	1.50
1.00	0.69	0.83	0.98	1.60
3.00	1.00	1.13	1.29	1.90

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0398	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.38	0.50	0.96
0.38	0.35	0.46	0.58	1.03
1.00	0.39	0.50	0.62	1.08
3.00	0.38	0.49	0.61	1.07

PATH CONDITION

PATH	CONDITION	FUNCTION
F->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0877	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.68	0.81	0.97	1.59
0.38	0.65	0.78	0.94	1.56
1.00	0.71	0.84	1.00	1.62
3.00	0.96	1.09	1.25	1.87

PATH CONDITION

PATH	CONDITION	FUNCTION
F->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0398	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.39	0.51	0.97
0.38	0.36	0.47	0.59	1.05
1.00	0.41	0.52	0.64	1.10
3.00	0.43	0.54	0.66	1.12

NR8 NR8 5/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0877	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.74	0.87	1.03	1.65
0.38	0.70	0.83	0.99	1.61
1.00	0.71	0.85	1.00	1.62
3.00	0.90	1.03	1.19	1.81

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0398	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.41	0.53	0.98
0.38	0.37	0.48	0.60	1.06
1.00	0.43	0.54	0.66	1.12
3.00	0.47	0.58	0.70	1.16

PATH CONDITION

PATH	CONDITION	FUNCTION
H->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0877	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.75	0.89	1.04	1.66
0.38	0.71	0.84	1.00	1.62
1.00	0.70	0.83	0.99	1.61
3.00	0.88	1.01	1.17	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION
H->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0398	0.07

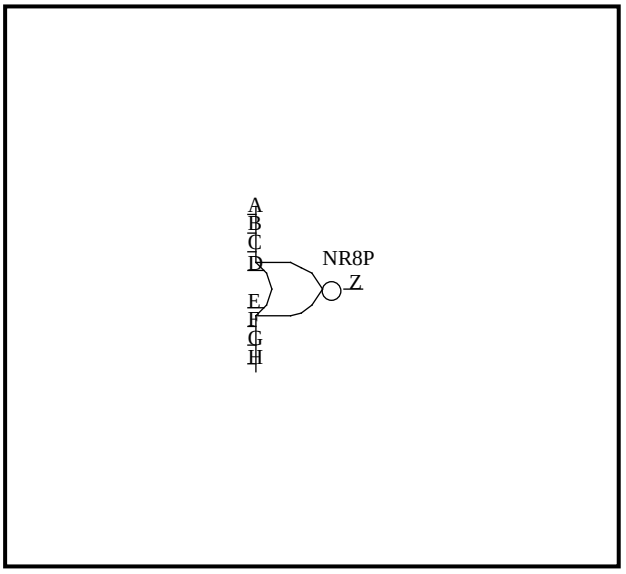
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.40	0.52	0.97
0.38	0.36	0.47	0.59	1.05
1.00	0.41	0.52	0.64	1.10
3.00	0.44	0.55	0.67	1.13

Rev.1.01.10

NR8P	NR8P	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
NR8P	8-INPUT NOR	6	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT								OUTPUT
A	B	C	D	E	F	G	H	Z
L	L	L	L	L	L	L	L	H
ALL OTHER COMBINATIONS								L

Verilog-HDL DESCRIPTION

```
NR8P  inst(Z,A,B,C,D,E,F,G,H);
```

VHDL DESCRIPTION

```
inst:NR8P
   port   map(Z,A,B,C,D,E,F,G,H);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.06
B	1.04
C,G	0.98
D	1.07
E	0.99
F,H	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	77.7

Rev.1.01.10

NR8P NR8P 2/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0545	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.62	0.71	0.80	1.18
0.38	0.62	0.70	0.80	1.17
1.00	0.71	0.80	0.89	1.27
3.00	1.02	1.10	1.20	1.57

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0238	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.34	0.42	0.70
0.38	0.34	0.41	0.49	0.77
1.00	0.38	0.45	0.53	0.81
3.00	0.37	0.44	0.52	0.81

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0545	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.70	0.78	0.88	1.25
0.38	0.67	0.75	0.85	1.22
1.00	0.73	0.81	0.91	1.28
3.00	0.98	1.07	1.16	1.53

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0238	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.35	0.43	0.71
0.38	0.35	0.43	0.51	0.79
1.00	0.40	0.48	0.55	0.84
3.00	0.42	0.49	0.57	0.85

NR8P NR8P 3/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0545	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.76	0.85	0.94	1.31
0.38	0.72	0.81	0.90	1.27
1.00	0.73	0.82	0.91	1.28
3.00	0.92	1.01	1.10	1.47

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0238	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.36	0.44	0.72
0.38	0.36	0.44	0.52	0.80
1.00	0.42	0.49	0.57	0.86
3.00	0.46	0.53	0.61	0.89

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0545	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.78	0.86	0.96	1.33
0.38	0.73	0.82	0.91	1.28
1.00	0.72	0.81	0.90	1.27
3.00	0.89	0.97	1.07	1.44

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0238	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.37	0.44	0.73
0.38	0.36	0.44	0.52	0.80
1.00	0.42	0.50	0.58	0.86
3.00	0.47	0.54	0.62	0.90

NR8P NR8P 4/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0545	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.61	0.69	0.79	1.16
0.38	0.60	0.68	0.78	1.15
1.00	0.70	0.78	0.88	1.25
3.00	1.00	1.08	1.18	1.55

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0238	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.36	0.45	0.73
0.38	0.36	0.44	0.52	0.80
1.00	0.40	0.48	0.56	0.85
3.00	0.40	0.48	0.56	0.84

PATH CONDITION

PATH	CONDITION	FUNCTION
F->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0545	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.68	0.77	0.86	1.24
0.38	0.65	0.74	0.83	1.20
1.00	0.71	0.80	0.89	1.27
3.00	0.96	1.05	1.14	1.52

PATH CONDITION

PATH	CONDITION	FUNCTION
F->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0238	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.37	0.45	0.74
0.38	0.37	0.45	0.53	0.82
1.00	0.42	0.50	0.58	0.87
3.00	0.44	0.52	0.60	0.89

NR8P NR8P 5/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0545	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.74	0.83	0.92	1.30
0.38	0.70	0.79	0.88	1.26
1.00	0.71	0.80	0.90	1.27
3.00	0.90	0.99	1.08	1.46

PATH CONDITION

PATH	CONDITION	FUNCTION
G->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0238	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.39	0.47	0.75
0.38	0.38	0.46	0.54	0.83
1.00	0.44	0.52	0.60	0.89
3.00	0.48	0.56	0.64	0.93

PATH CONDITION

PATH	CONDITION	FUNCTION
H->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0545	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.75	0.84	0.93	1.31
0.38	0.71	0.79	0.89	1.26
1.00	0.70	0.79	0.88	1.26
3.00	0.88	0.96	1.06	1.43

PATH CONDITION

PATH	CONDITION	FUNCTION
H->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0238	0.08

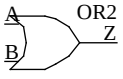
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.38	0.46	0.74
0.38	0.37	0.45	0.53	0.82
1.00	0.43	0.50	0.59	0.87
3.00	0.46	0.54	0.62	0.91

Rev.1.01.10

OR2	OR2	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
OR2	2-INPUT OR	2	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
A	B	Z
L	L	L
L	H	H
H	L	H
H	H	H

Verilog-HDL DESCRIPTION

```
OR2  inst(Z,A,B);
```

VHDL DESCRIPTION

```
inst:OR2
   port   map(Z,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.08
B	1.09

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	45.4

Rev.1.01.10

OR2 OR2 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0942	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.28	0.44	1.08
0.38	0.21	0.34	0.50	1.14
1.00	0.24	0.38	0.54	1.18
3.00	0.26	0.40	0.57	1.21

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0393	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.37	0.50	0.96
0.38	0.27	0.39	0.51	0.98
1.00	0.35	0.47	0.59	1.06
3.00	0.55	0.67	0.80	1.27

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0942	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.29	0.45	1.09
0.38	0.22	0.35	0.52	1.16
1.00	0.27	0.41	0.57	1.21
3.00	0.34	0.48	0.64	1.29

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0393	0.10

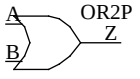
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.39	0.52	0.98
0.38	0.27	0.39	0.51	0.98
1.00	0.31	0.43	0.56	1.02
3.00	0.44	0.57	0.70	1.18

Rev.1.01.10

OR2P	OR2P	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
OR2P	2-INPUT OR	2	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
A	B	Z
L	L	L
L	H	H
H	L	H
H	H	H

Verilog-HDL DESCRIPTION

```
OR2P  inst(Z,A,B);
```

VHDL DESCRIPTION

```
inst:OR2P
   port   map(Z,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.08
B	1.04

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	77.5

Rev.1.01.10

OR2P | OR2P | 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0549	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.22	0.32	0.69
0.38	0.22	0.30	0.39	0.76
1.00	0.27	0.35	0.45	0.82
3.00	0.33	0.41	0.51	0.88

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0236	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.38	0.47	0.77
0.38	0.31	0.40	0.48	0.78
1.00	0.39	0.48	0.56	0.87
3.00	0.61	0.70	0.79	1.09

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0549	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.23	0.33	0.70
0.38	0.23	0.31	0.40	0.77
1.00	0.30	0.38	0.47	0.84
3.00	0.39	0.48	0.57	0.94

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

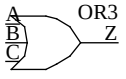
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0236	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.40	0.49	0.79
0.38	0.31	0.39	0.48	0.78
1.00	0.35	0.44	0.52	0.83
3.00	0.50	0.59	0.68	0.98

OR3	OR3	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
OR3	3-INPUT OR	2	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
A	B	C	Z
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	H

Verilog-HDL DESCRIPTION

```
OR3  inst(Z,A,B,C);
```

VHDL DESCRIPTION

```
inst:OR3
   port   map(Z,A,B,C);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.06
B	1.02
C	0.98

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	46.7

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OR3 OR3 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0888	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.28	0.44	1.05
0.38	0.22	0.35	0.51	1.12
1.00	0.26	0.39	0.55	1.16
3.00	0.26	0.40	0.55	1.17

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0394	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.39	0.53	0.67	1.17
0.38	0.39	0.53	0.67	1.17
1.00	0.48	0.62	0.76	1.26
3.00	0.75	0.89	1.04	1.54

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0888	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.29	0.45	1.06
0.38	0.23	0.36	0.52	1.13
1.00	0.29	0.42	0.57	1.19
3.00	0.31	0.45	0.60	1.22

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0394	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.44	0.58	0.72	1.22
0.38	0.42	0.56	0.70	1.20
1.00	0.47	0.61	0.76	1.26
3.00	0.69	0.83	0.98	1.48

OR3 OR3 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0888	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.28	0.44	1.05
0.38	0.23	0.36	0.51	1.12
1.00	0.29	0.41	0.57	1.18
3.00	0.35	0.48	0.63	1.24

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

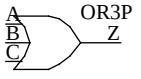
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0394	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.60	0.74	1.24
0.38	0.43	0.57	0.71	1.21
1.00	0.44	0.58	0.73	1.23
3.00	0.59	0.73	0.88	1.38

OR3P	OR3P	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
OR3P	3-INPUT OR	3	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
A	B	C	Z
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	H

Verilog-HDL DESCRIPTION

```
OR3P  inst(Z,A,B,C);
```

VHDL DESCRIPTION

```
inst:OR3P
   port   map(Z,A,B,C);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.07
B	1.04
C	0.99

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	84.3

Rev.1.01.10

OR3P | OR3P | 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0469	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.22	0.31	0.64
0.38	0.23	0.30	0.39	0.72
1.00	0.29	0.36	0.45	0.78
3.00	0.32	0.40	0.49	0.82

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0239	0.21

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.47	0.57	0.66	0.99
0.38	0.46	0.56	0.66	0.99
1.00	0.55	0.65	0.75	1.07
3.00	0.84	0.94	1.04	1.36

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0469	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.23	0.32	0.65
0.38	0.24	0.31	0.40	0.73
1.00	0.31	0.38	0.47	0.80
3.00	0.37	0.44	0.53	0.86

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0239	0.21

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.61	0.71	1.04
0.38	0.50	0.59	0.69	1.02
1.00	0.55	0.65	0.74	1.07
3.00	0.77	0.87	0.97	1.30

OR3P | OR3P | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0469	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.24	0.32	0.65
0.38	0.24	0.31	0.40	0.73
1.00	0.31	0.38	0.47	0.80
3.00	0.38	0.46	0.55	0.88

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0239	0.21

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.54	0.63	0.73	1.06
0.38	0.51	0.61	0.70	1.03
1.00	0.52	0.62	0.72	1.04
3.00	0.68	0.78	0.88	1.21

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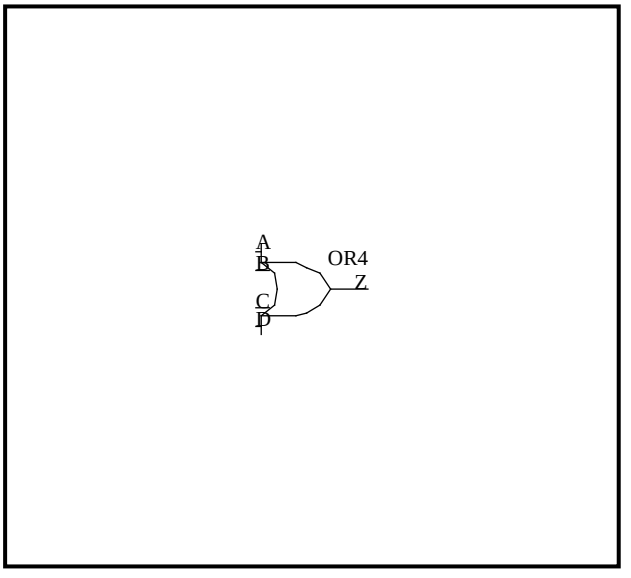
OR4	OR4	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
OR4	4-INPUT OR	3	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT
A	B	C	D	Z
L	L	L	L	L
ALL OTHER COMBINATIONS				H

Verilog-HDL DESCRIPTION

```
OR4  inst(Z,A,B,C,D);
```

VHDL DESCRIPTION

```
inst:OR4
   port   map(Z,A,B,C,D);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.04
B,D	1.03
C	0.98

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	45.5

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OR4 OR4 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0902	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.28	0.44	1.06
0.38	0.22	0.35	0.51	1.13
1.00	0.26	0.39	0.55	1.18
3.00	0.25	0.38	0.54	1.17

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0398	0.21

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.61	0.76	1.27
0.38	0.45	0.60	0.75	1.26
1.00	0.55	0.70	0.85	1.36
3.00	0.85	1.00	1.15	1.67

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0902	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.29	0.45	1.07
0.38	0.24	0.37	0.53	1.15
1.00	0.29	0.42	0.58	1.20
3.00	0.30	0.43	0.59	1.21

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0398	0.21

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.54	0.69	0.84	1.35
0.38	0.51	0.65	0.81	1.32
1.00	0.57	0.72	0.87	1.38
3.00	0.81	0.97	1.12	1.64

OR4 OR4 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0902	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.31	0.47	1.09
0.38	0.25	0.38	0.54	1.16
1.00	0.30	0.44	0.59	1.22
3.00	0.34	0.47	0.63	1.26

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0398	0.21

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.60	0.75	0.90	1.41
0.38	0.56	0.71	0.86	1.37
1.00	0.57	0.72	0.87	1.38
3.00	0.75	0.91	1.06	1.58

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0902	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.30	0.46	1.09
0.38	0.23	0.37	0.53	1.16
1.00	0.29	0.42	0.58	1.21
3.00	0.31	0.45	0.61	1.24

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	FALL

SLEW FACTOR

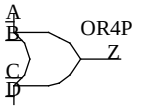
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0398	0.21

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.61	0.76	0.91	1.42
0.38	0.57	0.71	0.87	1.38
1.00	0.56	0.71	0.86	1.37
3.00	0.73	0.88	1.04	1.56

OR4P	OR4P	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
OR4P	4-INPUT OR	3	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT
A	B	C	D	Z
L	L	L	L	L
ALL OTHER COMBINATIONS				H

Verilog-HDL DESCRIPTION

```
OR4P  inst(Z,A,B,C,D);
```

VHDL DESCRIPTION

```
inst:OR4P
   port   map(Z,A,B,C,D);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A,B	1.06
C	0.98
D	1.00

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	82.8

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OR4P | OR4P | 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0470	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.22	0.31	0.63
0.38	0.23	0.30	0.38	0.71
1.00	0.28	0.36	0.44	0.77
3.00	0.31	0.38	0.47	0.80

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0244	0.27

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.57	0.68	0.78	1.13
0.38	0.56	0.67	0.77	1.12
1.00	0.65	0.76	0.86	1.21
3.00	0.97	1.08	1.18	1.53

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0470	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.23	0.32	0.65
0.38	0.24	0.31	0.40	0.73
1.00	0.31	0.38	0.47	0.79
3.00	0.35	0.43	0.51	0.84

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0244	0.27

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.65	0.76	0.87	1.22
0.38	0.62	0.73	0.84	1.18
1.00	0.68	0.78	0.89	1.24
3.00	0.93	1.04	1.15	1.50

OR4P | OR4P | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0470	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.24	0.33	0.66
0.38	0.25	0.32	0.41	0.74
1.00	0.32	0.39	0.48	0.81
3.00	0.39	0.46	0.55	0.88

PATH CONDITION

PATH	CONDITION	FUNCTION
C->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0244	0.27

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.72	0.82	0.93	1.28
0.38	0.68	0.79	0.89	1.24
1.00	0.68	0.79	0.90	1.24
3.00	0.87	0.97	1.08	1.43

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0470	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.23	0.32	0.65
0.38	0.23	0.31	0.39	0.73
1.00	0.30	0.38	0.46	0.79
3.00	0.36	0.43	0.52	0.85

PATH CONDITION

PATH	CONDITION	FUNCTION
D->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0244	0.27

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.73	0.84	0.94	1.29
0.38	0.69	0.80	0.90	1.25
1.00	0.67	0.78	0.89	1.23
3.00	0.84	0.95	1.06	1.41

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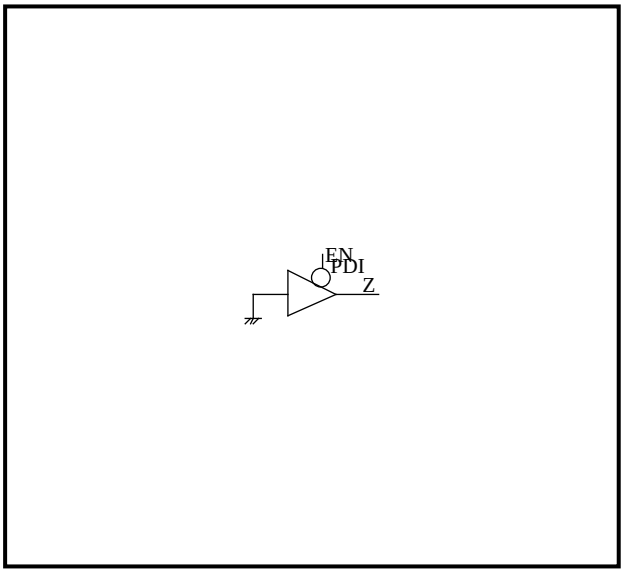
PDI	PDI	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
PDI	INTERNAL PULL-DOWN for PREVENTING BUS FLOATING	1	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
EN	Z
L	L
H	HZ

Verilog-HDL DESCRIPTION

```
PDI  inst(Z,EN);
```

VHDL DESCRIPTION

```
inst:PDI
   port   map(Z,EN);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT CAPACITANCE (LU)

PIN NAME	Z
Cin	0.39

INPUT LOAD (LU)

PIN NAME	TYPICAL
EN	1.01

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	168.1

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PDI | PDI | 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
EN->Z	---	0-Z

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0000	0.00

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.39	5.39	10.39	30.39
0.01	0.06	0.06	0.06	0.06
0.38	0.12	0.12	0.12	0.12
1.00	0.18	0.18	0.18	0.18
3.00	0.34	0.34	0.34	0.34

PATH CONDITION

PATH	CONDITION	FUNCTION
EN->Z	---	Z-0

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0386	0.05

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.39	5.39	10.39	30.39
0.01	0.11	0.21	0.32	0.76
0.38	0.14	0.24	0.35	0.79
1.00	0.18	0.29	0.40	0.85
3.00	0.27	0.40	0.52	0.97

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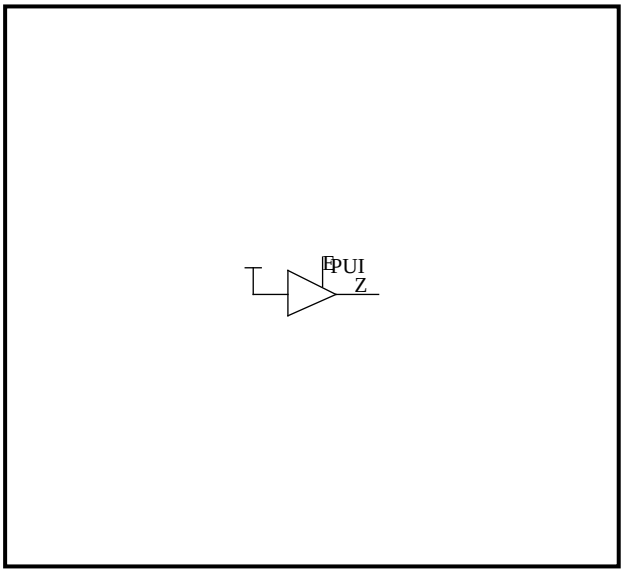
PUI	PUI	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
PUI	INTERNAL PULL-UP for PREVENTING BUS FLOATING	1	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
E	Z
L	HZ
H	H

Verilog-HDL DESCRIPTION

```
PUI  inst(Z,E);
```

VHDL DESCRIPTION

```
inst:PUI
   port   map(Z,E);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	6880.0

INPUT CAPACITANCE (LU)

PIN NAME	Z
Cin	0.39

INPUT LOAD (LU)

PIN NAME	TYPICAL
E	1.01

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	67.9

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PUI PUI 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	1-Z

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0000	0.00

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.39	5.39	10.39	30.39
0.01	0.11	0.11	0.11	0.11
0.38	0.15	0.15	0.15	0.15
1.00	0.24	0.24	0.24	0.24
3.00	0.49	0.49	0.49	0.49

PATH CONDITION

PATH	CONDITION	FUNCTION
E->Z	---	Z-1

SLEW FACTOR

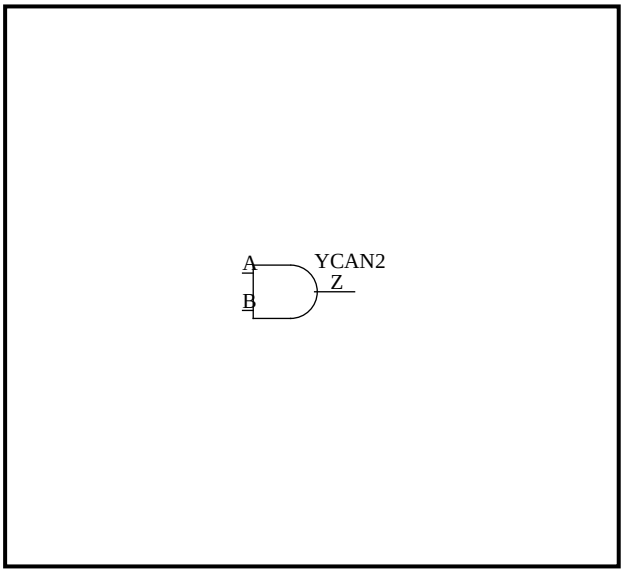
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0929	0.04

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.39	5.39	10.39	30.39
0.01	0.10	0.22	0.37	0.98
0.38	0.14	0.27	0.42	1.04
1.00	0.17	0.30	0.46	1.08
3.00	0.19	0.36	0.53	1.17

YCAN2	YCAN2	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YCAN2	CLOCK BUFFER with 2-INPUT AND	4	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
A	B	Z
L	L	L
L	H	L
H	L	L
H	H	H

Verilog-HDL DESCRIPTION

```
YCAN2  inst(Z,A,B);
```

VHDL DESCRIPTION

```
inst:YCAN2
   port   map(Z,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A,B	0.98

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	235.9

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YCAN2 YCAN2 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0145	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.24	0.28	0.40
0.38	0.29	0.32	0.36	0.48
1.00	0.40	0.43	0.47	0.59
3.00	0.62	0.66	0.69	0.82

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0118	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.32	0.37	0.53
0.38	0.31	0.36	0.40	0.57
1.00	0.39	0.43	0.47	0.64
3.00	0.54	0.58	0.63	0.79

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0145	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.25	0.29	0.41
0.38	0.27	0.31	0.34	0.46
1.00	0.35	0.38	0.42	0.54
3.00	0.51	0.54	0.58	0.70

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

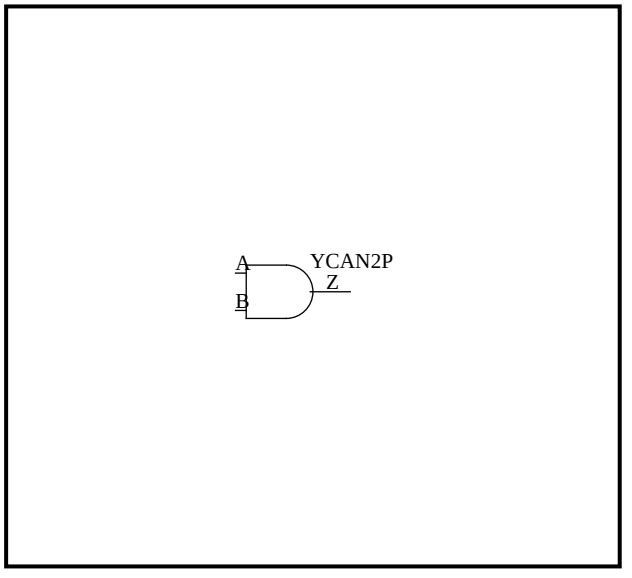
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0118	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.34	0.39	0.56
0.38	0.33	0.37	0.42	0.59
1.00	0.41	0.45	0.50	0.66
3.00	0.59	0.63	0.68	0.85

YCAN2P	YCAN2P	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YCAN2P	CLOCK BUFFER with 2-INPUT AND	8	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
A	B	Z
L	L	L
L	H	L
H	L	L
H	H	H

Verilog-HDL DESCRIPTION

```
YCAN2P  inst(Z,A,B);
```

VHDL DESCRIPTION

```
inst:YCAN2P
   port   map(Z,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.97
B	2.05

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	458.8

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YCAN2P | YCAN2P | 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0074	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.24	0.26	0.33
0.38	0.30	0.32	0.34	0.41
1.00	0.41	0.43	0.45	0.52
3.00	0.65	0.67	0.69	0.76

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0061	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.29	0.32	0.41
0.38	0.30	0.33	0.35	0.44
1.00	0.37	0.40	0.42	0.51
3.00	0.51	0.54	0.56	0.65

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0074	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.25	0.27	0.34
0.38	0.29	0.31	0.33	0.40
1.00	0.37	0.39	0.41	0.48
3.00	0.54	0.56	0.58	0.65

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0061	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.32	0.35	0.44
0.38	0.33	0.35	0.38	0.47
1.00	0.40	0.43	0.45	0.54
3.00	0.57	0.60	0.63	0.72

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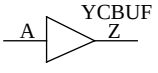
YCBUF	YCBUF	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YCBUF	CLOCK BUFFER	4	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	L
H	H

Verilog-HDL DESCRIPTION

```
YCBUF  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:YCBUF
   port   map(Z,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.11

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	236.1

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YCBUF YCBUF 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0144	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.18	0.22	0.33
0.38	0.24	0.27	0.30	0.41
1.00	0.33	0.36	0.39	0.51
3.00	0.50	0.53	0.56	0.68

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

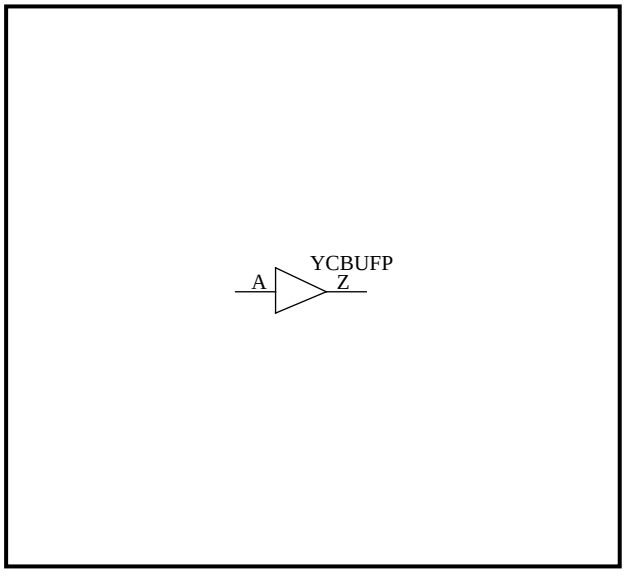
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0124	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.33	0.37	0.54
0.38	0.31	0.36	0.40	0.57
1.00	0.39	0.43	0.48	0.65
3.00	0.55	0.60	0.65	0.82

YCBUFP	YCBUFP	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YCBUFP	CLOCK BUFFER	7	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	L
H	H

Verilog-HDL DESCRIPTION

```
YCBUFP  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:YCBUFP
   port   map(Z,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	2.06

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	489.7

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YCBUFP YCBUFP 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0072	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.15	0.17	0.23
0.38	0.22	0.23	0.25	0.31
1.00	0.30	0.31	0.33	0.39
3.00	0.43	0.45	0.47	0.54

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

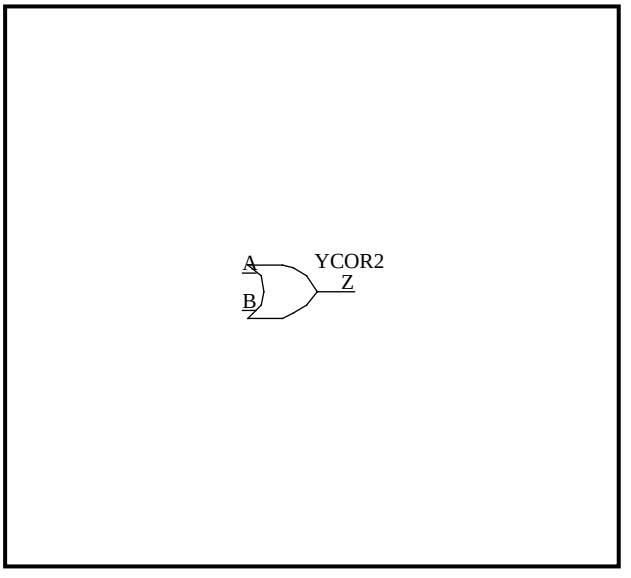
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0061	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.29	0.31	0.40
0.38	0.29	0.32	0.34	0.44
1.00	0.37	0.40	0.42	0.51
3.00	0.55	0.58	0.60	0.69

YCOR2	YCOR2	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YCOR2	CLOCK BUFFER with 2-INPUT OR	4	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
A	B	Z
L	L	L
L	H	H
H	L	H
H	H	H

Verilog-HDL DESCRIPTION

```
YCOR2  inst(Z,A,B);
```

VHDL DESCRIPTION

```
inst:YCOR2
   port   map(Z,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A,B	0.98

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	233.5

Rev.1.01.10

YCOR2 YCOR2 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0145	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.17	0.21	0.32
0.38	0.23	0.26	0.29	0.40
1.00	0.31	0.34	0.37	0.49
3.00	0.40	0.44	0.47	0.59

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0118	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.50	0.54	0.60	0.78
0.38	0.51	0.56	0.61	0.79
1.00	0.59	0.64	0.69	0.87
3.00	0.86	0.91	0.96	1.14

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0145	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.18	0.21	0.32
0.38	0.23	0.26	0.29	0.41
1.00	0.32	0.35	0.38	0.50
3.00	0.44	0.47	0.51	0.63

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

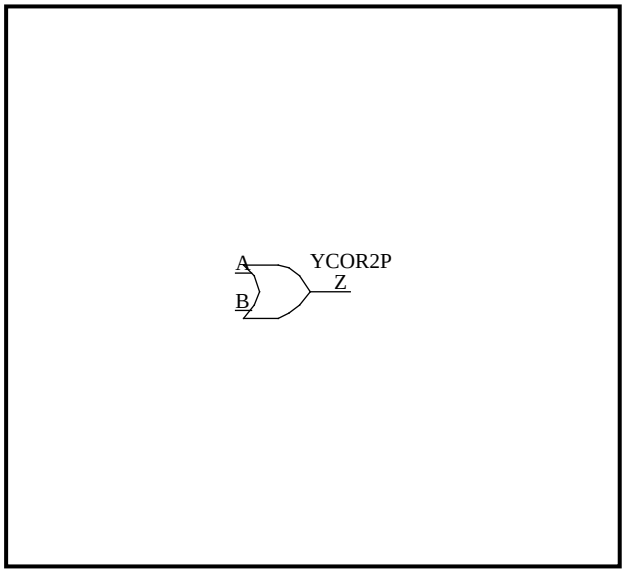
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0118	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.56	0.61	0.79
0.38	0.50	0.55	0.61	0.78
1.00	0.55	0.60	0.65	0.82
3.00	0.72	0.77	0.82	1.00

YCOR2P	YCOR2P	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YCOR2P	CLOCK BUFFER with 2-INPUT OR	8	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
A	B	Z
L	L	L
L	H	H
H	L	H
H	H	H

Verilog-HDL DESCRIPTION

```
YCOR2P  inst(Z,A,B);
```

VHDL DESCRIPTION

```
inst:YCOR2P
   port   map(Z,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.97
B	2.05

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	449.5

Rev.1.01.10

YCOR2P | YCOR2P | 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0071	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.15	0.17	0.23
0.38	0.22	0.24	0.26	0.32
1.00	0.30	0.32	0.33	0.40
3.00	0.39	0.40	0.42	0.49

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0066	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.54	0.58	0.68
0.38	0.53	0.56	0.59	0.69
1.00	0.61	0.64	0.67	0.77
3.00	0.89	0.91	0.95	1.05

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0071	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.16	0.18	0.24
0.38	0.23	0.25	0.26	0.33
1.00	0.32	0.33	0.35	0.41
3.00	0.43	0.45	0.47	0.54

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z	---	FALL

SLEW FACTOR

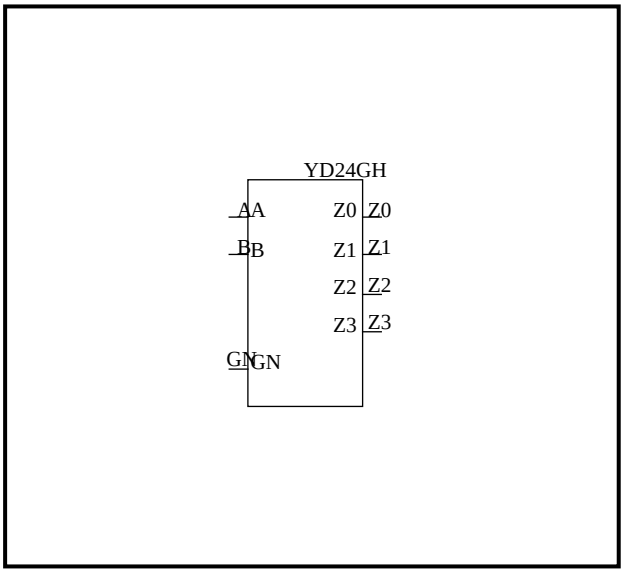
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0066	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.53	0.56	0.59	0.70
0.38	0.53	0.56	0.59	0.69
1.00	0.57	0.60	0.63	0.73
3.00	0.75	0.78	0.81	0.92

YD24GH	YD24GH	1/7

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YD24GH	2 TO 4 DECODER (GATED OUTPUTS ACTIVE HIGH)	7	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT			
GN	A	B	Z0	Z1	Z2	Z3
H	X	X	L	L	L	L
L	L	L	H	L	L	L
L	H	L	L	H	L	L
L	L	H	L	L	H	L
L	H	H	L	L	L	H

Verilog-HDL DESCRIPTION

```
YD24GH  inst(Z0,Z1,Z2,Z3,A,B,GN);
```

VHDL DESCRIPTION

```
inst:YD24GH
   port   map(Z0,Z1,Z2,Z3,A,B,GN);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z0,Z1,Z2,Z3
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	3.44
B	3.46
GN	4.21

OUTPUT DRIVE (LU)

PIN NAME	Z0	Z1	Z2	Z3
DRIVE	17.1	15.8	15.2	16.7

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z0	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.2629	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.70	1.17	3.02
0.38	0.31	0.69	1.16	3.02
1.00	0.35	0.72	1.18	3.02
3.00	0.54	0.91	1.35	3.13

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z0	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0412	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.08	0.18	0.30	0.78
0.38	0.15	0.26	0.39	0.87
1.00	0.18	0.35	0.50	1.01
3.00	0.17	0.44	0.68	1.36

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.2874	0.45

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.84	1.35	3.36
0.38	0.49	0.91	1.41	3.43
1.00	0.54	0.96	1.47	3.48
3.00	0.64	1.05	1.55	3.57

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0415	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.37	0.50	0.99
0.38	0.29	0.41	0.54	1.03
1.00	0.35	0.48	0.61	1.10
3.00	0.50	0.63	0.77	1.26

YD24GH YD24GH 3/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.2971	0.47

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.78	1.30	3.38
0.38	0.34	0.76	1.29	3.37
1.00	0.39	0.79	1.30	3.37
3.00	0.60	1.00	1.49	3.49

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0419	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.08	0.18	0.30	0.78
0.38	0.15	0.26	0.39	0.87
1.00	0.18	0.35	0.50	1.01
3.00	0.16	0.43	0.67	1.36

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.2971	0.46

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.44	0.87	1.39	3.47
0.38	0.50	0.93	1.46	3.54
1.00	0.56	0.99	1.51	3.60
3.00	0.65	1.08	1.60	3.69

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z3	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0419	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.37	0.50	0.99
0.38	0.29	0.41	0.53	1.02
1.00	0.35	0.47	0.60	1.10
3.00	0.50	0.63	0.76	1.26

YD24GH YD24GH 4/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z0	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.2629	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.65	1.11	2.97
0.38	0.28	0.65	1.12	2.97
1.00	0.36	0.72	1.17	3.01
3.00	0.60	0.98	1.43	3.21

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z0	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0412	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.07	0.17	0.29	0.77
0.38	0.14	0.25	0.38	0.86
1.00	0.16	0.33	0.49	1.00
3.00	0.13	0.41	0.66	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.2874	0.45

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.70	1.21	3.21
0.38	0.30	0.70	1.21	3.22
1.00	0.39	0.78	1.26	3.25
3.00	0.63	1.04	1.53	3.46

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0415	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.07	0.17	0.29	0.77
0.38	0.14	0.25	0.38	0.86
1.00	0.16	0.33	0.49	1.00
3.00	0.13	0.41	0.66	1.35

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.2971	0.47

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.79	1.32	3.40
0.38	0.43	0.86	1.38	3.47
1.00	0.49	0.91	1.44	3.52
3.00	0.59	1.01	1.53	3.61

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0419	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.35	0.48	0.97
0.38	0.27	0.38	0.51	1.00
1.00	0.33	0.45	0.58	1.07
3.00	0.47	0.60	0.73	1.23

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.2971	0.46

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.79	1.32	3.40
0.38	0.43	0.86	1.38	3.47
1.00	0.49	0.91	1.43	3.52
3.00	0.59	1.01	1.53	3.61

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z3	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0419	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.35	0.48	0.97
0.38	0.27	0.38	0.51	1.00
1.00	0.33	0.45	0.58	1.07
3.00	0.47	0.60	0.73	1.23

YD24GH YD24GH 6/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->Z0	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.2629	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.74	1.20	3.05
0.38	0.33	0.72	1.19	3.05
1.00	0.34	0.70	1.16	3.01
3.00	0.45	0.81	1.23	2.99

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->Z0	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0412	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.19	0.31	0.79
0.38	0.15	0.27	0.40	0.88
1.00	0.19	0.36	0.51	1.02
3.00	0.20	0.46	0.70	1.37

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.2874	0.45

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.40	0.80	1.31	3.32
0.38	0.36	0.78	1.29	3.31
1.00	0.36	0.76	1.25	3.26
3.00	0.49	0.87	1.32	3.23

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0415	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.19	0.31	0.79
0.38	0.15	0.27	0.40	0.88
1.00	0.19	0.36	0.51	1.02
3.00	0.20	0.46	0.69	1.37

YD24GH | YD24GH | 7/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.2971	0.47

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.84	1.36	3.44
0.38	0.38	0.81	1.34	3.43
1.00	0.38	0.79	1.31	3.38
3.00	0.51	0.90	1.38	3.36

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0419	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.19	0.31	0.79
0.38	0.15	0.27	0.40	0.88
1.00	0.19	0.36	0.51	1.02
3.00	0.19	0.46	0.69	1.37

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.2971	0.46

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.83	1.35	3.43
0.38	0.38	0.81	1.33	3.42
1.00	0.37	0.79	1.30	3.38
3.00	0.51	0.90	1.37	3.35

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->Z3	---	FALL

SLEW FACTOR

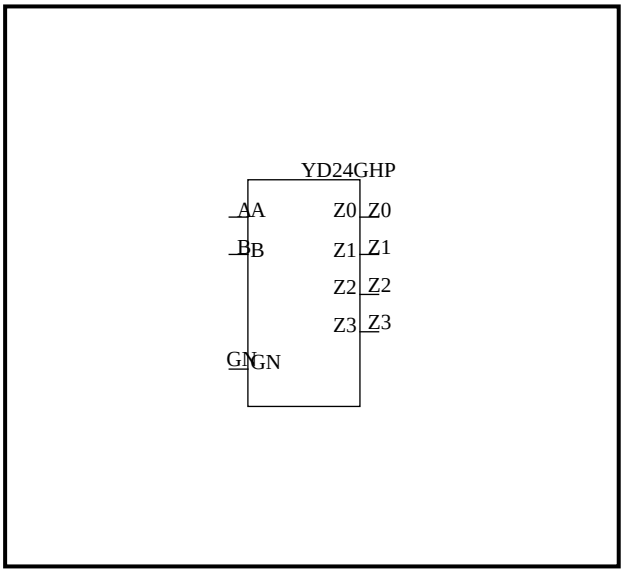
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0419	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.19	0.31	0.79
0.38	0.15	0.27	0.40	0.88
1.00	0.19	0.36	0.51	1.02
3.00	0.19	0.46	0.69	1.36

YD24GHP	YD24GHP	1/7

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YD24GHP	2 TO 4 DECODER (GATED OUTPUTS ACTIVE HIGH)	13	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT			
GN	A	B	Z0	Z1	Z2	Z3
H	X	X	L	L	L	L
L	L	L	H	L	L	L
L	H	L	L	H	L	L
L	L	H	L	L	H	L
L	H	H	L	L	L	H

Verilog-HDL DESCRIPTION

```
YD24GHP  inst(Z0,Z1,Z2,Z3,A,B,GN);
```

VHDL DESCRIPTION

```
inst:YD24GHP
   port   map(Z0,Z1,Z2,Z3,A,B,GN);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z0,Z1,Z2,Z3
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	5.79
B	5.57
GN	8.76

OUTPUT DRIVE (LU)

PIN NAME	Z0	Z1	Z2	Z3
DRIVE	30.7	30.3	30.2	32.4

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z0	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.1454	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.51	0.76	1.76
0.38	0.28	0.49	0.74	1.75
1.00	0.31	0.51	0.76	1.74
3.00	0.48	0.69	0.93	1.87

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z0	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0218	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.06	0.11	0.17	0.39
0.38	0.12	0.18	0.25	0.48
1.00	0.14	0.24	0.33	0.60
3.00	0.10	0.26	0.41	0.84

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.1475	0.41

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.41	0.62	0.88	1.91
0.38	0.49	0.70	0.96	1.99
1.00	0.57	0.78	1.04	2.06
3.00	0.71	0.92	1.17	2.19

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0218	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.39	0.46	0.72
0.38	0.34	0.42	0.49	0.75
1.00	0.42	0.49	0.57	0.82
3.00	0.59	0.67	0.75	1.02

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.1505	0.41

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.31	0.52	0.77	1.80
0.38	0.29	0.50	0.75	1.79
1.00	0.32	0.52	0.77	1.79
3.00	0.50	0.71	0.95	1.92

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0231	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.06	0.11	0.17	0.39
0.38	0.12	0.18	0.25	0.48
1.00	0.14	0.24	0.33	0.60
3.00	0.10	0.26	0.41	0.84

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.1501	0.43

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.64	0.90	1.94
0.38	0.50	0.71	0.98	2.02
1.00	0.57	0.79	1.06	2.10
3.00	0.72	0.93	1.19	2.22

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z3	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0241	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.40	0.48	0.75
0.38	0.35	0.43	0.51	0.78
1.00	0.43	0.50	0.58	0.86
3.00	0.59	0.68	0.77	1.05

YD24GHP | YD24GHP | 4/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z0	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.1454	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.44	0.69	1.69
0.38	0.24	0.44	0.69	1.70
1.00	0.32	0.52	0.76	1.74
3.00	0.54	0.77	1.02	1.99

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z0	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0218	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.06	0.12	0.18	0.45
0.38	0.12	0.19	0.27	0.54
1.00	0.14	0.25	0.36	0.67
3.00	0.09	0.28	0.45	0.93

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.1475	0.41

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.44	0.70	1.71
0.38	0.24	0.44	0.70	1.72
1.00	0.32	0.52	0.77	1.76
3.00	0.55	0.78	1.03	2.02

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0218	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.06	0.12	0.18	0.45
0.38	0.12	0.19	0.27	0.54
1.00	0.14	0.25	0.36	0.67
3.00	0.09	0.27	0.45	0.93

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.1505	0.41

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.56	0.82	1.86
0.38	0.42	0.63	0.90	1.94
1.00	0.51	0.72	0.98	2.02
3.00	0.66	0.86	1.12	2.15

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0231	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.37	0.46	0.75
0.38	0.32	0.40	0.49	0.78
1.00	0.39	0.47	0.56	0.86
3.00	0.55	0.64	0.74	1.04

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.1501	0.43

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.56	0.82	1.86
0.38	0.42	0.64	0.90	1.94
1.00	0.51	0.72	0.98	2.02
3.00	0.66	0.86	1.12	2.15

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z3	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0241	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.38	0.46	0.77
0.38	0.32	0.41	0.49	0.80
1.00	0.40	0.48	0.57	0.87
3.00	0.56	0.65	0.74	1.06

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->Z0	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.1454	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.32	0.53	0.78	1.78
0.38	0.29	0.50	0.75	1.76
1.00	0.30	0.49	0.74	1.73
3.00	0.43	0.62	0.86	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->Z0	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0218	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.06	0.11	0.17	0.40
0.38	0.12	0.19	0.25	0.49
1.00	0.15	0.24	0.34	0.61
3.00	0.12	0.28	0.43	0.85

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.1475	0.41

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.33	0.54	0.79	1.81
0.38	0.30	0.51	0.76	1.79
1.00	0.30	0.50	0.75	1.75
3.00	0.44	0.64	0.87	1.81

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0218	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.06	0.11	0.17	0.39
0.38	0.12	0.18	0.25	0.48
1.00	0.14	0.24	0.33	0.60
3.00	0.12	0.28	0.42	0.84

YD24GHP | YD24GHP | 7/7

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.1505	0.41

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.55	0.81	1.85
0.38	0.31	0.52	0.79	1.83
1.00	0.31	0.51	0.77	1.79
3.00	0.45	0.65	0.89	1.85

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0231	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.06	0.11	0.17	0.40
0.38	0.12	0.19	0.25	0.49
1.00	0.15	0.25	0.34	0.61
3.00	0.12	0.28	0.43	0.85

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.1501	0.43

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.56	0.81	1.85
0.38	0.31	0.52	0.79	1.83
1.00	0.31	0.51	0.77	1.80
3.00	0.44	0.64	0.88	1.84

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->Z3	---	FALL

SLEW FACTOR

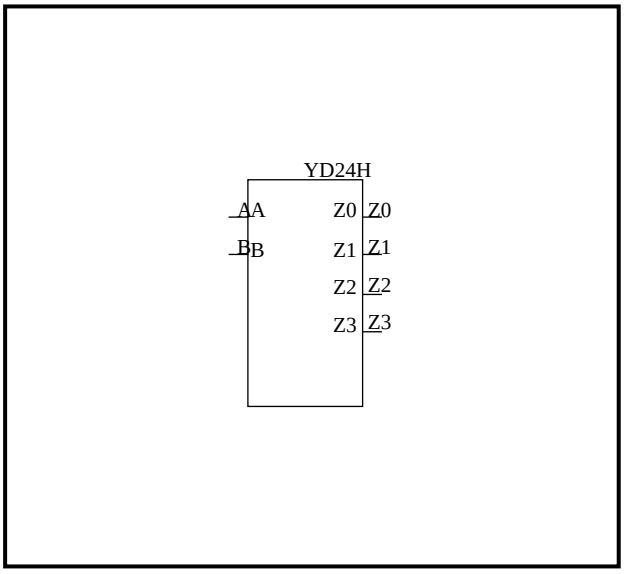
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0241	0.15

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.07	0.12	0.19	0.43
0.38	0.13	0.20	0.27	0.52
1.00	0.16	0.26	0.35	0.64
3.00	0.14	0.30	0.45	0.89

YD24H	YD24H	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YD24H	2 TO 4 DECODER (OUTPUTS ACTIVE HIGH)	5	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT			
A	B	Z0	Z1	Z2	Z3
L	L	H	L	L	L
H	L	L	H	L	L
L	H	L	L	H	L
H	H	L	L	L	H

Verilog-HDL DESCRIPTION

```
YD24H  inst(Z0,Z1,Z2,Z3,A,B);
```

VHDL DESCRIPTION

```
inst:YD24H
   port   map(Z0,Z1,Z2,Z3,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z0,Z1,Z2,Z3
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	3.19
B	3.22

OUTPUT DRIVE (LU)

PIN NAME	Z0	Z1	Z2	Z3
DRIVE	24.8	25.7	25.5	27.1

Rev.1.01.10

YD24H YD24H 2/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z0	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.1783	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.43	0.74	1.98
0.38	0.18	0.43	0.74	1.98
1.00	0.21	0.45	0.76	1.98
3.00	0.31	0.57	0.88	2.07

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z0	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0411	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.07	0.17	0.29	0.77
0.38	0.13	0.25	0.37	0.86
1.00	0.16	0.33	0.49	1.00
3.00	0.18	0.45	0.68	1.36

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.1784	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.51	0.82	2.06
0.38	0.32	0.58	0.89	2.13
1.00	0.38	0.63	0.95	2.19
3.00	0.48	0.72	1.03	2.27

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0334	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.33	0.44	0.85
0.38	0.26	0.36	0.47	0.88
1.00	0.32	0.43	0.54	0.95
3.00	0.46	0.58	0.70	1.12

YD24H | YD24H | 3/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.1784	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.43	0.74	1.97
0.38	0.18	0.43	0.73	1.97
1.00	0.21	0.45	0.76	1.98
3.00	0.32	0.59	0.89	2.08

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0338	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.06	0.14	0.25	0.66
0.38	0.12	0.22	0.33	0.75
1.00	0.15	0.30	0.45	0.89
3.00	0.15	0.40	0.63	1.24

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.1784	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.52	0.83	2.07
0.38	0.33	0.58	0.90	2.14
1.00	0.38	0.64	0.95	2.19
3.00	0.48	0.73	1.04	2.27

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z3	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0420	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.36	0.49	0.98
0.38	0.27	0.39	0.52	1.01
1.00	0.34	0.46	0.59	1.08
3.00	0.48	0.61	0.75	1.25

YD24H YD24H 4/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z0	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.1783	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.41	0.72	1.96
0.38	0.18	0.43	0.74	1.97
1.00	0.24	0.49	0.80	2.02
3.00	0.40	0.70	1.02	2.24

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z0	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0411	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.06	0.16	0.28	0.76
0.38	0.12	0.24	0.36	0.85
1.00	0.14	0.32	0.48	0.99
3.00	0.13	0.41	0.66	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.1784	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.16	0.41	0.72	1.96
0.38	0.18	0.42	0.73	1.97
1.00	0.25	0.50	0.80	2.02
3.00	0.42	0.72	1.04	2.25

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0334	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.05	0.13	0.23	0.63
0.38	0.11	0.21	0.32	0.72
1.00	0.12	0.29	0.43	0.86
3.00	0.09	0.36	0.59	1.21

YD24H | YD24H | 5/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.1784	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.48	0.79	2.03
0.38	0.30	0.55	0.86	2.10
1.00	0.35	0.61	0.92	2.16
3.00	0.45	0.70	1.01	2.25

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0338	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.30	0.41	0.82
0.38	0.23	0.34	0.45	0.85
1.00	0.29	0.40	0.51	0.92
3.00	0.43	0.55	0.66	1.08

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.1784	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.49	0.80	2.04
0.38	0.30	0.55	0.87	2.10
1.00	0.36	0.61	0.92	2.16
3.00	0.45	0.70	1.01	2.25

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z3	---	FALL

SLEW FACTOR

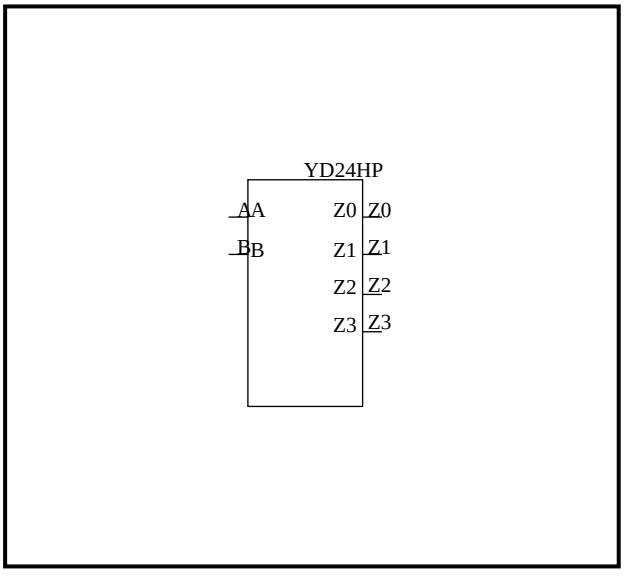
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0420	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.33	0.46	0.95
0.38	0.25	0.36	0.49	0.98
1.00	0.31	0.43	0.56	1.05
3.00	0.44	0.58	0.71	1.21

YD24HP	YD24HP	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YD24HP	2 TO 4 DECODER (OUTPUTS ACTIVE HIGH)	9	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT			
A	B	Z0	Z1	Z2	Z3
L	L	H	L	L	L
H	L	L	H	L	L
L	H	L	L	H	L
H	H	L	L	L	H

Verilog-HDL DESCRIPTION

```
YD24HP  inst(Z0,Z1,Z2,Z3,A,B);
```

VHDL DESCRIPTION

```
inst:YD24HP
   port   map(Z0,Z1,Z2,Z3,A,B);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z0,Z1,Z2,Z3
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	5.35
B	5.40

OUTPUT DRIVE (LU)

PIN NAME	Z0,Z2	Z1	Z3
DRIVE	48.8	51.6	54.3

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YD24HP YD24HP 2/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z0	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0889	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.26	0.41	1.03
0.38	0.15	0.27	0.42	1.04
1.00	0.20	0.34	0.49	1.10
3.00	0.36	0.52	0.70	1.33

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z0	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0193	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.05	0.10	0.16	0.40
0.38	0.10	0.17	0.24	0.49
1.00	0.11	0.22	0.32	0.61
3.00	0.07	0.25	0.41	0.86

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0834	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.36	0.51	1.10
0.38	0.32	0.44	0.59	1.18
1.00	0.40	0.52	0.67	1.26
3.00	0.55	0.67	0.82	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0208	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.34	0.42	0.69
0.38	0.30	0.37	0.45	0.72
1.00	0.37	0.45	0.53	0.80
3.00	0.53	0.62	0.70	0.98

YD24HP | YD24HP | 3/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0889	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.26	0.41	1.03
0.38	0.15	0.27	0.42	1.04
1.00	0.20	0.34	0.49	1.10
3.00	0.36	0.52	0.70	1.33

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0202	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.05	0.10	0.16	0.40
0.38	0.10	0.17	0.24	0.49
1.00	0.11	0.22	0.32	0.61
3.00	0.07	0.25	0.41	0.86

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0890	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.37	0.53	1.15
0.38	0.32	0.45	0.61	1.23
1.00	0.41	0.54	0.69	1.32
3.00	0.55	0.68	0.84	1.46

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z3	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0207	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.27	0.35	0.42	0.69
0.38	0.30	0.37	0.45	0.72
1.00	0.37	0.45	0.53	0.80
3.00	0.53	0.62	0.70	0.98

YD24HP YD24HP 4/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z0	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0889	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.28	0.44	1.05
0.38	0.14	0.27	0.43	1.05
1.00	0.18	0.30	0.45	1.06
3.00	0.27	0.41	0.58	1.18

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z0	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z0	0.0193	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.06	0.11	0.17	0.41
0.38	0.11	0.18	0.25	0.50
1.00	0.14	0.24	0.33	0.62
3.00	0.14	0.30	0.45	0.88

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0834	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.27	0.41	0.99
0.38	0.14	0.26	0.41	0.99
1.00	0.17	0.29	0.43	1.00
3.00	0.25	0.39	0.55	1.11

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0208	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.06	0.11	0.17	0.41
0.38	0.11	0.18	0.25	0.50
1.00	0.14	0.24	0.33	0.62
3.00	0.15	0.30	0.45	0.88

YD24HP | YD24HP | 5/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0889	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.39	0.55	1.17
0.38	0.34	0.47	0.63	1.25
1.00	0.42	0.55	0.71	1.33
3.00	0.57	0.69	0.85	1.46

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0202	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.38	0.46	0.73
0.38	0.33	0.40	0.48	0.76
1.00	0.40	0.48	0.56	0.83
3.00	0.57	0.65	0.74	1.02

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0890	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.26	0.39	0.56	1.18
0.38	0.34	0.48	0.64	1.26
1.00	0.42	0.55	0.71	1.34
3.00	0.57	0.69	0.85	1.46

PATH CONDITION

PATH	CONDITION	FUNCTION
B->Z3	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0207	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.30	0.38	0.46	0.73
0.38	0.33	0.41	0.49	0.76
1.00	0.40	0.48	0.56	0.83
3.00	0.57	0.65	0.74	1.02

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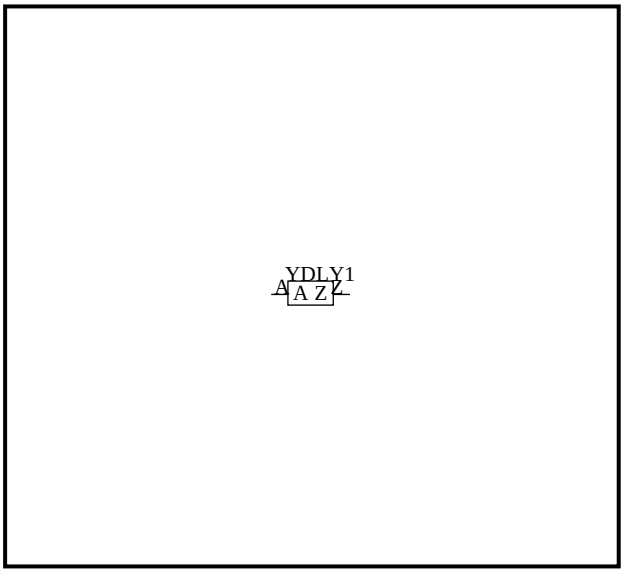
YDLY1	YDLY1	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YDLY1	DELAY BUFFER	4	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	L
H	H

Verilog-HDL DESCRIPTION

```
YDLY1  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:YDLY1
   port   map(Z,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.94

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	78.6

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YDLY1 YDLY1 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0436	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.57	0.64	0.72	1.03
0.38	0.66	0.74	0.82	1.13
1.00	0.76	0.83	0.91	1.22
3.00	0.92	0.99	1.07	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

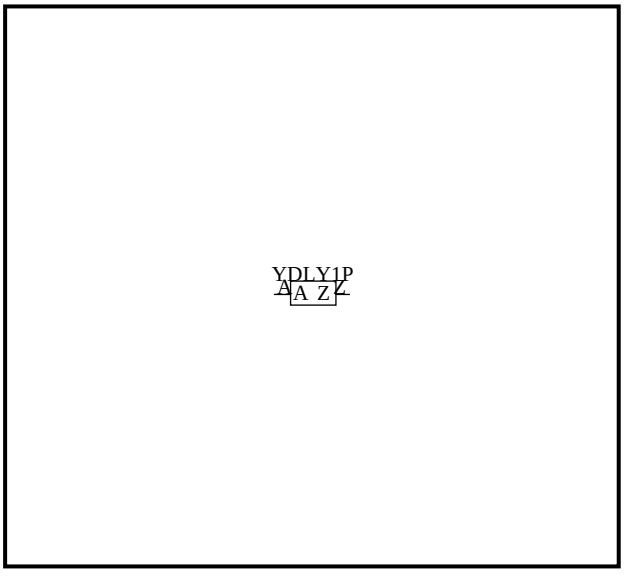
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0335	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.74	0.84	0.96	1.37
0.38	0.76	0.87	0.98	1.39
1.00	0.84	0.95	1.06	1.47
3.00	1.03	1.14	1.25	1.66

YDLY1P	YDLY1P	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YDLY1P	DELAY BUFFER	5	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	L
H	H

Verilog-HDL DESCRIPTION

```
YDLY1P  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:YDLY1P
   port   map(Z,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.94

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	150.9

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YDLY1P YDLY1P 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0216	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.61	0.66	0.71	0.87
0.38	0.71	0.75	0.80	0.97
1.00	0.80	0.84	0.89	1.06
3.00	0.96	1.01	1.05	1.22

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0182	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.84	0.91	0.98	1.22
0.38	0.86	0.93	1.00	1.25
1.00	0.94	1.01	1.08	1.33
3.00	1.13	1.20	1.27	1.52

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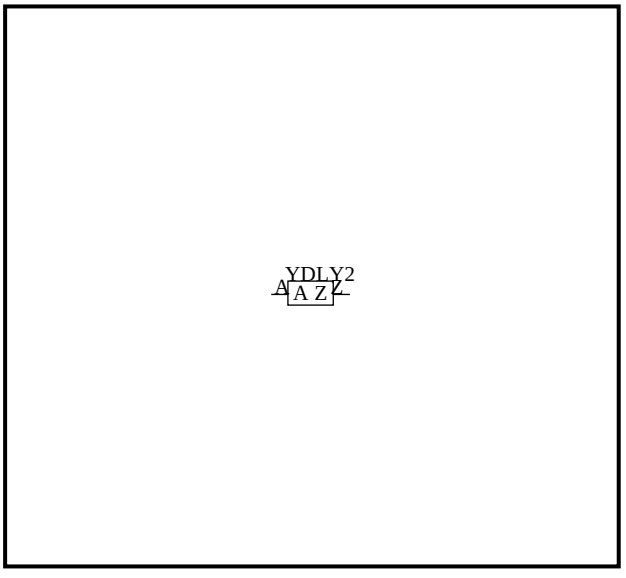
YDLY2	YDLY2	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YDLY2	DELAY BUFFER	8	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	B
L	L
H	H

Verilog-HDL DESCRIPTION

```
YDLY2  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:YDLY2
   port   map(Z,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.94

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	78.6

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YDLY2 YDLY2 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0436	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.43	1.51	1.59	1.90
0.38	1.53	1.60	1.68	1.99
1.00	1.62	1.69	1.77	2.08
3.00	1.78	1.85	1.94	2.24

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

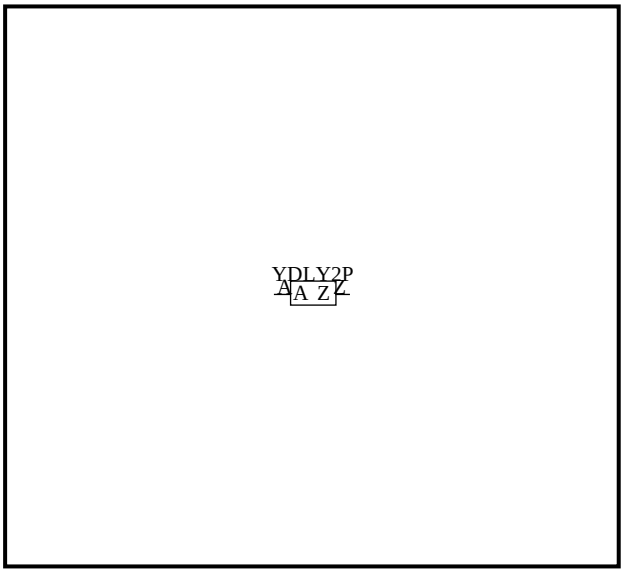
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0335	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.60	1.71	1.82	2.24
0.38	1.63	1.73	1.85	2.26
1.00	1.71	1.81	1.93	2.34
3.00	1.90	2.00	2.12	2.53

YDLY2P	YDLY2P	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YDLY2P	DELAY BUFFER	9	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	B
L	L
H	H

Verilog-HDL DESCRIPTION

```
YDLY2P  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:YDLY2P
   port   map(Z,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.94

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	150.9

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YDLY2P YDLY2P 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0216	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.48	1.52	1.57	1.74
0.38	1.57	1.61	1.66	1.83
1.00	1.66	1.71	1.76	1.92
3.00	1.83	1.87	1.92	2.08

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0181	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	1.71	1.77	1.84	2.09
0.38	1.73	1.80	1.87	2.11
1.00	1.81	1.88	1.95	2.19
3.00	2.00	2.07	2.14	2.38

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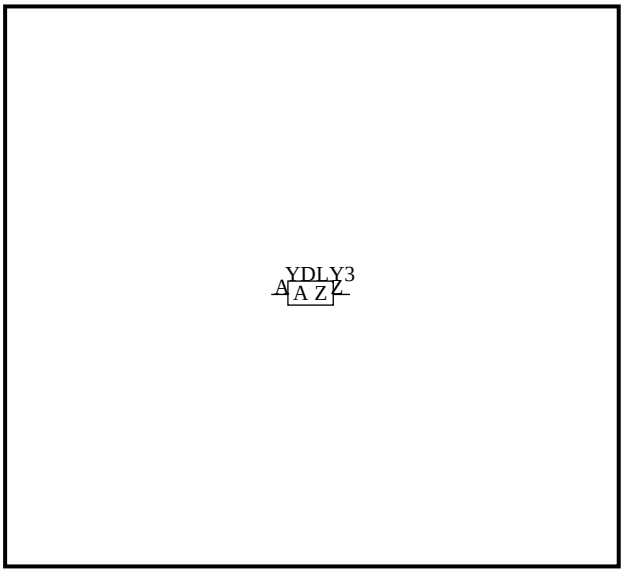
YDLY3	YDLY3	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YDLY3	DELAY BUFFER	16	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	L
H	H

Verilog-HDL DESCRIPTION

```
YDLY3  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:YDLY3
   port   map(Z,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.94

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	78.6

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YDLY3 YDLY3 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0436	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	3.16	3.23	3.31	3.62
0.38	3.25	3.32	3.41	3.72
1.00	3.34	3.42	3.50	3.81
3.00	3.51	3.58	3.66	3.97

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0335	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	3.33	3.44	3.55	3.97
0.38	3.36	3.46	3.58	3.99
1.00	3.44	3.54	3.66	4.07
3.00	3.63	3.73	3.85	4.26

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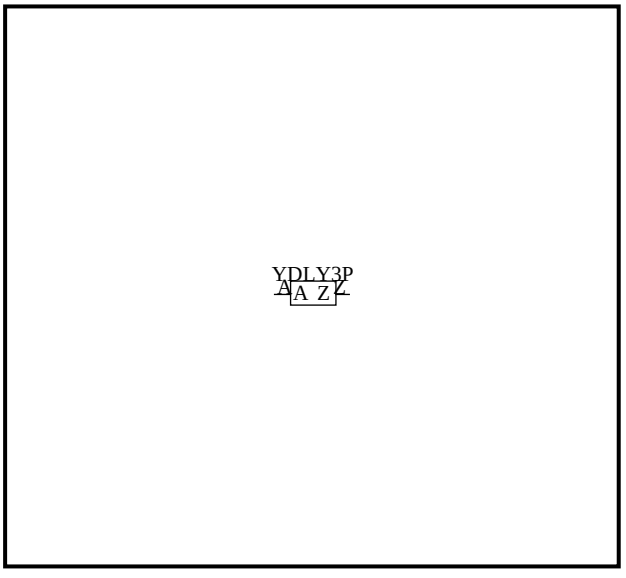
YDLY3P	YDLY3P	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YDLY3P	DELAY BUFFER	17	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	L
H	H

Verilog-HDL DESCRIPTION

```
YDLY3P  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:YDLY3P
   port   map(Z,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	1.94

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	150.8

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YDLY3P YDLY3P 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0216	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	3.20	3.25	3.29	3.46
0.38	3.30	3.34	3.39	3.56
1.00	3.39	3.43	3.48	3.65
3.00	3.55	3.60	3.64	3.81

PATH CONDITION

PATH	CONDITION	FUNCTION
A->Z	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0182	0.16

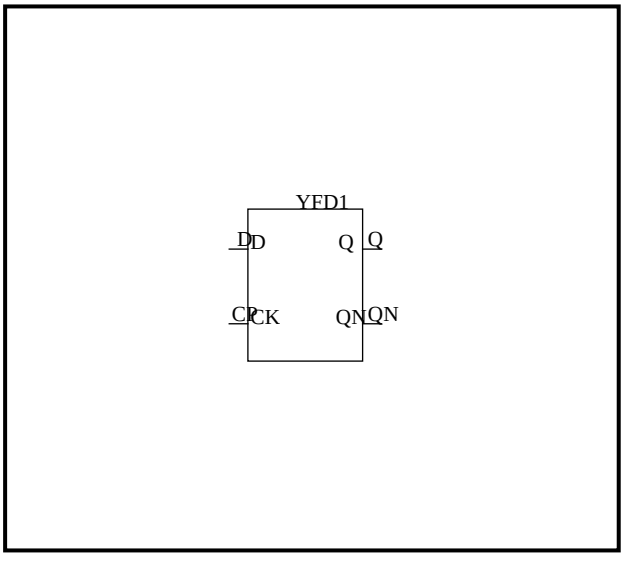
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	3.44	3.50	3.58	3.82
0.38	3.46	3.53	3.60	3.85
1.00	3.54	3.61	3.68	3.93
3.00	3.73	3.80	3.87	4.12

Rev.1.01.10

YFD1	YFD1	1/4

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YFD1	D-TYPE FLIP FLOP	5	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
D	CP	Qn+1	QNn+1
L	Up	L	H
H	Up	H	L
X	Dn	Qn	QNn

Verilog-HDL DESCRIPTION

```
YFD1  inst(Q,QN,D,CP);
```

VHDL DESCRIPTION

```
inst:YFD1
   port   map(Q,QN,D,CP);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D	3.36
CP	0.99

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	40.5	39.0

Rev.1.01.10

YFD1 YFD1 2/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.1006	0.25

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.60	0.78	1.47
0.38	0.54	0.68	0.86	1.55
1.00	0.61	0.76	0.94	1.63
3.00	0.75	0.90	1.07	1.76

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0436	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.39	0.52	0.66	1.18
0.38	0.47	0.60	0.74	1.26
1.00	0.55	0.68	0.82	1.34
3.00	0.70	0.83	0.97	1.48

PATH CONDITION

PATH	CONDITION	FUNCTION
Q->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0974	0.39

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.37	0.55	1.25
0.38	0.25	0.39	0.58	1.28
1.00	0.31	0.47	0.65	1.35
3.00	0.46	0.66	0.86	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
Q->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0397	0.22

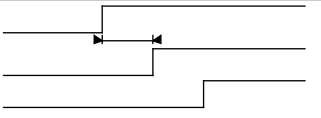
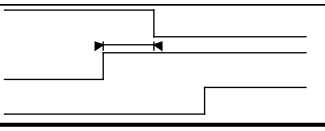
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.25	0.37	0.85
0.38	0.24	0.35	0.47	0.95
1.00	0.34	0.48	0.62	1.12
3.00	0.55	0.76	0.97	1.60

YFD1	YFD1	3/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	---

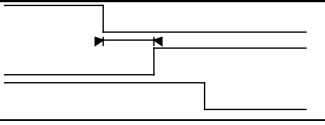
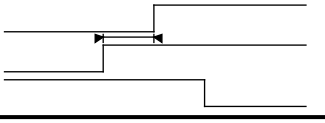
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.166	0.129	0.067	-0.133
0.38	0.207	0.172	0.113	-0.078
1.00	0.277	0.244	0.190	0.014
3.00	0.501	0.478	0.439	0.312

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.414	0.436	0.472	0.589
0.38	0.386	0.408	0.444	0.562
1.00	0.339	0.361	0.398	0.516
3.00	0.188	0.210	0.248	0.370

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.242	0.220	0.184	0.068
0.38	0.270	0.249	0.212	0.095
1.00	0.317	0.295	0.259	0.141
3.00	0.469	0.447	0.409	0.288

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.492	0.529	0.591	0.792
0.38	0.450	0.486	0.545	0.737
1.00	0.381	0.413	0.468	0.644
3.00	0.157	0.180	0.220	0.346

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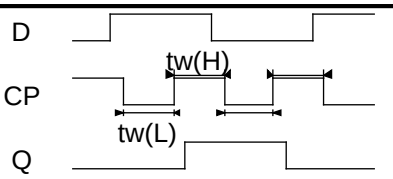
YFD1	YFD1	4/4

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	D

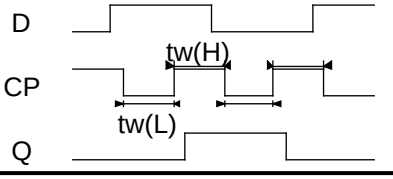
ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.710

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	~D

ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

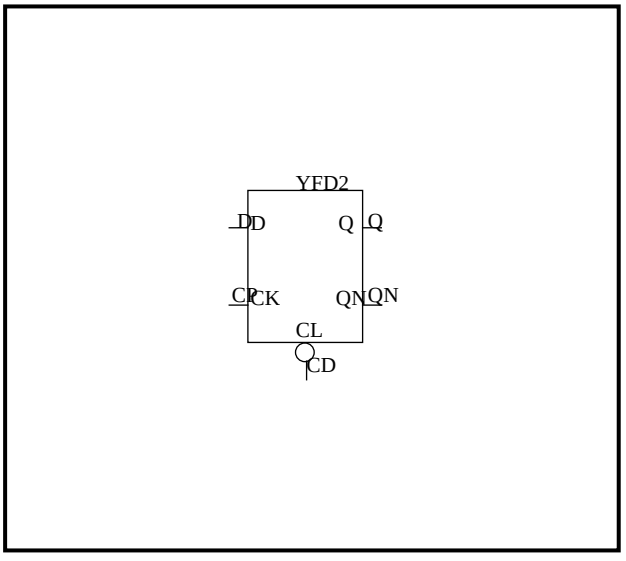
NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.710

Rev.1.01.10

YFD2	YFD2	1/6

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YFD2	D-TYPE FLIP FLOP with CLEAR	6	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT	
CD	D	CP	Qn+1	QNn+1
L	X	X*	L	H
H	L	Up	L	H
H	H	Up	H	L
H	X	Dn	Qn	QNn

*:Consider the HOLD Time of CLEAR

Verilog-HDL DESCRIPTION

```
YFD2  inst(Q,QN,D,CP,CD);
```

VHDL DESCRIPTION

```
inst:YFD2
   port   map(Q,QN,D,CP,CD);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D	3.34
CP	0.99
CD	2.21

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	45.5	35.5

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YFD2 YFD2 2/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QN->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0431	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.26	0.38	0.87
0.38	0.21	0.32	0.45	0.94
1.00	0.26	0.42	0.57	1.09
3.00	0.34	0.57	0.79	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0845	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.32	0.47	1.06
0.38	0.22	0.35	0.50	1.09
1.00	0.26	0.40	0.55	1.14
3.00	0.33	0.50	0.68	1.33

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0853	0.25

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.60	0.76	1.36
0.38	0.54	0.68	0.84	1.44
1.00	0.62	0.76	0.92	1.52
3.00	0.77	0.91	1.07	1.67

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0431	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.39	0.51	0.65	1.16
0.38	0.47	0.59	0.73	1.24
1.00	0.55	0.67	0.81	1.32
3.00	0.70	0.83	0.96	1.47

YFD2 YFD2 3/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
Q->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0845	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.32	0.47	1.06
0.38	0.22	0.35	0.50	1.09
1.00	0.26	0.40	0.55	1.14
3.00	0.33	0.50	0.68	1.33

PATH CONDITION

PATH	CONDITION	FUNCTION
Q->QN	---	FALL

SLEW FACTOR

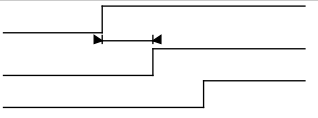
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0652	0.33

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.38	0.57	1.31
0.38	0.28	0.44	0.62	1.37
1.00	0.35	0.52	0.71	1.46
3.00	0.49	0.70	0.93	1.74

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

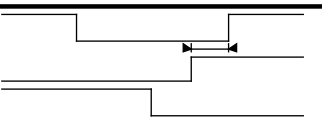
DATA	CLOCK	CONDITION
CD	CP	D

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.090	0.053	-0.010	-0.213
0.38	0.143	0.106	0.043	-0.157
1.00	0.230	0.194	0.133	-0.064
3.00	0.512	0.478	0.421	0.237

TIMING CONDITION

DATA	CLOCK	CONDITION
CD	CP	D

ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

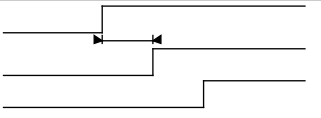
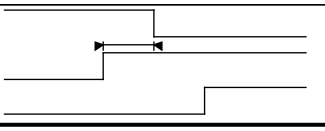
HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.564	0.602	0.666	0.870
0.38	0.512	0.550	0.612	0.814
1.00	0.425	0.461	0.523	0.721
3.00	0.143	0.177	0.234	0.418

YFD2 YFD2 5/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD

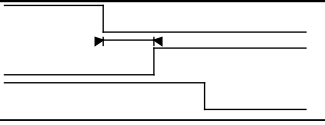
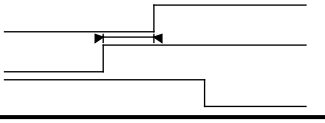
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.185	0.147	0.084	-0.121
0.38	0.234	0.198	0.136	-0.061
1.00	0.317	0.282	0.225	0.039
3.00	0.583	0.555	0.509	0.360

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.402	0.426	0.468	0.602
0.38	0.375	0.400	0.441	0.575
1.00	0.330	0.354	0.396	0.529
3.00	0.184	0.209	0.250	0.384

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.255	0.230	0.189	0.056
0.38	0.282	0.257	0.216	0.083
1.00	0.327	0.302	0.261	0.128
3.00	0.471	0.447	0.405	0.273

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.471	0.508	0.571	0.775
0.38	0.421	0.458	0.519	0.715
1.00	0.339	0.373	0.431	0.616
3.00	0.073	0.101	0.147	0.295

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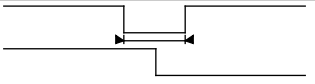
YFD2	YFD2	6/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

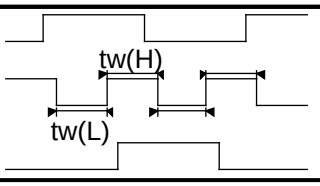
CLOCK	CONDITION
CD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.690

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	CD&D

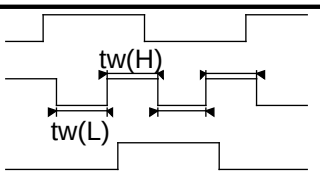
ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.710

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	CD&~D

ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.710

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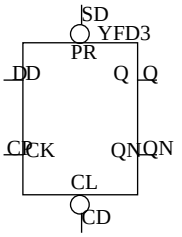
YFD3	YFD3	1/9

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YFD3	D-TYPE FLIP FLOP with CLEAR and PRESET	7	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT				OUTPUT	
CD	SD	D	CP	Qn+1	QNn+1
L	H	X	X*	L	H
H	L	X	X*	H	L
L	L	X	X	H	H
H	H	L	Up	L	H
H	H	H	Up	H	L
H	H	X	Dn	Qn	QNn

*:Consider the HOLD Time of CLEAR or PRESET

Verilog-HDL DESCRIPTION

```
YFD3 inst(Q,QN,D,CP,CD,SD);
```

VHDL DESCRIPTION

```
inst:YFD3
  port map(Q,QN,D,CP,CD,SD);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D	3.31
CP	0.99
CD	2.27
SD	2.16

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	34.6	36.5

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0662	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.27	0.46	1.20
0.38	0.19	0.35	0.54	1.28
1.00	0.26	0.46	0.66	1.42
3.00	0.39	0.67	0.94	1.82

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0985	0.35

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.26	0.42	1.00
0.38	0.15	0.29	0.45	1.03
1.00	0.18	0.34	0.50	1.09
3.00	0.22	0.41	0.61	1.27

PATH CONDITION

PATH	CONDITION	FUNCTION
QN->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0662	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.35	0.54	1.29
0.38	0.25	0.41	0.60	1.34
1.00	0.30	0.48	0.68	1.44
3.00	0.38	0.63	0.88	1.71

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0845	0.35

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.29	0.42	0.91
0.38	0.21	0.32	0.44	0.93
1.00	0.25	0.37	0.50	0.99
3.00	0.33	0.48	0.64	1.18

YFD3 YFD3 3/9

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CD->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0599	0.32

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.35	0.52	1.21
0.38	0.26	0.40	0.58	1.26
1.00	0.32	0.48	0.66	1.35
3.00	0.44	0.65	0.86	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0985	0.35

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.66	0.84	1.53
0.38	0.59	0.74	0.92	1.61
1.00	0.67	0.82	1.00	1.69
3.00	0.82	0.97	1.15	1.84

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0662	0.20

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.44	0.61	0.81	1.56
0.38	0.52	0.69	0.88	1.63
1.00	0.61	0.77	0.97	1.72
3.00	0.76	0.93	1.12	1.88

PATH CONDITION

PATH	CONDITION	FUNCTION
O->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0845	0.35

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.30	0.45	1.04
0.38	0.20	0.33	0.48	1.07
1.00	0.24	0.38	0.54	1.13
3.00	0.29	0.47	0.66	1.31

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
Q->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0599	0.32

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.34	0.51	1.19
0.38	0.27	0.42	0.59	1.27
1.00	0.36	0.53	0.72	1.42
3.00	0.55	0.77	1.01	1.81

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->QN	---	FALL

SLEW FACTOR

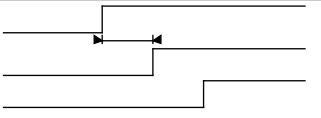
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0599	0.32

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.20	0.34	0.51	1.19
0.38	0.27	0.42	0.59	1.27
1.00	0.36	0.53	0.72	1.42
3.00	0.55	0.77	1.01	1.81

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

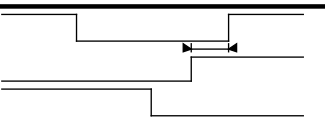
DATA	CLOCK	CONDITION
CD	CP	SD&D

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.080	0.041	-0.024	-0.232
0.38	0.130	0.092	0.029	-0.177
1.00	0.215	0.178	0.116	-0.084
3.00	0.489	0.455	0.398	0.214

TIMING CONDITION

DATA	CLOCK	CONDITION
CD	CP	SD&D

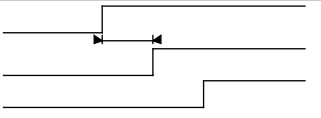
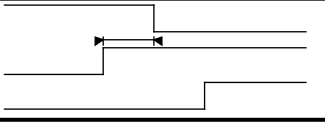
ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.577	0.616	0.680	0.886
0.38	0.527	0.564	0.627	0.831
1.00	0.441	0.478	0.540	0.739
3.00	0.167	0.201	0.258	0.442

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD&SD

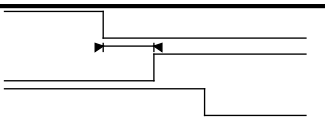
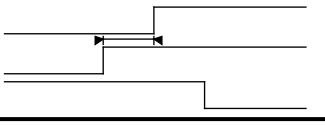
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.179	0.141	0.076	-0.132
0.38	0.227	0.190	0.128	-0.073
1.00	0.307	0.272	0.214	0.025
3.00	0.565	0.537	0.491	0.343

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.395	0.421	0.465	0.606
0.38	0.367	0.393	0.436	0.577
1.00	0.319	0.345	0.389	0.528
3.00	0.167	0.192	0.235	0.372

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	CD&SD

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

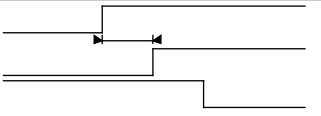
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.259	0.233	0.190	0.048
0.38	0.288	0.262	0.218	0.078
1.00	0.336	0.310	0.266	0.127
3.00	0.489	0.464	0.422	0.285

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.478	0.516	0.580	0.787
0.38	0.430	0.467	0.529	0.728
1.00	0.350	0.384	0.442	0.630
3.00	0.091	0.118	0.164	0.313

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

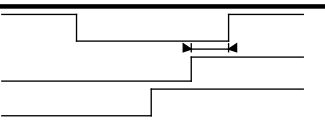
DATA	CLOCK	CONDITION
SD	CP	CD&~D

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.080	-0.122	-0.192	-0.419
0.38	-0.074	-0.116	-0.186	-0.413
1.00	-0.064	-0.106	-0.176	-0.404
3.00	-0.032	-0.074	-0.145	-0.372

TIMING CONDITION

DATA	CLOCK	CONDITION
SD	CP	CD&~D

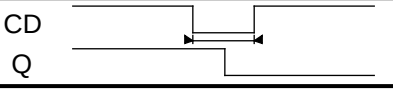
ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.734	0.777	0.849	1.081
0.38	0.728	0.771	0.843	1.075
1.00	0.719	0.761	0.833	1.064
3.00	0.688	0.730	0.801	1.028

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

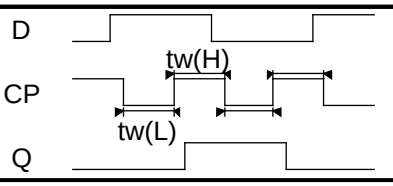
CLOCK	CONDITION
CD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.690

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	CD&SD&D

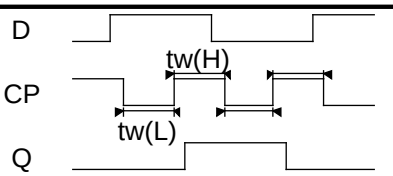
ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.710

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	CD&SD&~D

ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

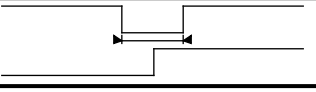
POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.710

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
SD	---

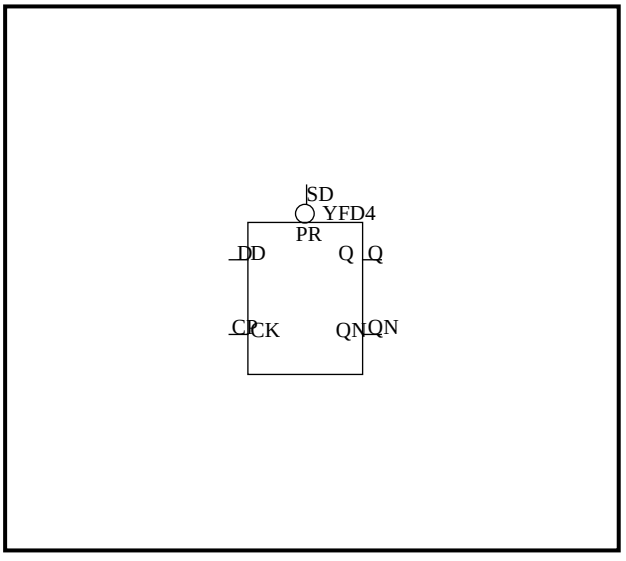
ITEM	WAVE_FORM
NEGLIMIT	SD Q 

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.690

YFD4	YFD4	1/6

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YFD4	D-TYPE FLIP FLOP with PRESET	6	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT	
SD	D	CP	Qn+1	QNn+1
L	X	X*	H	L
H	L	Up	L	H
H	H	Up	H	L
H	X	Dn	Qn	QNn

*:Consider the HOLD Time of PRESET

Verilog-HDL DESCRIPTION

```
YFD4  inst(Q,QN,D,CP,SD);
```

VHDL DESCRIPTION

```
inst:YFD4
   port   map(Q,QN,D,CP,SD);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D	3.36
CP	0.99
SD	2.17

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	35.6	36.1

Rev.1.01.10

YFD4 YFD4 2/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0947	0.32

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.48	0.62	0.79	1.46
0.38	0.56	0.70	0.87	1.54
1.00	0.64	0.78	0.95	1.62
3.00	0.79	0.93	1.10	1.77

PATH CONDITION

PATH	CONDITION	FUNCTION
CP->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0666	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.44	0.60	0.80	1.55
0.38	0.52	0.68	0.88	1.63
1.00	0.60	0.77	0.96	1.72
3.00	0.76	0.92	1.12	1.88

PATH CONDITION

PATH	CONDITION	FUNCTION
Q->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.1006	0.42

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.21	0.35	0.52	1.21
0.38	0.23	0.37	0.55	1.23
1.00	0.27	0.43	0.61	1.29
3.00	0.38	0.56	0.76	1.49

PATH CONDITION

PATH	CONDITION	FUNCTION
Q->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0417	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.24	0.36	0.84
0.38	0.21	0.32	0.45	0.93
1.00	0.29	0.43	0.57	1.08
3.00	0.40	0.60	0.81	1.45

YFD4 YFD4 3/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
SD->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0947	0.32

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.25	0.40	0.95
0.38	0.15	0.28	0.42	0.98
1.00	0.18	0.33	0.48	1.03
3.00	0.21	0.40	0.60	1.22

PATH CONDITION

PATH	CONDITION	FUNCTION
Q->QN	---	FALL

SLEW FACTOR

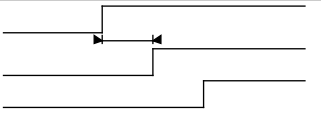
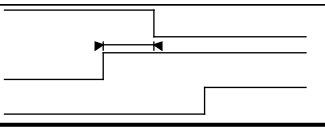
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0417	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.24	0.36	0.84
0.38	0.21	0.32	0.45	0.93
1.00	0.29	0.43	0.57	1.08
3.00	0.40	0.60	0.81	1.45

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	SD

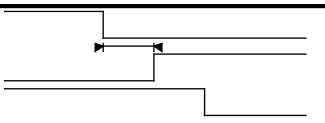
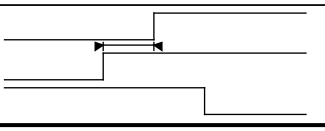
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.168	0.130	0.065	-0.143
0.38	0.211	0.174	0.112	-0.087
1.00	0.282	0.248	0.191	0.006
3.00	0.512	0.487	0.444	0.307

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.413	0.437	0.479	0.613
0.38	0.384	0.409	0.450	0.585
1.00	0.335	0.360	0.402	0.537
3.00	0.179	0.204	0.247	0.384

TIMING CONDITION

DATA	CLOCK	CONDITION
D	CP	SD

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

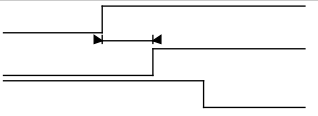
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.242	0.218	0.177	0.044
0.38	0.271	0.247	0.205	0.073
1.00	0.320	0.295	0.254	0.120
3.00	0.478	0.452	0.410	0.273

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.489	0.528	0.592	0.800
0.38	0.447	0.483	0.545	0.744
1.00	0.375	0.409	0.466	0.650
3.00	0.143	0.169	0.211	0.348

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

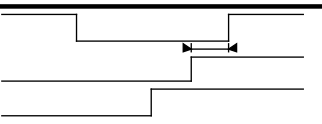
DATA	CLOCK	CONDITION
SD	CP	~D

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.027	-0.068	-0.137	-0.361
0.38	-0.030	-0.071	-0.140	-0.364
1.00	-0.034	-0.076	-0.146	-0.370
3.00	-0.050	-0.092	-0.162	-0.390

TIMING CONDITION

DATA	CLOCK	CONDITION
SD	CP	~D

ITEM	CLOCK	DATA	WAVE_FORM
HOLD	POSEDGE	LOW	

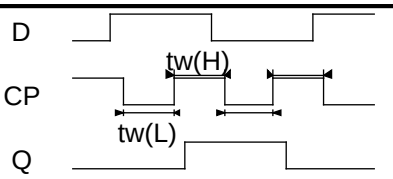
HOLD (ns)				
CLOCK SLEW (ns) DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.681	0.723	0.792	1.015
0.38	0.684	0.726	0.795	1.019
1.00	0.689	0.731	0.801	1.025
3.00	0.706	0.748	0.818	1.045

YFD4	YFD4	6/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	SD&D

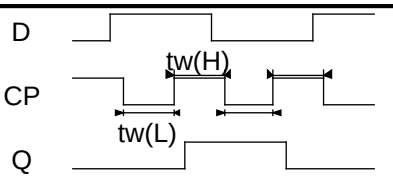
ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.710

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
CP	SD&~D

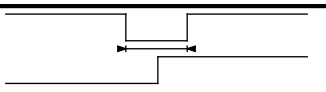
ITEM	WAVE_FORM
POSLIMIT	
NEGLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.710

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
SD	---

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.690

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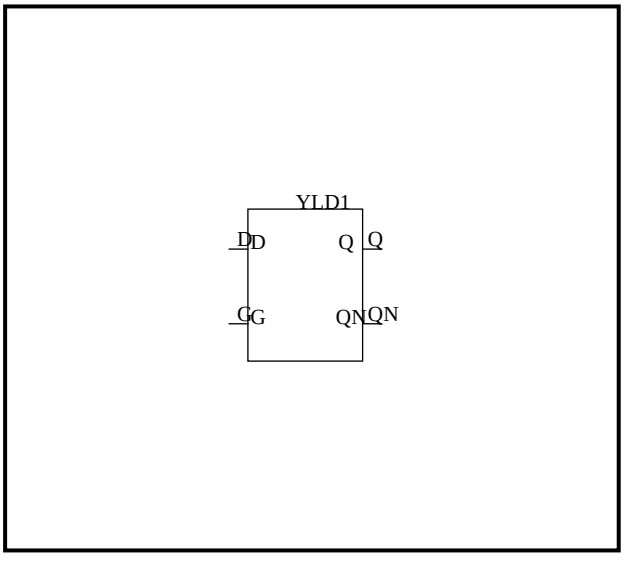
YLD1	YLD1	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YLD1	D-TYPE TRANSPARENT LATCH (HIGH ENABLE)	3	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
G	D	Q	QN
H	L	L	H
H	H	H	L
L	X	HOLD	

Verilog-HDL DESCRIPTION

```
YLD1  inst(Q,QN,D,G);
```

VHDL DESCRIPTION

```
inst:YLD1
   port   map(Q,QN,D,G);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D	3.27
G	0.99

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	36.2	42.8

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YLD1 YLD1 2/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QN->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.1033	0.41

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.38	0.56	1.29
0.38	0.25	0.40	0.59	1.33
1.00	0.31	0.47	0.66	1.39
3.00	0.45	0.66	0.87	1.65

PATH CONDITION

PATH	CONDITION	FUNCTION
QN->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0435	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.26	0.39	0.90
0.38	0.25	0.36	0.49	1.00
1.00	0.35	0.50	0.64	1.18
3.00	0.55	0.76	0.98	1.65

PATH CONDITION

PATH	CONDITION	FUNCTION
D->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0976	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.32	0.49	1.16
0.38	0.20	0.33	0.50	1.17
1.00	0.24	0.38	0.56	1.22
3.00	0.32	0.51	0.72	1.43

PATH CONDITION

PATH	CONDITION	FUNCTION
D->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0410	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.24	0.36	0.83
0.38	0.19	0.31	0.43	0.91
1.00	0.24	0.40	0.55	1.05
3.00	0.31	0.54	0.77	1.42

YLD1 YLD1 3/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QN->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.1033	0.41

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.38	0.56	1.29
0.38	0.25	0.40	0.59	1.33
1.00	0.31	0.47	0.66	1.39
3.00	0.45	0.66	0.87	1.65

PATH CONDITION

PATH	CONDITION	FUNCTION
QN->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0435	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.26	0.39	0.90
0.38	0.25	0.36	0.49	1.00
1.00	0.35	0.50	0.64	1.18
3.00	0.55	0.76	0.98	1.65

PATH CONDITION

PATH	CONDITION	FUNCTION
G->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0976	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.48	0.65	1.32
0.38	0.42	0.56	0.72	1.40
1.00	0.48	0.62	0.79	1.46
3.00	0.60	0.74	0.91	1.58

PATH CONDITION

PATH	CONDITION	FUNCTION
G->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0410	0.11

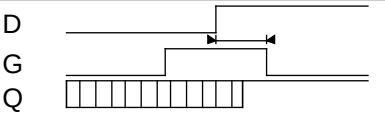
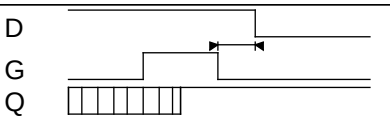
PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.39	0.52	0.99
0.38	0.37	0.47	0.59	1.06
1.00	0.44	0.54	0.66	1.13
3.00	0.56	0.67	0.79	1.26

YLD1	YLD1	4/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	G	---

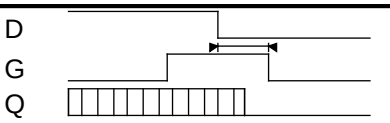
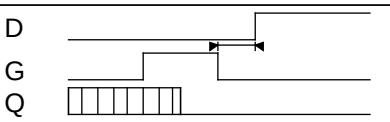
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.181	0.166	0.141	0.060
0.38	0.204	0.188	0.163	0.079
1.00	0.241	0.225	0.198	0.110
3.00	0.362	0.344	0.313	0.212

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.522	0.548	0.593	0.738
0.38	0.495	0.522	0.567	0.713
1.00	0.450	0.477	0.523	0.672
3.00	0.305	0.334	0.382	0.538

TIMING CONDITION

DATA	CLOCK	CONDITION
D	G	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.121	0.094	0.050	-0.094
0.38	0.148	0.121	0.076	-0.070
1.00	0.193	0.166	0.120	-0.028
3.00	0.339	0.310	0.262	0.106

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.463	0.478	0.503	0.585
0.38	0.441	0.456	0.482	0.566
1.00	0.403	0.419	0.447	0.535
3.00	0.282	0.301	0.332	0.433

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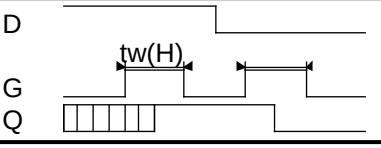
YLD1	YLD1	5/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

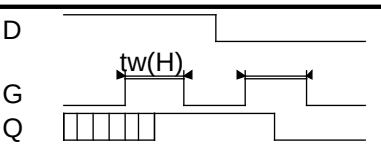
CLOCK	CONDITION
G	D

ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
G	~D

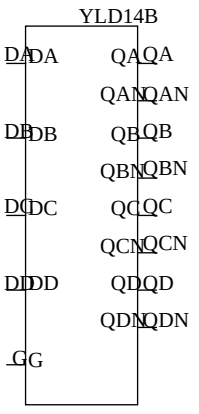
ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

YLD14B	YLD14B	1/16

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YLD14B	QUAD D-TYPE TRANSPARENT LATCH (HIGH ENABLE)	9	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
G	D	Q	QN
H	L	L	H
H	H	H	L
L	X	HOLD	

Verilog-HDL DESCRIPTION

```
YLD14B  inst(QA,QAN,QB,QBN,QC,QCN,
             QD,QDN,DA,DB,DC,DD,G)
             ;
```

VHDL DESCRIPTION

```
inst:YLD14B
   port   map(QA,QAN,QB,QBN,QC,
              QCN,QD,QDN,DA,DB,
              DC,DD,G);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	QA,QAN,QB,QBN,QC,QCN,QD,QDN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
DA	3.29
DB,DC,DD	3.30
G	0.99

OUTPUT DRIVE (LU)

PIN NAME	QA,QB,QC,QD	QAN,QBN,QCN,QDN
DRIVE	38.0	40.8

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YLD14B YLD14B 2/16

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QAN->QA	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QA	0.0995	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.37	0.55	1.26
0.38	0.25	0.40	0.58	1.30
1.00	0.31	0.47	0.65	1.36
3.00	0.46	0.65	0.86	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
QAN->QA	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QA	0.0408	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.25	0.37	0.86
0.38	0.24	0.35	0.47	0.96
1.00	0.34	0.48	0.63	1.13
3.00	0.54	0.75	0.97	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
DA->QAN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QAN	0.1014	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.32	0.49	1.18
0.38	0.20	0.34	0.51	1.19
1.00	0.23	0.39	0.57	1.25
3.00	0.32	0.51	0.72	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
DA->QAN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QAN	0.0436	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.25	0.38	0.87
0.38	0.19	0.31	0.44	0.94
1.00	0.24	0.40	0.56	1.08
3.00	0.31	0.54	0.77	1.44

YLD14B YLD14B 3/16

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QBN->QB	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QB	0.0995	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.37	0.55	1.26
0.38	0.25	0.40	0.58	1.30
1.00	0.31	0.47	0.65	1.36
3.00	0.46	0.65	0.86	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
QBN->QB	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QB	0.0408	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.25	0.37	0.86
0.38	0.24	0.35	0.47	0.96
1.00	0.34	0.48	0.63	1.13
3.00	0.54	0.75	0.97	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
DB->QBN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QBN	0.1013	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.32	0.49	1.18
0.38	0.20	0.34	0.51	1.19
1.00	0.23	0.39	0.57	1.25
3.00	0.32	0.51	0.72	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
DB->QBN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QBN	0.0436	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.25	0.38	0.87
0.38	0.19	0.31	0.44	0.94
1.00	0.24	0.40	0.56	1.08
3.00	0.31	0.54	0.77	1.44

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YLD14B | YLD14B | 4/16

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QCN->QC	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QC	0.0995	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.37	0.55	1.26
0.38	0.25	0.40	0.58	1.30
1.00	0.31	0.47	0.65	1.36
3.00	0.46	0.65	0.86	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
QCN->QC	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QC	0.0408	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.25	0.37	0.86
0.38	0.24	0.35	0.47	0.96
1.00	0.34	0.48	0.63	1.13
3.00	0.54	0.75	0.97	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
DC->QCN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QCN	0.1013	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.32	0.49	1.18
0.38	0.20	0.34	0.51	1.19
1.00	0.23	0.39	0.57	1.25
3.00	0.32	0.51	0.72	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
DC->QCN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QCN	0.0436	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.25	0.38	0.87
0.38	0.19	0.31	0.44	0.94
1.00	0.24	0.40	0.56	1.08
3.00	0.31	0.54	0.77	1.44

YLD14B YLD14B 5/16

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QDN->QD	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QD	0.0995	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.37	0.55	1.26
0.38	0.25	0.40	0.58	1.30
1.00	0.31	0.47	0.65	1.36
3.00	0.46	0.65	0.86	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
QDN->QD	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QD	0.0408	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.25	0.37	0.86
0.38	0.24	0.35	0.47	0.96
1.00	0.34	0.48	0.63	1.13
3.00	0.54	0.75	0.97	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
DD->QDN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QDN	0.1013	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.32	0.49	1.18
0.38	0.20	0.34	0.51	1.19
1.00	0.23	0.39	0.57	1.25
3.00	0.32	0.51	0.72	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
DD->QDN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QDN	0.0436	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.25	0.38	0.87
0.38	0.19	0.31	0.44	0.94
1.00	0.24	0.40	0.56	1.08
3.00	0.31	0.54	0.77	1.44

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YLD14B YLD14B 6/16

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QAN->QA	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QA	0.0995	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.37	0.55	1.26
0.38	0.25	0.40	0.58	1.30
1.00	0.31	0.47	0.65	1.36
3.00	0.46	0.65	0.86	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
QAN->QA	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QA	0.0408	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.25	0.37	0.86
0.38	0.24	0.35	0.47	0.96
1.00	0.34	0.48	0.63	1.13
3.00	0.54	0.75	0.97	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
G->QAN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QAN	0.1014	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.66	0.83	1.52
0.38	0.60	0.74	0.92	1.61
1.00	0.71	0.85	1.02	1.71
3.00	0.90	1.04	1.21	1.90

PATH CONDITION

PATH	CONDITION	FUNCTION
G->QAN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QAN	0.0436	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.47	0.60	1.09
0.38	0.45	0.56	0.68	1.18
1.00	0.55	0.66	0.79	1.28
3.00	0.74	0.85	0.98	1.47

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QBN->QB	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QB	0.0995	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.37	0.55	1.26
0.38	0.25	0.40	0.58	1.30
1.00	0.31	0.47	0.65	1.36
3.00	0.46	0.65	0.86	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
QBN->QB	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QB	0.0408	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.25	0.37	0.86
0.38	0.24	0.35	0.47	0.96
1.00	0.34	0.48	0.63	1.13
3.00	0.54	0.75	0.97	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
G->QBN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QBN	0.1013	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.66	0.83	1.52
0.38	0.60	0.74	0.92	1.61
1.00	0.71	0.85	1.02	1.71
3.00	0.90	1.04	1.21	1.90

PATH CONDITION

PATH	CONDITION	FUNCTION
G->QBN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QBN	0.0436	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.47	0.60	1.09
0.38	0.45	0.56	0.69	1.18
1.00	0.55	0.66	0.79	1.28
3.00	0.74	0.85	0.98	1.47

YLD14B YLD14B 8/16

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QCN->QC	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QC	0.0995	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.37	0.55	1.26
0.38	0.25	0.40	0.58	1.30
1.00	0.31	0.47	0.65	1.36
3.00	0.46	0.65	0.86	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
QCN->QC	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QC	0.0408	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.25	0.37	0.86
0.38	0.24	0.35	0.47	0.96
1.00	0.34	0.48	0.63	1.13
3.00	0.54	0.75	0.97	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
G->QCN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QCN	0.1013	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.66	0.83	1.52
0.38	0.60	0.74	0.92	1.61
1.00	0.71	0.85	1.02	1.71
3.00	0.90	1.04	1.21	1.90

PATH CONDITION

PATH	CONDITION	FUNCTION
G->QCN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QCN	0.0436	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.47	0.60	1.09
0.38	0.45	0.56	0.69	1.18
1.00	0.55	0.66	0.79	1.28
3.00	0.74	0.85	0.98	1.47

YLD14B | YLD14B | 9/16

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QDN->QD	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QD	0.0995	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.37	0.55	1.26
0.38	0.25	0.40	0.58	1.30
1.00	0.31	0.47	0.65	1.36
3.00	0.46	0.65	0.86	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
QDN->QD	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QD	0.0408	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.25	0.37	0.86
0.38	0.24	0.35	0.47	0.96
1.00	0.34	0.48	0.63	1.13
3.00	0.54	0.75	0.97	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
G->QDN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QDN	0.1013	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.66	0.83	1.52
0.38	0.60	0.74	0.92	1.61
1.00	0.71	0.85	1.02	1.71
3.00	0.90	1.04	1.21	1.90

PATH CONDITION

PATH	CONDITION	FUNCTION
G->QDN	---	FALL

SLEW FACTOR

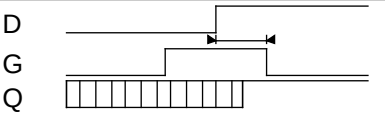
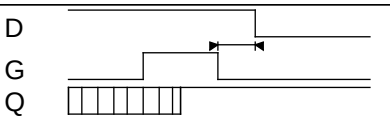
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QDN	0.0436	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.47	0.60	1.09
0.38	0.45	0.56	0.69	1.18
1.00	0.55	0.66	0.79	1.28
3.00	0.74	0.85	0.98	1.47

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
DA	G	---

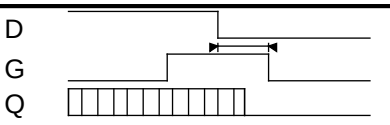
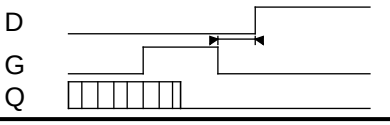
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.100	0.072	0.025	-0.127
0.38	0.120	0.092	0.046	-0.105
1.00	0.154	0.126	0.081	-0.067
3.00	0.262	0.237	0.193	0.054

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.688	0.721	0.778	0.959
0.38	0.662	0.696	0.754	0.938
1.00	0.619	0.654	0.713	0.903
3.00	0.481	0.519	0.583	0.790

TIMING CONDITION

DATA	CLOCK	CONDITION
DA	G	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

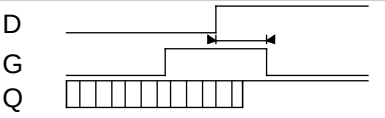
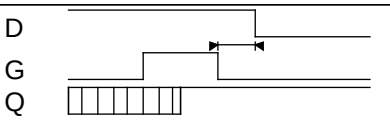
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.042	-0.076	-0.133	-0.317
0.38	-0.016	-0.051	-0.109	-0.296
1.00	0.026	-0.009	-0.069	-0.260
3.00	0.163	0.125	0.061	-0.145

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.546	0.574	0.621	0.773
0.38	0.526	0.553	0.600	0.750
1.00	0.491	0.519	0.565	0.713
3.00	0.381	0.407	0.451	0.591

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
DB	G	---

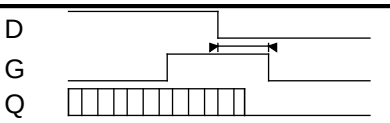
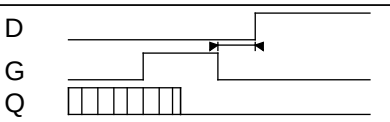
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.100	0.072	0.025	-0.127
0.38	0.120	0.092	0.046	-0.105
1.00	0.154	0.126	0.081	-0.067
3.00	0.262	0.237	0.193	0.054

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.688	0.721	0.778	0.959
0.38	0.662	0.696	0.754	0.938
1.00	0.619	0.654	0.713	0.903
3.00	0.481	0.519	0.583	0.790

TIMING CONDITION

DATA	CLOCK	CONDITION
DB	G	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

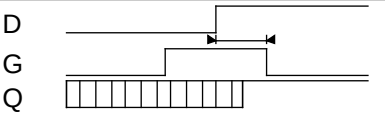
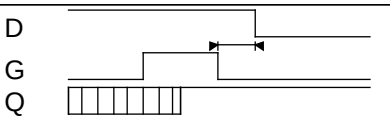
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.042	-0.076	-0.133	-0.317
0.38	-0.016	-0.051	-0.109	-0.296
1.00	0.026	-0.009	-0.069	-0.260
3.00	0.163	0.125	0.061	-0.145

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.546	0.574	0.621	0.773
0.38	0.526	0.553	0.600	0.750
1.00	0.491	0.519	0.565	0.713
3.00	0.381	0.407	0.451	0.591

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
DC	G	---

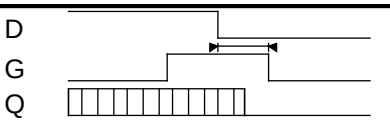
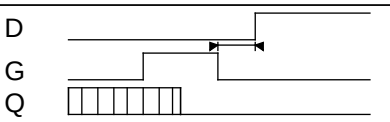
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.100	0.072	0.025	-0.127
0.38	0.120	0.092	0.046	-0.105
1.00	0.154	0.126	0.081	-0.067
3.00	0.262	0.237	0.193	0.054

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.688	0.721	0.778	0.959
0.38	0.662	0.696	0.754	0.938
1.00	0.619	0.654	0.713	0.903
3.00	0.481	0.519	0.583	0.790

TIMING CONDITION

DATA	CLOCK	CONDITION
DC	G	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

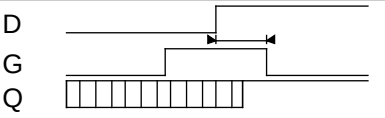
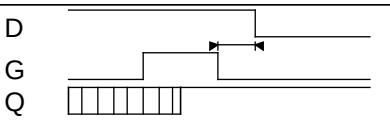
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.042	-0.076	-0.133	-0.317
0.38	-0.016	-0.051	-0.109	-0.296
1.00	0.026	-0.009	-0.069	-0.260
3.00	0.163	0.125	0.061	-0.145

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.546	0.574	0.621	0.773
0.38	0.526	0.553	0.600	0.750
1.00	0.491	0.519	0.565	0.713
3.00	0.381	0.407	0.451	0.591

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
DD	G	---

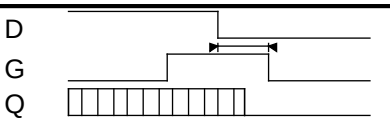
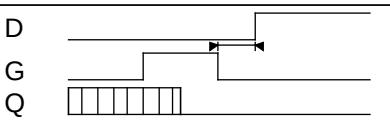
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	HIGH	
HOLD	NEGEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.100	0.072	0.025	-0.127
0.38	0.120	0.092	0.046	-0.105
1.00	0.154	0.126	0.081	-0.067
3.00	0.262	0.237	0.193	0.054

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.688	0.721	0.778	0.959
0.38	0.662	0.696	0.754	0.938
1.00	0.619	0.654	0.713	0.903
3.00	0.481	0.519	0.583	0.790

TIMING CONDITION

DATA	CLOCK	CONDITION
DD	G	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	NEGEDGE	LOW	
HOLD	NEGEDGE	LOW	

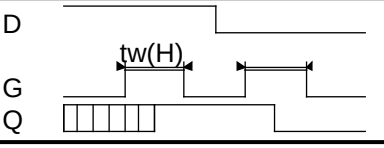
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	-0.042	-0.076	-0.133	-0.317
0.38	-0.016	-0.051	-0.109	-0.296
1.00	0.026	-0.009	-0.069	-0.260
3.00	0.163	0.125	0.061	-0.145

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.546	0.574	0.621	0.773
0.38	0.526	0.553	0.600	0.750
1.00	0.491	0.519	0.565	0.713
3.00	0.381	0.407	0.451	0.591

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

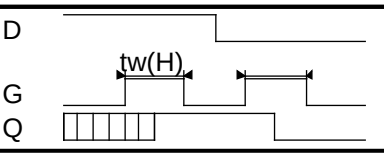
CLOCK	CONDITION
G	DA

ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

MINIMUM PULSE WIDTH CONDITION

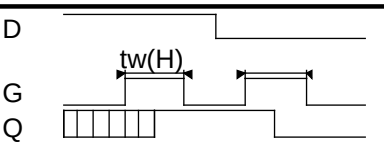
CLOCK	CONDITION
G	~DA

ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
G	DB

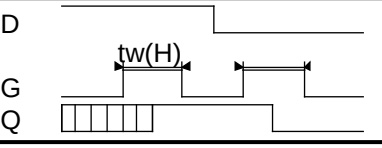
ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

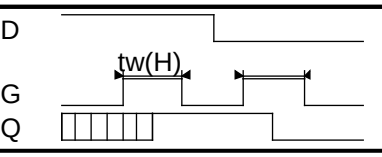
CLOCK	CONDITION
G	~DB

ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

MINIMUM PULSE WIDTH CONDITION

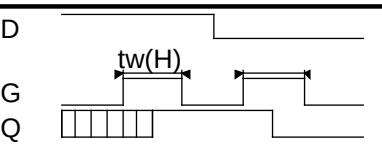
CLOCK	CONDITION
G	DC

ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
G	~DC

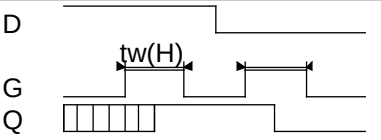
ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

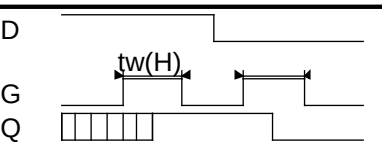
CLOCK	CONDITION
G	DD

ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
G	~DD

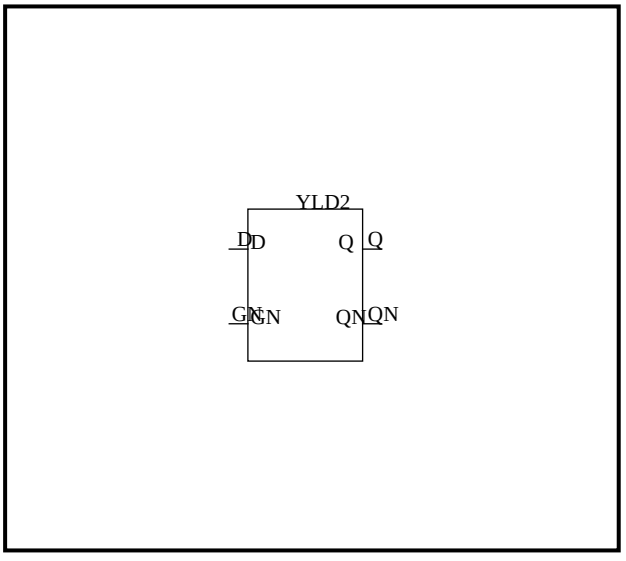
ITEM	WAVE_FORM
POSLIMIT	

POSLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.870

YLD2	YLD2	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YLD2	D-TYPE TRANSPARENT LATCH (LOW ENABLE)	3	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
GN	D	Q	QN
L	L	L	H
L	H	H	L
H	X	HOLD	

Verilog-HDL DESCRIPTION

```
YLD2  inst(Q,QN,D,GN);
```

VHDL DESCRIPTION

```
inst:YLD2
   port   map(Q,QN,D,GN);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Q,QN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
D	3.26
GN	0.99

OUTPUT DRIVE (LU)

PIN NAME	Q	QN
DRIVE	36.2	42.8

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YLD2 YLD2 2/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QN->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.1033	0.41

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.38	0.56	1.29
0.38	0.25	0.40	0.59	1.33
1.00	0.31	0.47	0.66	1.39
3.00	0.45	0.66	0.87	1.65

PATH CONDITION

PATH	CONDITION	FUNCTION
QN->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0435	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.26	0.39	0.90
0.38	0.25	0.36	0.49	1.00
1.00	0.35	0.50	0.64	1.18
3.00	0.55	0.76	0.98	1.65

PATH CONDITION

PATH	CONDITION	FUNCTION
D->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0976	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.32	0.49	1.16
0.38	0.20	0.33	0.50	1.17
1.00	0.24	0.38	0.56	1.22
3.00	0.32	0.51	0.72	1.43

PATH CONDITION

PATH	CONDITION	FUNCTION
D->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0410	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.24	0.36	0.83
0.38	0.19	0.31	0.43	0.91
1.00	0.24	0.40	0.55	1.05
3.00	0.31	0.54	0.77	1.42

YLD2 YLD2 3/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QN->Q	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.1033	0.41

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.38	0.56	1.29
0.38	0.25	0.40	0.59	1.33
1.00	0.31	0.47	0.66	1.39
3.00	0.45	0.66	0.87	1.65

PATH CONDITION

PATH	CONDITION	FUNCTION
QN->Q	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Q	0.0435	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.26	0.39	0.90
0.38	0.25	0.36	0.49	1.00
1.00	0.35	0.50	0.64	1.18
3.00	0.55	0.76	0.98	1.65

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->QN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0976	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.48	0.65	1.32
0.38	0.38	0.52	0.69	1.36
1.00	0.44	0.58	0.75	1.42
3.00	0.56	0.69	0.86	1.54

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->QN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QN	0.0410	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.44	0.56	1.03
0.38	0.37	0.48	0.60	1.07
1.00	0.43	0.54	0.66	1.13
3.00	0.55	0.65	0.77	1.24

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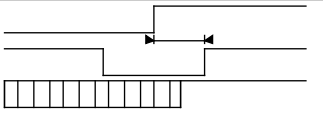
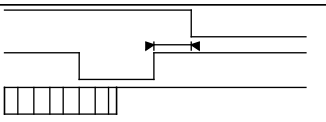
YLD2 YLD2 4/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
D	GN	---

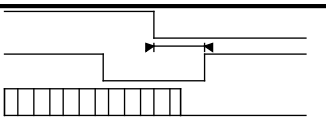
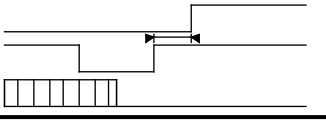
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.172	0.140	0.085	-0.091
0.38	0.205	0.174	0.122	-0.045
1.00	0.260	0.232	0.185	0.033
3.00	0.437	0.418	0.386	0.285

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.424	0.440	0.467	0.554
0.38	0.405	0.421	0.447	0.534
1.00	0.372	0.388	0.415	0.501
3.00	0.266	0.282	0.309	0.395

TIMING CONDITION

DATA	CLOCK	CONDITION
D	GN	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.219	0.203	0.176	0.090
0.38	0.238	0.222	0.196	0.109
1.00	0.271	0.255	0.229	0.143
3.00	0.378	0.362	0.335	0.249

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.471	0.503	0.558	0.734
0.38	0.438	0.469	0.521	0.687
1.00	0.384	0.412	0.459	0.610
3.00	0.208	0.227	0.258	0.360

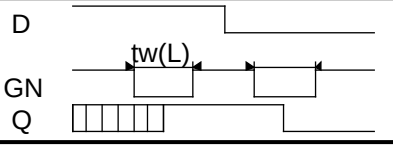
Rev.1.01.10

YLD2	YLD2	5/5

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

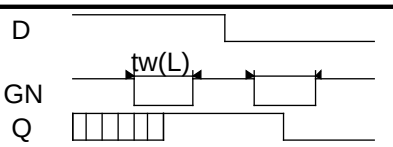
CLOCK	CONDITION
GN	D

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.690

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
GN	~D

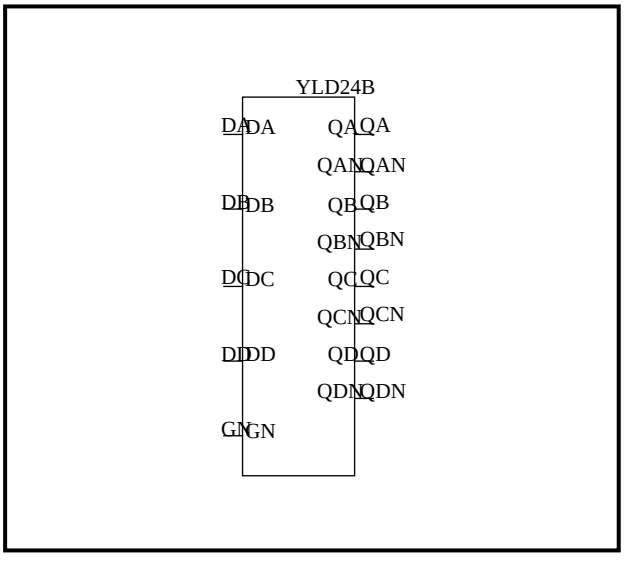
ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.690

YLD24B	YLD24B	1/16

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YLD24B	QUAD D-TYPE TRANSPARENT LATCH (LOW ENABLE)	9	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
GN	D	Q	QN
L	L	L	H
L	H	H	L
H	X	HOLD	

Verilog-HDL DESCRIPTION

```
YLD24B  inst(QA,QAN,QB,QBN,QC,QCN,
             QD,QDN,DA,DB,DC,DD,
             GN);
```

VHDL DESCRIPTION

```
inst:YLD24B
   port   map(QA,QAN,QB,QBN,QC,
              QCN,QD,QDN,DA,DB,
              DC,DD,GN);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	QA,QAN,QB,QBN,QC,QCN,QD,QDN
ELECTRO MIGRATION DRIVE	6880.0

INPUT LOAD (LU)

PIN NAME	LOAD
DA	3.29
DB,DC,DD	3.30
GN	0.99

OUTPUT DRIVE (LU)

PIN NAME	QA,QB,QC,QD	QAN,QBN,QDN	QCN
DRIVE	38.0	40.8	36.8

Rev.1.01.10

YLD24B | YLD24B | 2/16

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QAN->QA	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QA	0.0995	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.37	0.55	1.26
0.38	0.25	0.40	0.58	1.30
1.00	0.31	0.47	0.65	1.36
3.00	0.46	0.65	0.86	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
QAN->QA	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QA	0.0408	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.25	0.37	0.86
0.38	0.24	0.35	0.47	0.96
1.00	0.34	0.48	0.63	1.13
3.00	0.54	0.75	0.97	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
DA->QAN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QAN	0.1014	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.32	0.49	1.18
0.38	0.20	0.34	0.51	1.19
1.00	0.23	0.39	0.57	1.25
3.00	0.32	0.51	0.72	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
DA->QAN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QAN	0.0433	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.25	0.38	0.87
0.38	0.19	0.31	0.44	0.94
1.00	0.24	0.40	0.56	1.08
3.00	0.31	0.54	0.77	1.44

YLD24B | YLD24B | 3/16

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QBN->QB	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QB	0.0995	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.37	0.55	1.26
0.38	0.25	0.40	0.58	1.30
1.00	0.31	0.47	0.65	1.36
3.00	0.46	0.65	0.86	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
QBN->QB	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QB	0.0408	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.25	0.37	0.86
0.38	0.24	0.35	0.47	0.96
1.00	0.34	0.48	0.63	1.13
3.00	0.54	0.75	0.97	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
DB->QBN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QBN	0.1014	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.32	0.49	1.18
0.38	0.20	0.34	0.51	1.19
1.00	0.23	0.39	0.57	1.25
3.00	0.32	0.51	0.72	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
DB->QBN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QBN	0.0433	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.25	0.38	0.87
0.38	0.19	0.31	0.44	0.94
1.00	0.24	0.40	0.56	1.08
3.00	0.31	0.54	0.77	1.44

YLD24B YLD24B 4/16

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QCN->QC	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QC	0.0995	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.37	0.55	1.26
0.38	0.25	0.40	0.58	1.30
1.00	0.31	0.47	0.65	1.36
3.00	0.46	0.65	0.86	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
QCN->QC	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QC	0.0408	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.25	0.37	0.86
0.38	0.24	0.35	0.47	0.96
1.00	0.34	0.48	0.63	1.13
3.00	0.54	0.75	0.97	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
DC->QCN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QCN	0.1025	0.21

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.17	0.32	0.50	1.22
0.38	0.19	0.34	0.51	1.24
1.00	0.23	0.39	0.57	1.29
3.00	0.30	0.51	0.73	1.51

PATH CONDITION

PATH	CONDITION	FUNCTION
DC->QCN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QCN	0.0433	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.25	0.38	0.88
0.38	0.19	0.31	0.45	0.95
1.00	0.24	0.40	0.56	1.10
3.00	0.30	0.54	0.78	1.49

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QDN->QD	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QD	0.0995	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.37	0.55	1.26
0.38	0.25	0.40	0.58	1.30
1.00	0.31	0.47	0.65	1.36
3.00	0.46	0.65	0.86	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
QDN->QD	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QD	0.0408	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.25	0.37	0.86
0.38	0.24	0.35	0.47	0.96
1.00	0.34	0.48	0.63	1.13
3.00	0.54	0.75	0.97	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
DD->QDN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QDN	0.1014	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.18	0.32	0.49	1.18
0.38	0.20	0.34	0.51	1.19
1.00	0.23	0.39	0.57	1.25
3.00	0.32	0.51	0.72	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
DD->QDN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QDN	0.0433	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.14	0.25	0.38	0.87
0.38	0.19	0.31	0.44	0.94
1.00	0.24	0.40	0.56	1.08
3.00	0.31	0.54	0.77	1.44

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QAN->QA	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QA	0.0995	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.37	0.55	1.26
0.38	0.25	0.40	0.58	1.30
1.00	0.31	0.47	0.65	1.36
3.00	0.46	0.65	0.86	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
QAN->QA	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QA	0.0408	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.25	0.37	0.86
0.38	0.24	0.35	0.47	0.96
1.00	0.34	0.48	0.63	1.13
3.00	0.54	0.75	0.97	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->QAN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QAN	0.1014	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.60	0.77	1.46
0.38	0.49	0.63	0.80	1.49
1.00	0.56	0.70	0.88	1.57
3.00	0.72	0.86	1.04	1.73

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->QAN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QAN	0.0433	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.54	0.65	0.78	1.27
0.38	0.57	0.68	0.81	1.30
1.00	0.65	0.76	0.89	1.38
3.00	0.82	0.93	1.06	1.55

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QBN->QB	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QB	0.0995	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.37	0.55	1.26
0.38	0.25	0.40	0.58	1.30
1.00	0.31	0.47	0.65	1.36
3.00	0.46	0.65	0.86	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
QBN->QB	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QB	0.0408	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.25	0.37	0.86
0.38	0.24	0.35	0.47	0.96
1.00	0.34	0.48	0.63	1.13
3.00	0.54	0.75	0.97	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->QBN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QBN	0.1014	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.60	0.77	1.46
0.38	0.48	0.63	0.80	1.49
1.00	0.56	0.70	0.88	1.57
3.00	0.72	0.86	1.04	1.73

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->QBN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QBN	0.0433	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.54	0.65	0.78	1.27
0.38	0.57	0.68	0.81	1.30
1.00	0.65	0.76	0.89	1.38
3.00	0.82	0.93	1.06	1.55

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QCN->QC	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QC	0.0995	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.37	0.55	1.26
0.38	0.25	0.40	0.58	1.30
1.00	0.31	0.47	0.65	1.36
3.00	0.46	0.65	0.86	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
QCN->QC	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QC	0.0408	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.25	0.37	0.86
0.38	0.24	0.35	0.47	0.96
1.00	0.34	0.48	0.63	1.13
3.00	0.54	0.75	0.97	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->QCN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QCN	0.1025	0.21

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.60	0.77	1.46
0.38	0.48	0.63	0.80	1.49
1.00	0.56	0.70	0.88	1.57
3.00	0.72	0.86	1.04	1.73

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->QCN	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QCN	0.0433	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.54	0.65	0.78	1.27
0.38	0.57	0.68	0.81	1.30
1.00	0.65	0.76	0.89	1.38
3.00	0.82	0.93	1.06	1.55

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
QDN->QD	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QD	0.0995	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.22	0.37	0.55	1.26
0.38	0.25	0.40	0.58	1.30
1.00	0.31	0.47	0.65	1.36
3.00	0.46	0.65	0.86	1.62

PATH CONDITION

PATH	CONDITION	FUNCTION
QDN->QD	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QD	0.0408	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.15	0.25	0.37	0.86
0.38	0.24	0.35	0.47	0.96
1.00	0.34	0.48	0.63	1.13
3.00	0.54	0.75	0.97	1.61

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->QDN	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QDN	0.1014	0.23

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.60	0.77	1.46
0.38	0.48	0.63	0.80	1.49
1.00	0.56	0.70	0.88	1.57
3.00	0.72	0.86	1.04	1.73

PATH CONDITION

PATH	CONDITION	FUNCTION
GN->QDN	---	FALL

SLEW FACTOR

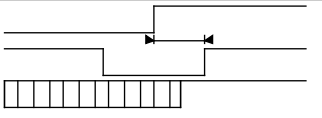
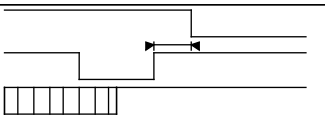
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
QDN	0.0433	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.54	0.65	0.78	1.27
0.38	0.57	0.68	0.81	1.30
1.00	0.65	0.76	0.89	1.38
3.00	0.82	0.93	1.06	1.55

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
DA	GN	---

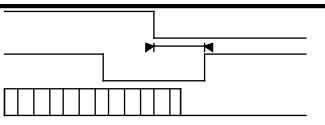
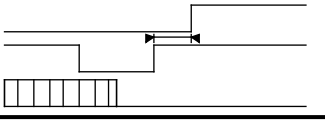
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.073	0.025	-0.055	-0.313
0.38	0.111	0.065	-0.012	-0.260
1.00	0.176	0.133	0.061	-0.171
3.00	0.384	0.351	0.295	0.115

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.472	0.506	0.563	0.746
0.38	0.455	0.488	0.543	0.720
1.00	0.427	0.458	0.510	0.676
3.00	0.337	0.362	0.403	0.535

TIMING CONDITION

DATA	CLOCK	CONDITION
DA	GN	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

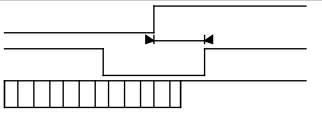
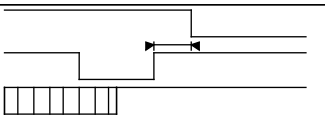
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.172	0.138	0.080	-0.103
0.38	0.189	0.156	0.101	-0.077
1.00	0.218	0.187	0.135	-0.033
3.00	0.313	0.288	0.245	0.108

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.570	0.618	0.698	0.957
0.38	0.532	0.578	0.655	0.904
1.00	0.468	0.511	0.583	0.816
3.00	0.261	0.294	0.350	0.530

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
DB	GN	---

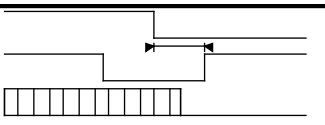
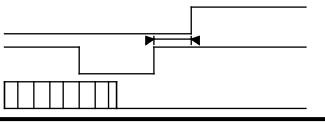
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.073	0.025	-0.055	-0.313
0.38	0.111	0.065	-0.012	-0.260
1.00	0.176	0.133	0.061	-0.171
3.00	0.384	0.351	0.295	0.115

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.472	0.506	0.563	0.746
0.38	0.455	0.488	0.543	0.720
1.00	0.427	0.458	0.510	0.676
3.00	0.337	0.362	0.403	0.535

TIMING CONDITION

DATA	CLOCK	CONDITION
DB	GN	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

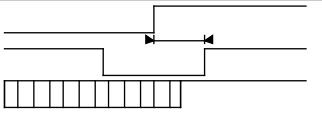
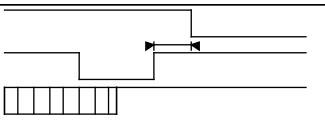
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.172	0.138	0.080	-0.103
0.38	0.189	0.156	0.101	-0.077
1.00	0.218	0.187	0.135	-0.033
3.00	0.313	0.288	0.245	0.108

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.570	0.618	0.698	0.957
0.38	0.532	0.578	0.655	0.904
1.00	0.468	0.511	0.583	0.816
3.00	0.261	0.294	0.350	0.530

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
DC	GN	---

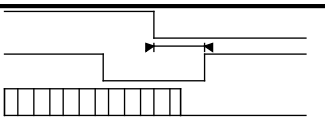
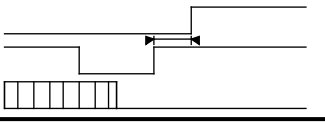
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.073	0.025	-0.055	-0.313
0.38	0.111	0.065	-0.012	-0.260
1.00	0.176	0.133	0.061	-0.171
3.00	0.384	0.351	0.295	0.115

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.472	0.506	0.563	0.746
0.38	0.455	0.488	0.543	0.720
1.00	0.427	0.458	0.510	0.676
3.00	0.337	0.362	0.403	0.535

TIMING CONDITION

DATA	CLOCK	CONDITION
DC	GN	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

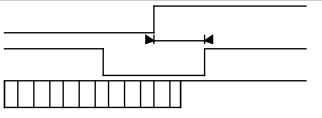
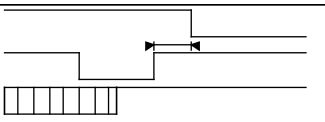
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.172	0.138	0.080	-0.103
0.38	0.189	0.156	0.101	-0.077
1.00	0.218	0.187	0.135	-0.033
3.00	0.313	0.288	0.245	0.108

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.570	0.618	0.698	0.957
0.38	0.532	0.578	0.655	0.904
1.00	0.468	0.511	0.583	0.816
3.00	0.261	0.294	0.350	0.530

CONDITION:VDD=3.3V, Ta=25°C, Typ.

TIMING CONDITION

DATA	CLOCK	CONDITION
DD	GN	---

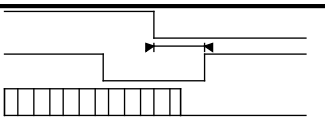
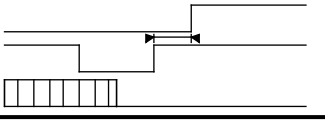
ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	HIGH	
HOLD	POSEDGE	HIGH	

SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.073	0.025	-0.055	-0.313
0.38	0.111	0.065	-0.012	-0.260
1.00	0.176	0.133	0.061	-0.171
3.00	0.384	0.351	0.295	0.115

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.472	0.506	0.563	0.746
0.38	0.455	0.488	0.543	0.720
1.00	0.427	0.458	0.510	0.676
3.00	0.337	0.362	0.403	0.535

TIMING CONDITION

DATA	CLOCK	CONDITION
DD	GN	---

ITEM	CLOCK	DATA	WAVE_FORM
SETUP	POSEDGE	LOW	
HOLD	POSEDGE	LOW	

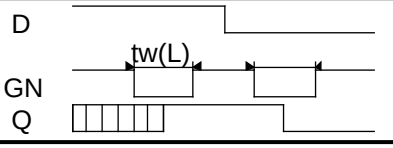
SETUP (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.172	0.138	0.080	-0.103
0.38	0.189	0.156	0.101	-0.077
1.00	0.218	0.187	0.135	-0.033
3.00	0.313	0.288	0.245	0.108

HOLD (ns)				
CLOCK SLEW (ns) / DATA SLEW (ns)	0.01	0.38	1.00	3.00
0.01	0.570	0.618	0.698	0.957
0.38	0.532	0.578	0.655	0.904
1.00	0.468	0.511	0.583	0.816
3.00	0.261	0.294	0.350	0.530

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

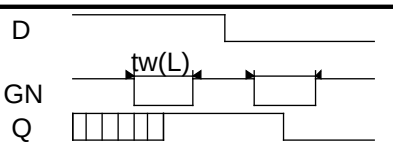
CLOCK	CONDITION
GN	DA

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.760

MINIMUM PULSE WIDTH CONDITION

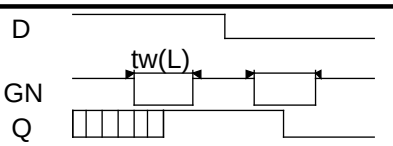
CLOCK	CONDITION
GN	~DA

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.720

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
GN	DB

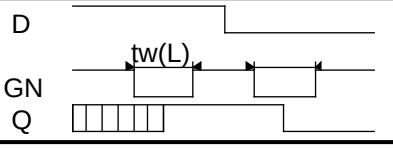
ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.760

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

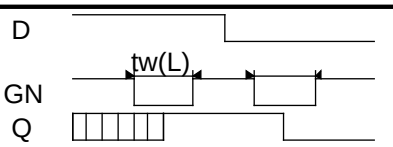
CLOCK	CONDITION
GN	~DB

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.720

MINIMUM PULSE WIDTH CONDITION

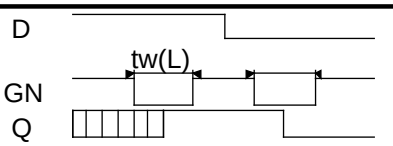
CLOCK	CONDITION
GN	DC

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.760

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
GN	~DC

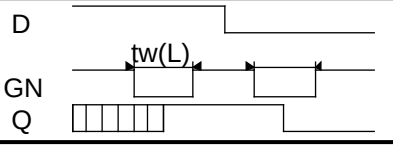
ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.720

CONDITION:VDD=3.3V, Ta=25°C, Typ.

MINIMUM PULSE WIDTH CONDITION

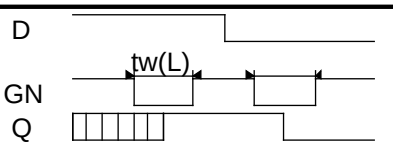
CLOCK	CONDITION
GN	DD

ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.760

MINIMUM PULSE WIDTH CONDITION

CLOCK	CONDITION
GN	~DD

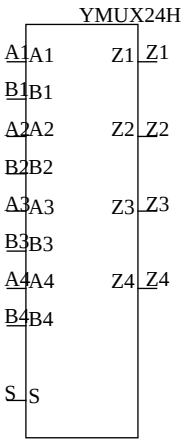
ITEM	WAVE_FORM
NEGLIMIT	

NEGLIMIT (ns)	
RISE SLEW (ns) FALL SLEW (ns)	0.01 to 3.00
0.01 to 3.00	0.720

YMUX24H	YMUX24H	1/9

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YMUX24H	QUAD 2 TO 1 MULTIPLEXER	11	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
S	A	B	Z
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

Verilog-HDL DESCRIPTION

```
YMUX24H  inst(Z1,Z2,Z3,Z4,A1,B1,
              A2,B2,A3,B3,A4,B4,S)
              ;
```

VHDL DESCRIPTION

```
inst:YMUX24H
   port   map(Z1,Z2,Z3,Z4,A1,B1,
              A2,B2,A3,B3,A4,B4,
              S);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z1,Z2,Z3,Z4
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A1,A2,A3	1.03
B1,B2,B3	1.01
A4	1.00
B4,S	0.99

OUTPUT DRIVE (LU)

PIN NAME	Z1,Z4	Z2,Z3
DRIVE	49.8	49.7

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A1->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0863	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.38	0.54	1.14
0.38	0.32	0.45	0.61	1.22
1.00	0.40	0.53	0.69	1.30
3.00	0.54	0.68	0.83	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
A1->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0352	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.41	0.53	0.98
0.38	0.31	0.44	0.57	1.01
1.00	0.38	0.51	0.64	1.08
3.00	0.52	0.66	0.79	1.24

PATH CONDITION

PATH	CONDITION	FUNCTION
A2->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0862	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.38	0.54	1.14
0.38	0.32	0.45	0.61	1.22
1.00	0.40	0.53	0.69	1.30
3.00	0.54	0.67	0.83	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
A2->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0352	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.41	0.53	0.98
0.38	0.31	0.44	0.57	1.01
1.00	0.38	0.51	0.64	1.08
3.00	0.52	0.66	0.79	1.24

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A3->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0862	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.38	0.54	1.14
0.38	0.32	0.45	0.61	1.22
1.00	0.40	0.53	0.69	1.30
3.00	0.54	0.68	0.83	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
A3->Z3	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0352	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.41	0.53	0.98
0.38	0.32	0.44	0.57	1.01
1.00	0.38	0.51	0.64	1.08
3.00	0.52	0.66	0.79	1.24

PATH CONDITION

PATH	CONDITION	FUNCTION
A4->Z4	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0862	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.38	0.54	1.14
0.38	0.32	0.45	0.61	1.22
1.00	0.40	0.53	0.69	1.30
3.00	0.54	0.67	0.83	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
A4->Z4	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0351	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.41	0.53	0.98
0.38	0.31	0.44	0.57	1.01
1.00	0.38	0.51	0.64	1.08
3.00	0.52	0.66	0.79	1.24

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B1->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0863	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.23	0.37	0.52	1.13
0.38	0.31	0.44	0.60	1.21
1.00	0.39	0.52	0.68	1.29
3.00	0.54	0.67	0.83	1.44

PATH CONDITION

PATH	CONDITION	FUNCTION
B1->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0352	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.40	0.53	0.97
0.38	0.31	0.44	0.56	1.00
1.00	0.38	0.51	0.63	1.07
3.00	0.53	0.66	0.80	1.24

PATH CONDITION

PATH	CONDITION	FUNCTION
B2->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0862	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.37	0.53	1.14
0.38	0.32	0.45	0.61	1.21
1.00	0.40	0.53	0.69	1.30
3.00	0.54	0.68	0.84	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
B2->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0352	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.41	0.53	0.97
0.38	0.31	0.44	0.56	1.00
1.00	0.38	0.51	0.64	1.08
3.00	0.53	0.67	0.80	1.25

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B3->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0862	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.37	0.53	1.13
0.38	0.31	0.45	0.60	1.21
1.00	0.40	0.53	0.69	1.29
3.00	0.54	0.68	0.84	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
B3->Z3	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0352	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.41	0.53	0.97
0.38	0.32	0.44	0.57	1.01
1.00	0.38	0.51	0.64	1.08
3.00	0.53	0.67	0.80	1.25

PATH CONDITION

PATH	CONDITION	FUNCTION
B4->Z4	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0862	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.37	0.53	1.13
0.38	0.31	0.45	0.60	1.21
1.00	0.39	0.53	0.68	1.29
3.00	0.54	0.68	0.83	1.45

PATH CONDITION

PATH	CONDITION	FUNCTION
B4->Z4	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0351	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.28	0.40	0.53	0.96
0.38	0.31	0.44	0.56	1.00
1.00	0.38	0.51	0.63	1.07
3.00	0.53	0.66	0.79	1.24

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z1	A1&~B1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0863	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.66	0.82	1.43
0.38	0.55	0.69	0.84	1.45
1.00	0.63	0.77	0.92	1.53
3.00	0.83	0.97	1.13	1.74

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z1	A1&~B1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0352	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.53	0.65	1.08
0.38	0.50	0.62	0.74	1.17
1.00	0.61	0.72	0.84	1.28
3.00	0.81	0.92	1.04	1.47

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z1	~A1&B1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0863	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.68	0.84	1.45
0.38	0.64	0.77	0.93	1.53
1.00	0.73	0.87	1.02	1.63
3.00	0.90	1.03	1.19	1.80

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z1	~A1&B1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0352	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.57	0.70	0.82	1.26
0.38	0.60	0.73	0.85	1.29
1.00	0.68	0.80	0.93	1.37
3.00	0.86	0.99	1.11	1.55

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z2	A2&~B2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0862	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.53	0.66	0.82	1.43
0.38	0.56	0.69	0.85	1.46
1.00	0.64	0.77	0.93	1.54
3.00	0.84	0.98	1.13	1.75

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z2	A2&~B2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0352	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.43	0.54	0.66	1.10
0.38	0.51	0.63	0.75	1.18
1.00	0.62	0.74	0.86	1.29
3.00	0.82	0.93	1.05	1.49

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z2	~A2&B2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0862	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.69	0.84	1.45
0.38	0.64	0.77	0.93	1.54
1.00	0.73	0.87	1.03	1.63
3.00	0.90	1.04	1.19	1.80

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z2	~A2&B2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0352	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.56	0.69	0.82	1.26
0.38	0.59	0.72	0.85	1.29
1.00	0.67	0.80	0.92	1.36
3.00	0.86	0.98	1.11	1.55

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z3	A3&~B3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0862	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.66	0.81	1.43
0.38	0.55	0.68	0.84	1.45
1.00	0.63	0.76	0.92	1.53
3.00	0.83	0.97	1.12	1.74

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z3	A3&~B3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0352	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.53	0.65	1.09
0.38	0.51	0.62	0.74	1.17
1.00	0.61	0.73	0.85	1.28
3.00	0.81	0.93	1.05	1.48

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z3	~A3&B3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0862	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.69	0.84	1.45
0.38	0.64	0.77	0.93	1.54
1.00	0.73	0.87	1.03	1.63
3.00	0.90	1.04	1.19	1.80

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z3	~A3&B3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0352	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.57	0.69	0.82	1.26
0.38	0.60	0.72	0.85	1.29
1.00	0.68	0.80	0.93	1.37
3.00	0.86	0.99	1.11	1.55

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z4	A4&~B4	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0862	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.53	0.67	0.82	1.44
0.38	0.56	0.69	0.85	1.46
1.00	0.64	0.77	0.93	1.54
3.00	0.84	0.98	1.14	1.75

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z4	A4&~B4	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0351	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.42	0.54	0.66	1.09
0.38	0.51	0.63	0.74	1.18
1.00	0.62	0.73	0.85	1.28
3.00	0.82	0.93	1.05	1.48

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z4	~A4&B4	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0862	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.68	0.84	1.45
0.38	0.64	0.77	0.93	1.53
1.00	0.73	0.87	1.02	1.63
3.00	0.90	1.03	1.19	1.80

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z4	~A4&B4	FALL

SLEW FACTOR

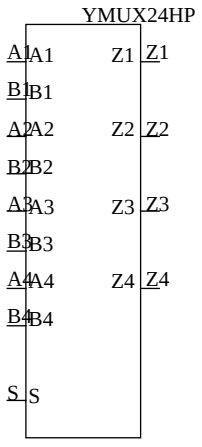
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0351	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.57	0.69	0.82	1.26
0.38	0.60	0.72	0.85	1.29
1.00	0.67	0.80	0.93	1.37
3.00	0.86	0.98	1.11	1.55

YMUX24HP	YMUX24HP	1/9

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YMUX24HP	QUAD 2 TO 1 MULTIPLEXER	13	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
S	A	B	Z
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

Verilog-HDL DESCRIPTION

```
YMUX24HP  inst(Z1,Z2,Z3,Z4,A1,B1,
               A2,B2,A3,B3,A4,B4,
               S);
```

VHDL DESCRIPTION

```
inst:YMUX24HP
   port   map(Z1,Z2,Z3,Z4,A1,B1,
              A2,B2,A3,B3,A4,B4,
              S);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z1,Z2,Z3,Z4
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A1,A2,A3	1.03
B1,B2,B3	1.01
A4	1.00
B4,S	0.99

OUTPUT DRIVE (LU)

PIN NAME	Z1,Z2,Z3,Z4
DRIVE	94.7

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A1->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0434	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.33	0.41	0.73
0.38	0.33	0.40	0.49	0.80
1.00	0.41	0.49	0.57	0.89
3.00	0.57	0.65	0.74	1.06

PATH CONDITION

PATH	CONDITION	FUNCTION
A1->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0204	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.37	0.46	0.73
0.38	0.32	0.41	0.49	0.76
1.00	0.39	0.48	0.56	0.83
3.00	0.55	0.63	0.72	1.00

PATH CONDITION

PATH	CONDITION	FUNCTION
A2->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0434	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.33	0.41	0.73
0.38	0.33	0.40	0.49	0.81
1.00	0.41	0.49	0.57	0.89
3.00	0.57	0.65	0.74	1.06

PATH CONDITION

PATH	CONDITION	FUNCTION
A2->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0204	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.37	0.46	0.73
0.38	0.32	0.41	0.49	0.76
1.00	0.39	0.48	0.56	0.83
3.00	0.55	0.63	0.72	1.00

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A3->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0434	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.33	0.41	0.73
0.38	0.33	0.40	0.49	0.80
1.00	0.41	0.49	0.57	0.89
3.00	0.57	0.65	0.74	1.06

PATH CONDITION

PATH	CONDITION	FUNCTION
A3->Z3	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0204	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.37	0.46	0.73
0.38	0.32	0.41	0.49	0.76
1.00	0.39	0.48	0.56	0.83
3.00	0.55	0.63	0.72	1.00

PATH CONDITION

PATH	CONDITION	FUNCTION
A4->Z4	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0434	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.25	0.33	0.41	0.73
0.38	0.33	0.40	0.49	0.81
1.00	0.41	0.49	0.57	0.89
3.00	0.57	0.65	0.74	1.06

PATH CONDITION

PATH	CONDITION	FUNCTION
A4->Z4	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0204	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.37	0.46	0.73
0.38	0.32	0.41	0.49	0.76
1.00	0.39	0.48	0.56	0.83
3.00	0.55	0.63	0.72	1.00

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B1->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0434	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.31	0.40	0.71
0.38	0.31	0.39	0.47	0.79
1.00	0.40	0.48	0.56	0.88
3.00	0.57	0.65	0.73	1.05

PATH CONDITION

PATH	CONDITION	FUNCTION
B1->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0204	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.37	0.45	0.72
0.38	0.32	0.40	0.48	0.75
1.00	0.39	0.47	0.56	0.82
3.00	0.55	0.64	0.73	1.00

PATH CONDITION

PATH	CONDITION	FUNCTION
B2->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0434	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.31	0.40	0.71
0.38	0.32	0.39	0.48	0.79
1.00	0.41	0.48	0.57	0.88
3.00	0.57	0.65	0.74	1.05

PATH CONDITION

PATH	CONDITION	FUNCTION
B2->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0204	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.37	0.45	0.72
0.38	0.32	0.40	0.48	0.75
1.00	0.39	0.47	0.55	0.82
3.00	0.55	0.64	0.72	1.00

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B3->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0434	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.31	0.40	0.71
0.38	0.31	0.39	0.47	0.79
1.00	0.40	0.48	0.56	0.88
3.00	0.57	0.65	0.73	1.05

PATH CONDITION

PATH	CONDITION	FUNCTION
B3->Z3	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0204	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.37	0.45	0.72
0.38	0.32	0.40	0.48	0.75
1.00	0.39	0.47	0.56	0.82
3.00	0.55	0.64	0.73	1.00

PATH CONDITION

PATH	CONDITION	FUNCTION
B4->Z4	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0434	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.24	0.31	0.40	0.71
0.38	0.32	0.39	0.48	0.79
1.00	0.41	0.48	0.57	0.88
3.00	0.57	0.65	0.74	1.05

PATH CONDITION

PATH	CONDITION	FUNCTION
B4->Z4	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0204	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.29	0.37	0.45	0.71
0.38	0.32	0.40	0.48	0.75
1.00	0.39	0.47	0.55	0.82
3.00	0.55	0.64	0.72	1.00

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z1	A1&~B1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0434	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.63	0.71	1.03
0.38	0.58	0.65	0.74	1.06
1.00	0.66	0.73	0.82	1.14
3.00	0.86	0.94	1.02	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z1	A1&~B1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0204	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.54	0.61	0.87
0.38	0.54	0.62	0.70	0.96
1.00	0.65	0.73	0.81	1.07
3.00	0.85	0.93	1.01	1.27

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z1	~A1&B1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0434	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.57	0.64	0.72	1.04
0.38	0.65	0.73	0.81	1.12
1.00	0.75	0.82	0.91	1.22
3.00	0.92	1.00	1.08	1.39

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z1	~A1&B1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0204	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.57	0.66	0.74	1.01
0.38	0.60	0.69	0.77	1.04
1.00	0.68	0.77	0.85	1.12
3.00	0.87	0.95	1.04	1.31

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z2	A2&~B2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0434	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.56	0.63	0.72	1.04
0.38	0.59	0.66	0.75	1.07
1.00	0.67	0.74	0.83	1.15
3.00	0.87	0.95	1.03	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z2	A2&~B2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0204	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.47	0.55	0.62	0.88
0.38	0.55	0.63	0.71	0.97
1.00	0.66	0.74	0.82	1.08
3.00	0.86	0.94	1.01	1.27

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z2	~A2&B2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0434	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.57	0.64	0.72	1.04
0.38	0.65	0.73	0.81	1.12
1.00	0.75	0.83	0.91	1.22
3.00	0.92	1.00	1.08	1.39

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z2	~A2&B2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0204	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.57	0.65	0.74	1.01
0.38	0.60	0.68	0.77	1.04
1.00	0.68	0.76	0.85	1.12
3.00	0.87	0.95	1.03	1.30

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z3	A3&~B3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0434	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.55	0.63	0.71	1.03
0.38	0.58	0.65	0.74	1.06
1.00	0.66	0.73	0.82	1.14
3.00	0.86	0.94	1.02	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z3	A3&~B3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0204	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.54	0.61	0.87
0.38	0.54	0.62	0.70	0.96
1.00	0.65	0.73	0.81	1.07
3.00	0.85	0.93	1.01	1.27

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z3	~A3&B3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0434	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.57	0.64	0.72	1.04
0.38	0.65	0.73	0.81	1.12
1.00	0.75	0.82	0.91	1.22
3.00	0.92	1.00	1.08	1.39

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z3	~A3&B3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0204	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.57	0.66	0.74	1.01
0.38	0.60	0.69	0.77	1.04
1.00	0.68	0.77	0.85	1.12
3.00	0.87	0.95	1.04	1.31

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z4	A4&~B4	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0434	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.56	0.63	0.72	1.04
0.38	0.59	0.66	0.75	1.07
1.00	0.67	0.74	0.83	1.15
3.00	0.87	0.95	1.03	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z4	A4&~B4	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0204	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.47	0.54	0.62	0.88
0.38	0.55	0.63	0.71	0.97
1.00	0.66	0.74	0.82	1.08
3.00	0.86	0.94	1.01	1.27

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z4	~A4&B4	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0434	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.57	0.64	0.72	1.04
0.38	0.65	0.73	0.81	1.12
1.00	0.75	0.83	0.91	1.22
3.00	0.92	1.00	1.08	1.39

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z4	~A4&B4	FALL

SLEW FACTOR

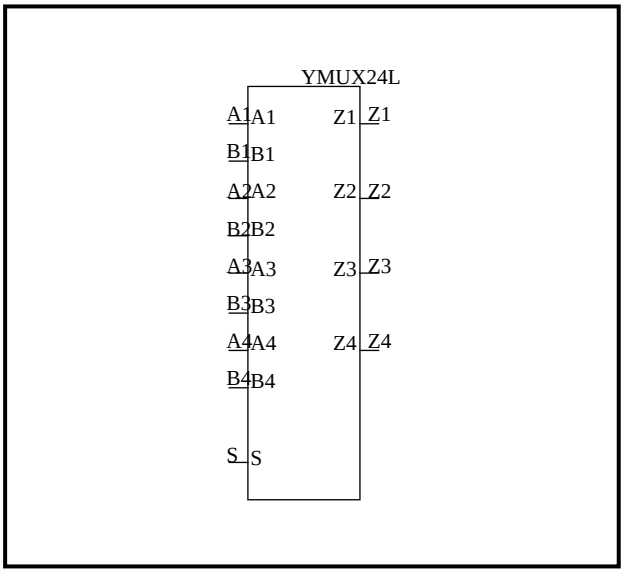
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0204	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.57	0.65	0.74	1.01
0.38	0.60	0.68	0.77	1.04
1.00	0.68	0.76	0.85	1.12
3.00	0.87	0.95	1.03	1.30

YMUX24L	YMUX24L	1/9

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YMUX24L	QUAD 2 TO 1 MULTIPLEXER (INVERTED OUTPUT)	7	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
S	A	B	Z
L	L	X	H
L	H	X	L
H	X	L	H
H	X	H	L

Verilog-HDL DESCRIPTION

```
YMUX24L  inst(Z1,Z2,Z3,Z4,A1,B1,
              A2,B2,A3,B3,A4,B4,S)
              ;
```

VHDL DESCRIPTION

```
inst:YMUX24L
   port   map(Z1,Z2,Z3,Z4,A1,B1,
              A2,B2,A3,B3,A4,B4,
              S);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z1,Z2,Z3,Z4
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A1,A2,B4	3.34
B1,B2,A3	3.35
B3	3.36
A4	3.33
S	0.99

OUTPUT DRIVE (LU)

PIN NAME	Z1,Z3	Z2,Z4
DRIVE	44.2	45.2

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A1->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0887	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.26	0.41	1.02
0.38	0.14	0.27	0.43	1.04
1.00	0.18	0.32	0.49	1.10
3.00	0.25	0.44	0.64	1.30

PATH CONDITION

PATH	CONDITION	FUNCTION
A1->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0363	0.06

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.20	0.31	0.74
0.38	0.15	0.26	0.38	0.81
1.00	0.18	0.34	0.49	0.95
3.00	0.23	0.47	0.68	1.30

PATH CONDITION

PATH	CONDITION	FUNCTION
A2->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0865	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.25	0.41	1.01
0.38	0.14	0.27	0.42	1.03
1.00	0.18	0.32	0.48	1.08
3.00	0.25	0.44	0.64	1.29

PATH CONDITION

PATH	CONDITION	FUNCTION
A2->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0353	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.20	0.31	0.72
0.38	0.15	0.26	0.38	0.80
1.00	0.18	0.34	0.49	0.94
3.00	0.23	0.47	0.68	1.30

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A3->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0887	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.26	0.41	1.02
0.38	0.14	0.27	0.43	1.04
1.00	0.18	0.32	0.49	1.10
3.00	0.25	0.44	0.64	1.30

PATH CONDITION

PATH	CONDITION	FUNCTION
A3->Z3	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0363	0.06

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.20	0.31	0.74
0.38	0.15	0.26	0.38	0.81
1.00	0.18	0.34	0.49	0.95
3.00	0.23	0.47	0.68	1.30

PATH CONDITION

PATH	CONDITION	FUNCTION
A4->Z4	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0865	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.25	0.40	1.01
0.38	0.14	0.27	0.42	1.03
1.00	0.18	0.32	0.48	1.08
3.00	0.25	0.44	0.64	1.29

PATH CONDITION

PATH	CONDITION	FUNCTION
A4->Z4	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0353	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.20	0.31	0.72
0.38	0.15	0.26	0.38	0.80
1.00	0.18	0.34	0.49	0.94
3.00	0.23	0.47	0.68	1.29

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B1->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0887	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.26	0.41	1.03
0.38	0.15	0.28	0.43	1.04
1.00	0.18	0.33	0.49	1.10
3.00	0.25	0.44	0.64	1.30

PATH CONDITION

PATH	CONDITION	FUNCTION
B1->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0363	0.06

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.20	0.31	0.74
0.38	0.15	0.26	0.38	0.81
1.00	0.18	0.34	0.49	0.95
3.00	0.23	0.47	0.68	1.31

PATH CONDITION

PATH	CONDITION	FUNCTION
B2->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0865	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.26	0.41	1.01
0.38	0.15	0.27	0.43	1.03
1.00	0.18	0.32	0.48	1.09
3.00	0.25	0.44	0.64	1.29

PATH CONDITION

PATH	CONDITION	FUNCTION
B2->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0353	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.20	0.31	0.72
0.38	0.15	0.26	0.38	0.80
1.00	0.19	0.34	0.49	0.94
3.00	0.23	0.47	0.68	1.30

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B3->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0887	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.26	0.41	1.03
0.38	0.15	0.28	0.43	1.04
1.00	0.18	0.33	0.49	1.10
3.00	0.25	0.44	0.64	1.30

PATH CONDITION

PATH	CONDITION	FUNCTION
B3->Z3	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0363	0.06

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.20	0.31	0.74
0.38	0.15	0.27	0.38	0.81
1.00	0.19	0.34	0.49	0.95
3.00	0.23	0.47	0.68	1.31

PATH CONDITION

PATH	CONDITION	FUNCTION
B4->Z4	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0865	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.13	0.26	0.41	1.01
0.38	0.15	0.27	0.42	1.03
1.00	0.18	0.32	0.48	1.09
3.00	0.25	0.44	0.64	1.29

PATH CONDITION

PATH	CONDITION	FUNCTION
B4->Z4	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0353	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.20	0.31	0.72
0.38	0.15	0.26	0.38	0.80
1.00	0.19	0.34	0.49	0.94
3.00	0.23	0.47	0.68	1.30

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z1	A1&~B1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0887	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.64	0.80	1.41
0.38	0.60	0.73	0.89	1.50
1.00	0.70	0.83	0.98	1.60
3.00	0.86	0.99	1.15	1.76

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z1	A1&~B1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0363	0.06

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.62	0.73	1.15
0.38	0.54	0.65	0.76	1.18
1.00	0.62	0.73	0.84	1.26
3.00	0.80	0.90	1.01	1.44

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z1	~A1&B1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0887	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.58	0.74	1.36
0.38	0.48	0.61	0.77	1.38
1.00	0.56	0.69	0.85	1.47
3.00	0.76	0.89	1.05	1.67

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z1	~A1&B1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0363	0.06

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.44	0.55	0.97
0.38	0.43	0.53	0.64	1.06
1.00	0.54	0.64	0.75	1.17
3.00	0.74	0.84	0.95	1.38

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z2	A2&~B2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0865	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.64	0.79	1.40
0.38	0.60	0.73	0.88	1.48
1.00	0.69	0.82	0.98	1.58
3.00	0.86	0.99	1.14	1.75

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z2	A2&~B2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0353	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.61	0.72	1.14
0.38	0.54	0.64	0.75	1.17
1.00	0.62	0.72	0.83	1.25
3.00	0.80	0.90	1.01	1.42

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z2	~A2&B2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0865	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.59	0.74	1.35
0.38	0.49	0.62	0.77	1.38
1.00	0.57	0.70	0.85	1.46
3.00	0.77	0.90	1.05	1.66

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z2	~A2&B2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0353	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.44	0.55	0.97
0.38	0.43	0.53	0.64	1.05
1.00	0.55	0.64	0.75	1.17
3.00	0.75	0.84	0.95	1.37

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z3	A3&~B3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0887	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.64	0.80	1.41
0.38	0.60	0.73	0.89	1.50
1.00	0.70	0.83	0.98	1.60
3.00	0.86	0.99	1.15	1.76

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z3	A3&~B3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0363	0.06

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.62	0.73	1.16
0.38	0.55	0.65	0.76	1.19
1.00	0.62	0.73	0.84	1.26
3.00	0.80	0.90	1.01	1.44

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z3	~A3&B3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0887	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.45	0.58	0.74	1.36
0.38	0.48	0.61	0.77	1.38
1.00	0.56	0.70	0.85	1.47
3.00	0.76	0.90	1.05	1.67

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z3	~A3&B3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0363	0.06

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.34	0.44	0.55	0.97
0.38	0.43	0.53	0.64	1.06
1.00	0.54	0.64	0.75	1.17
3.00	0.74	0.84	0.95	1.38

YMUX24L | YMUX24L | 9/9

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z4	A4&~B4	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0865	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.64	0.79	1.40
0.38	0.60	0.73	0.88	1.48
1.00	0.69	0.82	0.97	1.58
3.00	0.86	0.99	1.14	1.75

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z4	A4&~B4	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0353	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.61	0.72	1.14
0.38	0.54	0.64	0.75	1.17
1.00	0.62	0.72	0.83	1.25
3.00	0.80	0.90	1.01	1.42

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z4	~A4&B4	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0865	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.59	0.74	1.35
0.38	0.49	0.62	0.77	1.38
1.00	0.57	0.70	0.85	1.46
3.00	0.77	0.90	1.05	1.66

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z4	~A4&B4	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0353	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.35	0.44	0.55	0.97
0.38	0.43	0.53	0.64	1.05
1.00	0.54	0.64	0.75	1.16
3.00	0.75	0.84	0.95	1.37

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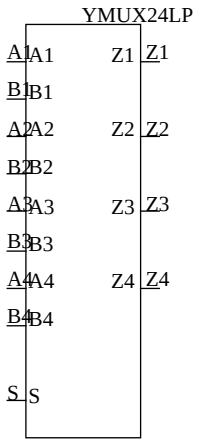
YMUX24LP	YMUX24LP	1/9

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
YMUX24LP	QUAD 2 TO 1 MULTIPLEXER (INVERTED OUTPUT)	9	0	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
S	A	B	Z
L	L	X	H
L	H	X	L
H	X	L	H
H	X	H	L

Verilog-HDL DESCRIPTION

```
YMUX24LP  inst(Z1,Z2,Z3,Z4,A1,B1,
               A2,B2,A3,B3,A4,B4,
               S);
```

VHDL DESCRIPTION

```
inst:YMUX24LP
  port  map(Z1,Z2,Z3,Z4,A1,B1,
            A2,B2,A3,B3,A4,B4,
            S);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z1,Z2,Z3,Z4
ELECTRO MIGRATION DRIVE	12880.0

INPUT LOAD (LU)

PIN NAME	LOAD
A1,A2,A3,A4	4.30
B1,B2,B3,B4	4.31
S	0.99

OUTPUT DRIVE (LU)

PIN NAME	Z1,Z2,Z3,Z4
DRIVE	84.1

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A1->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0437	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.18	0.26	0.57
0.38	0.13	0.20	0.28	0.58
1.00	0.15	0.24	0.32	0.64
3.00	0.21	0.32	0.43	0.80

PATH CONDITION

PATH	CONDITION	FUNCTION
A1->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0188	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.16	0.22	0.46
0.38	0.13	0.21	0.28	0.52
1.00	0.15	0.25	0.35	0.63
3.00	0.17	0.32	0.47	0.87

PATH CONDITION

PATH	CONDITION	FUNCTION
A2->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0437	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.18	0.26	0.57
0.38	0.13	0.20	0.28	0.58
1.00	0.15	0.24	0.32	0.64
3.00	0.21	0.32	0.43	0.80

PATH CONDITION

PATH	CONDITION	FUNCTION
A2->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0188	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.16	0.22	0.45
0.38	0.13	0.21	0.28	0.52
1.00	0.15	0.25	0.35	0.63
3.00	0.17	0.32	0.47	0.87

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
A3->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0437	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.18	0.26	0.57
0.38	0.13	0.20	0.28	0.58
1.00	0.15	0.24	0.32	0.64
3.00	0.21	0.32	0.43	0.80

PATH CONDITION

PATH	CONDITION	FUNCTION
A3->Z3	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0188	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.16	0.22	0.46
0.38	0.13	0.21	0.28	0.52
1.00	0.15	0.25	0.35	0.63
3.00	0.17	0.32	0.47	0.87

PATH CONDITION

PATH	CONDITION	FUNCTION
A4->Z4	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0437	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.18	0.26	0.57
0.38	0.13	0.20	0.28	0.58
1.00	0.15	0.24	0.32	0.64
3.00	0.21	0.32	0.43	0.80

PATH CONDITION

PATH	CONDITION	FUNCTION
A4->Z4	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0188	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.16	0.22	0.45
0.38	0.13	0.21	0.28	0.52
1.00	0.15	0.25	0.35	0.63
3.00	0.17	0.32	0.47	0.87

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B1->Z1	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0437	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.19	0.27	0.57
0.38	0.13	0.20	0.28	0.59
1.00	0.16	0.24	0.33	0.64
3.00	0.21	0.32	0.43	0.80

PATH CONDITION

PATH	CONDITION	FUNCTION
B1->Z1	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0188	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.16	0.22	0.45
0.38	0.13	0.21	0.28	0.52
1.00	0.16	0.26	0.35	0.64
3.00	0.18	0.33	0.47	0.87

PATH CONDITION

PATH	CONDITION	FUNCTION
B2->Z2	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0437	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.19	0.27	0.57
0.38	0.13	0.20	0.28	0.59
1.00	0.16	0.24	0.33	0.64
3.00	0.21	0.32	0.43	0.80

PATH CONDITION

PATH	CONDITION	FUNCTION
B2->Z2	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0188	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.16	0.22	0.45
0.38	0.13	0.21	0.28	0.52
1.00	0.16	0.26	0.35	0.64
3.00	0.18	0.33	0.47	0.87

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
B3->Z3	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0437	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.19	0.27	0.57
0.38	0.13	0.20	0.28	0.59
1.00	0.16	0.24	0.33	0.64
3.00	0.21	0.32	0.43	0.80

PATH CONDITION

PATH	CONDITION	FUNCTION
B3->Z3	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0188	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.16	0.22	0.45
0.38	0.13	0.21	0.28	0.52
1.00	0.16	0.26	0.35	0.64
3.00	0.18	0.33	0.47	0.87

PATH CONDITION

PATH	CONDITION	FUNCTION
B4->Z4	---	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0437	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.12	0.19	0.27	0.57
0.38	0.13	0.20	0.28	0.59
1.00	0.16	0.24	0.33	0.64
3.00	0.21	0.32	0.43	0.80

PATH CONDITION

PATH	CONDITION	FUNCTION
B4->Z4	---	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0188	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.16	0.22	0.45
0.38	0.13	0.21	0.28	0.52
1.00	0.16	0.26	0.35	0.64
3.00	0.18	0.33	0.47	0.87

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z1	A1&~B1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0437	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.59	0.66	0.97
0.38	0.60	0.67	0.75	1.06
1.00	0.70	0.77	0.85	1.16
3.00	0.87	0.94	1.02	1.33

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z1	A1&~B1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0188	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.58	0.65	0.88
0.38	0.54	0.61	0.68	0.91
1.00	0.62	0.69	0.76	0.99
3.00	0.80	0.87	0.94	1.17

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z1	~A1&B1	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0437	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.53	0.61	0.92
0.38	0.49	0.56	0.64	0.94
1.00	0.57	0.64	0.72	1.02
3.00	0.78	0.84	0.92	1.23

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z1	~A1&B1	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z1	0.0188	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.42	0.48	0.72
0.38	0.44	0.51	0.57	0.80
1.00	0.56	0.62	0.68	0.92
3.00	0.76	0.82	0.89	1.12

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z2	A2&~B2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0437	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.58	0.66	0.97
0.38	0.60	0.67	0.75	1.06
1.00	0.70	0.77	0.85	1.15
3.00	0.87	0.94	1.02	1.32

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z2	A2&~B2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0188	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.58	0.64	0.88
0.38	0.54	0.61	0.67	0.91
1.00	0.62	0.69	0.75	0.99
3.00	0.80	0.87	0.93	1.17

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z2	~A2&B2	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0437	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.47	0.53	0.61	0.92
0.38	0.49	0.56	0.64	0.95
1.00	0.58	0.64	0.72	1.03
3.00	0.78	0.85	0.93	1.24

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z2	~A2&B2	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z2	0.0188	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.42	0.49	0.72
0.38	0.45	0.51	0.58	0.81
1.00	0.56	0.62	0.69	0.92
3.00	0.77	0.83	0.90	1.13

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z3	A3&~B3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0437	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.59	0.66	0.97
0.38	0.60	0.67	0.75	1.06
1.00	0.70	0.77	0.85	1.16
3.00	0.87	0.94	1.02	1.33

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z3	A3&~B3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0188	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.58	0.65	0.88
0.38	0.54	0.61	0.68	0.91
1.00	0.62	0.69	0.76	0.99
3.00	0.80	0.87	0.94	1.17

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z3	~A3&B3	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0437	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.46	0.53	0.61	0.92
0.38	0.49	0.56	0.64	0.94
1.00	0.57	0.64	0.72	1.02
3.00	0.78	0.84	0.92	1.23

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z3	~A3&B3	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z3	0.0188	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.42	0.48	0.72
0.38	0.44	0.51	0.57	0.80
1.00	0.56	0.62	0.68	0.92
3.00	0.76	0.82	0.89	1.12

YMUX24LP | YMUX24LP | 9/9

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z4	A4&~B4	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0437	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.52	0.58	0.66	0.97
0.38	0.60	0.67	0.75	1.06
1.00	0.70	0.77	0.85	1.15
3.00	0.87	0.94	1.02	1.32

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z4	A4&~B4	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0188	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.51	0.58	0.64	0.88
0.38	0.54	0.61	0.67	0.91
1.00	0.62	0.69	0.75	0.99
3.00	0.80	0.87	0.93	1.17

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z4	~A4&B4	RISE

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0437	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.47	0.53	0.61	0.92
0.38	0.49	0.56	0.64	0.95
1.00	0.58	0.64	0.72	1.03
3.00	0.78	0.85	0.93	1.24

PATH CONDITION

PATH	CONDITION	FUNCTION
S->Z4	~A4&B4	FALL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z4	0.0188	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.36	0.42	0.49	0.72
0.38	0.45	0.51	0.58	0.81
1.00	0.56	0.62	0.69	0.92
3.00	0.77	0.83	0.90	1.13

Rev.1.01.10

Chapter 3

I/O Macrocells

Alphanumeric Index

I/O Macrocell Data Sheets

ver. 1.10.5

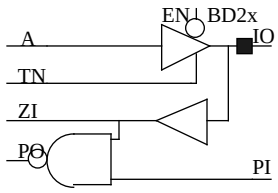
BD2x	BD2x	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BD2x	BIDIRECTIONAL OUTPUT BUFFER (LOW ENABLE) 2mA	4	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

		no resistor	PULL-DOWN	PULL-UP
CMOS LEVEL		BD2C	BD2CD	BD2CU
	INVERT	BD2CN	BD2CND	BD2CNU
LVTTL LEVEL		BD2TH	BD2THD	BD2THU
	INVERT	BD2TN	BD2TND	BD2TNU
HIGH-SPEED CMOS LEVEL	INVERT	BD2CNH	BD2CNHD	BD2CNHU
HIGH-SPEED LVTTL LEVEL	INVERT	BD2TNH	BD2TNHD	BD2TNHU
CMOS SCHMITT TRIGGER		BD2SC	BD2SCD	BD2SCU
LVTTL SCHMITT TRIGGER		BD2ST	BD2STD	BD2STU

LOGIC SYMBOL



TRUTH TABLE (OUTPUT BUFFER)

INPUT			OUTPUT
EN	A	TN	IO
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Note : IO is input when EN=H or TN=L

Verilog-HDL DESCRIPTION

```
BD2x  inst(IO,ZI,PO,A,EN,TN,PI);
```

VHDL DESCRIPTION

```
inst:BD2x
   port   map(IO,ZI,PO,A,EN,TN,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	ZI	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	6.31
EN	0.98
TN	1.00
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	ZI	PO
DRIVE	312.6	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0115	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.22	0.29	0.36	0.53
0.38	0.28	0.35	0.42	0.59
1.00	0.35	0.42	0.49	0.66
3.00	0.48	0.56	0.63	0.81

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0080	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.23	0.32	0.41	0.61
0.38	0.28	0.37	0.45	0.65
1.00	0.35	0.44	0.53	0.73
3.00	0.51	0.61	0.69	0.90

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0002	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	1.63	2.09	2.98	4.71
0.38	1.71	2.18	3.06	4.79
1.00	1.87	2.34	3.23	4.96
3.00	2.38	2.85	3.75	5.48

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0003	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	1.84	2.53	3.89	6.58
0.38	1.84	2.53	3.88	6.58
1.00	1.88	2.57	3.92	6.62
3.00	2.05	2.74	4.10	6.79

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0003	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	0.83	0.83	0.83	0.83
0.38	0.92	0.92	0.92	0.92
1.00	1.02	1.02	1.02	1.02
3.00	1.17	1.17	1.17	1.17

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0002	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	0.40	0.40	0.40	0.40
0.38	0.49	0.49	0.49	0.49
1.00	0.59	0.59	0.59	0.59
3.00	0.74	0.74	0.74	0.74

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0002	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	2.14	2.62	3.51	5.24
0.38	2.15	2.63	3.52	5.25
1.00	2.23	2.70	3.60	5.33
3.00	2.50	2.97	3.87	5.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0003	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	2.43	3.11	4.47	7.16
0.38	2.44	3.13	4.48	7.17
1.00	2.51	3.20	4.56	7.25
3.00	2.78	3.47	4.82	7.52

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0003	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	0.97	0.97	0.97	0.97
0.38	1.00	1.00	1.00	1.00
1.00	1.05	1.05	1.05	1.05
3.00	1.18	1.18	1.18	1.18

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0002	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	0.53	0.53	0.53	0.53
0.38	0.56	0.56	0.56	0.56
1.00	0.62	0.62	0.62	0.62
3.00	0.74	0.74	0.74	0.74

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0002	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	2.21	2.69	3.58	5.31
0.38	2.26	2.74	3.63	5.37
1.00	2.30	2.78	3.67	5.41
3.00	2.37	2.85	3.74	5.48

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0003	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	2.50	3.18	4.54	7.23
0.38	2.55	3.24	4.59	7.29
1.00	2.59	3.28	4.63	7.33
3.00	2.66	3.35	4.70	7.39

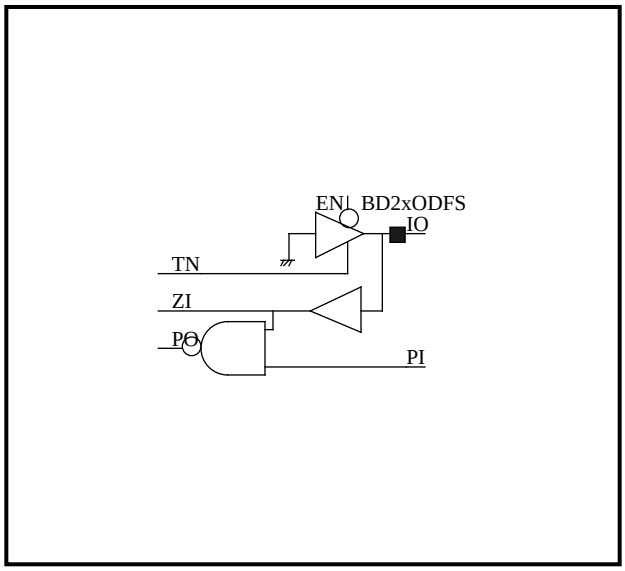
BD2xODFS	BD2xODFS	1/4

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BD2xODFS	BIDIRECTIONAL OUTPUT BUFFER (LOW ENABLE) 2mA OPEN DRAIN with FAILSAFE	4	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

CMOS LEVEL		BD2CODFS
	INVERT	BD2CNODFS
LVTTL LEVEL		BD2THODFS
	INVERT	BD2TNODFS
HIGH-SPEED CMOS LEVEL	INVERT	BD2CNHODFS
HIGH-SPEED LVTTL LEVEL	INVERT	BD2TNHODFS
CMOS SCHMITT TRIGGER		BD2SCODFS
LVTTL SCHMITT TRIGGER		BD2STODFS

LOGIC SYMBOL



TRUTH TABLE (OUTPUT BUFFER)

INPUT		OUTPUT
EN	TN	IO
L	H	L
H	X	Hz
X	L	Hz

Note : IO is input when EN=H or TN=L

Verilog-HDL DESCRIPTION

```
BD2xODFS  inst(IO,ZI,PO,EN,TN,PI);
```

VHDL DESCRIPTION

```
inst:BD2xODFS
   port   map(IO,ZI,PO,EN,TN,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	ZI	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
EN	0.98
TN	1.00
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	ZI	PO
DRIVE	312.6	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0115	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.22	0.29	0.36	0.53
0.38	0.28	0.35	0.42	0.59
1.00	0.35	0.42	0.49	0.66
3.00	0.48	0.56	0.63	0.81

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0080	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.23	0.32	0.41	0.61
0.38	0.28	0.37	0.45	0.65
1.00	0.35	0.44	0.53	0.73
3.00	0.51	0.61	0.69	0.90

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	0.34	0.34	0.34	0.34
0.38	0.43	0.43	0.43	0.43
1.00	0.52	0.52	0.52	0.52
3.00	0.64	0.64	0.64	0.64

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0098	0.63

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	2.11	2.81	4.17	6.86
0.38	2.13	2.82	4.18	6.87
1.00	2.21	2.90	4.26	6.95
3.00	2.46	3.16	4.51	7.21

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	0.47	0.47	0.47	0.47
0.38	0.50	0.50	0.50	0.50
1.00	0.56	0.56	0.56	0.56
3.00	0.68	0.68	0.68	0.68

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0098	0.63

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	2.18	2.88	4.24	6.93
0.38	2.24	2.93	4.29	6.98
1.00	2.28	2.97	4.33	7.02
3.00	2.35	3.04	4.40	7.09

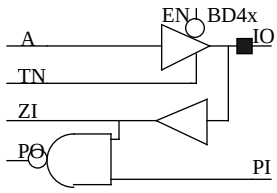
BD4x	BD4x	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BD4x	BIDIRECTIONAL OUTPUT BUFFER (LOW ENABLE) 4mA	4	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

		no resistor	PULL-DOWN	PULL-UP
CMOS LEVEL		BD4C	BD4CD	BD4CU
	INVERT	BD4CN	BD4CND	BD4CNU
LVTTL LEVEL		BD4TH	BD4THD	BD4THU
	INVERT	BD4TN	BD4TND	BD4TNU
HIGH-SPEED CMOS LEVEL	INVERT	BD4CNH	BD4CNHD	BD4CNHU
HIGH-SPEED LVTTL LEVEL	INVERT	BD4TNH	BD4TNHD	BD4TNHU
CMOS SCHMITT TRIGGER		BD4SC	BD4SCD	BD4SCU
LVTTL SCHMITT TRIGGER		BD4ST	BD4STD	BD4STU

LOGIC SYMBOL



TRUTH TABLE (OUTPUT BUFFER)

INPUT			OUTPUT
EN	A	TN	IO
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Note : IO is input when EN=H or TN=L

Verilog-HDL DESCRIPTION

```
BD4x  inst(IO,ZI,PO,A,EN,TN,PI);
```

VHDL DESCRIPTION

```
inst:BD4x
   port   map(IO,ZI,PO,A,EN,TN,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	ZI	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	6.31
EN	0.98
TN	1.00
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	ZI	PO
DRIVE	312.6	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0115	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.22	0.29	0.36	0.53
0.38	0.28	0.35	0.42	0.59
1.00	0.35	0.42	0.49	0.66
3.00	0.48	0.56	0.63	0.81

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0080	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.23	0.32	0.41	0.61
0.38	0.28	0.37	0.45	0.65
1.00	0.35	0.44	0.53	0.73
3.00	0.51	0.61	0.69	0.90

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0001	0.83

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.85	3.00	4.61	6.70
0.38	1.93	3.08	4.69	6.78
1.00	2.09	3.24	4.85	6.95
3.00	2.63	3.78	5.39	7.48

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0050	0.65

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.79	3.21	5.30	8.06
0.38	1.78	3.21	5.29	8.06
1.00	1.82	3.25	5.33	8.09
3.00	1.99	3.42	5.50	8.27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0050	0.65

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.07	1.07	1.07	1.07
0.38	1.16	1.16	1.16	1.16
1.00	1.26	1.26	1.26	1.26
3.00	1.40	1.40	1.40	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0001	0.83

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.41	0.41	0.41	0.41
0.38	0.50	0.50	0.50	0.50
1.00	0.60	0.60	0.60	0.60
3.00	0.75	0.75	0.75	0.75

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0001	0.83

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.38	3.54	5.15	7.25
0.38	2.39	3.55	5.16	7.26
1.00	2.47	3.63	5.24	7.34
3.00	2.74	3.90	5.51	7.61

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0050	0.65

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.37	3.80	5.88	8.65
0.38	2.38	3.81	5.90	8.66
1.00	2.46	3.89	5.97	8.74
3.00	2.72	4.15	6.24	9.00

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0050	0.65

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.20	1.20	1.20	1.20
0.38	1.23	1.23	1.23	1.23
1.00	1.29	1.29	1.29	1.29
3.00	1.41	1.41	1.41	1.41

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0001	0.83

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.54	0.54	0.54	0.54
0.38	0.58	0.58	0.58	0.58
1.00	0.63	0.63	0.63	0.63
3.00	0.76	0.76	0.76	0.76

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0001	0.83

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.45	3.61	5.22	7.32
0.38	2.51	3.67	5.28	7.38
1.00	2.55	3.71	5.32	7.42
3.00	2.62	3.78	5.38	7.48

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0050	0.65

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.44	3.87	5.96	8.72
0.38	2.49	3.92	6.01	8.77
1.00	2.53	3.96	6.05	8.81
3.00	2.60	4.03	6.12	8.88

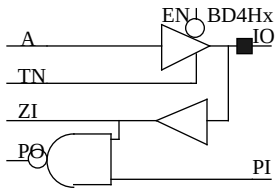
BD4Hx	BD4Hx	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BD4Hx	BIDIRECTIONAL OUTPUT BUFFER (LOW ENABLE) 4mA HIGH-SPEED	4	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

		no resistor	PULL-DOWN	PULL-UP
CMOS LEVEL		BD4HC	BD4HCD	BD4HCU
	INVERT	BD4HCN	BD4HCND	BD4HCNU
LVTTL LEVEL		BD4HTH	BD4HTHD	BD4HTHU
	INVERT	BD4HTN	BD4HTND	BD4HTNU
HIGH-SPEED CMOS LEVEL	INVERT	BD4HCNH	BD4HCNHD	BD4HCNHU
HIGH-SPEED LVTTL LEVEL	INVERT	BD4HTNH	BD4HTNHD	BD4HTNHU
CMOS SCHMITT TRIGGER		BD4HSC	BD4HSCD	BD4HSCU
LVTTL SCHMITT TRIGGER		BD4HST	BD4HSTD	BD4HSTU

LOGIC SYMBOL



TRUTH TABLE (OUTPUT BUFFER)

INPUT			OUTPUT
EN	A	TN	IO
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Note : IO is input when EN=H or TN=L

Verilog-HDL DESCRIPTION

```
BD4Hx  inst(IO,ZI,PO,A,EN,TN,PI);
```

VHDL DESCRIPTION

```
inst:BD4Hx
   port   map(IO,ZI,PO,A,EN,TN,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	ZI	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	9.03
EN	0.98
TN	1.00
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	ZI	PO
DRIVE	312.6	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0115	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.22	0.29	0.36	0.53
0.38	0.28	0.35	0.42	0.59
1.00	0.35	0.42	0.49	0.66
3.00	0.48	0.56	0.63	0.81

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0080	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.23	0.32	0.41	0.61
0.38	0.28	0.37	0.45	0.65
1.00	0.35	0.44	0.53	0.73
3.00	0.51	0.61	0.69	0.90

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0047	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.10	2.15	3.71	5.79
0.38	1.19	2.24	3.80	5.88
1.00	1.32	2.37	3.93	6.01
3.00	1.62	2.67	4.23	6.31

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0050	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.43	2.82	4.89	7.65
0.38	1.44	2.83	4.90	7.65
1.00	1.45	2.84	4.91	7.66
3.00	1.52	2.89	4.95	7.71

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0050	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.97	0.97	0.97	0.97
0.38	1.06	1.06	1.06	1.06
1.00	1.17	1.17	1.17	1.17
3.00	1.34	1.34	1.34	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0047	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.52	0.52	0.52	0.52
0.38	0.61	0.61	0.61	0.61
1.00	0.71	0.71	0.71	0.71
3.00	0.87	0.87	0.87	0.87

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0047	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.67	2.73	4.29	6.37
0.38	1.68	2.74	4.30	6.38
1.00	1.76	2.81	4.38	6.46
3.00	2.03	3.09	4.65	6.73

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0050	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.07	3.46	5.53	8.29
0.38	2.08	3.47	5.54	8.30
1.00	2.15	3.55	5.62	8.38
3.00	2.42	3.81	5.89	8.65

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0050	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.10	1.10	1.10	1.10
0.38	1.14	1.14	1.14	1.14
1.00	1.19	1.19	1.19	1.19
3.00	1.32	1.32	1.32	1.32

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0047	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.65	0.65	0.65	0.65
0.38	0.68	0.68	0.68	0.68
1.00	0.74	0.74	0.74	0.74
3.00	0.86	0.86	0.86	0.86

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0047	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.74	2.80	4.36	6.44
0.38	1.80	2.85	4.41	6.49
1.00	1.83	2.89	4.45	6.53
3.00	1.90	2.96	4.52	6.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0050	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.14	3.53	5.60	8.36
0.38	2.19	3.58	5.66	8.41
1.00	2.23	3.62	5.69	8.45
3.00	2.30	3.69	5.76	8.52

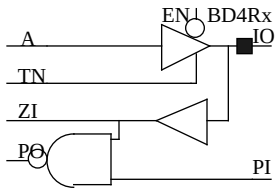
BD4Rx	BD4Rx	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BD4Rx	BIDIRECTIONAL OUTPUT BUFFER (LOW ENABLE) 4mA SLEW RATE CONTROL	4	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

		no resistor	PULL-DOWN	PULL-UP
CMOS LEVEL		BD4RC	BD4RCD	BD4RCU
	INVERT	BD4RCN	BD4RCND	BD4RCNU
LVTTL LEVEL		BD4RTH	BD4RTHD	BD4RTHU
	INVERT	BD4RTN	BD4RTND	BD4RTNU
HIGH-SPEED CMOS LEVEL	INVERT	BD4RCNH	BD4RCNHD	BD4RCNHU
HIGH-SPEED LVTTL LEVEL	INVERT	BD4RTNH	BD4RTNHD	BD4RTNHU
CMOS SCHMITT TRIGGER		BD4RSC	BD4RSCD	BD4RSCU
LVTTL SCHMITT TRIGGER		BD4RST	BD4RSTD	BD4RSTU

LOGIC SYMBOL



TRUTH TABLE (OUTPUT BUFFER)

INPUT			OUTPUT
EN	A	TN	IO
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Note : IO is input when EN=H or TN=L

Verilog-HDL DESCRIPTION

```
BD4Rx  inst(IO,ZI,PO,A,EN,TN,PI);
```

VHDL DESCRIPTION

```
inst:BD4Rx
   port   map(IO,ZI,PO,A,EN,TN,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	ZI	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	7.58
EN	0.98
TN	1.00
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	ZI	PO
DRIVE	312.6	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0115	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.22	0.29	0.36	0.53
0.38	0.28	0.35	0.42	0.59
1.00	0.35	0.42	0.49	0.66
3.00	0.48	0.56	0.63	0.81

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0080	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.23	0.32	0.41	0.61
0.38	0.28	0.37	0.45	0.65
1.00	0.35	0.44	0.53	0.73
3.00	0.51	0.61	0.69	0.90

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0058	1.47

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.52	4.10	6.26	8.90
0.38	2.61	4.20	6.36	9.00
1.00	2.79	4.37	6.53	9.18
3.00	3.39	4.98	7.14	9.79

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0066	1.71

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	3.43	5.68	8.75	12.52
0.38	3.48	5.73	8.80	12.57
1.00	3.62	5.87	8.94	12.71
3.00	4.08	6.33	9.40	13.17

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0066	1.71

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.82	0.82	0.82	0.82
0.38	0.91	0.91	0.91	0.91
1.00	1.01	1.01	1.01	1.01
3.00	1.17	1.17	1.17	1.17

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0058	1.47

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.51	0.51	0.51	0.51
0.38	0.60	0.60	0.60	0.60
1.00	0.69	0.69	0.69	0.69
3.00	0.84	0.84	0.84	0.84

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0058	1.47

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	3.18	4.78	6.95	9.60
0.38	3.19	4.79	6.96	9.61
1.00	3.27	4.87	7.04	9.68
3.00	3.55	5.15	7.32	9.97

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0066	1.71

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	4.26	6.51	9.58	13.35
0.38	4.27	6.53	9.59	13.37
1.00	4.35	6.60	9.67	13.44
3.00	4.61	6.86	9.93	13.70

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0066	1.71

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.95	0.95	0.95	0.95
0.38	0.99	0.99	0.99	0.99
1.00	1.04	1.04	1.04	1.04
3.00	1.18	1.18	1.18	1.18

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0058	1.47

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.64	0.64	0.64	0.64
0.38	0.67	0.67	0.67	0.67
1.00	0.73	0.73	0.73	0.73
3.00	0.85	0.85	0.85	0.85

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0058	1.47

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	3.25	4.85	7.02	9.67
0.38	3.31	4.90	7.07	9.72
1.00	3.35	4.94	7.11	9.76
3.00	3.42	5.01	7.18	9.83

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0066	1.71

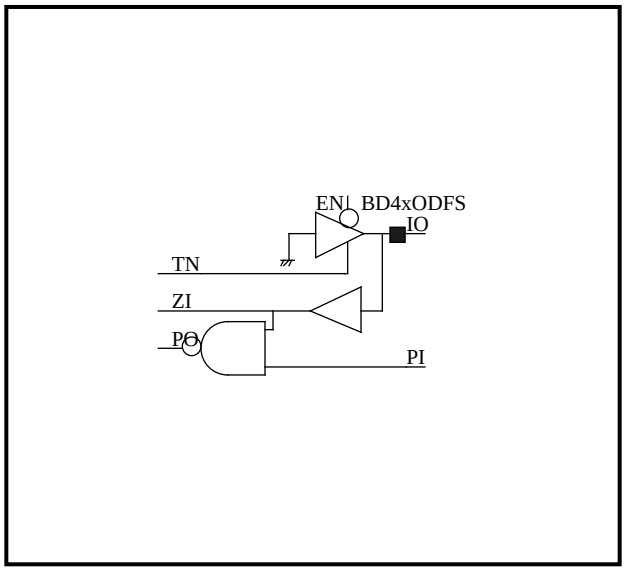
PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	4.33	6.58	9.65	13.42
0.38	4.39	6.64	9.71	13.48
1.00	4.43	6.68	9.75	13.52
3.00	4.49	6.75	9.81	13.59

BD4xODFS			BD4xODFS	1/4
CELL NAME	FUNCTION	CELL COUNT		CONDITION
BD4xODFS	BIDIRECTIONAL OUTPUT BUFFER (LOW ENABLE) 4mA OPEN DRAIN with FAILSAFE	GATE	I/O	VDD=3.3V, Ta=25°C, Typ.
		4	1	

CELL NAME

CMOS LEVEL		BD4CODFS
	INVERT	BD4CNODFS
LVTTL LEVEL		BD4THODFS
	INVERT	BD4TNODFS
HIGH-SPEED CMOS LEVEL	INVERT	BD4CNHODFS
HIGH-SPEED LVTTL LEVEL	INVERT	BD4TNHODFS
CMOS SCHMITT TRIGGER		BD4SCODFS
LVTTL SCHMITT TRIGGER		BD4STODFS

LOGIC SYMBOL



TRUTH TABLE (OUTPUT BUFFER)

INPUT		OUTPUT
EN	TN	IO
L	H	L
H	X	Hz
X	L	Hz

Note : IO is input when EN=H or TN=L

Verilog-HDL DESCRIPTION

```
BD4xODFS  inst(IO,ZI,PO,EN,TN,PI);
```

VHDL DESCRIPTION

```
inst:BD4xODFS
   port   map(IO,ZI,PO,EN,TN,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	ZI	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
EN	0.98
TN	1.00
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	ZI	PO
DRIVE	312.6	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0115	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.22	0.29	0.36	0.53
0.38	0.28	0.35	0.42	0.59
1.00	0.35	0.42	0.49	0.66
3.00	0.48	0.56	0.63	0.81

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0080	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.23	0.32	0.41	0.61
0.38	0.28	0.37	0.45	0.65
1.00	0.35	0.44	0.53	0.73
3.00	0.51	0.61	0.69	0.90

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.35	0.35	0.35	0.35
0.38	0.44	0.44	0.44	0.44
1.00	0.53	0.53	0.53	0.53
3.00	0.66	0.66	0.66	0.66

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0050	0.48

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.16	3.59	5.68	8.44
0.38	2.17	3.61	5.69	8.46
1.00	2.25	3.69	5.77	8.54
3.00	2.50	3.94	6.03	8.79

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.48	0.48	0.48	0.48
0.38	0.52	0.52	0.52	0.52
1.00	0.57	0.57	0.57	0.57
3.00	0.69	0.69	0.69	0.69

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0050	0.48

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.23	3.66	5.75	8.51
0.38	2.28	3.72	5.80	8.57
1.00	2.32	3.76	5.84	8.61
3.00	2.39	3.83	5.91	8.67

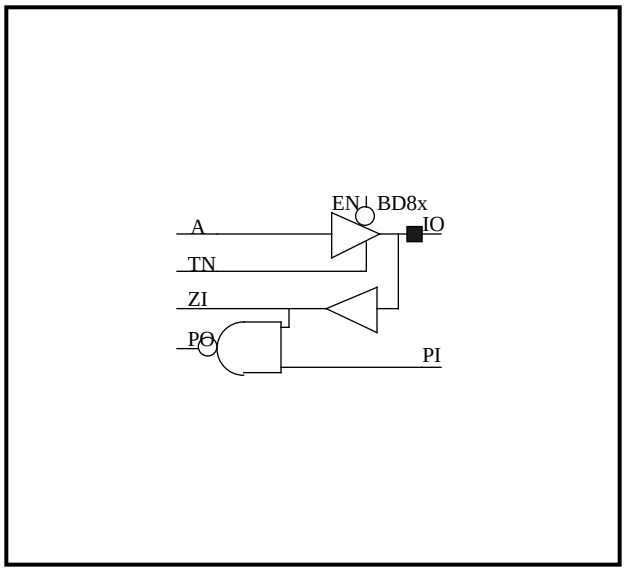
BD8x	BD8x	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BD8x	BIDIRECTIONAL OUTPUT BUFFER (LOW ENABLE) 8mA	4	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

		no resistor	PULL-DOWN	PULL-UP
CMOS LEVEL		BD8C	BD8CD	BD8CU
	INVERT	BD8CN	BD8CND	BD8CNU
LVTTL LEVEL		BD8TH	BD8THD	BD8THU
	INVERT	BD8TN	BD8TND	BD8TNU
HIGH-SPEED CMOS LEVEL	INVERT	BD8CNH	BD8CNHD	BD8CNHU
HIGH-SPEED LVTTL LEVEL	INVERT	BD8TNH	BD8TNHD	BD8TNHU
CMOS SCHMITT TRIGGER		BD8SC	BD8SCD	BD8SCU
LVTTL SCHMITT TRIGGER		BD8ST	BD8STD	BD8STU

LOGIC SYMBOL



TRUTH TABLE (OUTPUT BUFFER)

INPUT			OUTPUT
EN	A	TN	IO
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Note : IO is input when EN=H or TN=L

Verilog-HDL DESCRIPTION

```
BD8x  inst(IO,ZI,PO,A,EN,TN,PI);
```

VHDL DESCRIPTION

```
inst:BD8x
   port   map(IO,ZI,PO,A,EN,TN,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	ZI	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	6.31
EN	0.98
TN	1.00
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	ZI	PO
DRIVE	312.6	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0115	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.22	0.29	0.36	0.53
0.38	0.28	0.35	0.42	0.59
1.00	0.35	0.42	0.49	0.66
3.00	0.48	0.56	0.63	0.81

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0080	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.23	0.32	0.41	0.61
0.38	0.28	0.37	0.45	0.65
1.00	0.35	0.44	0.53	0.73
3.00	0.51	0.61	0.69	0.90

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0023	1.03

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.93	2.69	3.62	4.76
0.38	2.01	2.77	3.71	4.84
1.00	2.17	2.93	3.86	5.00
3.00	2.71	3.48	4.41	5.55

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0025	0.61

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.57	2.36	3.44	4.85
0.38	1.58	2.36	3.44	4.85
1.00	1.61	2.39	3.47	4.88
3.00	1.79	2.56	3.64	5.05

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0025	0.61

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.67	1.67	1.67	1.67
0.38	1.75	1.75	1.75	1.75
1.00	1.85	1.85	1.85	1.85
3.00	2.00	2.00	2.00	2.00

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0023	1.03

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.44	0.44	0.44	0.44
0.38	0.53	0.53	0.53	0.53
1.00	0.63	0.63	0.63	0.63
3.00	0.78	0.78	0.78	0.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0023	1.03

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.46	3.24	4.18	5.32
0.38	2.47	3.25	4.19	5.33
1.00	2.55	3.33	4.27	5.40
3.00	2.81	3.59	4.53	5.67

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0025	0.61

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.10	2.92	4.02	5.43
0.38	2.11	2.93	4.03	5.44
1.00	2.19	3.01	4.11	5.52
3.00	2.45	3.27	4.37	5.78

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0025	0.61

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.80	1.80	1.80	1.80
0.38	1.83	1.83	1.83	1.83
1.00	1.89	1.89	1.89	1.89
3.00	2.01	2.01	2.01	2.01

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0023	1.03

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.57	0.57	0.57	0.57
0.38	0.60	0.60	0.60	0.60
1.00	0.66	0.66	0.66	0.66
3.00	0.78	0.78	0.78	0.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0023	1.03

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.53	3.31	4.25	5.39
0.38	2.58	3.36	4.30	5.44
1.00	2.62	3.40	4.34	5.48
3.00	2.69	3.47	4.41	5.55

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0025	0.61

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.17	2.99	4.09	5.50
0.38	2.23	3.04	4.14	5.55
1.00	2.27	3.08	4.18	5.59
3.00	2.33	3.15	4.25	5.66

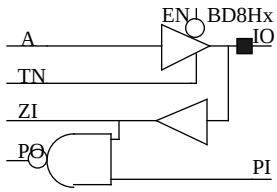
BD8Hx	BD8Hx	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BD8Hx	BIDIRECTIONAL OUTPUT BUFFER (LOW ENABLE) 8mA HIGH-SPEED	4	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

		no resistor	PULL-DOWN	PULL-UP
CMOS LEVEL		BD8HC	BD8HCD	BD8HCU
	INVERT	BD8HCN	BD8HCND	BD8HCNU
LVTTL LEVEL		BD8HTH	BD8HTHD	BD8HTHU
	INVERT	BD8HTN	BD8HTND	BD8HTNU
HIGH-SPEED CMOS LEVEL	INVERT	BD8HCNH	BD8HCNHD	BD8HCNHU
HIGH-SPEED LVTTL LEVEL	INVERT	BD8HTNH	BD8HTNHD	BD8HTNHU
CMOS SCHMITT TRIGGER		BD8HSC	BD8HSCD	BD8HSCU
LVTTL SCHMITT TRIGGER		BD8HST	BD8HSTD	BD8HSTU

LOGIC SYMBOL



TRUTH TABLE (OUTPUT BUFFER)

INPUT			OUTPUT
EN	A	TN	IO
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Note : IO is input when EN=H or TN=L

Verilog-HDL DESCRIPTION

```
BD8Hx  inst(IO,ZI,PO,A,EN,TN,PI);
```

VHDL DESCRIPTION

```
inst:BD8Hx
   port   map(IO,ZI,PO,A,EN,TN,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	ZI	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	9.03
EN	0.98
TN	1.00
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	ZI	PO
DRIVE	312.6	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0115	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.22	0.29	0.36	0.53
0.38	0.28	0.35	0.42	0.59
1.00	0.35	0.42	0.49	0.66
3.00	0.48	0.56	0.63	0.81

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0080	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.23	0.32	0.41	0.61
0.38	0.28	0.37	0.45	0.65
1.00	0.35	0.44	0.53	0.73
3.00	0.51	0.61	0.69	0.90

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0024	0.42

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.93	1.50	2.31	3.36
0.38	1.02	1.59	2.39	3.44
1.00	1.17	1.74	2.54	3.59
3.00	1.53	2.10	2.90	3.95

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0025	0.39

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.12	1.83	2.86	4.24
0.38	1.13	1.84	2.87	4.25
1.00	1.16	1.85	2.88	4.26
3.00	1.27	1.95	2.96	4.33

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0025	0.39

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.44	1.44	1.44	1.44
0.38	1.53	1.53	1.53	1.53
1.00	1.64	1.64	1.64	1.64
3.00	1.81	1.81	1.81	1.81

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0024	0.42

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.55	0.55	0.55	0.55
0.38	0.64	0.64	0.64	0.64
1.00	0.74	0.74	0.74	0.74
3.00	0.90	0.90	0.90	0.90

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0024	0.42

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.51	2.10	2.90	3.95
0.38	1.52	2.11	2.91	3.97
1.00	1.60	2.18	2.99	4.04
3.00	1.87	2.46	3.27	4.32

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0025	0.39

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.70	2.43	3.48	4.87
0.38	1.71	2.44	3.50	4.88
1.00	1.79	2.52	3.57	4.96
3.00	2.06	2.79	3.84	5.22

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0025	0.39

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.58	1.58	1.58	1.58
0.38	1.61	1.61	1.61	1.61
1.00	1.66	1.66	1.66	1.66
3.00	1.79	1.79	1.79	1.79

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0024	0.42

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.68	0.68	0.68	0.68
0.38	0.71	0.71	0.71	0.71
1.00	0.77	0.77	0.77	0.77
3.00	0.89	0.89	0.89	0.89

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0024	0.42

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.58	2.17	2.97	4.03
0.38	1.64	2.22	3.03	4.08
1.00	1.68	2.26	3.07	4.12
3.00	1.74	2.33	3.14	4.19

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0025	0.39

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.77	2.50	3.56	4.94
0.38	1.83	2.56	3.61	4.99
1.00	1.86	2.60	3.65	5.03
3.00	1.93	2.67	3.72	5.10

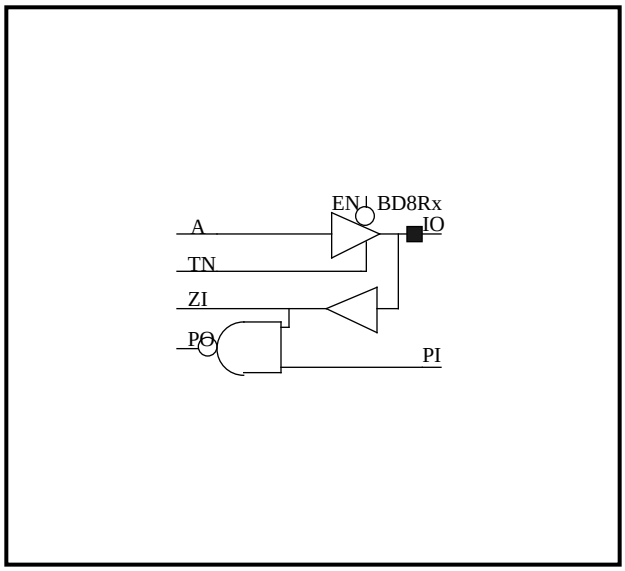
BD8Rx	BD8Rx	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BD8Rx	BIDIRECTIONAL OUTPUT BUFFER (LOW ENABLE) 8mA SLEW RATE CONTROL	4	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

		no resistor	PULL-DOWN	PULL-UP
CMOS LEVEL		BD8RC	BD8RCD	BD8RCU
	INVERT	BD8RCN	BD8RCND	BD8RCNU
LVTTL LEVEL		BD8RTH	BD8RTHD	BD8RTHU
	INVERT	BD8RTN	BD8RTND	BD8RTNU
HIGH-SPEED CMOS LEVEL	INVERT	BD8RCNH	BD8RCNHD	BD8RCNHU
HIGH-SPEED LVTTL LEVEL	INVERT	BD8RTNH	BD8RTNHD	BD8RTNHU
CMOS SCHMITT TRIGGER		BD8RSC	BD8RSCD	BD8RSCU
LVTTL SCHMITT TRIGGER		BD8RST	BD8RSTD	BD8RSTU

LOGIC SYMBOL



TRUTH TABLE (OUTPUT BUFFER)

INPUT			OUTPUT
EN	A	TN	IO
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Note : IO is input when EN=H or TN=L

Verilog-HDL DESCRIPTION

```
BD8Rx  inst(IO,ZI,PO,A,EN,TN,PI);
```

VHDL DESCRIPTION

```
inst:BD8Rx
   port   map(IO,ZI,PO,A,EN,TN,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	ZI	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	7.58
EN	0.98
TN	1.00
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	ZI	PO
DRIVE	312.6	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0115	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.22	0.29	0.36	0.53
0.38	0.28	0.35	0.42	0.59
1.00	0.35	0.42	0.49	0.66
3.00	0.48	0.56	0.63	0.81

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0080	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.23	0.32	0.41	0.61
0.38	0.28	0.37	0.45	0.65
1.00	0.35	0.44	0.53	0.73
3.00	0.51	0.61	0.69	0.90

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0032	1.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.56	3.57	4.84	6.40
0.38	2.66	3.67	4.95	6.51
1.00	2.84	3.85	5.12	6.68
3.00	3.43	4.45	5.72	7.28

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0035	1.46

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	3.24	4.63	6.40	8.57
0.38	3.28	4.68	6.44	8.62
1.00	3.41	4.80	6.57	8.74
3.00	3.85	5.24	7.01	9.18

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0035	1.46

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.19	1.19	1.19	1.19
0.38	1.28	1.28	1.28	1.28
1.00	1.39	1.39	1.39	1.39
3.00	1.55	1.55	1.55	1.55

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0032	1.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.54	0.54	0.54	0.54
0.38	0.63	0.63	0.63	0.63
1.00	0.73	0.73	0.73	0.73
3.00	0.87	0.87	0.87	0.87

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0032	1.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	3.23	4.26	5.54	7.11
0.38	3.25	4.27	5.56	7.12
1.00	3.32	4.35	5.63	7.20
3.00	3.61	4.63	5.92	7.48

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0035	1.46

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	4.05	5.44	7.20	9.38
0.38	4.06	5.45	7.22	9.39
1.00	4.14	5.53	7.29	9.47
3.00	4.40	5.79	7.56	9.73

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0035	1.46

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.32	1.32	1.32	1.32
0.38	1.36	1.36	1.36	1.36
1.00	1.42	1.42	1.42	1.42
3.00	1.56	1.56	1.56	1.56

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0032	1.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.67	0.67	0.67	0.67
0.38	0.71	0.71	0.71	0.71
1.00	0.76	0.76	0.76	0.76
3.00	0.89	0.89	0.89	0.89

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0032	1.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	3.31	4.33	5.61	7.18
0.38	3.36	4.39	5.67	7.23
1.00	3.40	4.43	5.71	7.27
3.00	3.47	4.50	5.78	7.34

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0035	1.46

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	4.12	5.51	7.28	9.45
0.38	4.17	5.56	7.33	9.50
1.00	4.21	5.60	7.37	9.54
3.00	4.28	5.67	7.44	9.61

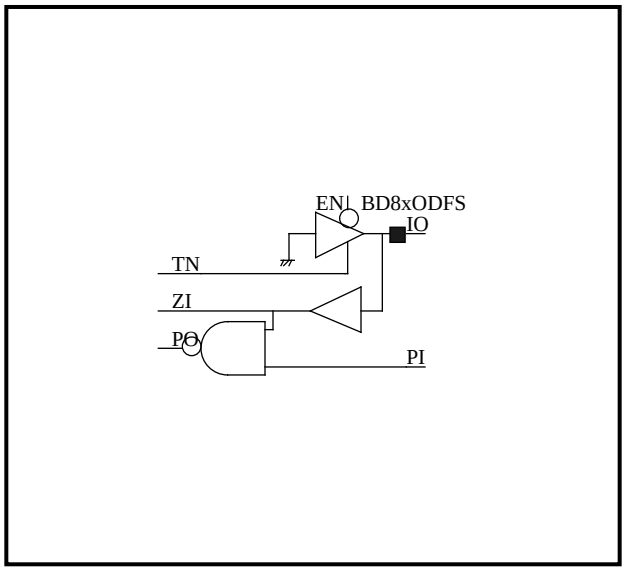
BD8xODFS	BD8xODFS	1/4

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BD8xODFS	BIDIRECTIONAL OUTPUT BUFFER (LOW ENABLE) 8mA OPEN DRAIN with FAILSAFE	4	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

CMOS LEVEL		BD8CODFS
	INVERT	BD8CNODFS
LVTTL LEVEL		BD8THODFS
	INVERT	BD8TNODFS
HIGH-SPEED CMOS LEVEL	INVERT	BD8CNHODFS
HIGH-SPEED LVTTL LEVEL	INVERT	BD8TNHODFS
CMOS SCHMITT TRIGGER		BD8SCODFS
LVTTL SCHMITT TRIGGER		BD8STODFS

LOGIC SYMBOL



TRUTH TABLE (OUTPUT BUFFER)

INPUT		OUTPUT
EN	TN	IO
L	H	L
H	X	Hz
X	L	Hz

Note : IO is input when EN=H or TN=L

Verilog-HDL DESCRIPTION

```
BD8xODFS  inst(IO,ZI,PO,EN,TN,PI);
```

VHDL DESCRIPTION

```
inst:BD8xODFS
   port   map(IO,ZI,PO,EN,TN,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	ZI	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
EN	0.98
TN	1.00
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	ZI	PO
DRIVE	312.6	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0115	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.22	0.29	0.36	0.53
0.38	0.28	0.35	0.42	0.59
1.00	0.35	0.42	0.49	0.66
3.00	0.48	0.56	0.63	0.81

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0080	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.23	0.32	0.41	0.61
0.38	0.28	0.37	0.45	0.65
1.00	0.35	0.44	0.53	0.73
3.00	0.51	0.61	0.69	0.90

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.38	0.38	0.38	0.38
0.38	0.46	0.46	0.46	0.46
1.00	0.55	0.55	0.55	0.55
3.00	0.68	0.68	0.68	0.68

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0024	0.57

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.93	2.76	3.87	5.28
0.38	1.94	2.77	3.88	5.29
1.00	2.02	2.86	3.96	5.37
3.00	2.28	3.11	4.21	5.62

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.51	0.51	0.51	0.51
0.38	0.54	0.54	0.54	0.54
1.00	0.60	0.60	0.60	0.60
3.00	0.72	0.72	0.72	0.72

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0024	0.57

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.00	2.83	3.94	5.35
0.38	2.05	2.89	3.99	5.40
1.00	2.09	2.93	4.03	5.44
3.00	2.16	2.99	4.10	5.51

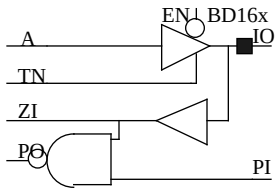
BD16x	BD16x	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BD16x	BIDIRECTIONAL OUTPUT BUFFER (LOW ENABLE) 16mA	4	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

		no resistor	PULL-DOWN	PULL-UP
CMOS LEVEL		BD16C	BD16CD	BD16CU
	INVERT	BD16CN	BD16CND	BD16CNU
LVTTL LEVEL		BD16TH	BD16THD	BD16THU
	INVERT	BD16TN	BD16TND	BD16TNU
HIGH-SPEED CMOS LEVEL	INVERT	BD16CNH	BD16CNHD	BD16CNHU
HIGH-SPEED LVTTL LEVEL	INVERT	BD16TNH	BD16TNHD	BD16TNHU
CMOS SCHMITT TRIGGER		BD16SC	BD16SCD	BD16SCU
LVTTL SCHMITT TRIGGER		BD16ST	BD16STD	BD16STU

LOGIC SYMBOL



TRUTH TABLE (OUTPUT BUFFER)

INPUT			OUTPUT
EN	A	TN	IO
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Note : IO is input when EN=H or TN=L

Verilog-HDL DESCRIPTION

```
BD16x  inst(IO,ZI,PO,A,EN,TN,PI);
```

VHDL DESCRIPTION

```
inst:BD16x
   port   map(IO,ZI,PO,A,EN,TN,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	ZI	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	7.75
EN	0.98
TN	1.00
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	ZI	PO
DRIVE	312.6	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0115	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.22	0.29	0.36	0.53
0.38	0.28	0.35	0.42	0.59
1.00	0.35	0.42	0.49	0.66
3.00	0.48	0.56	0.63	0.81

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0080	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.23	0.32	0.41	0.61
0.38	0.28	0.37	0.45	0.65
1.00	0.35	0.44	0.53	0.73
3.00	0.51	0.61	0.69	0.90

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0011	0.94

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.72	2.44	3.25	3.98
0.38	1.80	2.52	3.33	4.06
1.00	1.95	2.67	3.48	4.21
3.00	2.47	3.20	4.00	4.73

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0012	0.52

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.30	2.01	2.93	3.82
0.38	1.31	2.01	2.93	3.82
1.00	1.35	2.05	2.96	3.85
3.00	1.53	2.22	3.14	4.02

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0012	0.52

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.50	1.50	1.50	1.50
0.38	1.58	1.58	1.58	1.58
1.00	1.68	1.68	1.68	1.68
3.00	1.83	1.83	1.83	1.83

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0011	0.94

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.50	0.50	0.50	0.50
0.38	0.59	0.59	0.59	0.59
1.00	0.69	0.69	0.69	0.69
3.00	0.84	0.84	0.84	0.84

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0011	0.94

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.23	2.97	3.78	4.51
0.38	2.24	2.98	3.79	4.52
1.00	2.32	3.06	3.87	4.60
3.00	2.58	3.33	4.14	4.87

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0012	0.52

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.88	2.63	3.57	4.46
0.38	1.90	2.65	3.58	4.47
1.00	1.97	2.72	3.65	4.55
3.00	2.24	2.99	3.92	4.81

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0012	0.52

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.63	1.63	1.63	1.63
0.38	1.66	1.66	1.66	1.66
1.00	1.72	1.72	1.72	1.72
3.00	1.84	1.84	1.84	1.84

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0011	0.94

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.63	0.63	0.63	0.63
0.38	0.66	0.66	0.66	0.66
1.00	0.72	0.72	0.72	0.72
3.00	0.84	0.84	0.84	0.84

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0011	0.94

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.30	3.04	3.85	4.58
0.38	2.35	3.09	3.90	4.64
1.00	2.39	3.13	3.94	4.68
3.00	2.46	3.20	4.01	4.74

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0012	0.52

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.96	2.71	3.64	4.53
0.38	2.01	2.76	3.69	4.58
1.00	2.05	2.80	3.73	4.62
3.00	2.12	2.87	3.80	4.69

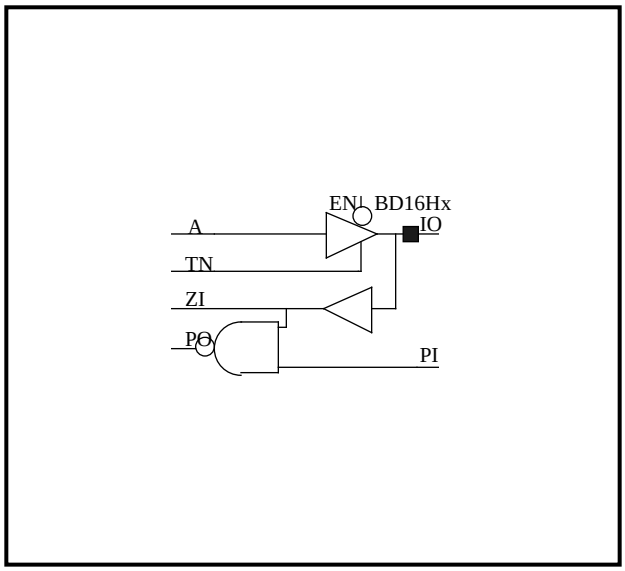
BD16Hx	BD16Hx	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BD16Hx	BIDIRECTIONAL OUTPUT BUFFER (LOW ENABLE) 16mA HIGH-SPEED	4	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

		no resistor	PULL-DOWN	PULL-UP
CMOS LEVEL		BD16HC	BD16HCD	BD16HCU
	INVERT	BD16HCN	BD16HCND	BD16HCNU
LVTTL LEVEL		BD16HTH	BD16HTHD	BD16HTHU
	INVERT	BD16HTN	BD16HTND	BD16HTNU
HIGH-SPEED CMOS LEVEL	INVERT	BD16HCNH	BD16HCNHD	BD16HCNHU
HIGH-SPEED LVTTL LEVEL	INVERT	BD16HTNH	BD16HTNHD	BD16HTNHU
CMOS SCHMITT TRIGGER		BD16HSC	BD16HSCD	BD16HSCU
LVTTL SCHMITT TRIGGER		BD16HST	BD16HSTD	BD16HSTU

LOGIC SYMBOL



TRUTH TABLE (OUTPUT BUFFER)

INPUT			OUTPUT
EN	A	TN	IO
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Note : IO is input when EN=H or TN=L

Verilog-HDL DESCRIPTION

```
BD16Hx  inst(IO,ZI,PO,A,EN,TN,PI);
```

VHDL DESCRIPTION

```
inst:BD16Hx
   port   map(IO,ZI,PO,A,EN,TN,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	ZI	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	10.65
EN	0.98
TN	1.00
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	ZI	PO
DRIVE	312.6	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0115	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.22	0.29	0.36	0.53
0.38	0.28	0.35	0.42	0.59
1.00	0.35	0.42	0.49	0.66
3.00	0.48	0.56	0.63	0.81

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0080	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.23	0.32	0.41	0.61
0.38	0.28	0.37	0.45	0.65
1.00	0.35	0.44	0.53	0.73
3.00	0.51	0.61	0.69	0.90

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0012	0.33

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.78	1.31	1.99	2.65
0.38	0.87	1.39	2.07	2.74
1.00	1.01	1.54	2.22	2.88
3.00	1.36	1.89	2.58	3.24

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0012	0.28

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.90	1.52	2.38	3.23
0.38	0.91	1.52	2.39	3.23
1.00	0.94	1.55	2.40	3.25
3.00	1.06	1.65	2.50	3.35

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0012	0.28

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.33	1.33	1.33	1.33
0.38	1.42	1.42	1.42	1.42
1.00	1.53	1.53	1.53	1.53
3.00	1.73	1.73	1.73	1.73

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0012	0.33

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.66	0.66	0.66	0.66
0.38	0.75	0.75	0.75	0.75
1.00	0.87	0.87	0.87	0.87
3.00	1.06	1.06	1.06	1.06

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0012	0.33

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.43	1.97	2.66	3.32
0.38	1.44	1.98	2.67	3.33
1.00	1.51	2.06	2.74	3.41
3.00	1.79	2.34	3.02	3.69

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0012	0.28

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.66	2.31	3.20	4.07
0.38	1.67	2.32	3.21	4.08
1.00	1.74	2.40	3.28	4.15
3.00	2.02	2.68	3.56	4.43

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0012	0.28

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.46	1.46	1.46	1.46
0.38	1.49	1.49	1.49	1.49
1.00	1.55	1.55	1.55	1.55
3.00	1.67	1.67	1.67	1.67

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0012	0.33

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.79	0.79	0.79	0.79
0.38	0.83	0.83	0.83	0.83
1.00	0.88	0.88	0.88	0.88
3.00	1.01	1.01	1.01	1.01

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0012	0.33

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.50	2.04	2.73	3.39
0.38	1.55	2.10	2.78	3.45
1.00	1.59	2.14	2.82	3.49
3.00	1.66	2.20	2.89	3.55

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0012	0.28

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.73	2.39	3.27	4.14
0.38	1.78	2.44	3.32	4.19
1.00	1.82	2.48	3.36	4.23
3.00	1.89	2.55	3.43	4.30

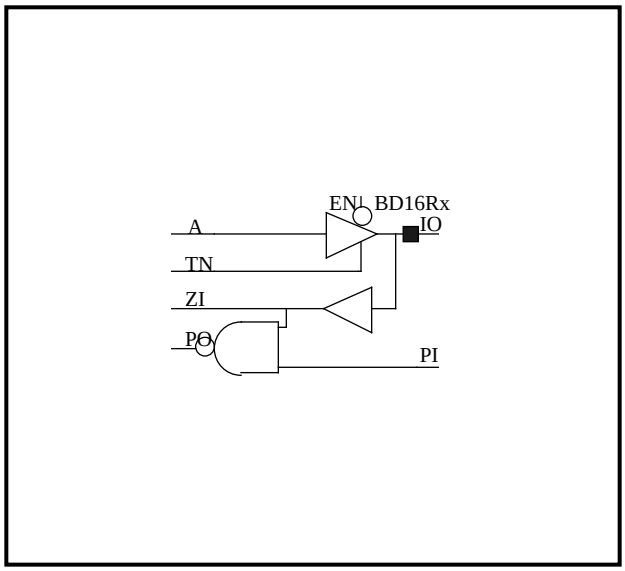
BD16Rx	BD16Rx	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BD16Rx	BIDIRECTIONAL OUTPUT BUFFER (LOW ENABLE) 16mA SLEW RATE CONTROL	4	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

		no resistor	PULL-DOWN	PULL-UP
CMOS LEVEL		BD16RC	BD16RCD	BD16RCU
	INVERT	BD16RCN	BD16RCND	BD16RCNU
LVTTL LEVEL		BD16RTH	BD16RTHD	BD16RTHU
	INVERT	BD16RTN	BD16RTND	BD16RTNU
HIGH-SPEED CMOS LEVEL	INVERT	BD16RCNH	BD16RCNHD	BD16RCNHU
HIGH-SPEED LVTTL LEVEL	INVERT	BD16RTNH	BD16RTNHD	BD16RTNHU
CMOS SCHMITT TRIGGER		BD16RSC	BD16RSCD	BD16RSCU
LVTTL SCHMITT TRIGGER		BD16RST	BD16RSTD	BD16RSTU

LOGIC SYMBOL



TRUTH TABLE (OUTPUT BUFFER)

INPUT			OUTPUT
EN	A	TN	IO
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Note : IO is input when EN=H or TN=L

Verilog-HDL DESCRIPTION

```
BD16Rx  inst(IO,ZI,PO,A,EN,TN,PI);
```

VHDL DESCRIPTION

```
inst:BD16Rx
   port   map(IO,ZI,PO,A,EN,TN,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	ZI	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	8.93
EN	0.98
TN	1.00
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	ZI	PO
DRIVE	312.6	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0115	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.22	0.29	0.36	0.53
0.38	0.28	0.35	0.42	0.59
1.00	0.35	0.42	0.49	0.66
3.00	0.48	0.56	0.63	0.81

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0080	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.23	0.32	0.41	0.61
0.38	0.28	0.37	0.45	0.65
1.00	0.35	0.44	0.53	0.73
3.00	0.51	0.61	0.69	0.90

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0016	1.16

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.25	3.22	4.33	5.34
0.38	2.37	3.34	4.45	5.46
1.00	2.57	3.54	4.65	5.66
3.00	3.24	4.21	5.32	6.32

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0018	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.77	4.02	5.52	6.90
0.38	2.82	4.08	5.57	6.96
1.00	2.93	4.19	5.69	7.07
3.00	3.28	4.55	6.05	7.44

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0018	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.02	2.02	2.02	2.02
0.38	2.12	2.12	2.12	2.12
1.00	2.23	2.23	2.23	2.23
3.00	2.40	2.40	2.40	2.40

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0016	1.16

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.61	0.61	0.61	0.61
0.38	0.70	0.70	0.70	0.70
1.00	0.80	0.80	0.80	0.80
3.00	0.95	0.95	0.95	0.95

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0016	1.16

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.90	3.89	5.01	6.02
0.38	2.91	3.91	5.02	6.03
1.00	2.99	3.98	5.10	6.11
3.00	3.27	4.27	5.38	6.39

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0018	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	3.12	4.40	5.90	7.28
0.38	3.14	4.41	5.91	7.30
1.00	3.21	4.49	5.99	7.37
3.00	3.48	4.75	6.25	7.64

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0018	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.16	2.16	2.16	2.16
0.38	2.20	2.20	2.20	2.20
1.00	2.26	2.26	2.26	2.26
3.00	2.41	2.41	2.41	2.41

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0016	1.16

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.74	0.74	0.74	0.74
0.38	0.77	0.77	0.77	0.77
1.00	0.83	0.83	0.83	0.83
3.00	0.95	0.95	0.95	0.95

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0016	1.16

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.97	3.96	5.08	6.09
0.38	3.02	4.02	5.13	6.14
1.00	3.06	4.06	5.17	6.18
3.00	3.13	4.13	5.24	6.25

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0018	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	3.20	4.47	5.97	7.36
0.38	3.25	4.52	6.02	7.41
1.00	3.29	4.56	6.06	7.45
3.00	3.36	4.63	6.13	7.52

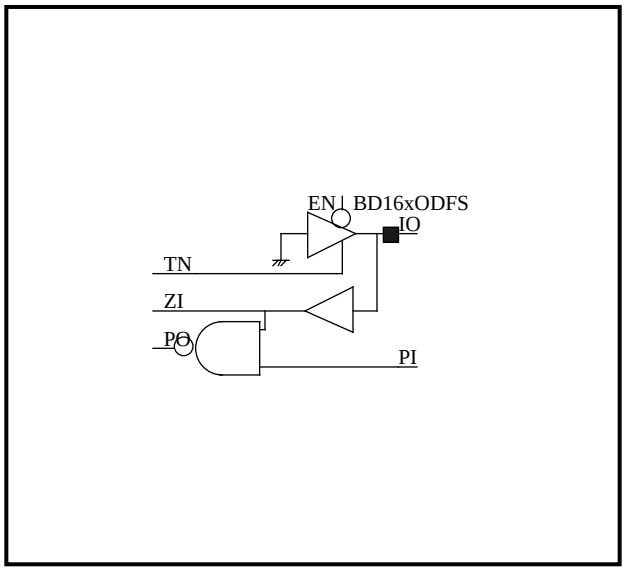
BD16xODFS	BD16xODFS	1/4

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BD16xODFS	BIDIRECTIONAL OUTPUT BUFFER (LOW ENABLE) 16mA OPEN DRAIN with FAILSAFE	4	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

CMOS LEVEL		BD16CODFS
	INVERT	BD16CNODFS
LVTTL LEVEL		BD16THODFS
	INVERT	BD16TNODFS
HIGH-SPEED CMOS LEVEL	INVERT	BD16CNHODFS
HIGH-SPEED LVTTL LEVEL	INVERT	BD16TNHODFS
CMOS SCHMITT TRIGGER		BD16SCODFS
LVTTL SCHMITT TRIGGER		BD16STODFS

LOGIC SYMBOL



TRUTH TABLE (OUTPUT BUFFER)

INPUT		OUTPUT
EN	TN	IO
L	H	L
H	X	Hz
X	L	Hz

Note : IO is input when EN=H or TN=L

Verilog-HDL DESCRIPTION

```
BD16xODFS  inst(IO,ZI,PO,EN,TN,PI);
```

VHDL DESCRIPTION

```
inst:BD16xODFS
   port   map(IO,ZI,PO,EN,TN,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	ZI	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
EN	0.98
TN	1.00
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	ZI	PO
DRIVE	312.6	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0115	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.22	0.29	0.36	0.53
0.38	0.28	0.35	0.42	0.59
1.00	0.35	0.42	0.49	0.66
3.00	0.48	0.56	0.63	0.81

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0080	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.23	0.32	0.41	0.61
0.38	0.28	0.37	0.45	0.65
1.00	0.35	0.44	0.53	0.73
3.00	0.51	0.61	0.69	0.90

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.44	0.44	0.44	0.44
0.38	0.52	0.52	0.52	0.52
1.00	0.61	0.61	0.61	0.61
3.00	0.74	0.74	0.74	0.74

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0012	0.48

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.75	2.51	3.44	4.33
0.38	1.76	2.52	3.45	4.34
1.00	1.84	2.60	3.53	4.42
3.00	2.09	2.85	3.79	4.68

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.57	0.57	0.57	0.57
0.38	0.60	0.60	0.60	0.60
1.00	0.66	0.66	0.66	0.66
3.00	0.78	0.78	0.78	0.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0012	0.48

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.82	2.58	3.51	4.40
0.38	1.87	2.63	3.56	4.46
1.00	1.91	2.67	3.60	4.49
3.00	1.98	2.74	3.67	4.56

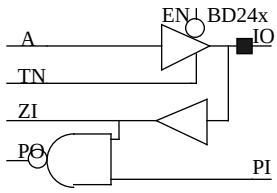
BD24x	BD24x	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BD24x	BIDIRECTIONAL OUTPUT BUFFER (LOW ENABLE) 24mA	4	2	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

		no resistor	PULL-DOWN	PULL-UP
CMOS LEVEL		BD24C	BD24CD	BD24CU
	INVERT	BD24CN	BD24CND	BD24CNU
LVTTL LEVEL		BD24TH	BD24THD	BD24THU
	INVERT	BD24TN	BD24TND	BD24TNU
HIGH-SPEED CMOS LEVEL	INVERT	BD24CNH	BD24CNHD	BD24CNHU
HIGH-SPEED LVTTL LEVEL	INVERT	BD24TNH	BD24TNHD	BD24TNHU
CMOS SCHMITT TRIGGER		BD24SC	BD24SCD	BD24SCU
LVTTL SCHMITT TRIGGER		BD24ST	BD24STD	BD24STU

LOGIC SYMBOL



TRUTH TABLE (OUTPUT BUFFER)

INPUT			OUTPUT
EN	A	TN	IO
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Note : IO is input when EN=H or TN=L

Verilog-HDL DESCRIPTION

```
BD24x  inst(IO,ZI,PO,A,EN,TN,PI);
```

VHDL DESCRIPTION

```
inst:BD24x
   port   map(IO,ZI,PO,A,EN,TN,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	ZI	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	13.11
EN	0.98
TN	1.00
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	ZI	PO
DRIVE	312.6	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0115	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.22	0.29	0.36	0.53
0.38	0.28	0.35	0.42	0.59
1.00	0.35	0.42	0.49	0.66
3.00	0.48	0.56	0.63	0.81

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0080	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.23	0.32	0.41	0.61
0.38	0.28	0.37	0.45	0.65
1.00	0.35	0.44	0.53	0.73
3.00	0.51	0.61	0.69	0.90

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0008	0.88

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.60	2.15	2.75	3.28
0.38	1.68	2.23	2.83	3.36
1.00	1.83	2.39	2.99	3.51
3.00	2.36	2.92	3.52	4.04

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0008	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.23	1.73	2.37	2.97
0.38	1.24	1.73	2.36	2.97
1.00	1.28	1.77	2.40	3.00
3.00	1.46	1.94	2.57	3.17

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0008	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.66	1.66	1.66	1.66
0.38	1.75	1.75	1.75	1.75
1.00	1.87	1.87	1.87	1.87
3.00	2.09	2.09	2.09	2.09

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0008	0.88

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.68	0.68	0.68	0.68
0.38	0.77	0.77	0.77	0.77
1.00	0.89	0.89	0.89	0.89
3.00	1.11	1.11	1.11	1.11

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0008	0.88

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.38	2.96	3.57	4.10
0.38	2.39	2.97	3.58	4.11
1.00	2.46	3.04	3.65	4.18
3.00	2.74	3.32	3.93	4.46

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0008	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.12	2.67	3.32	3.93
0.38	2.14	2.68	3.34	3.95
1.00	2.20	2.75	3.41	4.02
3.00	2.48	3.03	3.69	4.30

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0008	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.80	1.80	1.80	1.80
0.38	1.83	1.83	1.83	1.83
1.00	1.88	1.88	1.88	1.88
3.00	2.01	2.01	2.01	2.01

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0008	0.88

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.81	0.81	0.81	0.81
0.38	0.84	0.84	0.84	0.84
1.00	0.90	0.90	0.90	0.90
3.00	1.03	1.03	1.03	1.03

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0008	0.88

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.45	3.03	3.64	4.17
0.38	2.51	3.09	3.70	4.23
1.00	2.55	3.13	3.74	4.27
3.00	2.61	3.19	3.80	4.33

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0008	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.20	2.75	3.40	4.01
0.38	2.25	2.80	3.45	4.06
1.00	2.29	2.84	3.49	4.10
3.00	2.36	2.91	3.56	4.17

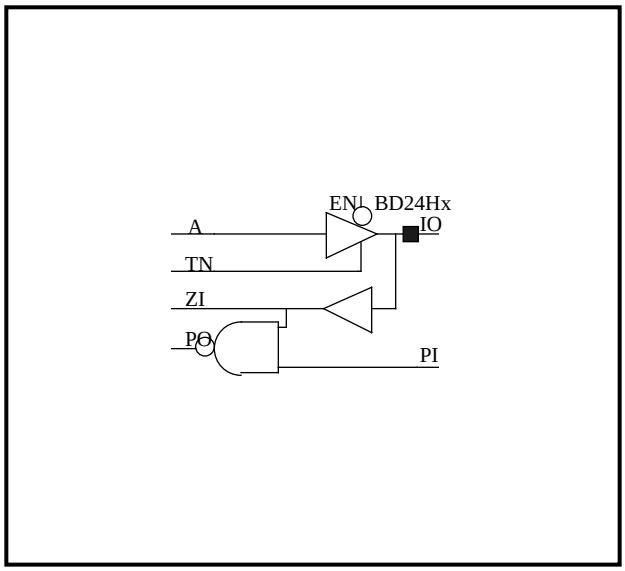
BD24Hx	BD24Hx	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BD24Hx	BIDIRECTIONAL OUTPUT BUFFER (LOW ENABLE) 24mA HIGH-SPEED	4	2	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

		no resistor	PULL-DOWN	PULL-UP
CMOS LEVEL		BD24HC	BD24HCD	BD24HCU
	INVERT	BD24HCN	BD24HCND	BD24HCNU
LVTTL LEVEL		BD24HTH	BD24HTHD	BD24HTHU
	INVERT	BD24HTN	BD24HTND	BD24HTNU
HIGH-SPEED CMOS LEVEL	INVERT	BD24HCNH	BD24HCNHD	BD24HCNHU
HIGH-SPEED LVTTL LEVEL	INVERT	BD24HTNH	BD24HTNHD	BD24HTNHU
CMOS SCHMITT TRIGGER		BD24HSC	BD24HSCD	BD24HSCU
LVTTL SCHMITT TRIGGER		BD24HST	BD24HSTD	BD24HSTU

LOGIC SYMBOL



TRUTH TABLE (OUTPUT BUFFER)

INPUT			OUTPUT
EN	A	TN	IO
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Note : IO is input when EN=H or TN=L

Verilog-HDL DESCRIPTION

```
BD24Hx  inst(IO,ZI,PO,A,EN,TN,PI);
```

VHDL DESCRIPTION

```
inst:BD24Hx
   port   map(IO,ZI,PO,A,EN,TN,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	ZI	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	18.71
EN	0.98
TN	1.00
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	ZI	PO
DRIVE	312.6	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0115	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.22	0.29	0.36	0.53
0.38	0.28	0.35	0.42	0.59
1.00	0.35	0.42	0.49	0.66
3.00	0.48	0.56	0.63	0.81

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0080	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.23	0.32	0.41	0.61
0.38	0.28	0.37	0.45	0.65
1.00	0.35	0.44	0.53	0.73
3.00	0.51	0.61	0.69	0.90

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0008	0.35

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.71	1.08	1.55	2.00
0.38	0.79	1.16	1.63	2.08
1.00	0.94	1.31	1.78	2.23
3.00	1.29	1.67	2.14	2.59

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0008	0.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.85	1.27	1.85	2.42
0.38	0.86	1.27	1.85	2.42
1.00	0.89	1.29	1.87	2.44
3.00	1.02	1.40	1.96	2.52

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0008	0.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.51	1.51	1.51	1.51
0.38	1.60	1.60	1.60	1.60
1.00	1.73	1.73	1.73	1.73
3.00	2.00	2.00	2.00	2.00

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0008	0.35

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.92	0.92	0.92	0.92
0.38	1.01	1.01	1.01	1.01
1.00	1.15	1.15	1.15	1.15
3.00	1.41	1.41	1.41	1.41

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0008	0.35

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.66	2.06	2.54	3.00
0.38	1.68	2.08	2.56	3.01
1.00	1.74	2.14	2.62	3.07
3.00	2.02	2.42	2.90	3.36

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0008	0.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.99	2.45	3.05	3.63
0.38	2.01	2.47	3.06	3.65
1.00	2.07	2.53	3.13	3.71
3.00	2.35	2.81	3.41	3.99

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0008	0.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.64	1.64	1.64	1.64
0.38	1.68	1.68	1.68	1.68
1.00	1.73	1.73	1.73	1.73
3.00	1.86	1.86	1.86	1.86

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0008	0.35

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.06	1.06	1.06	1.06
0.38	1.09	1.09	1.09	1.09
1.00	1.15	1.15	1.15	1.15
3.00	1.27	1.27	1.27	1.27

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0008	0.35

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.74	2.14	2.62	3.07
0.38	1.79	2.19	2.67	3.13
1.00	1.83	2.23	2.71	3.17
3.00	1.90	2.30	2.78	3.23

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0008	0.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.07	2.53	3.13	3.71
0.38	2.12	2.58	3.18	3.76
1.00	2.16	2.62	3.22	3.80
3.00	2.23	2.69	3.29	3.87

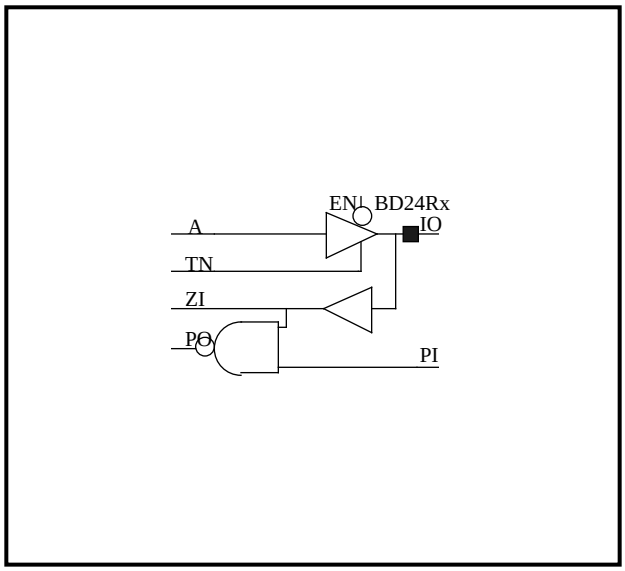
BD24Rx	BD24Rx	1/5

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BD24Rx	BIDIRECTIONAL OUTPUT BUFFER (LOW ENABLE) 24mA SLEW RATE CONTROL	4	2	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

		no resistor	PULL-DOWN	PULL-UP
CMOS LEVEL		BD24RC	BD24RCD	BD24RCU
	INVERT	BD24RCN	BD24RCND	BD24RCNU
LVTTL LEVEL		BD24RTH	BD24RTHD	BD24RTHU
	INVERT	BD24RTN	BD24RTND	BD24RTNU
HIGH-SPEED CMOS LEVEL	INVERT	BD24RCNH	BD24RCNHD	BD24RCNHU
HIGH-SPEED LVTTL LEVEL	INVERT	BD24RTNH	BD24RTNHD	BD24RTNHU
CMOS SCHMITT TRIGGER		BD24RSC	BD24RSCD	BD24RSCU
LVTTL SCHMITT TRIGGER		BD24RST	BD24RSTD	BD24RSTU

LOGIC SYMBOL



TRUTH TABLE (OUTPUT BUFFER)

INPUT			OUTPUT
EN	A	TN	IO
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Note : IO is input when EN=H or TN=L

Verilog-HDL DESCRIPTION

```
BD24Rx  inst(IO,ZI,PO,A,EN,TN,PI);
```

VHDL DESCRIPTION

```
inst:BD24Rx
   port   map(IO,ZI,PO,A,EN,TN,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	ZI	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	15.44
EN	0.98
TN	1.00
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	ZI	PO
DRIVE	312.6	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0115	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.22	0.29	0.36	0.53
0.38	0.28	0.35	0.42	0.59
1.00	0.35	0.42	0.49	0.66
3.00	0.48	0.56	0.63	0.81

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0080	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.23	0.32	0.41	0.61
0.38	0.28	0.37	0.45	0.65
1.00	0.35	0.44	0.53	0.73
3.00	0.51	0.61	0.69	0.90

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0011	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.11	2.84	3.65	4.38
0.38	2.23	2.96	3.77	4.49
1.00	2.42	3.15	3.96	4.68
3.00	3.06	3.79	4.60	5.32

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0012	1.14

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.57	3.52	4.61	5.59
0.38	2.62	3.58	4.66	5.65
1.00	2.74	3.69	4.78	5.76
3.00	3.13	4.09	5.17	6.15

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0012	1.14

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.70	1.70	1.70	1.70
0.38	1.80	1.80	1.80	1.80
1.00	1.93	1.93	1.93	1.93
3.00	2.16	2.16	2.16	2.16

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0011	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.82	0.82	0.82	0.82
0.38	0.91	0.91	0.91	0.91
1.00	1.03	1.03	1.03	1.03
3.00	1.24	1.24	1.24	1.24

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0011	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	3.11	3.87	4.70	5.42
0.38	3.13	3.89	4.71	5.43
1.00	3.19	3.96	4.78	5.50
3.00	3.48	4.24	5.06	5.79

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0012	1.14

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	3.46	4.42	5.50	6.48
0.38	3.48	4.43	5.52	6.50
1.00	3.54	4.50	5.58	6.56
3.00	3.82	4.78	5.86	6.84

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0012	1.14

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.84	1.84	1.84	1.84
0.38	1.88	1.88	1.88	1.88
1.00	1.94	1.94	1.94	1.94
3.00	2.09	2.09	2.09	2.09

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0011	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.96	0.96	0.96	0.96
0.38	0.99	0.99	0.99	0.99
1.00	1.05	1.05	1.05	1.05
3.00	1.17	1.17	1.17	1.17

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0011	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	3.19	3.95	4.77	5.49
0.38	3.24	4.00	4.82	5.55
1.00	3.28	4.04	4.86	5.59
3.00	3.35	4.11	4.93	5.66

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0012	1.14

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	3.54	4.49	5.58	6.56
0.38	3.59	4.54	5.63	6.61
1.00	3.63	4.59	5.67	6.65
3.00	3.70	4.65	5.74	6.72

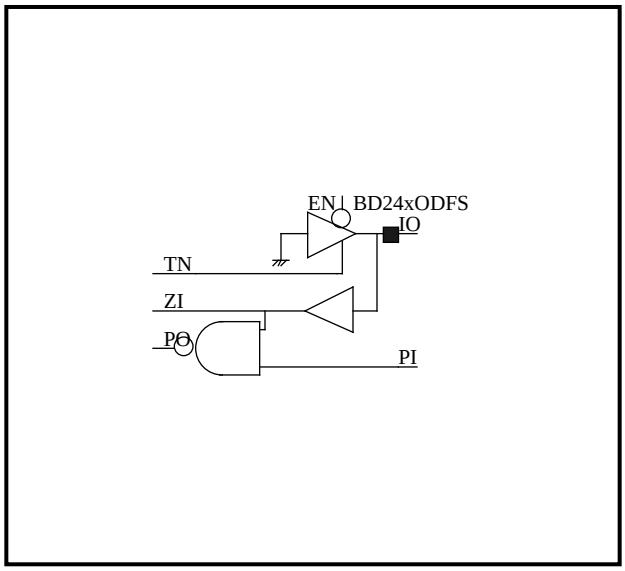
BD24xODFS	BD24xODFS	1/4

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BD24xODFS	BIDIRECTIONAL OUTPUT BUFFER (LOW ENABLE) 24mA OPEN DRAIN with FAILSAFE	4	2	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

CMOS LEVEL		BD24CODFS
	INVERT	BD24CNODFS
LVTTL LEVEL		BD24THODFS
	INVERT	BD24TNODFS
HIGH-SPEED CMOS LEVEL	INVERT	BD24CNHODFS
HIGH-SPEED LVTTL LEVEL	INVERT	BD24TNHODFS
CMOS SCHMITT TRIGGER		BD24SCODFS
LVTTL SCHMITT TRIGGER		BD24STODFS

LOGIC SYMBOL



TRUTH TABLE (OUTPUT BUFFER)

INPUT		OUTPUT
EN	TN	IO
L	H	L
H	X	Hz
X	L	Hz

Note : IO is input when EN=H or TN=L

Verilog-HDL DESCRIPTION

```
BD24xODFS  inst(IO,ZI,PO,EN,TN,PI);
```

VHDL DESCRIPTION

```
inst:BD24xODFS
   port   map(IO,ZI,PO,EN,TN,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	ZI	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
EN	0.98
TN	1.00
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	ZI	PO
DRIVE	312.6	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
ZI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0115	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.22	0.29	0.36	0.53
0.38	0.28	0.35	0.42	0.59
1.00	0.35	0.42	0.49	0.66
3.00	0.48	0.56	0.63	0.81

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0080	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.23	0.32	0.41	0.61
0.38	0.28	0.37	0.45	0.65
1.00	0.35	0.44	0.53	0.73
3.00	0.51	0.61	0.69	0.90

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.62	0.62	0.62	0.62
0.38	0.71	0.71	0.71	0.71
1.00	0.83	0.83	0.83	0.83
3.00	1.03	1.03	1.03	1.03

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0008	0.48

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.96	2.53	3.19	3.80
0.38	1.98	2.54	3.20	3.81
1.00	2.05	2.61	3.27	3.88
3.00	2.33	2.89	3.55	4.16

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.75	0.75	0.75	0.75
0.38	0.79	0.79	0.79	0.79
1.00	0.84	0.84	0.84	0.84
3.00	0.97	0.97	0.97	0.97

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->IO	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0008	0.48

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.04	2.60	3.26	3.87
0.38	2.09	2.66	3.31	3.93
1.00	2.13	2.70	3.35	3.96
3.00	2.20	2.76	3.42	4.03

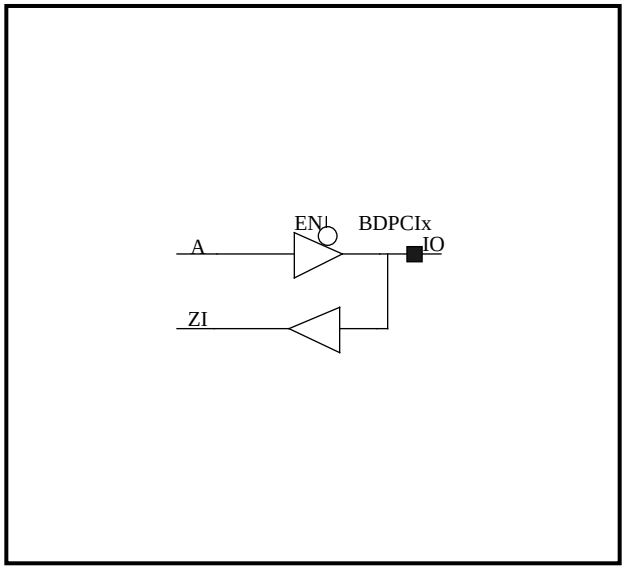
BDPCIx	BDPCIx	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BDPCIx	PCI (Peripheral Component Interconnect) BUS BIDIRECTIONAL OUTPUT BUFFER (LOW ENABLE)	0	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN	PULL-UP
BDPCI	BDPCID	BDPCIU

LOGIC SYMBOL



TRUTH TABLE (OUTPUT BUFFER)

INPUT		OUTPUT
EN	A	IO
L	L	L
L	H	H
H	X	Hz

Note : IO is input when EN=H

Verilog-HDL DESCRIPTION

```
BDPCIx  inst(IO,ZI,A,EN);
```

VHDL DESCRIPTION

```
inst:BDPCIx
   port   map(IO,ZI,A,EN);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	ZI
ELECTRO MIGRATION DRIVE	12064.0

INPUT LOAD (LU)

PIN NAME	LOAD
A	3.92
EN	3.97

OUTPUT DRIVE (LU)

PIN NAME	ZI
DRIVE	411.4

Rev.1.01.08

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0016	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.84	2.77	3.84	4.84
0.38	1.93	2.86	3.93	4.93
1.00	2.10	3.02	4.09	5.09
3.00	2.64	3.57	4.65	5.65

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->IO	---	FALL	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0012	0.75

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.71	2.51	3.49	4.41
0.38	1.74	2.54	3.51	4.43
1.00	1.80	2.59	3.57	4.49
3.00	2.03	2.84	3.82	4.74

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0012	0.75

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.01	2.01	2.01	2.01
0.38	2.08	2.08	2.08	2.08
1.00	2.15	2.15	2.15	2.15
3.00	2.28	2.28	2.28	2.28

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0016	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.15	0.15	0.15	0.15
0.38	0.24	0.24	0.24	0.24
1.00	0.37	0.37	0.37	0.37
3.00	0.56	0.56	0.56	0.56

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0016	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.88	2.84	3.93	4.93
0.38	1.92	2.88	3.97	4.97
1.00	1.98	2.94	4.03	5.03
3.00	2.11	3.07	4.16	5.16

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->IO	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
IO	0.0012	0.75

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.62	2.49	3.49	4.41
0.38	1.62	2.49	3.49	4.41
1.00	1.64	2.50	3.50	4.42
3.00	1.75	2.61	3.61	4.54

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0114	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.25	0.32	0.38	0.55
0.38	0.25	0.31	0.38	0.55
1.00	0.26	0.32	0.39	0.55
3.00	0.26	0.33	0.39	0.56

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
IO->ZI	---	FALL	---

SLEW FACTOR

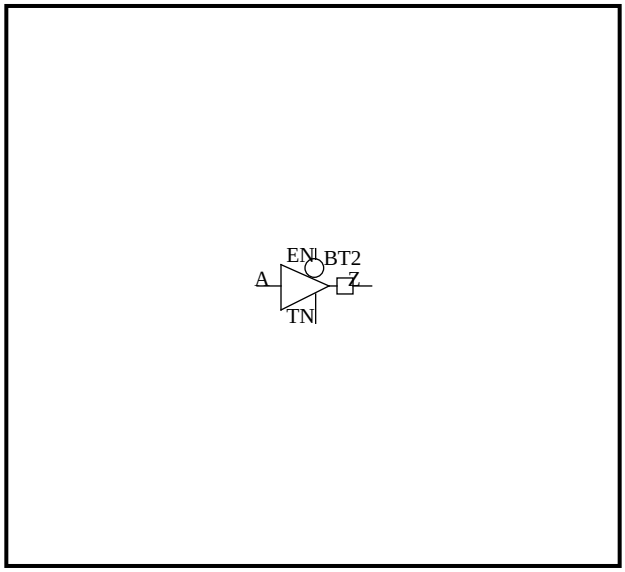
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
ZI	0.0037	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.29	0.35	0.40	0.51
0.38	0.31	0.37	0.43	0.54
1.00	0.38	0.44	0.49	0.60
3.00	0.62	0.68	0.73	0.85

BT2	BT2	1/6

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BT2	TRI-STATE OUTPUT BUFFER (LOW ENABLE) 2mA	3	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
EN	A	TN	Z
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Verilog-HDL DESCRIPTION

```
BT2  inst(Z,A,EN,TN);
```

VHDL DESCRIPTION

```
inst:BT2
  port  map(Z,A,EN,TN);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	6.31
EN	0.98
TN	1.00

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0002	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	1.63	2.09	2.98	4.71
0.38	1.71	2.18	3.06	4.79
1.00	1.87	2.34	3.23	4.96
3.00	2.38	2.85	3.75	5.48

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0003	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	1.84	2.53	3.89	6.58
0.38	1.84	2.53	3.88	6.58
1.00	1.88	2.57	3.92	6.62
3.00	2.05	2.74	4.10	6.79

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0002	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	1.63	2.09	2.98	4.71
0.38	1.71	2.18	3.06	4.79
1.00	1.87	2.34	3.23	4.96
3.00	2.38	2.85	3.75	5.48

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0003	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	1.84	2.53	3.89	6.58
0.38	1.84	2.53	3.88	6.58
1.00	1.88	2.57	3.92	6.62
3.00	2.05	2.74	4.10	6.79

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0003	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	0.83	0.83	0.83	0.83
0.38	0.92	0.92	0.92	0.92
1.00	1.02	1.02	1.02	1.02
3.00	1.17	1.17	1.17	1.17

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0002	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	0.40	0.40	0.40	0.40
0.38	0.49	0.49	0.49	0.49
1.00	0.59	0.59	0.59	0.59
3.00	0.74	0.74	0.74	0.74

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0002	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	2.14	2.62	3.51	5.24
0.38	2.15	2.63	3.52	5.25
1.00	2.23	2.70	3.60	5.33
3.00	2.50	2.97	3.87	5.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0003	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	2.43	3.11	4.47	7.16
0.38	2.44	3.13	4.48	7.17
1.00	2.51	3.20	4.56	7.25
3.00	2.78	3.47	4.82	7.52

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0003	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	0.83	0.83	0.83	0.83
0.38	0.92	0.92	0.92	0.92
1.00	1.02	1.02	1.02	1.02
3.00	1.17	1.17	1.17	1.17

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0002	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	0.40	0.40	0.40	0.40
0.38	0.49	0.49	0.49	0.49
1.00	0.59	0.59	0.59	0.59
3.00	0.74	0.74	0.74	0.74

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0002	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	2.14	2.62	3.51	5.24
0.38	2.15	2.63	3.52	5.25
1.00	2.23	2.70	3.60	5.33
3.00	2.50	2.97	3.87	5.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0003	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	2.43	3.11	4.47	7.16
0.38	2.44	3.13	4.48	7.17
1.00	2.51	3.20	4.56	7.25
3.00	2.78	3.47	4.82	7.52

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0003	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	0.97	0.97	0.97	0.97
0.38	1.00	1.00	1.00	1.00
1.00	1.05	1.05	1.05	1.05
3.00	1.18	1.18	1.18	1.18

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0002	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	0.53	0.53	0.53	0.53
0.38	0.56	0.56	0.56	0.56
1.00	0.62	0.62	0.62	0.62
3.00	0.74	0.74	0.74	0.74

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0002	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	2.21	2.69	3.58	5.31
0.38	2.26	2.74	3.63	5.37
1.00	2.30	2.78	3.67	5.41
3.00	2.37	2.85	3.74	5.48

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0003	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	2.50	3.18	4.54	7.23
0.38	2.55	3.24	4.59	7.29
1.00	2.59	3.28	4.63	7.33
3.00	2.66	3.35	4.70	7.39

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0003	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	0.97	0.97	0.97	0.97
0.38	1.00	1.00	1.00	1.00
1.00	1.05	1.05	1.05	1.05
3.00	1.18	1.18	1.18	1.18

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0002	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	0.53	0.53	0.53	0.53
0.38	0.56	0.56	0.56	0.56
1.00	0.62	0.62	0.62	0.62
3.00	0.74	0.74	0.74	0.74

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0002	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	2.21	2.69	3.58	5.31
0.38	2.26	2.74	3.63	5.37
1.00	2.30	2.78	3.67	5.41
3.00	2.37	2.85	3.74	5.48

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	CMOS

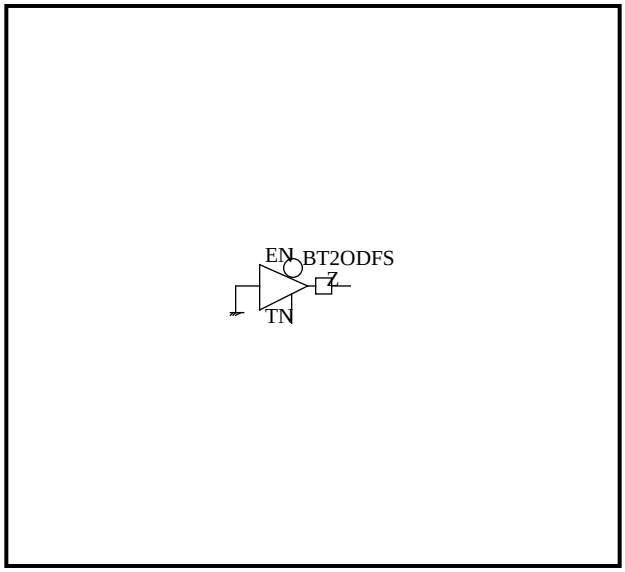
SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0003	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	2.50	3.18	4.54	7.23
0.38	2.55	3.24	4.59	7.29
1.00	2.59	3.28	4.63	7.33
3.00	2.66	3.35	4.70	7.39

BT2ODFS				BT2ODFS	1/3
CELL NAME	FUNCTION	CELL COUNT		CONDITION	
BT2ODFS	TRI-STATE OUTPUT BUFFER (LOW ENABLE) 2mA OPEN DRAIN with FAILSAFE	GATE	I/O	VDD=3.3V, Ta=25°C, Typ.	
		3	1		

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
EN	TN	Z
L	H	L
H	X	Hz
X	L	Hz

Verilog-HDL DESCRIPTION

```
BT2ODFS  inst(Z,EN,TN);
```

VHDL DESCRIPTION

```
inst:BT2ODFS
   port   map(Z,EN,TN);
```

INPUT LOAD (LU)

PIN NAME	LOAD
EN	0.98
TN	1.00

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	0.34	0.34	0.34	0.34
0.38	0.43	0.43	0.43	0.43
1.00	0.52	0.52	0.52	0.52
3.00	0.64	0.64	0.64	0.64

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0098	0.63

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	2.11	2.81	4.17	6.86
0.38	2.13	2.82	4.18	6.87
1.00	2.21	2.90	4.26	6.95
3.00	2.46	3.16	4.51	7.21

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	0.34	0.34	0.34	0.34
0.38	0.43	0.43	0.43	0.43
1.00	0.52	0.52	0.52	0.52
3.00	0.64	0.64	0.64	0.64

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0098	0.63

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	2.11	2.81	4.17	6.86
0.38	2.13	2.82	4.18	6.87
1.00	2.21	2.90	4.26	6.95
3.00	2.46	3.16	4.51	7.21

BT2ODFS | BT2ODFS | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	0.47	0.47	0.47	0.47
0.38	0.50	0.50	0.50	0.50
1.00	0.56	0.56	0.56	0.56
3.00	0.68	0.68	0.68	0.68

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0098	0.63

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	2.18	2.88	4.24	6.93
0.38	2.24	2.93	4.29	6.98
1.00	2.28	2.97	4.33	7.02
3.00	2.35	3.04	4.40	7.09

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	0.47	0.47	0.47	0.47
0.38	0.50	0.50	0.50	0.50
1.00	0.56	0.56	0.56	0.56
3.00	0.68	0.68	0.68	0.68

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	CMOS

SLEW FACTOR

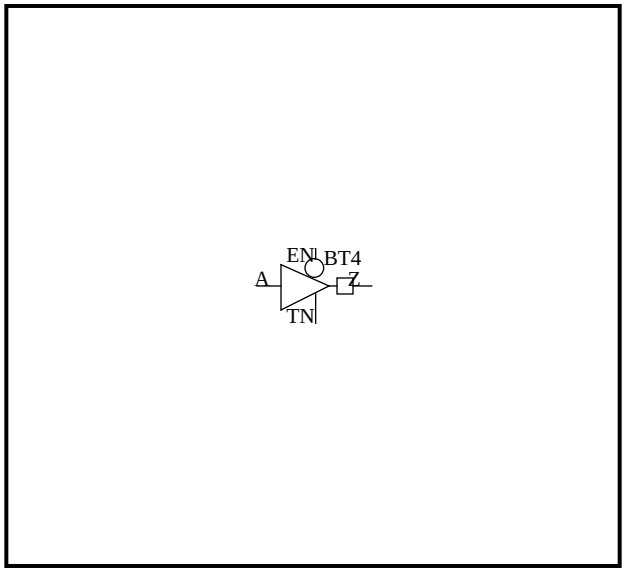
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0098	0.63

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	2.18	2.88	4.24	6.93
0.38	2.24	2.93	4.29	6.98
1.00	2.28	2.97	4.33	7.02
3.00	2.35	3.04	4.40	7.09

BT4	BT4	1/6

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BT4	TRI-STATE OUTPUT BUFFER (LOW ENABLE) 4mA	3	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
EN	A	TN	Z
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Verilog-HDL DESCRIPTION

```
BT4  inst(Z,A,EN,TN);
```

VHDL DESCRIPTION

```
inst:BT4
  port  map(Z,A,EN,TN);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	6.31
EN	0.98
TN	1.00

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0001	0.83

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.85	3.00	4.61	6.70
0.38	1.93	3.08	4.69	6.78
1.00	2.09	3.24	4.85	6.95
3.00	2.63	3.78	5.39	7.48

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.65

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.79	3.21	5.30	8.06
0.38	1.78	3.21	5.29	8.06
1.00	1.82	3.25	5.33	8.09
3.00	1.99	3.42	5.50	8.27

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0001	0.83

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.85	3.00	4.61	6.70
0.38	1.93	3.08	4.69	6.78
1.00	2.09	3.24	4.85	6.95
3.00	2.63	3.78	5.39	7.48

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.65

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.79	3.21	5.30	8.06
0.38	1.78	3.21	5.29	8.06
1.00	1.82	3.25	5.33	8.09
3.00	1.99	3.42	5.50	8.27

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.65

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.07	1.07	1.07	1.07
0.38	1.16	1.16	1.16	1.16
1.00	1.26	1.26	1.26	1.26
3.00	1.40	1.40	1.40	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0001	0.83

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.41	0.41	0.41	0.41
0.38	0.50	0.50	0.50	0.50
1.00	0.60	0.60	0.60	0.60
3.00	0.75	0.75	0.75	0.75

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0001	0.83

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.38	3.54	5.15	7.25
0.38	2.39	3.55	5.16	7.26
1.00	2.47	3.63	5.24	7.34
3.00	2.74	3.90	5.51	7.61

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.65

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.37	3.80	5.88	8.65
0.38	2.38	3.81	5.90	8.66
1.00	2.46	3.89	5.97	8.74
3.00	2.72	4.15	6.24	9.00

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.65

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.07	1.07	1.07	1.07
0.38	1.16	1.16	1.16	1.16
1.00	1.26	1.26	1.26	1.26
3.00	1.40	1.40	1.40	1.40

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0001	0.83

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.41	0.41	0.41	0.41
0.38	0.50	0.50	0.50	0.50
1.00	0.60	0.60	0.60	0.60
3.00	0.75	0.75	0.75	0.75

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0001	0.83

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.38	3.54	5.15	7.25
0.38	2.39	3.55	5.16	7.26
1.00	2.47	3.63	5.24	7.34
3.00	2.74	3.90	5.51	7.61

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.65

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.37	3.80	5.88	8.65
0.38	2.38	3.81	5.90	8.66
1.00	2.46	3.89	5.97	8.74
3.00	2.72	4.15	6.24	9.00

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.65

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.20	1.20	1.20	1.20
0.38	1.23	1.23	1.23	1.23
1.00	1.29	1.29	1.29	1.29
3.00	1.41	1.41	1.41	1.41

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0001	0.83

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.54	0.54	0.54	0.54
0.38	0.58	0.58	0.58	0.58
1.00	0.63	0.63	0.63	0.63
3.00	0.76	0.76	0.76	0.76

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0001	0.83

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.45	3.61	5.22	7.32
0.38	2.51	3.67	5.28	7.38
1.00	2.55	3.71	5.32	7.42
3.00	2.62	3.78	5.38	7.48

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.65

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.44	3.87	5.96	8.72
0.38	2.49	3.92	6.01	8.77
1.00	2.53	3.96	6.05	8.81
3.00	2.60	4.03	6.12	8.88

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.65

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.20	1.20	1.20	1.20
0.38	1.23	1.23	1.23	1.23
1.00	1.29	1.29	1.29	1.29
3.00	1.41	1.41	1.41	1.41

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0001	0.83

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.54	0.54	0.54	0.54
0.38	0.58	0.58	0.58	0.58
1.00	0.63	0.63	0.63	0.63
3.00	0.76	0.76	0.76	0.76

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0001	0.83

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.45	3.61	5.22	7.32
0.38	2.51	3.67	5.28	7.38
1.00	2.55	3.71	5.32	7.42
3.00	2.62	3.78	5.38	7.48

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	CMOS

SLEW FACTOR

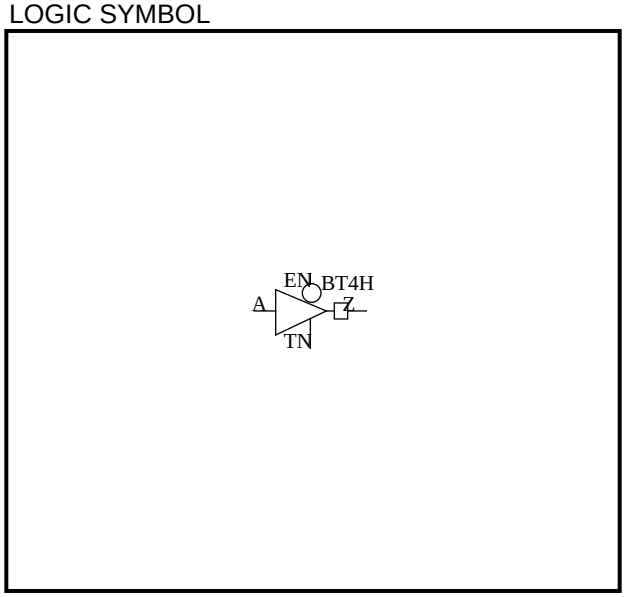
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.65

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.44	3.87	5.96	8.72
0.38	2.49	3.92	6.01	8.77
1.00	2.53	3.96	6.05	8.81
3.00	2.60	4.03	6.12	8.88

BT4H	BT4H	1/6

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BT4H	TRI-STATE OUTPUT BUFFER (LOW ENABLE) 4mA HIGH-SPEED	3	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
EN	A	TN	Z
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Verilog-HDL DESCRIPTION

```
BT4H  inst(Z,A,EN,TN);
```

VHDL DESCRIPTION

```
inst:BT4H
  port  map(Z,A,EN,TN);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	9.03
EN	0.98
TN	1.00

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0047	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.10	2.15	3.71	5.79
0.38	1.19	2.24	3.80	5.88
1.00	1.32	2.37	3.93	6.01
3.00	1.62	2.67	4.23	6.31

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.43	2.82	4.89	7.65
0.38	1.44	2.83	4.90	7.65
1.00	1.45	2.84	4.91	7.66
3.00	1.52	2.89	4.95	7.71

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0047	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.10	2.15	3.71	5.79
0.38	1.19	2.24	3.80	5.88
1.00	1.32	2.37	3.93	6.01
3.00	1.62	2.67	4.23	6.31

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.43	2.82	4.89	7.65
0.38	1.44	2.83	4.90	7.65
1.00	1.45	2.84	4.91	7.66
3.00	1.52	2.89	4.95	7.71

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.97	0.97	0.97	0.97
0.38	1.06	1.06	1.06	1.06
1.00	1.17	1.17	1.17	1.17
3.00	1.34	1.34	1.34	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0047	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.52	0.52	0.52	0.52
0.38	0.61	0.61	0.61	0.61
1.00	0.71	0.71	0.71	0.71
3.00	0.87	0.87	0.87	0.87

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0047	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.67	2.73	4.29	6.37
0.38	1.68	2.74	4.30	6.38
1.00	1.76	2.81	4.38	6.46
3.00	2.03	3.09	4.65	6.73

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.07	3.46	5.53	8.29
0.38	2.08	3.47	5.54	8.30
1.00	2.15	3.55	5.62	8.38
3.00	2.42	3.81	5.89	8.65

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.97	0.97	0.97	0.97
0.38	1.06	1.06	1.06	1.06
1.00	1.17	1.17	1.17	1.17
3.00	1.34	1.34	1.34	1.34

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0047	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.52	0.52	0.52	0.52
0.38	0.61	0.61	0.61	0.61
1.00	0.71	0.71	0.71	0.71
3.00	0.87	0.87	0.87	0.87

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0047	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.67	2.73	4.29	6.37
0.38	1.68	2.74	4.30	6.38
1.00	1.76	2.81	4.38	6.46
3.00	2.03	3.09	4.65	6.73

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.07	3.46	5.53	8.29
0.38	2.08	3.47	5.54	8.30
1.00	2.15	3.55	5.62	8.38
3.00	2.42	3.81	5.89	8.65

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.10	1.10	1.10	1.10
0.38	1.14	1.14	1.14	1.14
1.00	1.19	1.19	1.19	1.19
3.00	1.32	1.32	1.32	1.32

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0047	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.65	0.65	0.65	0.65
0.38	0.68	0.68	0.68	0.68
1.00	0.74	0.74	0.74	0.74
3.00	0.86	0.86	0.86	0.86

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0047	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.74	2.80	4.36	6.44
0.38	1.80	2.85	4.41	6.49
1.00	1.83	2.89	4.45	6.53
3.00	1.90	2.96	4.52	6.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.14	3.53	5.60	8.36
0.38	2.19	3.58	5.66	8.41
1.00	2.23	3.62	5.69	8.45
3.00	2.30	3.69	5.76	8.52

BT4H BT4H 6/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.10	1.10	1.10	1.10
0.38	1.14	1.14	1.14	1.14
1.00	1.19	1.19	1.19	1.19
3.00	1.32	1.32	1.32	1.32

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0047	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.65	0.65	0.65	0.65
0.38	0.68	0.68	0.68	0.68
1.00	0.74	0.74	0.74	0.74
3.00	0.86	0.86	0.86	0.86

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0047	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.74	2.80	4.36	6.44
0.38	1.80	2.85	4.41	6.49
1.00	1.83	2.89	4.45	6.53
3.00	1.90	2.96	4.52	6.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.14	3.53	5.60	8.36
0.38	2.19	3.58	5.66	8.41
1.00	2.23	3.62	5.69	8.45
3.00	2.30	3.69	5.76	8.52

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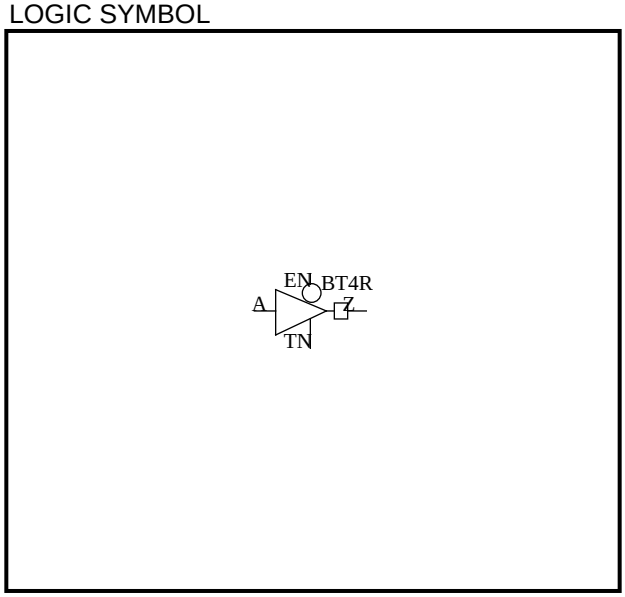
BT4R	BT4R	1/6

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BT4R	TRI-STATE OUTPUT BUFFER (LOW ENABLE) 4mA SLEW RATE CONTROL	3	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
EN	A	TN	Z
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Verilog-HDL DESCRIPTION

```
BT4R  inst(Z,A,EN,TN);
```

VHDL DESCRIPTION

```
inst:BT4R
   port   map(Z,A,EN,TN);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	7.58
EN	0.98
TN	1.00

Rev.1.01.10

BT4R | BT4R | 2/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0058	1.47

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.52	4.10	6.26	8.90
0.38	2.61	4.20	6.36	9.00
1.00	2.79	4.37	6.53	9.18
3.00	3.39	4.98	7.14	9.79

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0066	1.71

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	3.43	5.68	8.75	12.52
0.38	3.48	5.73	8.80	12.57
1.00	3.62	5.87	8.94	12.71
3.00	4.08	6.33	9.40	13.17

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0058	1.47

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.52	4.10	6.26	8.90
0.38	2.61	4.20	6.36	9.00
1.00	2.79	4.37	6.53	9.18
3.00	3.39	4.98	7.14	9.79

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0066	1.71

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	3.43	5.68	8.75	12.52
0.38	3.48	5.73	8.80	12.57
1.00	3.62	5.87	8.94	12.71
3.00	4.08	6.33	9.40	13.17

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0066	1.71

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.82	0.82	0.82	0.82
0.38	0.91	0.91	0.91	0.91
1.00	1.01	1.01	1.01	1.01
3.00	1.17	1.17	1.17	1.17

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0058	1.47

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.51	0.51	0.51	0.51
0.38	0.60	0.60	0.60	0.60
1.00	0.69	0.69	0.69	0.69
3.00	0.84	0.84	0.84	0.84

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0058	1.47

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	3.18	4.78	6.95	9.60
0.38	3.19	4.79	6.96	9.61
1.00	3.27	4.87	7.04	9.68
3.00	3.55	5.15	7.32	9.97

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0066	1.71

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	4.26	6.51	9.58	13.35
0.38	4.27	6.53	9.59	13.37
1.00	4.35	6.60	9.67	13.44
3.00	4.61	6.86	9.93	13.70

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0066	1.71

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.82	0.82	0.82	0.82
0.38	0.91	0.91	0.91	0.91
1.00	1.01	1.01	1.01	1.01
3.00	1.17	1.17	1.17	1.17

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0058	1.47

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.51	0.51	0.51	0.51
0.38	0.60	0.60	0.60	0.60
1.00	0.69	0.69	0.69	0.69
3.00	0.84	0.84	0.84	0.84

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0058	1.47

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	3.18	4.78	6.95	9.60
0.38	3.19	4.79	6.96	9.61
1.00	3.27	4.87	7.04	9.68
3.00	3.55	5.15	7.32	9.97

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0066	1.71

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	4.26	6.51	9.58	13.35
0.38	4.27	6.53	9.59	13.37
1.00	4.35	6.60	9.67	13.44
3.00	4.61	6.86	9.93	13.70

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0066	1.71

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.95	0.95	0.95	0.95
0.38	0.99	0.99	0.99	0.99
1.00	1.04	1.04	1.04	1.04
3.00	1.18	1.18	1.18	1.18

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0058	1.47

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.64	0.64	0.64	0.64
0.38	0.67	0.67	0.67	0.67
1.00	0.73	0.73	0.73	0.73
3.00	0.85	0.85	0.85	0.85

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0058	1.47

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	3.25	4.85	7.02	9.67
0.38	3.31	4.90	7.07	9.72
1.00	3.35	4.94	7.11	9.76
3.00	3.42	5.01	7.18	9.83

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0066	1.71

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	4.33	6.58	9.65	13.42
0.38	4.39	6.64	9.71	13.48
1.00	4.43	6.68	9.75	13.52
3.00	4.49	6.75	9.81	13.59

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0066	1.71

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.95	0.95	0.95	0.95
0.38	0.99	0.99	0.99	0.99
1.00	1.04	1.04	1.04	1.04
3.00	1.18	1.18	1.18	1.18

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0058	1.47

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.64	0.64	0.64	0.64
0.38	0.67	0.67	0.67	0.67
1.00	0.73	0.73	0.73	0.73
3.00	0.85	0.85	0.85	0.85

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0058	1.47

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	3.25	4.85	7.02	9.67
0.38	3.31	4.90	7.07	9.72
1.00	3.35	4.94	7.11	9.76
3.00	3.42	5.01	7.18	9.83

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	CMOS

SLEW FACTOR

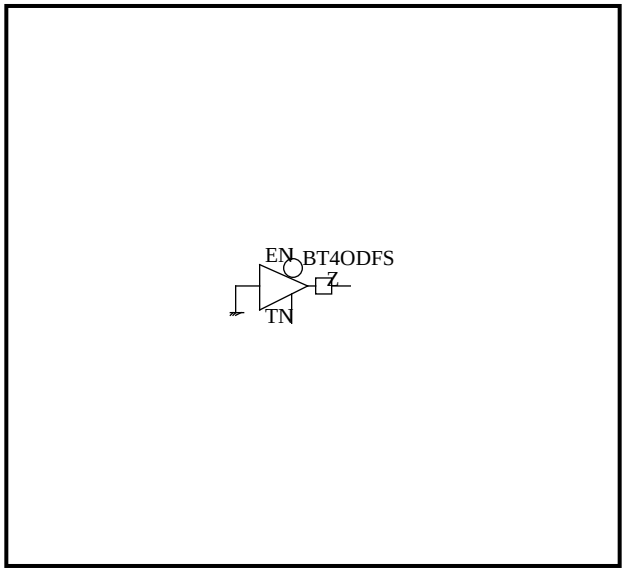
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0066	1.71

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	4.33	6.58	9.65	13.42
0.38	4.39	6.64	9.71	13.48
1.00	4.43	6.68	9.75	13.52
3.00	4.49	6.75	9.81	13.59

BT4ODFS	BT4ODFS	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BT4ODFS	TRI-STATE OUTPUT BUFFER (LOW ENABLE) 4mA OPEN DRAIN with FAILSAFE	3	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
EN	TN	Z
L	H	L
H	X	Hz
X	L	Hz

Verilog-HDL DESCRIPTION

```
BT4ODFS  inst(Z,EN,TN);
```

VHDL DESCRIPTION

```
inst:BT4ODFS
   port   map(Z,EN,TN);
```

INPUT LOAD (LU)

PIN NAME	LOAD
EN	0.98
TN	1.00

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.35	0.35	0.35	0.35
0.38	0.44	0.44	0.44	0.44
1.00	0.53	0.53	0.53	0.53
3.00	0.66	0.66	0.66	0.66

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.48

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.16	3.59	5.68	8.44
0.38	2.17	3.61	5.69	8.46
1.00	2.25	3.69	5.77	8.54
3.00	2.50	3.94	6.03	8.79

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.35	0.35	0.35	0.35
0.38	0.44	0.44	0.44	0.44
1.00	0.53	0.53	0.53	0.53
3.00	0.66	0.66	0.66	0.66

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.48

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.16	3.59	5.68	8.44
0.38	2.17	3.61	5.69	8.46
1.00	2.25	3.69	5.77	8.54
3.00	2.50	3.94	6.03	8.79

BT4ODFS | BT4ODFS | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.48	0.48	0.48	0.48
0.38	0.52	0.52	0.52	0.52
1.00	0.57	0.57	0.57	0.57
3.00	0.69	0.69	0.69	0.69

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.48

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.23	3.66	5.75	8.51
0.38	2.28	3.72	5.80	8.57
1.00	2.32	3.76	5.84	8.61
3.00	2.39	3.83	5.91	8.67

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.48	0.48	0.48	0.48
0.38	0.52	0.52	0.52	0.52
1.00	0.57	0.57	0.57	0.57
3.00	0.69	0.69	0.69	0.69

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.48

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.23	3.66	5.75	8.51
0.38	2.28	3.72	5.80	8.57
1.00	2.32	3.76	5.84	8.61
3.00	2.39	3.83	5.91	8.67

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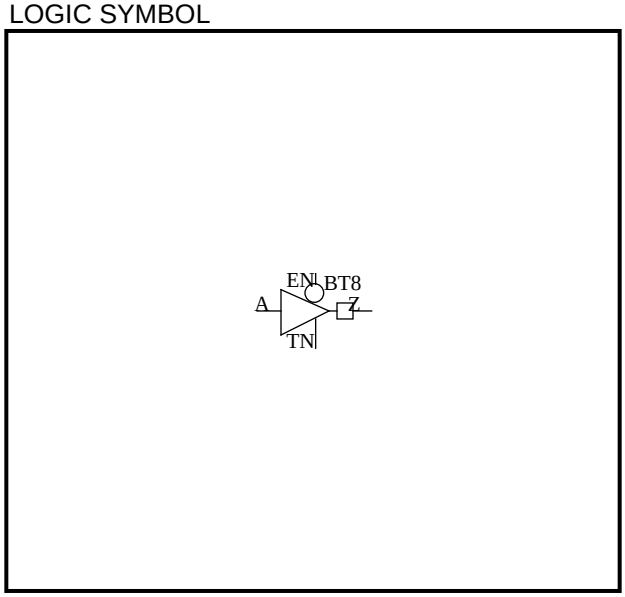
BT8	BT8	1/6

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BT8	TRI-STATE OUTPUT BUFFER (LOW ENABLE) 8mA	3	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
EN	A	TN	Z
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Verilog-HDL DESCRIPTION

```
BT8  inst(Z,A,EN,TN);
```

VHDL DESCRIPTION

```
inst:BT8
   port   map(Z,A,EN,TN);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	6.31
EN	0.98
TN	1.00

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BT8 BT8 2/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0023	1.03

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.93	2.69	3.62	4.76
0.38	2.01	2.77	3.71	4.84
1.00	2.17	2.93	3.86	5.00
3.00	2.71	3.48	4.41	5.55

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.61

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.57	2.36	3.44	4.85
0.38	1.58	2.36	3.44	4.85
1.00	1.61	2.39	3.47	4.88
3.00	1.79	2.56	3.64	5.05

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0023	1.03

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.93	2.69	3.62	4.76
0.38	2.01	2.77	3.71	4.84
1.00	2.17	2.93	3.86	5.00
3.00	2.71	3.48	4.41	5.55

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.61

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.57	2.36	3.44	4.85
0.38	1.58	2.36	3.44	4.85
1.00	1.61	2.39	3.47	4.88
3.00	1.79	2.56	3.64	5.05

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.61

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.67	1.67	1.67	1.67
0.38	1.75	1.75	1.75	1.75
1.00	1.85	1.85	1.85	1.85
3.00	2.00	2.00	2.00	2.00

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0023	1.03

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.44	0.44	0.44	0.44
0.38	0.53	0.53	0.53	0.53
1.00	0.63	0.63	0.63	0.63
3.00	0.78	0.78	0.78	0.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0023	1.03

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.46	3.24	4.18	5.32
0.38	2.47	3.25	4.19	5.33
1.00	2.55	3.33	4.27	5.40
3.00	2.81	3.59	4.53	5.67

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.61

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.10	2.92	4.02	5.43
0.38	2.11	2.93	4.03	5.44
1.00	2.19	3.01	4.11	5.52
3.00	2.45	3.27	4.37	5.78

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.61

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.67	1.67	1.67	1.67
0.38	1.75	1.75	1.75	1.75
1.00	1.85	1.85	1.85	1.85
3.00	2.00	2.00	2.00	2.00

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0023	1.03

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.44	0.44	0.44	0.44
0.38	0.53	0.53	0.53	0.53
1.00	0.63	0.63	0.63	0.63
3.00	0.78	0.78	0.78	0.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0023	1.03

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.46	3.24	4.18	5.32
0.38	2.47	3.25	4.19	5.33
1.00	2.55	3.33	4.27	5.40
3.00	2.81	3.59	4.53	5.67

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.61

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.10	2.92	4.02	5.43
0.38	2.11	2.93	4.03	5.44
1.00	2.19	3.01	4.11	5.52
3.00	2.45	3.27	4.37	5.78

BT8 BT8 5/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.61

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.80	1.80	1.80	1.80
0.38	1.83	1.83	1.83	1.83
1.00	1.89	1.89	1.89	1.89
3.00	2.01	2.01	2.01	2.01

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0023	1.03

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.57	0.57	0.57	0.57
0.38	0.60	0.60	0.60	0.60
1.00	0.66	0.66	0.66	0.66
3.00	0.78	0.78	0.78	0.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0023	1.03

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.53	3.31	4.25	5.39
0.38	2.58	3.36	4.30	5.44
1.00	2.62	3.40	4.34	5.48
3.00	2.69	3.47	4.41	5.55

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.61

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.17	2.99	4.09	5.50
0.38	2.23	3.04	4.14	5.55
1.00	2.27	3.08	4.18	5.59
3.00	2.33	3.15	4.25	5.66

BT8 BT8 6/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.61

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.80	1.80	1.80	1.80
0.38	1.83	1.83	1.83	1.83
1.00	1.89	1.89	1.89	1.89
3.00	2.01	2.01	2.01	2.01

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0023	1.03

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.57	0.57	0.57	0.57
0.38	0.60	0.60	0.60	0.60
1.00	0.66	0.66	0.66	0.66
3.00	0.78	0.78	0.78	0.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0023	1.03

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.53	3.31	4.25	5.39
0.38	2.58	3.36	4.30	5.44
1.00	2.62	3.40	4.34	5.48
3.00	2.69	3.47	4.41	5.55

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.61

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.17	2.99	4.09	5.50
0.38	2.23	3.04	4.14	5.55
1.00	2.27	3.08	4.18	5.59
3.00	2.33	3.15	4.25	5.66

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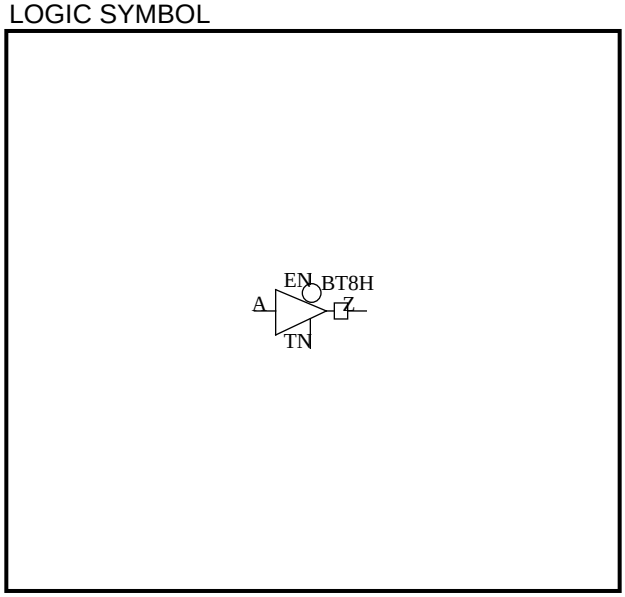
BT8H	BT8H	1/6

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BT8H	TRI-STATE OUTPUT BUFFER (LOW ENABLE) 8mA HIGH-SPEED	3	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
EN	A	TN	Z
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Verilog-HDL DESCRIPTION

```
BT8H  inst(Z,A,EN,TN);
```

VHDL DESCRIPTION

```
inst:BT8H
  port  map(Z,A,EN,TN);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	9.03
EN	0.98
TN	1.00

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0024	0.42

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.93	1.50	2.31	3.36
0.38	1.02	1.59	2.39	3.44
1.00	1.17	1.74	2.54	3.59
3.00	1.53	2.10	2.90	3.95

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.39

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.12	1.83	2.86	4.24
0.38	1.13	1.84	2.87	4.25
1.00	1.16	1.85	2.88	4.26
3.00	1.27	1.95	2.96	4.33

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0024	0.42

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.93	1.50	2.31	3.36
0.38	1.02	1.59	2.39	3.44
1.00	1.17	1.74	2.54	3.59
3.00	1.53	2.10	2.90	3.95

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.39

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.12	1.83	2.86	4.24
0.38	1.13	1.84	2.87	4.25
1.00	1.16	1.85	2.88	4.26
3.00	1.27	1.95	2.96	4.33

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.39

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.44	1.44	1.44	1.44
0.38	1.53	1.53	1.53	1.53
1.00	1.64	1.64	1.64	1.64
3.00	1.81	1.81	1.81	1.81

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0024	0.42

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.55	0.55	0.55	0.55
0.38	0.64	0.64	0.64	0.64
1.00	0.74	0.74	0.74	0.74
3.00	0.90	0.90	0.90	0.90

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0024	0.42

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.51	2.10	2.90	3.95
0.38	1.52	2.11	2.91	3.97
1.00	1.60	2.18	2.99	4.04
3.00	1.87	2.46	3.27	4.32

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.39

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.70	2.43	3.48	4.87
0.38	1.71	2.44	3.50	4.88
1.00	1.79	2.52	3.57	4.96
3.00	2.06	2.79	3.84	5.22

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.39

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.44	1.44	1.44	1.44
0.38	1.53	1.53	1.53	1.53
1.00	1.64	1.64	1.64	1.64
3.00	1.81	1.81	1.81	1.81

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0024	0.42

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.55	0.55	0.55	0.55
0.38	0.64	0.64	0.64	0.64
1.00	0.74	0.74	0.74	0.74
3.00	0.90	0.90	0.90	0.90

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0024	0.42

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.51	2.10	2.90	3.95
0.38	1.52	2.11	2.91	3.97
1.00	1.60	2.18	2.99	4.04
3.00	1.87	2.46	3.27	4.32

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.39

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.70	2.43	3.48	4.87
0.38	1.71	2.44	3.50	4.88
1.00	1.79	2.52	3.57	4.96
3.00	2.06	2.79	3.84	5.22

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.39

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.58	1.58	1.58	1.58
0.38	1.61	1.61	1.61	1.61
1.00	1.66	1.66	1.66	1.66
3.00	1.79	1.79	1.79	1.79

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0024	0.42

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.68	0.68	0.68	0.68
0.38	0.71	0.71	0.71	0.71
1.00	0.77	0.77	0.77	0.77
3.00	0.89	0.89	0.89	0.89

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0024	0.42

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.58	2.17	2.97	4.03
0.38	1.64	2.22	3.03	4.08
1.00	1.68	2.26	3.07	4.12
3.00	1.74	2.33	3.14	4.19

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.39

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.77	2.50	3.56	4.94
0.38	1.83	2.56	3.61	4.99
1.00	1.86	2.60	3.65	5.03
3.00	1.93	2.67	3.72	5.10

BT8H BT8H 6/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.39

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.58	1.58	1.58	1.58
0.38	1.61	1.61	1.61	1.61
1.00	1.66	1.66	1.66	1.66
3.00	1.79	1.79	1.79	1.79

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0024	0.42

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.68	0.68	0.68	0.68
0.38	0.71	0.71	0.71	0.71
1.00	0.77	0.77	0.77	0.77
3.00	0.89	0.89	0.89	0.89

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0024	0.42

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.58	2.17	2.97	4.03
0.38	1.64	2.22	3.03	4.08
1.00	1.68	2.26	3.07	4.12
3.00	1.74	2.33	3.14	4.19

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.39

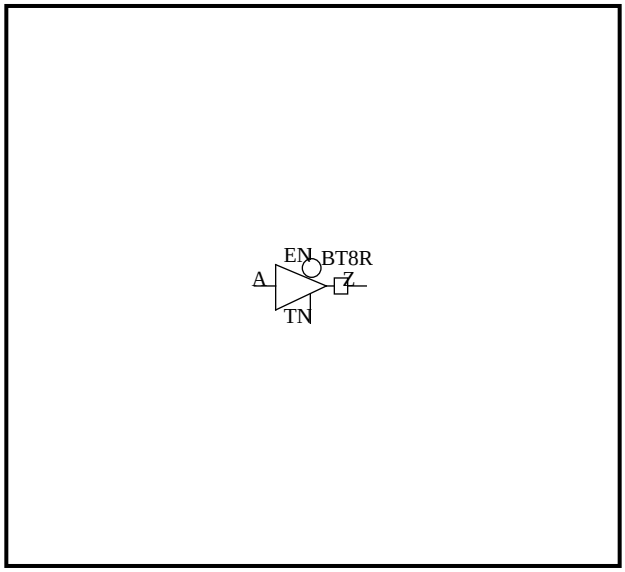
PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.77	2.50	3.56	4.94
0.38	1.83	2.56	3.61	4.99
1.00	1.86	2.60	3.65	5.03
3.00	1.93	2.67	3.72	5.10

Rev.1.01.10

BT8R	BT8R	1/6

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BT8R	TRI-STATE OUTPUT BUFFER (LOW ENABLE) 8mA SLEW RATE CONTROL	3	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
EN	A	TN	Z
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Verilog-HDL DESCRIPTION

```
BT8R  inst(Z,A,EN,TN);
```

VHDL DESCRIPTION

```
inst:BT8R
   port   map(Z,A,EN,TN);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	7.58
EN	0.98
TN	1.00

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0032	1.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.56	3.57	4.84	6.40
0.38	2.66	3.67	4.95	6.51
1.00	2.84	3.85	5.12	6.68
3.00	3.43	4.45	5.72	7.28

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0035	1.46

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	3.24	4.63	6.40	8.57
0.38	3.28	4.68	6.44	8.62
1.00	3.41	4.80	6.57	8.74
3.00	3.85	5.24	7.01	9.18

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0032	1.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.56	3.57	4.84	6.40
0.38	2.66	3.67	4.95	6.51
1.00	2.84	3.85	5.12	6.68
3.00	3.43	4.45	5.72	7.28

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0035	1.46

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	3.24	4.63	6.40	8.57
0.38	3.28	4.68	6.44	8.62
1.00	3.41	4.80	6.57	8.74
3.00	3.85	5.24	7.01	9.18

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0035	1.46

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.19	1.19	1.19	1.19
0.38	1.28	1.28	1.28	1.28
1.00	1.39	1.39	1.39	1.39
3.00	1.55	1.55	1.55	1.55

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0032	1.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.54	0.54	0.54	0.54
0.38	0.63	0.63	0.63	0.63
1.00	0.73	0.73	0.73	0.73
3.00	0.87	0.87	0.87	0.87

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0032	1.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	3.23	4.26	5.54	7.11
0.38	3.25	4.27	5.56	7.12
1.00	3.32	4.35	5.63	7.20
3.00	3.61	4.63	5.92	7.48

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0035	1.46

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	4.05	5.44	7.20	9.38
0.38	4.06	5.45	7.22	9.39
1.00	4.14	5.53	7.29	9.47
3.00	4.40	5.79	7.56	9.73

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0035	1.46

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.19	1.19	1.19	1.19
0.38	1.28	1.28	1.28	1.28
1.00	1.39	1.39	1.39	1.39
3.00	1.55	1.55	1.55	1.55

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0032	1.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.54	0.54	0.54	0.54
0.38	0.63	0.63	0.63	0.63
1.00	0.73	0.73	0.73	0.73
3.00	0.87	0.87	0.87	0.87

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0032	1.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	3.23	4.26	5.54	7.11
0.38	3.25	4.27	5.56	7.12
1.00	3.32	4.35	5.63	7.20
3.00	3.61	4.63	5.92	7.48

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0035	1.46

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	4.05	5.44	7.20	9.38
0.38	4.06	5.45	7.22	9.39
1.00	4.14	5.53	7.29	9.47
3.00	4.40	5.79	7.56	9.73

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0035	1.46

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.32	1.32	1.32	1.32
0.38	1.36	1.36	1.36	1.36
1.00	1.42	1.42	1.42	1.42
3.00	1.56	1.56	1.56	1.56

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0032	1.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.67	0.67	0.67	0.67
0.38	0.71	0.71	0.71	0.71
1.00	0.76	0.76	0.76	0.76
3.00	0.89	0.89	0.89	0.89

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0032	1.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	3.31	4.33	5.61	7.18
0.38	3.36	4.39	5.67	7.23
1.00	3.40	4.43	5.71	7.27
3.00	3.47	4.50	5.78	7.34

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0035	1.46

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	4.12	5.51	7.28	9.45
0.38	4.17	5.56	7.33	9.50
1.00	4.21	5.60	7.37	9.54
3.00	4.28	5.67	7.44	9.61

BT8R BT8R 6/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0035	1.46

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.32	1.32	1.32	1.32
0.38	1.36	1.36	1.36	1.36
1.00	1.42	1.42	1.42	1.42
3.00	1.56	1.56	1.56	1.56

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0032	1.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.67	0.67	0.67	0.67
0.38	0.71	0.71	0.71	0.71
1.00	0.76	0.76	0.76	0.76
3.00	0.89	0.89	0.89	0.89

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0032	1.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	3.31	4.33	5.61	7.18
0.38	3.36	4.39	5.67	7.23
1.00	3.40	4.43	5.71	7.27
3.00	3.47	4.50	5.78	7.34

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0035	1.46

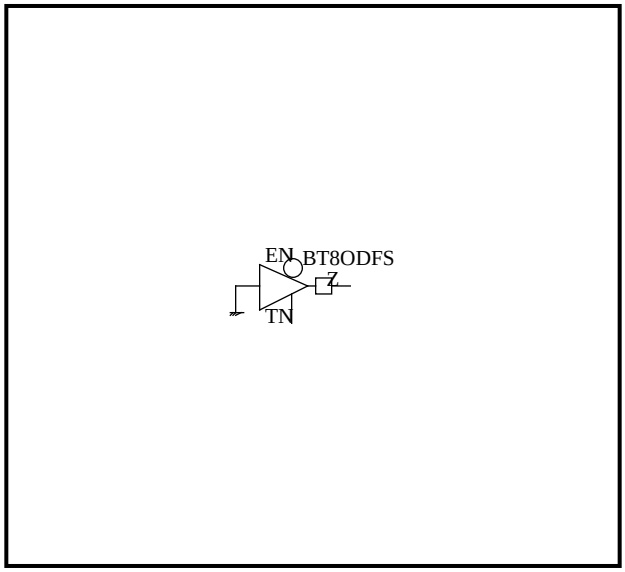
PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	4.12	5.51	7.28	9.45
0.38	4.17	5.56	7.33	9.50
1.00	4.21	5.60	7.37	9.54
3.00	4.28	5.67	7.44	9.61

Rev.1.01.10

BT8ODFS	BT8ODFS	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BT8ODFS	TRI-STATE OUTPUT BUFFER (LOW ENABLE) 8mA OPEN DRAIN with FAILSAFE	3	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
EN	TN	Z
L	H	L
H	X	Hz
X	L	Hz

Verilog-HDL DESCRIPTION

```
BT8ODFS  inst(Z,EN,TN);
```

VHDL DESCRIPTION

```
inst:BT8ODFS
   port   map(Z,EN,TN);
```

INPUT LOAD (LU)

PIN NAME	LOAD
EN	0.98
TN	1.00

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.38	0.38	0.38	0.38
0.38	0.46	0.46	0.46	0.46
1.00	0.55	0.55	0.55	0.55
3.00	0.68	0.68	0.68	0.68

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0024	0.57

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.93	2.76	3.87	5.28
0.38	1.94	2.77	3.88	5.29
1.00	2.02	2.86	3.96	5.37
3.00	2.28	3.11	4.21	5.62

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.38	0.38	0.38	0.38
0.38	0.46	0.46	0.46	0.46
1.00	0.55	0.55	0.55	0.55
3.00	0.68	0.68	0.68	0.68

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0024	0.57

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.93	2.76	3.87	5.28
0.38	1.94	2.77	3.88	5.29
1.00	2.02	2.86	3.96	5.37
3.00	2.28	3.11	4.21	5.62

BT8ODFS | BT8ODFS | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.51	0.51	0.51	0.51
0.38	0.54	0.54	0.54	0.54
1.00	0.60	0.60	0.60	0.60
3.00	0.72	0.72	0.72	0.72

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0024	0.57

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.00	2.83	3.94	5.35
0.38	2.05	2.89	3.99	5.40
1.00	2.09	2.93	4.03	5.44
3.00	2.16	2.99	4.10	5.51

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.51	0.51	0.51	0.51
0.38	0.54	0.54	0.54	0.54
1.00	0.60	0.60	0.60	0.60
3.00	0.72	0.72	0.72	0.72

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0024	0.57

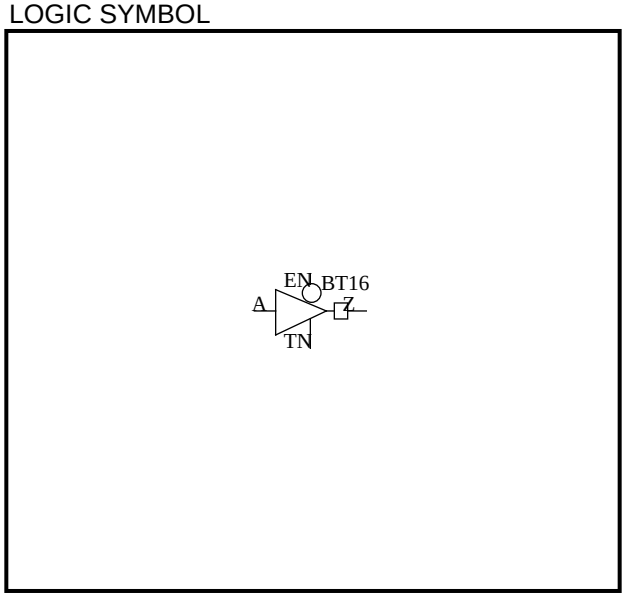
PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.00	2.83	3.94	5.35
0.38	2.05	2.89	3.99	5.40
1.00	2.09	2.93	4.03	5.44
3.00	2.16	2.99	4.10	5.51

Rev.1.01.10

BT16	BT16	1/6

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BT16	TRI-STATE OUTPUT BUFFER (LOW ENABLE) 16mA	3	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
EN	A	TN	Z
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Verilog-HDL DESCRIPTION

```
BT16  inst(Z,A,EN,TN);
```

VHDL DESCRIPTION

```
inst:BT16
   port   map(Z,A,EN,TN);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	7.75
EN	0.98
TN	1.00

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0011	0.94

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.72	2.44	3.25	3.98
0.38	1.80	2.52	3.33	4.06
1.00	1.95	2.67	3.48	4.21
3.00	2.47	3.20	4.00	4.73

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.52

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.30	2.01	2.93	3.82
0.38	1.31	2.01	2.93	3.82
1.00	1.35	2.05	2.96	3.85
3.00	1.53	2.22	3.14	4.02

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0011	0.94

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.72	2.44	3.25	3.98
0.38	1.80	2.52	3.33	4.06
1.00	1.95	2.67	3.48	4.21
3.00	2.47	3.20	4.00	4.73

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.52

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.30	2.01	2.93	3.82
0.38	1.31	2.01	2.93	3.82
1.00	1.35	2.05	2.96	3.85
3.00	1.53	2.22	3.14	4.02

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.52

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.50	1.50	1.50	1.50
0.38	1.58	1.58	1.58	1.58
1.00	1.68	1.68	1.68	1.68
3.00	1.83	1.83	1.83	1.83

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0011	0.94

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.50	0.50	0.50	0.50
0.38	0.59	0.59	0.59	0.59
1.00	0.69	0.69	0.69	0.69
3.00	0.84	0.84	0.84	0.84

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0011	0.94

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.23	2.97	3.78	4.51
0.38	2.24	2.98	3.79	4.52
1.00	2.32	3.06	3.87	4.60
3.00	2.58	3.33	4.14	4.87

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.52

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.88	2.63	3.57	4.46
0.38	1.90	2.65	3.58	4.47
1.00	1.97	2.72	3.65	4.55
3.00	2.24	2.99	3.92	4.81

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.52

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.50	1.50	1.50	1.50
0.38	1.58	1.58	1.58	1.58
1.00	1.68	1.68	1.68	1.68
3.00	1.83	1.83	1.83	1.83

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0011	0.94

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.50	0.50	0.50	0.50
0.38	0.59	0.59	0.59	0.59
1.00	0.69	0.69	0.69	0.69
3.00	0.84	0.84	0.84	0.84

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0011	0.94

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.23	2.97	3.78	4.51
0.38	2.24	2.98	3.79	4.52
1.00	2.32	3.06	3.87	4.60
3.00	2.58	3.33	4.14	4.87

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.52

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.88	2.63	3.57	4.46
0.38	1.90	2.65	3.58	4.47
1.00	1.97	2.72	3.65	4.55
3.00	2.24	2.99	3.92	4.81

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.52

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.63	1.63	1.63	1.63
0.38	1.66	1.66	1.66	1.66
1.00	1.72	1.72	1.72	1.72
3.00	1.84	1.84	1.84	1.84

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0011	0.94

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.63	0.63	0.63	0.63
0.38	0.66	0.66	0.66	0.66
1.00	0.72	0.72	0.72	0.72
3.00	0.84	0.84	0.84	0.84

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0011	0.94

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.30	3.04	3.85	4.58
0.38	2.35	3.09	3.90	4.64
1.00	2.39	3.13	3.94	4.68
3.00	2.46	3.20	4.01	4.74

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.52

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.96	2.71	3.64	4.53
0.38	2.01	2.76	3.69	4.58
1.00	2.05	2.80	3.73	4.62
3.00	2.12	2.87	3.80	4.69

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.52

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.63	1.63	1.63	1.63
0.38	1.66	1.66	1.66	1.66
1.00	1.72	1.72	1.72	1.72
3.00	1.84	1.84	1.84	1.84

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0011	0.94

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.63	0.63	0.63	0.63
0.38	0.66	0.66	0.66	0.66
1.00	0.72	0.72	0.72	0.72
3.00	0.84	0.84	0.84	0.84

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0011	0.94

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.30	3.04	3.85	4.58
0.38	2.35	3.09	3.90	4.64
1.00	2.39	3.13	3.94	4.68
3.00	2.46	3.20	4.01	4.74

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	CMOS

SLEW FACTOR

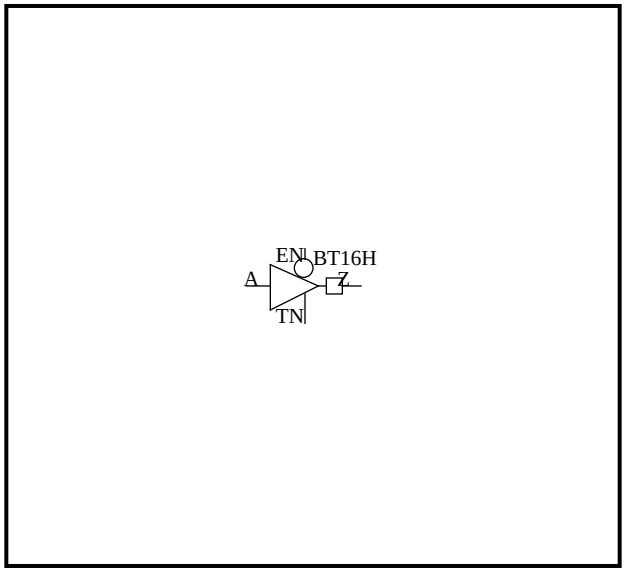
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.52

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.96	2.71	3.64	4.53
0.38	2.01	2.76	3.69	4.58
1.00	2.05	2.80	3.73	4.62
3.00	2.12	2.87	3.80	4.69

BT16H	BT16H	1/6

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BT16H	TRI-STATE OUTPUT BUFFER (LOW ENABLE) 16mA HIGH-SPEED	3	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
EN	A	TN	Z
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Verilog-HDL DESCRIPTION

```
BT16H  inst(Z,A,EN,TN);
```

VHDL DESCRIPTION

```
inst:BT16H
   port   map(Z,A,EN,TN);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	10.65
EN	0.98
TN	1.00

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.33

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.78	1.31	1.99	2.65
0.38	0.87	1.39	2.07	2.74
1.00	1.01	1.54	2.22	2.88
3.00	1.36	1.89	2.58	3.24

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.28

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.90	1.52	2.38	3.23
0.38	0.91	1.52	2.39	3.23
1.00	0.94	1.55	2.40	3.25
3.00	1.06	1.65	2.50	3.35

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.33

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.78	1.31	1.99	2.65
0.38	0.87	1.39	2.07	2.74
1.00	1.01	1.54	2.22	2.88
3.00	1.36	1.89	2.58	3.24

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.28

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.90	1.52	2.38	3.23
0.38	0.91	1.52	2.39	3.23
1.00	0.94	1.55	2.40	3.25
3.00	1.06	1.65	2.50	3.35

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.28

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.33	1.33	1.33	1.33
0.38	1.42	1.42	1.42	1.42
1.00	1.53	1.53	1.53	1.53
3.00	1.73	1.73	1.73	1.73

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.33

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.66	0.66	0.66	0.66
0.38	0.75	0.75	0.75	0.75
1.00	0.87	0.87	0.87	0.87
3.00	1.06	1.06	1.06	1.06

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.33

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.43	1.97	2.66	3.32
0.38	1.44	1.98	2.67	3.33
1.00	1.51	2.06	2.74	3.41
3.00	1.79	2.34	3.02	3.69

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.28

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.66	2.31	3.20	4.07
0.38	1.67	2.32	3.21	4.08
1.00	1.74	2.40	3.28	4.15
3.00	2.02	2.68	3.56	4.43

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.28

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.33	1.33	1.33	1.33
0.38	1.42	1.42	1.42	1.42
1.00	1.53	1.53	1.53	1.53
3.00	1.73	1.73	1.73	1.73

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.33

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.66	0.66	0.66	0.66
0.38	0.75	0.75	0.75	0.75
1.00	0.87	0.87	0.87	0.87
3.00	1.06	1.06	1.06	1.06

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.33

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.43	1.97	2.66	3.32
0.38	1.44	1.98	2.67	3.33
1.00	1.51	2.06	2.74	3.41
3.00	1.79	2.34	3.02	3.69

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.28

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.66	2.31	3.20	4.07
0.38	1.67	2.32	3.21	4.08
1.00	1.74	2.40	3.28	4.15
3.00	2.02	2.68	3.56	4.43

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.28

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.46	1.46	1.46	1.46
0.38	1.49	1.49	1.49	1.49
1.00	1.55	1.55	1.55	1.55
3.00	1.67	1.67	1.67	1.67

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.33

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.79	0.79	0.79	0.79
0.38	0.83	0.83	0.83	0.83
1.00	0.88	0.88	0.88	0.88
3.00	1.01	1.01	1.01	1.01

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.33

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.50	2.04	2.73	3.39
0.38	1.55	2.10	2.78	3.45
1.00	1.59	2.14	2.82	3.49
3.00	1.66	2.20	2.89	3.55

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.28

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.73	2.39	3.27	4.14
0.38	1.78	2.44	3.32	4.19
1.00	1.82	2.48	3.36	4.23
3.00	1.89	2.55	3.43	4.30

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.28

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.46	1.46	1.46	1.46
0.38	1.49	1.49	1.49	1.49
1.00	1.55	1.55	1.55	1.55
3.00	1.67	1.67	1.67	1.67

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.33

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.79	0.79	0.79	0.79
0.38	0.83	0.83	0.83	0.83
1.00	0.88	0.88	0.88	0.88
3.00	1.01	1.01	1.01	1.01

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.33

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.50	2.04	2.73	3.39
0.38	1.55	2.10	2.78	3.45
1.00	1.59	2.14	2.82	3.49
3.00	1.66	2.20	2.89	3.55

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	CMOS

SLEW FACTOR

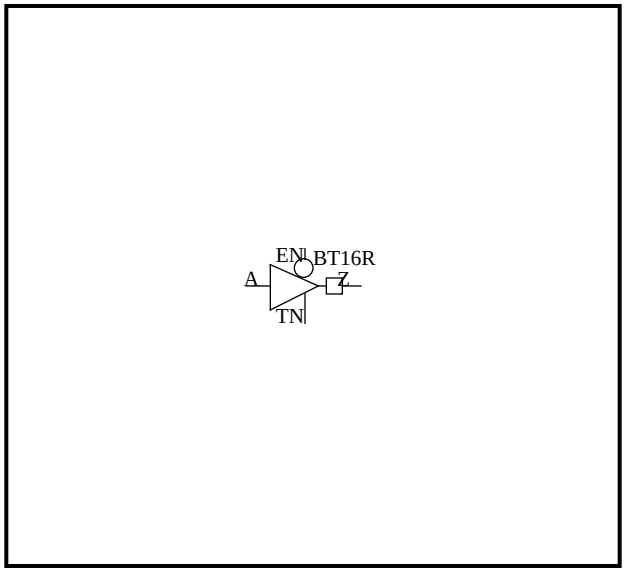
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.28

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.73	2.39	3.27	4.14
0.38	1.78	2.44	3.32	4.19
1.00	1.82	2.48	3.36	4.23
3.00	1.89	2.55	3.43	4.30

BT16R	BT16R	1/6

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BT16R	TRI-STATE OUTPUT BUFFER (LOW ENABLE) 16mA SLEW RATE CONTROL	3	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
EN	A	TN	Z
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Verilog-HDL DESCRIPTION

```
BT16R  inst(Z,A,EN,TN);
```

VHDL DESCRIPTION

```
inst:BT16R
   port   map(Z,A,EN,TN);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	8.93
EN	0.98
TN	1.00

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0016	1.16

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.25	3.22	4.33	5.34
0.38	2.37	3.34	4.45	5.46
1.00	2.57	3.54	4.65	5.66
3.00	3.24	4.21	5.32	6.32

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0018	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.77	4.02	5.52	6.90
0.38	2.82	4.08	5.57	6.96
1.00	2.93	4.19	5.69	7.07
3.00	3.28	4.55	6.05	7.44

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0016	1.16

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.25	3.22	4.33	5.34
0.38	2.37	3.34	4.45	5.46
1.00	2.57	3.54	4.65	5.66
3.00	3.24	4.21	5.32	6.32

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0018	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.77	4.02	5.52	6.90
0.38	2.82	4.08	5.57	6.96
1.00	2.93	4.19	5.69	7.07
3.00	3.28	4.55	6.05	7.44

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0018	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.02	2.02	2.02	2.02
0.38	2.12	2.12	2.12	2.12
1.00	2.23	2.23	2.23	2.23
3.00	2.40	2.40	2.40	2.40

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0016	1.16

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.61	0.61	0.61	0.61
0.38	0.70	0.70	0.70	0.70
1.00	0.80	0.80	0.80	0.80
3.00	0.95	0.95	0.95	0.95

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0016	1.16

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.90	3.89	5.01	6.02
0.38	2.91	3.91	5.02	6.03
1.00	2.99	3.98	5.10	6.11
3.00	3.27	4.27	5.38	6.39

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0018	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	3.12	4.40	5.90	7.28
0.38	3.14	4.41	5.91	7.30
1.00	3.21	4.49	5.99	7.37
3.00	3.48	4.75	6.25	7.64

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0018	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.02	2.02	2.02	2.02
0.38	2.12	2.12	2.12	2.12
1.00	2.23	2.23	2.23	2.23
3.00	2.40	2.40	2.40	2.40

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0016	1.16

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.61	0.61	0.61	0.61
0.38	0.70	0.70	0.70	0.70
1.00	0.80	0.80	0.80	0.80
3.00	0.95	0.95	0.95	0.95

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0016	1.16

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.90	3.89	5.01	6.02
0.38	2.91	3.91	5.02	6.03
1.00	2.99	3.98	5.10	6.11
3.00	3.27	4.27	5.38	6.39

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0018	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	3.12	4.40	5.90	7.28
0.38	3.14	4.41	5.91	7.30
1.00	3.21	4.49	5.99	7.37
3.00	3.48	4.75	6.25	7.64

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0018	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.16	2.16	2.16	2.16
0.38	2.20	2.20	2.20	2.20
1.00	2.26	2.26	2.26	2.26
3.00	2.41	2.41	2.41	2.41

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0016	1.16

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.74	0.74	0.74	0.74
0.38	0.77	0.77	0.77	0.77
1.00	0.83	0.83	0.83	0.83
3.00	0.95	0.95	0.95	0.95

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0016	1.16

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.97	3.96	5.08	6.09
0.38	3.02	4.02	5.13	6.14
1.00	3.06	4.06	5.17	6.18
3.00	3.13	4.13	5.24	6.25

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0018	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	3.20	4.47	5.97	7.36
0.38	3.25	4.52	6.02	7.41
1.00	3.29	4.56	6.06	7.45
3.00	3.36	4.63	6.13	7.52

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0018	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.16	2.16	2.16	2.16
0.38	2.20	2.20	2.20	2.20
1.00	2.26	2.26	2.26	2.26
3.00	2.41	2.41	2.41	2.41

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0016	1.16

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.74	0.74	0.74	0.74
0.38	0.77	0.77	0.77	0.77
1.00	0.83	0.83	0.83	0.83
3.00	0.95	0.95	0.95	0.95

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0016	1.16

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.97	3.96	5.08	6.09
0.38	3.02	4.02	5.13	6.14
1.00	3.06	4.06	5.17	6.18
3.00	3.13	4.13	5.24	6.25

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	CMOS

SLEW FACTOR

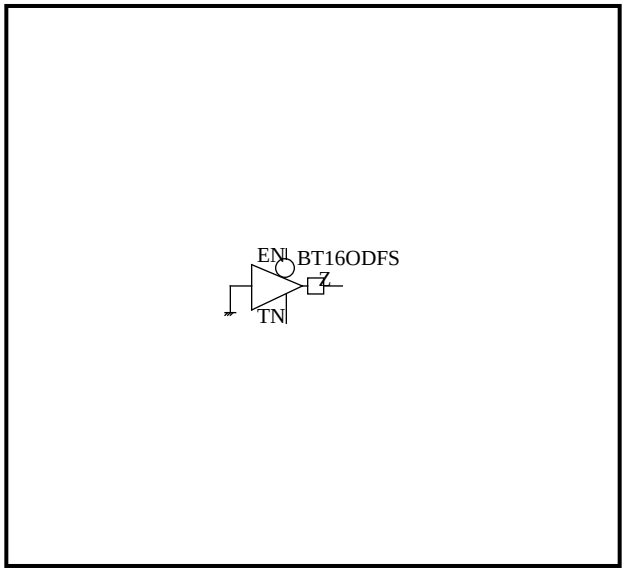
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0018	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	3.20	4.47	5.97	7.36
0.38	3.25	4.52	6.02	7.41
1.00	3.29	4.56	6.06	7.45
3.00	3.36	4.63	6.13	7.52

BT16ODFS	BT16ODFS	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BT16ODFS	TRI-STATE OUTPUT BUFFER (LOW ENABLE) 16mA OPEN DRAIN with FAILSAFE	3	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
EN	TN	Z
L	H	L
H	X	Hz
X	L	Hz

Verilog-HDL DESCRIPTION

```
BT16ODFS  inst(Z,EN,TN);
```

VHDL DESCRIPTION

```
inst:BT16ODFS
   port   map(Z,EN,TN);
```

INPUT LOAD (LU)

PIN NAME	LOAD
EN	0.98
TN	1.00

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.44	0.44	0.44	0.44
0.38	0.52	0.52	0.52	0.52
1.00	0.61	0.61	0.61	0.61
3.00	0.74	0.74	0.74	0.74

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.48

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.75	2.51	3.44	4.33
0.38	1.76	2.52	3.45	4.34
1.00	1.84	2.60	3.53	4.42
3.00	2.09	2.85	3.79	4.68

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.44	0.44	0.44	0.44
0.38	0.52	0.52	0.52	0.52
1.00	0.61	0.61	0.61	0.61
3.00	0.74	0.74	0.74	0.74

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.48

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.75	2.51	3.44	4.33
0.38	1.76	2.52	3.45	4.34
1.00	1.84	2.60	3.53	4.42
3.00	2.09	2.85	3.79	4.68

BT16ODFS BT16ODFS 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.57	0.57	0.57	0.57
0.38	0.60	0.60	0.60	0.60
1.00	0.66	0.66	0.66	0.66
3.00	0.78	0.78	0.78	0.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.48

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.82	2.58	3.51	4.40
0.38	1.87	2.63	3.56	4.46
1.00	1.91	2.67	3.60	4.49
3.00	1.98	2.74	3.67	4.56

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.57	0.57	0.57	0.57
0.38	0.60	0.60	0.60	0.60
1.00	0.66	0.66	0.66	0.66
3.00	0.78	0.78	0.78	0.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	CMOS

SLEW FACTOR

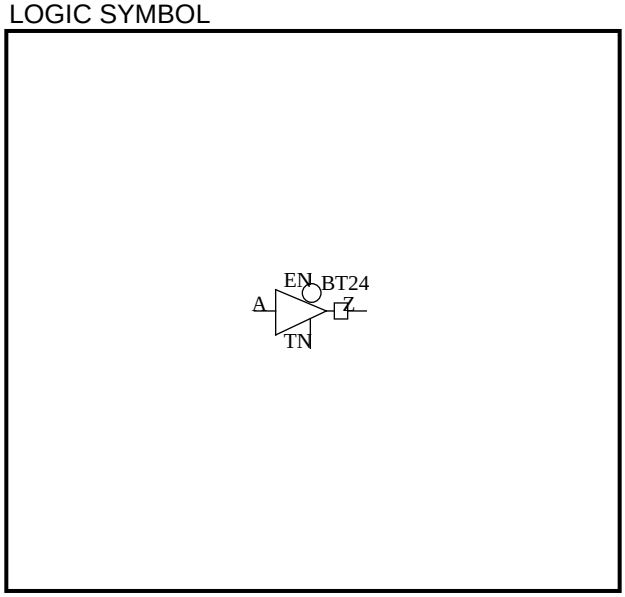
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.48

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.82	2.58	3.51	4.40
0.38	1.87	2.63	3.56	4.46
1.00	1.91	2.67	3.60	4.49
3.00	1.98	2.74	3.67	4.56

BT24	BT24	1/6

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BT24	TRI-STATE OUTPUT BUFFER (LOW ENABLE) 24mA	3	2	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
EN	A	TN	Z
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Verilog-HDL DESCRIPTION

```
BT24  inst(Z,A,EN,TN);
```

VHDL DESCRIPTION

```
inst:BT24
  port  map(Z,A,EN,TN);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	13.11
EN	0.98
TN	1.00

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.88

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.60	2.15	2.75	3.28
0.38	1.68	2.23	2.83	3.36
1.00	1.83	2.39	2.99	3.51
3.00	2.36	2.92	3.52	4.04

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.23	1.73	2.37	2.97
0.38	1.24	1.73	2.36	2.97
1.00	1.28	1.77	2.40	3.00
3.00	1.46	1.94	2.57	3.17

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.88

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.60	2.15	2.75	3.28
0.38	1.68	2.23	2.83	3.36
1.00	1.83	2.39	2.99	3.51
3.00	2.36	2.92	3.52	4.04

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.23	1.73	2.37	2.97
0.38	1.24	1.73	2.36	2.97
1.00	1.28	1.77	2.40	3.00
3.00	1.46	1.94	2.57	3.17

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.66	1.66	1.66	1.66
0.38	1.75	1.75	1.75	1.75
1.00	1.87	1.87	1.87	1.87
3.00	2.09	2.09	2.09	2.09

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.88

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.68	0.68	0.68	0.68
0.38	0.77	0.77	0.77	0.77
1.00	0.89	0.89	0.89	0.89
3.00	1.11	1.11	1.11	1.11

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.88

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.38	2.96	3.57	4.10
0.38	2.39	2.97	3.58	4.11
1.00	2.46	3.04	3.65	4.18
3.00	2.74	3.32	3.93	4.46

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.12	2.67	3.32	3.93
0.38	2.14	2.68	3.34	3.95
1.00	2.20	2.75	3.41	4.02
3.00	2.48	3.03	3.69	4.30

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.66	1.66	1.66	1.66
0.38	1.75	1.75	1.75	1.75
1.00	1.87	1.87	1.87	1.87
3.00	2.09	2.09	2.09	2.09

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.88

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.68	0.68	0.68	0.68
0.38	0.77	0.77	0.77	0.77
1.00	0.89	0.89	0.89	0.89
3.00	1.11	1.11	1.11	1.11

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.88

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.38	2.96	3.57	4.10
0.38	2.39	2.97	3.58	4.11
1.00	2.46	3.04	3.65	4.18
3.00	2.74	3.32	3.93	4.46

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.12	2.67	3.32	3.93
0.38	2.14	2.68	3.34	3.95
1.00	2.20	2.75	3.41	4.02
3.00	2.48	3.03	3.69	4.30

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.80	1.80	1.80	1.80
0.38	1.83	1.83	1.83	1.83
1.00	1.88	1.88	1.88	1.88
3.00	2.01	2.01	2.01	2.01

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.88

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.81	0.81	0.81	0.81
0.38	0.84	0.84	0.84	0.84
1.00	0.90	0.90	0.90	0.90
3.00	1.03	1.03	1.03	1.03

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.88

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.45	3.03	3.64	4.17
0.38	2.51	3.09	3.70	4.23
1.00	2.55	3.13	3.74	4.27
3.00	2.61	3.19	3.80	4.33

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.20	2.75	3.40	4.01
0.38	2.25	2.80	3.45	4.06
1.00	2.29	2.84	3.49	4.10
3.00	2.36	2.91	3.56	4.17

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.80	1.80	1.80	1.80
0.38	1.83	1.83	1.83	1.83
1.00	1.88	1.88	1.88	1.88
3.00	2.01	2.01	2.01	2.01

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.88

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.81	0.81	0.81	0.81
0.38	0.84	0.84	0.84	0.84
1.00	0.90	0.90	0.90	0.90
3.00	1.03	1.03	1.03	1.03

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.88

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.45	3.03	3.64	4.17
0.38	2.51	3.09	3.70	4.23
1.00	2.55	3.13	3.74	4.27
3.00	2.61	3.19	3.80	4.33

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	CMOS

SLEW FACTOR

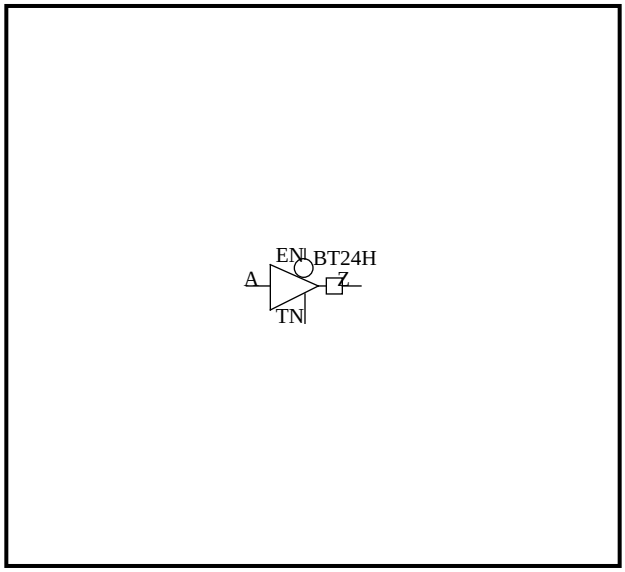
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.20	2.75	3.40	4.01
0.38	2.25	2.80	3.45	4.06
1.00	2.29	2.84	3.49	4.10
3.00	2.36	2.91	3.56	4.17

BT24H	BT24H	1/6

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BT24H	TRI-STATE OUTPUT BUFFER (LOW ENABLE) 24mA HIGH-SPEED	3	2	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
EN	A	TN	Z
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Verilog-HDL DESCRIPTION

```
BT24H  inst(Z,A,EN,TN);
```

VHDL DESCRIPTION

```
inst:BT24H
   port   map(Z,A,EN,TN);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	18.71
EN	0.98
TN	1.00

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.35

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.71	1.08	1.55	2.00
0.38	0.79	1.16	1.63	2.08
1.00	0.94	1.31	1.78	2.23
3.00	1.29	1.67	2.14	2.59

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.85	1.27	1.85	2.42
0.38	0.86	1.27	1.85	2.42
1.00	0.89	1.29	1.87	2.44
3.00	1.02	1.40	1.96	2.52

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.35

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.71	1.08	1.55	2.00
0.38	0.79	1.16	1.63	2.08
1.00	0.94	1.31	1.78	2.23
3.00	1.29	1.67	2.14	2.59

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.85	1.27	1.85	2.42
0.38	0.86	1.27	1.85	2.42
1.00	0.89	1.29	1.87	2.44
3.00	1.02	1.40	1.96	2.52

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.51	1.51	1.51	1.51
0.38	1.60	1.60	1.60	1.60
1.00	1.73	1.73	1.73	1.73
3.00	2.00	2.00	2.00	2.00

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.35

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.92	0.92	0.92	0.92
0.38	1.01	1.01	1.01	1.01
1.00	1.15	1.15	1.15	1.15
3.00	1.41	1.41	1.41	1.41

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.35

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.66	2.06	2.54	3.00
0.38	1.68	2.08	2.56	3.01
1.00	1.74	2.14	2.62	3.07
3.00	2.02	2.42	2.90	3.36

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.99	2.45	3.05	3.63
0.38	2.01	2.47	3.06	3.65
1.00	2.07	2.53	3.13	3.71
3.00	2.35	2.81	3.41	3.99

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.51	1.51	1.51	1.51
0.38	1.60	1.60	1.60	1.60
1.00	1.73	1.73	1.73	1.73
3.00	2.00	2.00	2.00	2.00

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.35

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.92	0.92	0.92	0.92
0.38	1.01	1.01	1.01	1.01
1.00	1.15	1.15	1.15	1.15
3.00	1.41	1.41	1.41	1.41

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.35

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.66	2.06	2.54	3.00
0.38	1.68	2.08	2.56	3.01
1.00	1.74	2.14	2.62	3.07
3.00	2.02	2.42	2.90	3.36

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.99	2.45	3.05	3.63
0.38	2.01	2.47	3.06	3.65
1.00	2.07	2.53	3.13	3.71
3.00	2.35	2.81	3.41	3.99

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.64	1.64	1.64	1.64
0.38	1.68	1.68	1.68	1.68
1.00	1.73	1.73	1.73	1.73
3.00	1.86	1.86	1.86	1.86

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.35

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.06	1.06	1.06	1.06
0.38	1.09	1.09	1.09	1.09
1.00	1.15	1.15	1.15	1.15
3.00	1.27	1.27	1.27	1.27

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.35

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.74	2.14	2.62	3.07
0.38	1.79	2.19	2.67	3.13
1.00	1.83	2.23	2.71	3.17
3.00	1.90	2.30	2.78	3.23

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.07	2.53	3.13	3.71
0.38	2.12	2.58	3.18	3.76
1.00	2.16	2.62	3.22	3.80
3.00	2.23	2.69	3.29	3.87

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.64	1.64	1.64	1.64
0.38	1.68	1.68	1.68	1.68
1.00	1.73	1.73	1.73	1.73
3.00	1.86	1.86	1.86	1.86

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.35

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.06	1.06	1.06	1.06
0.38	1.09	1.09	1.09	1.09
1.00	1.15	1.15	1.15	1.15
3.00	1.27	1.27	1.27	1.27

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.35

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.74	2.14	2.62	3.07
0.38	1.79	2.19	2.67	3.13
1.00	1.83	2.23	2.71	3.17
3.00	1.90	2.30	2.78	3.23

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	CMOS

SLEW FACTOR

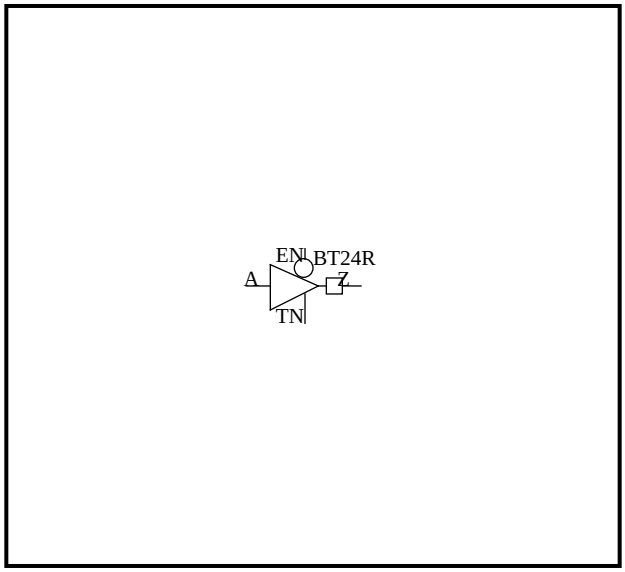
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.31

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.07	2.53	3.13	3.71
0.38	2.12	2.58	3.18	3.76
1.00	2.16	2.62	3.22	3.80
3.00	2.23	2.69	3.29	3.87

BT24R	BT24R	1/6

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BT24R	TRI-STATE OUTPUT BUFFER (LOW ENABLE) 24mA SLEW RATE CONTROL	3	2	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT			OUTPUT
EN	A	TN	Z
L	L	H	L
L	H	H	H
H	X	X	Hz
X	X	L	Hz

Verilog-HDL DESCRIPTION

```
BT24R  inst(Z,A,EN,TN);
```

VHDL DESCRIPTION

```
inst:BT24R
   port   map(Z,A,EN,TN);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	15.44
EN	0.98
TN	1.00

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0011	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.11	2.84	3.65	4.38
0.38	2.23	2.96	3.77	4.49
1.00	2.42	3.15	3.96	4.68
3.00	3.06	3.79	4.60	5.32

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	1.14

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.57	3.52	4.61	5.59
0.38	2.62	3.58	4.66	5.65
1.00	2.74	3.69	4.78	5.76
3.00	3.13	4.09	5.17	6.15

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0011	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.11	2.84	3.65	4.38
0.38	2.23	2.96	3.77	4.49
1.00	2.42	3.15	3.96	4.68
3.00	3.06	3.79	4.60	5.32

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	1.14

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.57	3.52	4.61	5.59
0.38	2.62	3.58	4.66	5.65
1.00	2.74	3.69	4.78	5.76
3.00	3.13	4.09	5.17	6.15

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	1.14

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.70	1.70	1.70	1.70
0.38	1.80	1.80	1.80	1.80
1.00	1.93	1.93	1.93	1.93
3.00	2.16	2.16	2.16	2.16

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0011	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.82	0.82	0.82	0.82
0.38	0.91	0.91	0.91	0.91
1.00	1.03	1.03	1.03	1.03
3.00	1.24	1.24	1.24	1.24

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0011	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	3.11	3.87	4.70	5.42
0.38	3.13	3.89	4.71	5.43
1.00	3.19	3.96	4.78	5.50
3.00	3.48	4.24	5.06	5.79

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	1.14

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	3.46	4.42	5.50	6.48
0.38	3.48	4.43	5.52	6.50
1.00	3.54	4.50	5.58	6.56
3.00	3.82	4.78	5.86	6.84

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	1.14

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.70	1.70	1.70	1.70
0.38	1.80	1.80	1.80	1.80
1.00	1.93	1.93	1.93	1.93
3.00	2.16	2.16	2.16	2.16

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0011	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.82	0.82	0.82	0.82
0.38	0.91	0.91	0.91	0.91
1.00	1.03	1.03	1.03	1.03
3.00	1.24	1.24	1.24	1.24

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0011	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	3.11	3.87	4.70	5.42
0.38	3.13	3.89	4.71	5.43
1.00	3.19	3.96	4.78	5.50
3.00	3.48	4.24	5.06	5.79

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	1.14

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	3.46	4.42	5.50	6.48
0.38	3.48	4.43	5.52	6.50
1.00	3.54	4.50	5.58	6.56
3.00	3.82	4.78	5.86	6.84

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	1.14

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.84	1.84	1.84	1.84
0.38	1.88	1.88	1.88	1.88
1.00	1.94	1.94	1.94	1.94
3.00	2.09	2.09	2.09	2.09

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0011	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.96	0.96	0.96	0.96
0.38	0.99	0.99	0.99	0.99
1.00	1.05	1.05	1.05	1.05
3.00	1.17	1.17	1.17	1.17

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0011	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	3.19	3.95	4.77	5.49
0.38	3.24	4.00	4.82	5.55
1.00	3.28	4.04	4.86	5.59
3.00	3.35	4.11	4.93	5.66

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	1.14

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	3.54	4.49	5.58	6.56
0.38	3.59	4.54	5.63	6.61
1.00	3.63	4.59	5.67	6.65
3.00	3.70	4.65	5.74	6.72

BT24R | BT24R | 6/6

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	1-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	1.14

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.84	1.84	1.84	1.84
0.38	1.88	1.88	1.88	1.88
1.00	1.94	1.94	1.94	1.94
3.00	2.09	2.09	2.09	2.09

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0011	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.96	0.96	0.96	0.96
0.38	0.99	0.99	0.99	0.99
1.00	1.05	1.05	1.05	1.05
3.00	1.17	1.17	1.17	1.17

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-1	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0011	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	3.19	3.95	4.77	5.49
0.38	3.24	4.00	4.82	5.55
1.00	3.28	4.04	4.86	5.59
3.00	3.35	4.11	4.93	5.66

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	1.14

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	3.54	4.49	5.58	6.56
0.38	3.59	4.54	5.63	6.61
1.00	3.63	4.59	5.67	6.65
3.00	3.70	4.65	5.74	6.72

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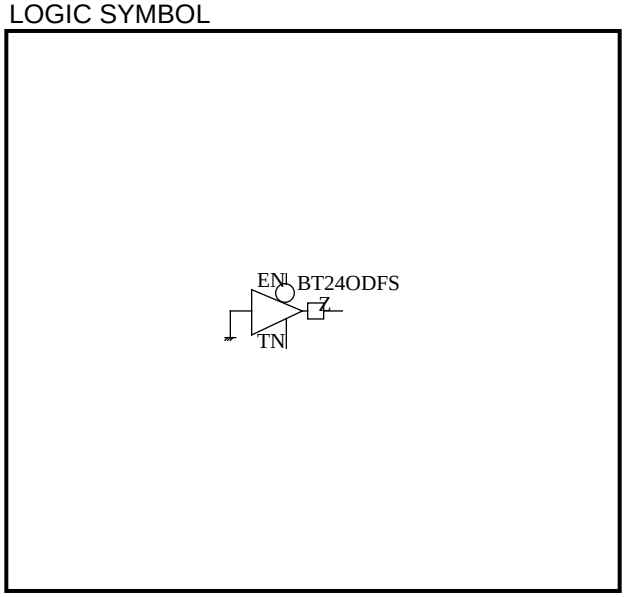
BT24ODFS	BT24ODFS	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BT24ODFS	TRI-STATE OUTPUT BUFFER (LOW ENABLE) 24mA OPEN DRAIN with FAILSAFE	3	2	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
EN	TN	Z
L	H	L
H	X	Hz
X	L	Hz

Verilog-HDL DESCRIPTION

```
BT24ODFS  inst(Z,EN,TN);
```

VHDL DESCRIPTION

```
inst:BT24ODFS
   port   map(Z,EN,TN);
```

INPUT LOAD (LU)

PIN NAME	LOAD
EN	0.98
TN	1.00

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.62	0.62	0.62	0.62
0.38	0.71	0.71	0.71	0.71
1.00	0.83	0.83	0.83	0.83
3.00	1.03	1.03	1.03	1.03

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.48

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.96	2.53	3.19	3.80
0.38	1.98	2.54	3.20	3.81
1.00	2.05	2.61	3.27	3.88
3.00	2.33	2.89	3.55	4.16

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.62	0.62	0.62	0.62
0.38	0.71	0.71	0.71	0.71
1.00	0.83	0.83	0.83	0.83
3.00	1.03	1.03	1.03	1.03

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.48

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.96	2.53	3.19	3.80
0.38	1.98	2.54	3.20	3.81
1.00	2.05	2.61	3.27	3.88
3.00	2.33	2.89	3.55	4.16

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.75	0.75	0.75	0.75
0.38	0.79	0.79	0.79	0.79
1.00	0.84	0.84	0.84	0.84
3.00	0.97	0.97	0.97	0.97

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.48

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.04	2.60	3.26	3.87
0.38	2.09	2.66	3.31	3.93
1.00	2.13	2.70	3.35	3.96
3.00	2.20	2.76	3.42	4.03

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	0-Z	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0000	0.00

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.75	0.75	0.75	0.75
0.38	0.79	0.79	0.79	0.79
1.00	0.84	0.84	0.84	0.84
3.00	0.97	0.97	0.97	0.97

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
TN->Z	---	Z-0	CMOS

SLEW FACTOR

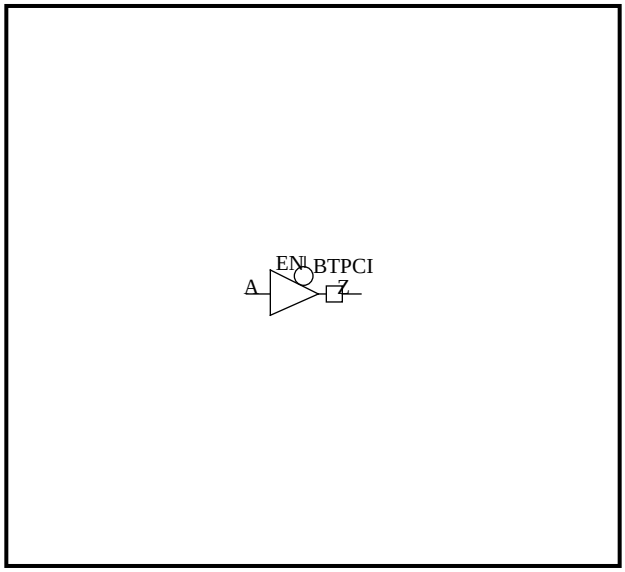
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.48

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.04	2.60	3.26	3.87
0.38	2.09	2.66	3.31	3.93
1.00	2.13	2.70	3.35	3.96
3.00	2.20	2.76	3.42	4.03

BTPCI	BTPCI	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BTPCI	PCI (Peripheral Component Interconnect) BUS TRI-STATE OUTPUT BUFFER (LOW ENABLE)	0	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT
EN	A	Z
L	L	L
L	H	H
H	X	Hz
X	X	Hz

Verilog-HDL DESCRIPTION

```
BTPCI  inst(Z,A,EN);
```

VHDL DESCRIPTION

```
inst:BTPCI
   port   map(Z,A,EN);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	3.92
EN	3.97

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BTPCI BTPCI 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0016	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.84	2.77	3.84	4.84
0.38	1.93	2.86	3.93	4.93
1.00	2.10	3.02	4.09	5.09
3.00	2.64	3.57	4.65	5.65

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.75

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.71	2.51	3.49	4.41
0.38	1.74	2.54	3.51	4.43
1.00	1.80	2.59	3.57	4.49
3.00	2.03	2.84	3.82	4.74

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	1-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.75

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.01	2.01	2.01	2.01
0.38	2.08	2.08	2.08	2.08
1.00	2.15	2.15	2.15	2.15
3.00	2.28	2.28	2.28	2.28

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	0-Z	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0016	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.15	0.15	0.15	0.15
0.38	0.24	0.24	0.24	0.24
1.00	0.37	0.37	0.37	0.37
3.00	0.56	0.56	0.56	0.56

BTPCI BTPCI 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-1	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0016	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.88	2.84	3.93	4.93
0.38	1.92	2.88	3.97	4.97
1.00	1.98	2.94	4.03	5.03
3.00	2.11	3.07	4.16	5.16

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
EN->Z	---	Z-0	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.75

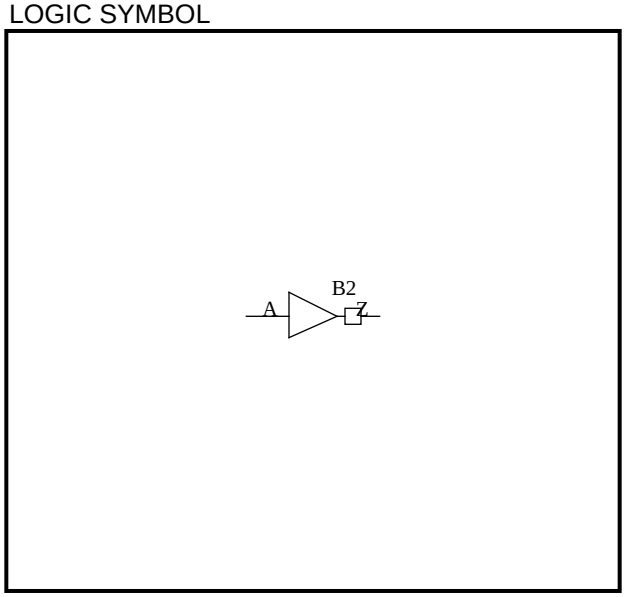
PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.62	2.49	3.49	4.41
0.38	1.62	2.49	3.49	4.41
1.00	1.64	2.50	3.50	4.42
3.00	1.75	2.61	3.61	4.54

Rev.1.01.08

B2	B2	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
B2	OUTPUT BUFFER (2mA DRIVE)	0	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	L
H	H

Verilog-HDL DESCRIPTION

```
B2  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:B2
   port   map(Z,A);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	5.21

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B2 B2 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0002	0.90

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	1.51	1.97	2.85	4.57
0.38	1.59	2.05	2.94	4.66
1.00	1.76	2.22	3.10	4.82
3.00	2.25	2.72	3.60	5.33

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0003	0.93

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	1.79	2.48	3.83	6.52
0.38	1.79	2.47	3.83	6.52
1.00	1.83	2.51	3.87	6.56
3.00	2.00	2.69	4.04	6.74

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0002	0.90

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	1.51	1.97	2.85	4.57
0.38	1.59	2.05	2.94	4.66
1.00	1.76	2.22	3.10	4.82
3.00	2.25	2.72	3.60	5.33

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

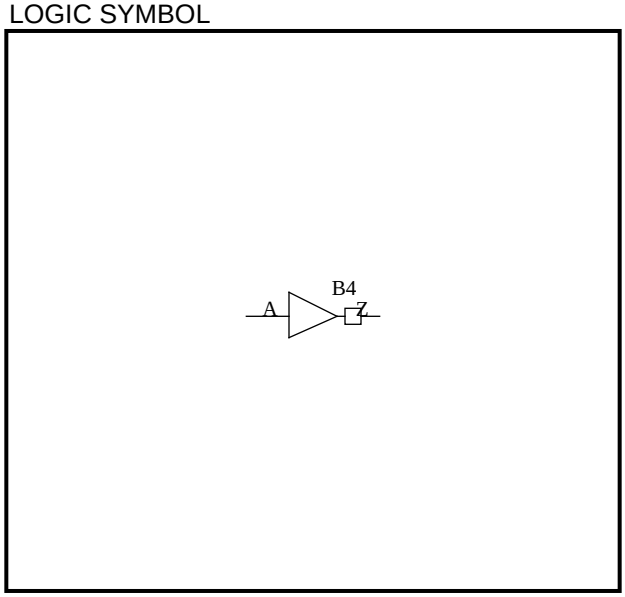
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0003	0.93

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	5.00	10.00	20.00	40.00
0.01	1.79	2.48	3.83	6.52
0.38	1.79	2.47	3.83	6.52
1.00	1.83	2.51	3.87	6.56
3.00	2.00	2.69	4.04	6.74

B4	B4	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
B4	OUTPUT BUFFER 4mA	0	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	L
H	H

Verilog-HDL DESCRIPTION

```
B4  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:B4
   port   map(Z,A);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	5.21

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B4 B4 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0001	0.77

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.75	2.88	4.48	6.57
0.38	1.83	2.96	4.56	6.65
1.00	1.99	3.13	4.72	6.81
3.00	2.52	3.66	5.25	7.35

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0001	0.61

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.74	3.16	5.25	8.01
0.38	1.74	3.16	5.24	8.01
1.00	1.78	3.20	5.28	8.04
3.00	1.95	3.37	5.46	8.22

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0001	0.77

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.75	2.88	4.48	6.57
0.38	1.83	2.96	4.56	6.65
1.00	1.99	3.13	4.72	6.81
3.00	2.52	3.66	5.25	7.35

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

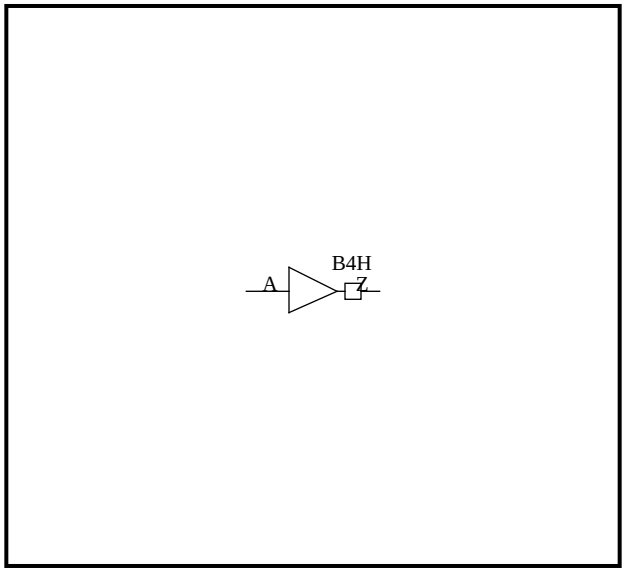
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0001	0.61

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.74	3.16	5.25	8.01
0.38	1.74	3.16	5.24	8.01
1.00	1.78	3.20	5.28	8.04
3.00	1.95	3.37	5.46	8.22

B4H	B4H	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
B4H	OUTPUT BUFFER 4mA HIGH-SPEED	0	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	L
H	H

Verilog-HDL DESCRIPTION

```
B4H  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:B4H
   port   map(Z,A);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	9.56

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B4H | B4H | 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0047	0.46

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.97	2.02	3.58	5.65
0.38	1.05	2.10	3.66	5.74
1.00	1.17	2.21	3.77	5.85
3.00	1.41	2.46	4.02	6.10

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.47

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.23	2.62	4.69	7.45
0.38	1.24	2.62	4.69	7.45
1.00	1.26	2.64	4.71	7.47
3.00	1.31	2.68	4.75	7.50

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0047	0.46

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.97	2.02	3.58	5.65
0.38	1.05	2.10	3.66	5.74
1.00	1.17	2.21	3.77	5.85
3.00	1.41	2.46	4.02	6.10

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

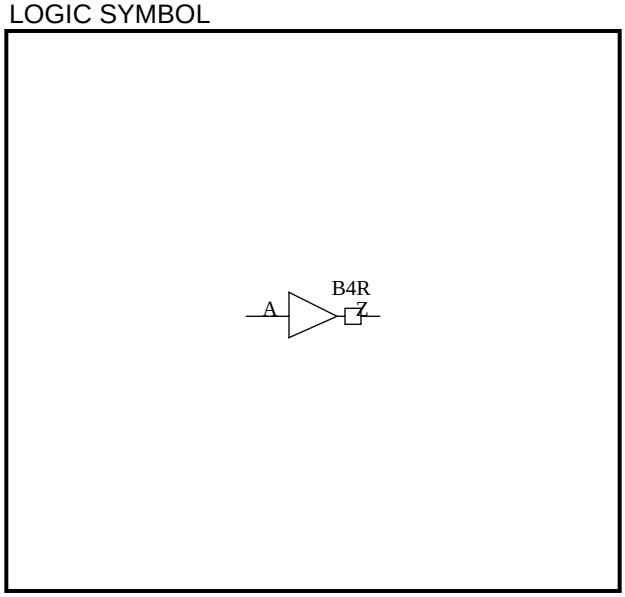
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0050	0.47

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.23	2.62	4.69	7.45
0.38	1.24	2.62	4.69	7.45
1.00	1.26	2.64	4.71	7.47
3.00	1.31	2.68	4.75	7.50

B4R	B4R	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
B4R	OUTPUT BUFFER 4mA SLEW RATE CONTROL	0	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	L
H	H

Verilog-HDL DESCRIPTION

```
B4R  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:B4R
   port   map(Z,A);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	6.50

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B4R | B4R | 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0057	1.42

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.36	3.92	6.05	8.65
0.38	2.45	4.02	6.15	8.76
1.00	2.63	4.20	6.33	8.93
3.00	3.25	4.82	6.95	9.56

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0065	1.67

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	3.35	5.58	8.63	12.38
0.38	3.39	5.62	8.67	12.42
1.00	3.53	5.77	8.82	12.56
3.00	3.99	6.23	9.28	13.02

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0057	1.42

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.36	3.92	6.05	8.65
0.38	2.45	4.02	6.15	8.76
1.00	2.63	4.20	6.33	8.93
3.00	3.25	4.82	6.95	9.56

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

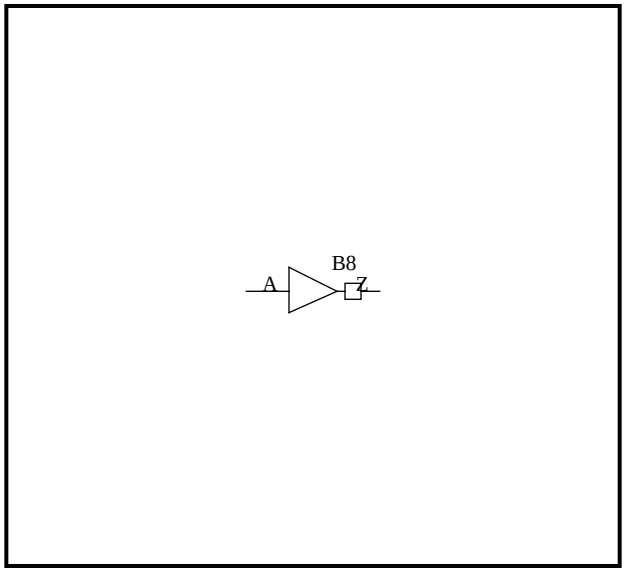
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0065	1.67

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	3.35	5.58	8.63	12.38
0.38	3.39	5.62	8.67	12.42
1.00	3.53	5.77	8.82	12.56
3.00	3.99	6.23	9.28	13.02

B8	B8	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
B8	OUTPUT BUFFER 8mA	0	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	L
H	H

Verilog-HDL DESCRIPTION

```
B8  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:B8
   port   map(Z,A);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	5.21

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B8	B8	2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0001	0.98

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.85	2.60	3.52	4.65
0.38	1.93	2.68	3.60	4.73
1.00	2.09	2.84	3.76	4.89
3.00	2.63	3.38	4.30	5.43

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0001	0.59

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.53	2.31	3.40	4.80
0.38	1.53	2.31	3.40	4.80
1.00	1.57	2.35	3.43	4.83
3.00	1.75	2.52	3.60	5.01

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0001	0.98

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.85	2.60	3.52	4.65
0.38	1.93	2.68	3.60	4.73
1.00	2.09	2.84	3.76	4.89
3.00	2.63	3.38	4.30	5.43

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

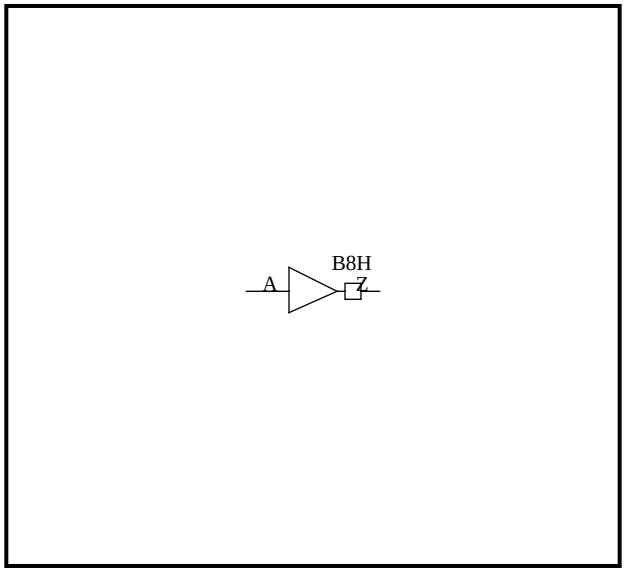
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0001	0.59

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.53	2.31	3.40	4.80
0.38	1.53	2.31	3.40	4.80
1.00	1.57	2.35	3.43	4.83
3.00	1.75	2.52	3.60	5.01

B8H	B8H	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
B8H	OUTPUT BUFFER 8mA HIGH-SPEED	0	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	L
H	H

Verilog-HDL DESCRIPTION

```
B8H  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:B8H
   port   map(Z,A);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	7.94

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B8H | B8H | 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0024	0.40

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.90	1.47	2.27	3.32
0.38	0.99	1.55	2.35	3.40
1.00	1.13	1.70	2.50	3.55
3.00	1.49	2.05	2.85	3.90

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.38

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.09	1.80	2.83	4.21
0.38	1.10	1.81	2.84	4.22
1.00	1.13	1.83	2.86	4.23
3.00	1.24	1.92	2.94	4.30

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0024	0.40

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	0.90	1.47	2.27	3.32
0.38	0.99	1.55	2.35	3.40
1.00	1.13	1.70	2.50	3.55
3.00	1.49	2.05	2.85	3.90

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

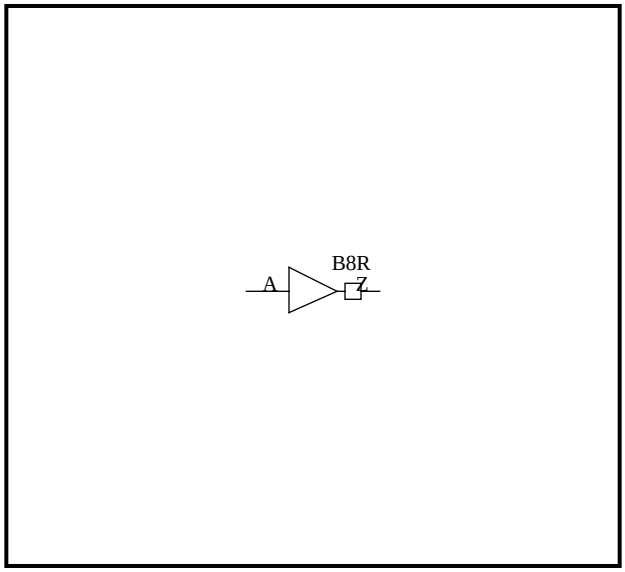
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.38

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	1.09	1.80	2.83	4.21
0.38	1.10	1.81	2.84	4.22
1.00	1.13	1.83	2.86	4.23
3.00	1.24	1.92	2.94	4.30

B8R	B8R	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
B8R	OUTPUT BUFFER 8mA SLEW RATE CONTROL	0	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	L
H	H

Verilog-HDL DESCRIPTION

```
B8R  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:B8R
   port   map(Z,A);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	6.50

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B8R | B8R | 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0032	1.25

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.42	3.41	4.67	6.22
0.38	2.52	3.52	4.78	6.32
1.00	2.70	3.70	4.96	6.51
3.00	3.31	4.31	5.57	7.12

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0035	1.42

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	3.16	4.55	6.30	8.47
0.38	3.21	4.59	6.35	8.51
1.00	3.34	4.72	6.47	8.64
3.00	3.77	5.15	6.91	9.07

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0032	1.25

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	2.42	3.41	4.67	6.22
0.38	2.52	3.52	4.78	6.32
1.00	2.70	3.70	4.96	6.51
3.00	3.31	4.31	5.57	7.12

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

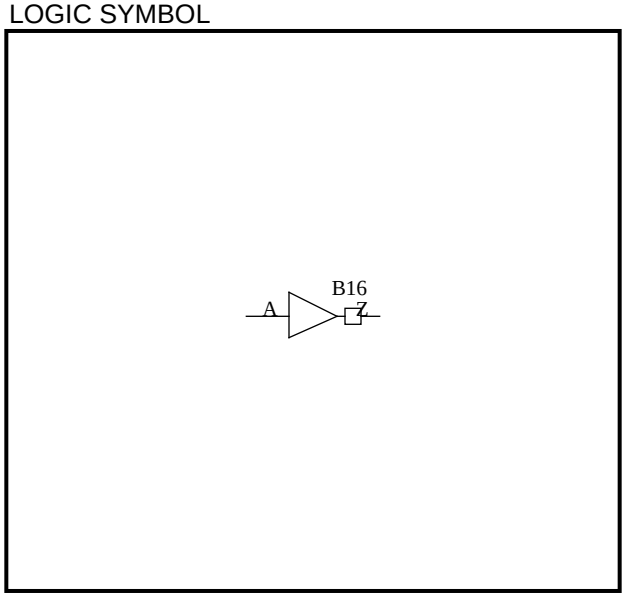
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0035	1.42

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	10.00	30.00	60.00	100.00
0.01	3.16	4.55	6.30	8.47
0.38	3.21	4.59	6.35	8.51
1.00	3.34	4.72	6.47	8.64
3.00	3.77	5.15	6.91	9.07

B16	B16	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
B16	OUTPUT BUFFER 16mA	0	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	L
H	H

Verilog-HDL DESCRIPTION

```
B16  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:B16
   port   map(Z,A);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	6.66

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B16 B16 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.88

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.73	2.45	3.25	3.98
0.38	1.80	2.52	3.33	4.06
1.00	1.95	2.67	3.48	4.21
3.00	2.47	3.20	4.00	4.73

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.48

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.30	2.00	2.92	3.81
0.38	1.30	2.01	2.92	3.81
1.00	1.34	2.04	2.95	3.84
3.00	1.52	2.22	3.13	4.02

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.88

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.73	2.45	3.25	3.98
0.38	1.80	2.52	3.33	4.06
1.00	1.95	2.67	3.48	4.21
3.00	2.47	3.20	4.00	4.73

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

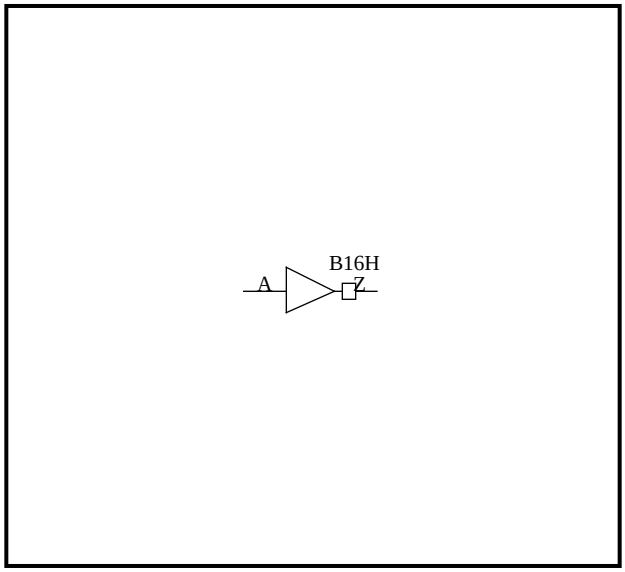
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.48

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.30	2.00	2.92	3.81
0.38	1.30	2.01	2.92	3.81
1.00	1.34	2.04	2.95	3.84
3.00	1.52	2.22	3.13	4.02

B16H	B16H	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
B16H	OUTPUT BUFFER 16mA HIGH-SPEED	0	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	L
H	H

Verilog-HDL DESCRIPTION

```
B16H  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:B16H
   port   map(Z,A);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	9.56

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B16H B16H 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.33

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.78	1.31	1.99	2.65
0.38	0.87	1.39	2.07	2.74
1.00	1.01	1.54	2.22	2.88
3.00	1.36	1.89	2.58	3.24

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.33

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.88	1.50	2.37	3.23
0.38	0.90	1.51	2.37	3.23
1.00	0.93	1.54	2.40	3.26
3.00	1.06	1.65	2.49	3.34

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.33

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.78	1.31	1.99	2.65
0.38	0.87	1.39	2.07	2.74
1.00	1.01	1.54	2.22	2.88
3.00	1.36	1.89	2.58	3.24

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.33

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.88	1.50	2.37	3.23
0.38	0.90	1.51	2.37	3.23
1.00	0.93	1.54	2.40	3.26
3.00	1.06	1.65	2.49	3.34

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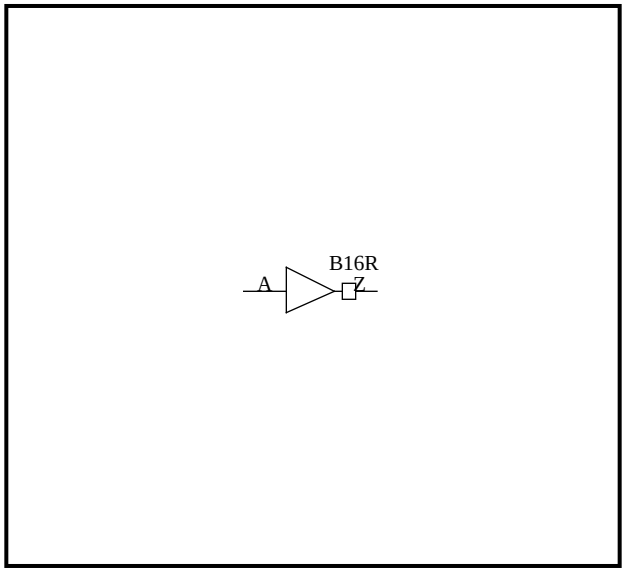
B16R	B16R	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
B16R	OUTPUT BUFFER 16mA SLEW RATE CONTROL	0	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	L
H	H

Verilog-HDL DESCRIPTION

```
B16R  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:B16R
   port   map(Z,A);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	7.85

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B16R | B16R | 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0016	1.15

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.25	3.22	4.32	5.33
0.38	2.37	3.34	4.44	5.45
1.00	2.57	3.54	4.64	5.65
3.00	3.24	4.21	5.31	6.32

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0018	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.75	4.00	5.50	6.89
0.38	2.81	4.06	5.56	6.94
1.00	2.91	4.17	5.67	7.06
3.00	3.27	4.54	6.04	7.43

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0016	1.15

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.25	3.22	4.32	5.33
0.38	2.37	3.34	4.44	5.45
1.00	2.57	3.54	4.64	5.65
3.00	3.24	4.21	5.31	6.32

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

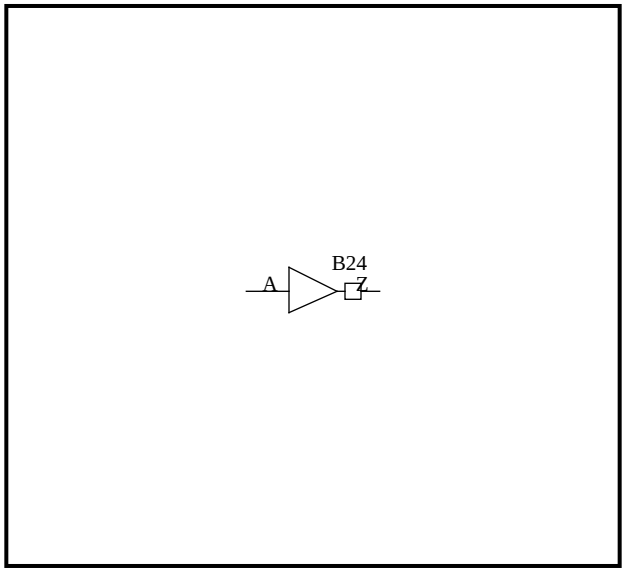
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0018	1.13

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.75	4.00	5.50	6.89
0.38	2.81	4.06	5.56	6.94
1.00	2.91	4.17	5.67	7.06
3.00	3.27	4.54	6.04	7.43

B24	B24	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
B24	OUTPUT BUFFER 24mA	0	2	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	L
H	H

Verilog-HDL DESCRIPTION

```
B24  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:B24
   port   map(Z,A);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	12.02

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B24 B24 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.88

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.60	2.16	2.76	3.28
0.38	1.68	2.24	2.84	3.36
1.00	1.83	2.39	2.99	3.51
3.00	2.36	2.92	3.52	4.04

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.22	1.72	2.35	2.95
0.38	1.23	1.72	2.35	2.96
1.00	1.27	1.76	2.39	2.99
3.00	1.45	1.94	2.56	3.16

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.88

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.60	2.16	2.76	3.28
0.38	1.68	2.24	2.84	3.36
1.00	1.83	2.39	2.99	3.51
3.00	2.36	2.92	3.52	4.04

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

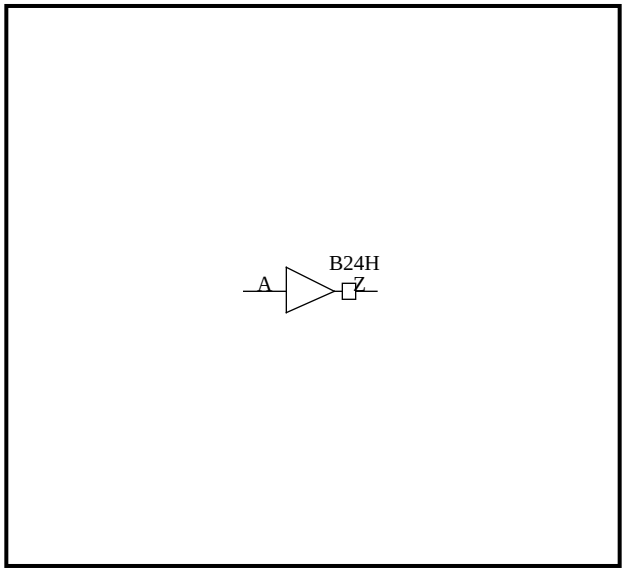
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.50

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.22	1.72	2.35	2.95
0.38	1.23	1.72	2.35	2.96
1.00	1.27	1.76	2.39	2.99
3.00	1.45	1.94	2.56	3.16

B24H	B24H	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
B24H	OUTPUT BUFFER 24mA HIGH-SPEED	0	2	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	L
H	H

Verilog-HDL DESCRIPTION

```
B24H  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:B24H
   port   map(Z,A);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	17.61

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B24H | B24H | 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.35

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.71	1.08	1.55	2.00
0.38	0.79	1.16	1.63	2.08
1.00	0.94	1.31	1.78	2.23
3.00	1.29	1.67	2.14	2.59

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.38

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.83	1.24	1.82	2.39
0.38	0.84	1.25	1.83	2.40
1.00	0.88	1.28	1.85	2.42
3.00	1.01	1.39	1.96	2.52

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.35

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.71	1.08	1.55	2.00
0.38	0.79	1.16	1.63	2.08
1.00	0.94	1.31	1.78	2.23
3.00	1.29	1.67	2.14	2.59

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

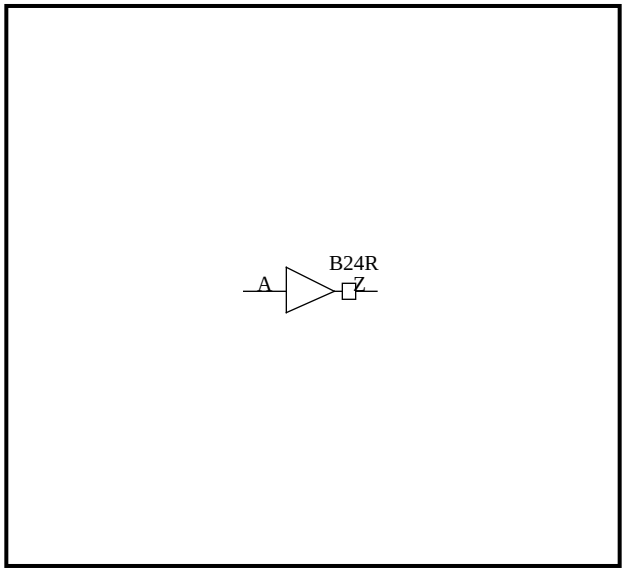
PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0008	0.38

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	0.83	1.24	1.82	2.39
0.38	0.84	1.25	1.83	2.40
1.00	0.88	1.28	1.85	2.42
3.00	1.01	1.39	1.96	2.52

B24R	B24R	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
B24R	OUTPUT BUFFER 24mA SLEW RATE CONTROL	0	2	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	L
H	H

Verilog-HDL DESCRIPTION

```
B24R  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:B24R
   port   map(Z,A);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	14.33

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B24R | B24R | 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0011	1.12

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.09	2.82	3.63	4.35
0.38	2.21	2.93	3.74	4.46
1.00	2.40	3.13	3.94	4.66
3.00	3.05	3.78	4.58	5.31

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	CMOS

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	1.14

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.56	3.51	4.60	5.58
0.38	2.61	3.56	4.65	5.63
1.00	2.73	3.68	4.77	5.75
3.00	3.12	4.08	5.16	6.14

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0011	1.12

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.09	2.82	3.63	4.35
0.38	2.21	2.93	3.74	4.46
1.00	2.40	3.13	3.94	4.66
3.00	3.05	3.78	4.58	5.31

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	1.14

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	2.56	3.51	4.60	5.58
0.38	2.61	3.56	4.65	5.63
1.00	2.73	3.68	4.77	5.75
3.00	3.12	4.08	5.16	6.14

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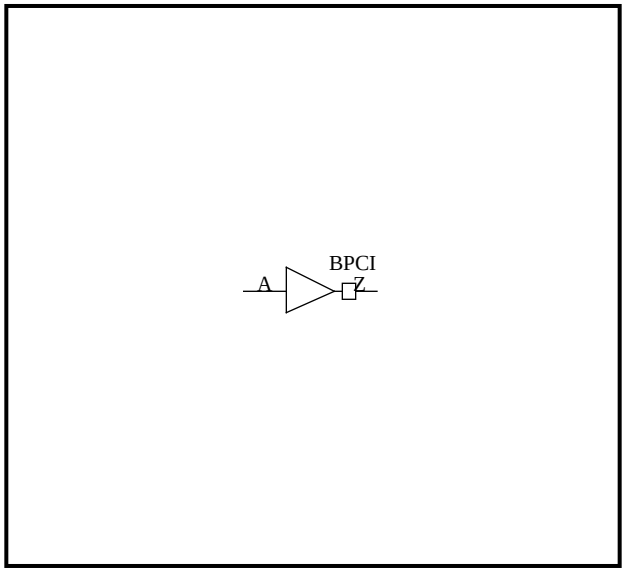
BPCI	BPCI	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
BPCI	PCI (Peripheral Component Interconnect) BUS OUTPUT BUFFER	0	1	VDD=3.3V, Ta=25°C, Typ.

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	L
H	H

Verilog-HDL DESCRIPTION

```
BPCI  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:BPCI
   port   map(Z,A);
```

INPUT LOAD (LU)

PIN NAME	LOAD
A	3.92

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BPCI

BPCI

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0016	0.96

PATH DELAY (ns)				
LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01	1.84	2.77	3.84	4.84
0.38	1.93	2.86	3.93	4.93
1.00	2.10	3.02	4.09	5.09
3.00	2.64	3.57	4.65	5.65

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	TTL

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.75

ns)

LOAD (pF) SLEW (ns)	15.00	50.00	100.00	150.00
0.01				
0.38				
1.00				
3.00				3820

1.(1.38)Tj 140 0 0 4 5343.277051.76 Tm 2/20

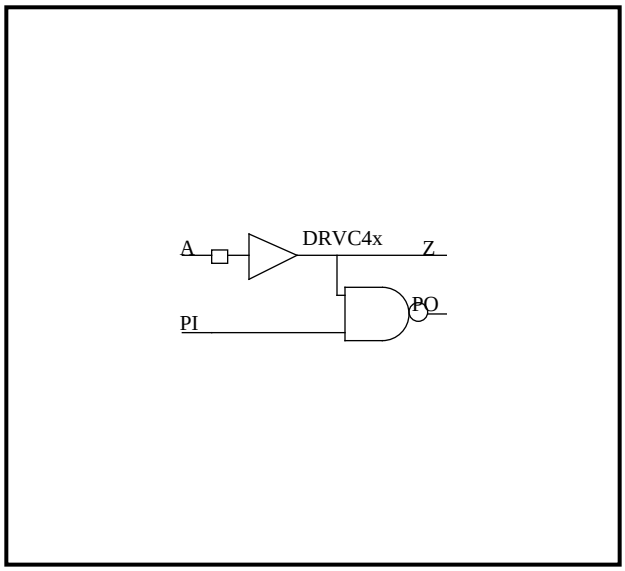
DRVC4x	DRVC4x	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
DRVC4x	CLOCK DRIVER with CMOS LEVEL INPUT BUFFER (equal 4mA DRIVER)	1	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN	PULL-UP
DRVC4	DRVC4D	DRVC4U

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	L	H
L	H	L	H
H	L	H	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
DRVC4x  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:DRVC4x
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	17240.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	537.0	34.3

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CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0061	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	266.67	800.00	1600.00	2666.67
0.01	0.77	1.90	3.59	5.85
0.38	0.83	1.95	3.65	5.90
1.00	0.89	2.02	3.71	5.97
3.00	1.01	2.14	3.83	6.08

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0052	0.06

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	266.67	800.00	1600.00	2666.67
0.01	1.04	2.64	5.00	7.61
0.38	1.07	2.67	5.04	7.69
1.00	1.15	2.75	5.12	7.83
3.00	1.30	2.91	5.29	8.15

DRVC4x | DRVC4x | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

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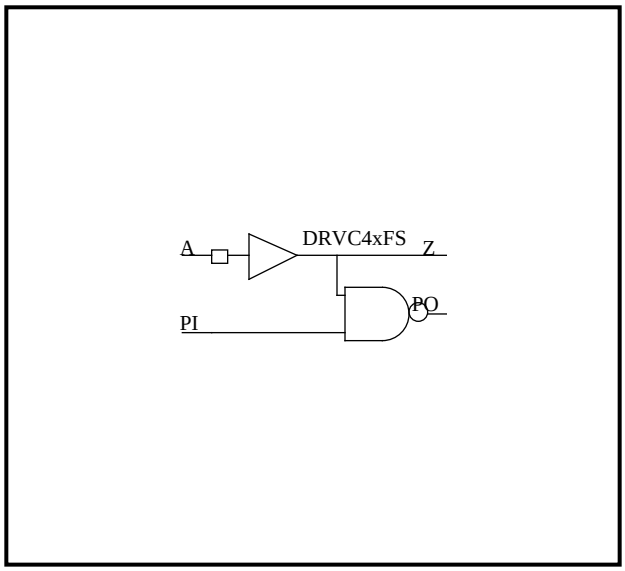
DRVC4xFS			DRVC4xFS	1/3
CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
DRVC4xFS	CLOCK DRIVER with CMOS LEVEL INPUT BUFFER (equal 4mA DRIVER) with FAILSAFE	1	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN
DRVC4FS	DRVC4DFS

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	L	H
L	H	L	H
H	L	H	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
DRVC4xFS  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:DRVC4xFS
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	17240.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	537.0	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0061	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	266.67	800.00	1600.00	2666.67
0.01	0.77	1.90	3.59	5.85
0.38	0.83	1.95	3.65	5.90
1.00	0.89	2.02	3.71	5.97
3.00	1.01	2.14	3.83	6.08

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0052	0.06

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	266.67	800.00	1600.00	2666.67
0.01	1.04	2.64	5.00	7.61
0.38	1.07	2.67	5.04	7.69
1.00	1.15	2.75	5.12	7.83
3.00	1.30	2.91	5.29	8.15

DRVC4xFS | DRVC4xFS | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

Rev.1.01.10

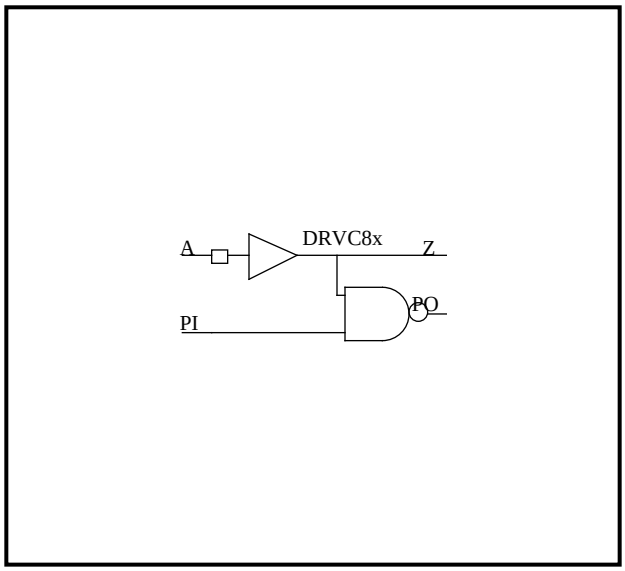
DRVC8x	DRVC8x	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
DRVC8x	CLOCK DRIVER with CMOS LEVEL INPUT BUFFER (equal 8mA DRIVER)	1	2	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN	PULL-UP
DRVC8	DRVC8D	DRVC8U

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	L	H
L	H	L	H
H	L	H	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
DRVC8x  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:DRVC8x
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	17240.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	1171.4	34.3

Rev.1.01.10

DRVC8x | DRVC8x | 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0024	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	266.67	800.00	1600.00	2666.67
0.01	0.61	1.06	1.73	2.62
0.38	0.67	1.12	1.79	2.67
1.00	0.76	1.21	1.88	2.77
3.00	0.93	1.39	2.06	2.95

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.25

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	266.67	800.00	1600.00	2666.67
0.01	0.89	1.67	2.83	4.37
0.38	0.92	1.70	2.86	4.40
1.00	1.01	1.79	2.95	4.49
3.00	1.23	2.01	3.17	4.71

Rev.1.01.10

DRVC8x | DRVC8x | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

Rev.1.01.10

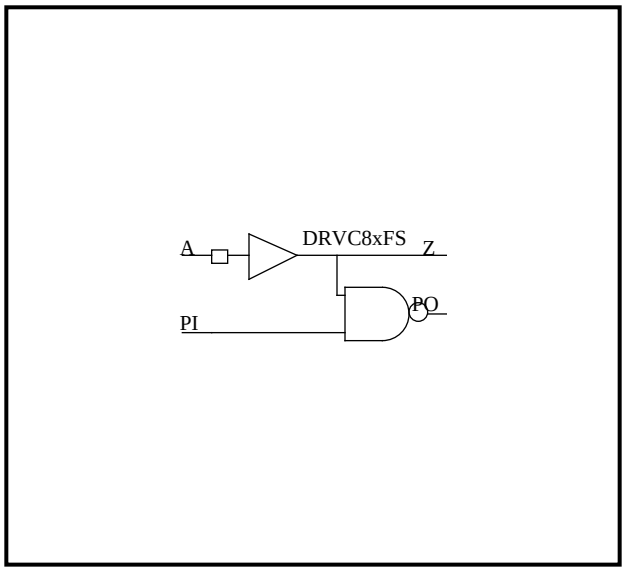
DRVC8xFS	DRVC8xFS	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
DRVC8xFS	CLOCK DRIVER with CMOS LEVEL INPUT BUFFER (equal 8mA DRIVER) with FAILSAFE	1	2	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN
DRVC8FS	DRVC8DFS

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	L	H
L	H	L	H
H	L	H	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
DRVC8xFS  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:DRVC8xFS
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	17240.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	1171.4	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0024	0.24

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	266.67	800.00	1600.00	2666.67
0.01	0.61	1.06	1.73	2.62
0.38	0.67	1.12	1.79	2.67
1.00	0.76	1.21	1.88	2.77
3.00	0.93	1.39	2.06	2.95

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.25

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	266.67	800.00	1600.00	2666.67
0.01	0.89	1.67	2.83	4.37
0.38	0.92	1.70	2.86	4.40
1.00	1.01	1.79	2.95	4.49
3.00	1.23	2.01	3.17	4.71

DRVC8xFS | DRVC8xFS | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

Rev.1.01.10

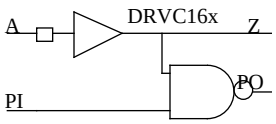
DRVC16x	DRVC16x	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
DRVC16x	CLOCK DRIVER with CMOS LEVEL INPUT BUFFER (equal 16mA DRIVER)	1	2	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN	PULL-UP
DRVC16	DRVC16D	DRVC16U

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	L	H
L	H	L	H
H	L	H	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
DRVC16x  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:DRVC16x
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	17240.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	2389.3	34.3

Rev.1.01.10

DRVC16x | DRVC16x | 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	400.00	1333.33	2666.67	4000.00
0.01	0.64	1.05	1.61	2.17
0.38	0.69	1.10	1.66	2.22
1.00	0.80	1.21	1.77	2.33
3.00	1.02	1.44	2.00	2.56

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0013	0.21

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	400.00	1333.33	2666.67	4000.00
0.01	0.87	1.57	2.55	3.52
0.38	0.91	1.61	2.58	3.55
1.00	1.01	1.70	2.68	3.65
3.00	1.27	1.97	2.94	3.91

Rev.1.01.10

DRVC16x | DRVC16x | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

Rev.1.01.10

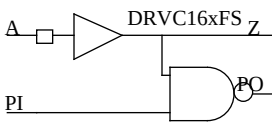
DRVC16xFS	DRVC16xFS	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
DRVC16xFS	CLOCK DRIVER with CMOS LEVEL INPUT BUFFER (equal 16mA DRIVER) with FAILSAFE	1	2	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN
DRVC16FS	DRVC16DFS

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	L	H
L	H	L	H
H	L	H	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
DRVC16xFS  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:DRVC16xFS
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	17240.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	2389.3	34.3

Rev.1.01.10

DRVC16xFS | DRVC16xFS | 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.19

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	400.00	1333.33	2666.67	4000.00
0.01	0.64	1.05	1.61	2.17
0.38	0.69	1.10	1.66	2.22
1.00	0.80	1.21	1.77	2.33
3.00	1.02	1.44	2.00	2.56

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0013	0.21

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	400.00	1333.33	2666.67	4000.00
0.01	0.87	1.57	2.55	3.52
0.38	0.91	1.61	2.58	3.55
1.00	1.01	1.70	2.68	3.65
3.00	1.27	1.97	2.94	3.91

Rev.1.01.10

DRVC16xFS | DRVC16xFS | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

Rev.1.01.10

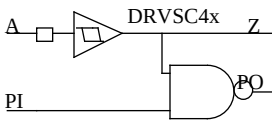
DRVSC4x	DRVSC4x	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
DRVSC4x	CLOCK DRIVER with CMOS LEVEL SCHMITT INPUT BUFFER (equal 4mA DRIVER)	1	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN	PULL-UP
DRVSC4	DRVSC4D	DRVSC4U

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	L	H
L	H	L	H
H	L	H	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
DRVSC4x  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:DRVSC4x
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	17240.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	548.3	34.3

Rev.1.01.10

DRVSC4x | DRVSC4x | 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0057	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	266.67	800.00	1600.00	2666.67
0.01	1.13	2.18	3.75	5.83
0.38	1.20	2.25	3.82	5.90
1.00	1.34	2.38	3.95	6.04
3.00	1.64	2.69	4.26	6.35

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0055	0.07

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	266.67	800.00	1600.00	2666.67
0.01	1.65	3.33	5.81	8.71
0.38	1.68	3.36	5.84	8.77
1.00	1.80	3.47	5.96	8.94
3.00	2.14	3.81	6.31	9.41

Rev.1.01.10

DRVSC4x | DRVSC4x | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

Rev.1.01.10

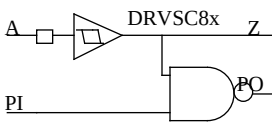
DRVSC8x	DRVSC8x	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
DRVSC8x	CLOCK DRIVER with CMOS LEVEL SCHMITT INPUT BUFFER (equal 8mA DRIVER)	1	2	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN	PULL-UP
DRVC8	DRVC8D	DRVC8U

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	L	H
L	H	L	H
H	L	H	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
DRVSC8x  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:DRVSC8x
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	17240.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	1162.4	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0024	0.26

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	266.67	800.00	1600.00	2666.67
0.01	1.11	1.57	2.24	3.12
0.38	1.18	1.64	2.31	3.20
1.00	1.31	1.77	2.44	3.33
3.00	1.62	2.08	2.75	3.63

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.32

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	266.67	800.00	1600.00	2666.67
0.01	1.63	2.43	3.59	5.13
0.38	1.66	2.45	3.62	5.16
1.00	1.78	2.57	3.73	5.27
3.00	2.12	2.91	4.07	5.61

DRVSC8x | DRVSC8x | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

Rev.1.01.10

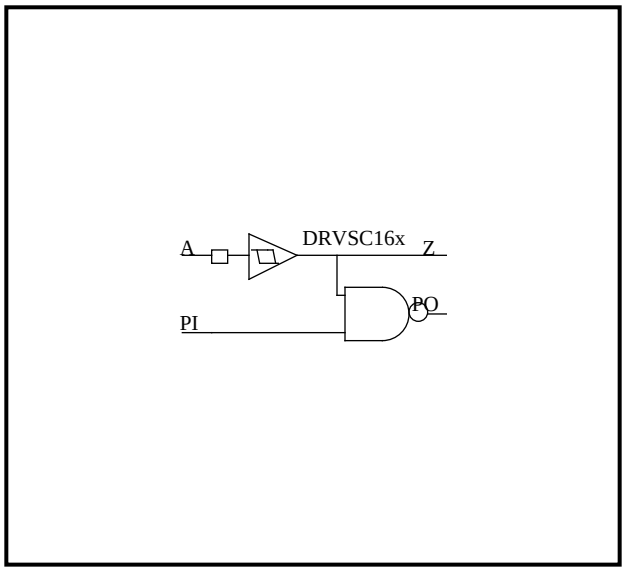
DRVSC16x	DRVSC16x	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
DRVSC16x	CLOCK DRIVER with CMOS LEVEL SCHMITT INPUT BUFFER (equal 16mA DRIVER)	1	2	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN	PULL-UP
DRVSC16	DRVSC16D	DRVSC16U

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	L	H
L	H	L	H
H	L	H	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
DRVSC16x  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:DRVSC16x
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	17240.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	2397.1	34.3

Rev.1.01.10

DRVSC16x | DRVSC16x | 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.18

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	400.00	1333.33	2666.67	4000.00
0.01	1.09	1.50	2.06	2.62
0.38	1.16	1.57	2.13	2.69
1.00	1.30	1.71	2.27	2.82
3.00	1.60	2.01	2.57	3.13

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0013	0.22

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	400.00	1333.33	2666.67	4000.00
0.01	1.51	2.22	3.19	4.16
0.38	1.54	2.25	3.22	4.19
1.00	1.66	2.36	3.33	4.30
3.00	2.00	2.70	3.67	4.64

Rev.1.01.10

DRVSC16x | DRVSC16x | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

Rev.1.01.10

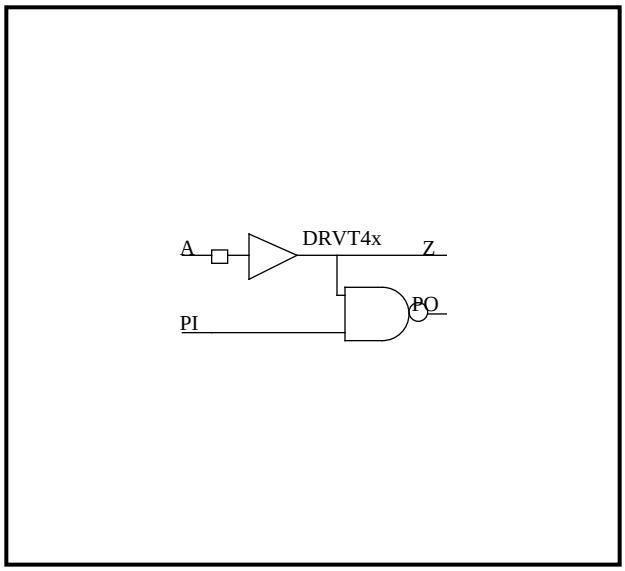
DRVT4x	DRVT4x	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
DRVT4x	CLOCK DRIVER with LVTTL LEVEL INPUT BUFFER (equal 4mA DRIVER)	1	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN	PULL-UP
DRVT4	DRVT4D	DRVT4U

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	L	H
L	H	L	H
H	L	H	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
DRVT4x  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:DRVT4x
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	17240.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	520.7	34.3

Rev.1.01.10

DRVT4x | DRVT4x | 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0064	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	266.67	800.00	1600.00	2666.67
0.01	0.93	2.12	3.91	6.29
0.38	0.93	2.12	3.91	6.28
1.00	0.94	2.13	3.92	6.30
3.00	1.02	2.21	3.99	6.37

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0053	0.06

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	266.67	800.00	1600.00	2666.67
0.01	1.10	2.73	5.17	8.41
0.38	1.12	2.75	5.19	8.43
1.00	1.17	2.80	5.24	8.47
3.00	1.31	2.94	5.38	8.62

Rev.1.01.10

DRVT4x | DRVT4x | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

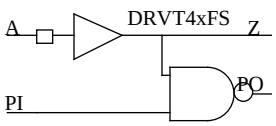
Rev.1.01.10

DRVT4xFS			DRVT4xFS	1/3
CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
DRVT4xFS	CLOCK DRIVER with LVTTL LEVEL INPUT BUFFER (equal 4mA DRIVER) with FAILSAFE	1	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN
DRVT4FS	DRVT4DFS

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	L	H
L	H	L	H
H	L	H	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
DRVT4xFS  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:DRVT4xFS
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	17240.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	520.7	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0064	0.08

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	266.67	800.00	1600.00	2666.67
0.01	0.93	2.12	3.91	6.29
0.38	0.93	2.12	3.91	6.28
1.00	0.94	2.13	3.92	6.30
3.00	1.02	2.21	3.99	6.37

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0053	0.06

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	266.67	800.00	1600.00	2666.67
0.01	1.10	2.73	5.17	8.41
0.38	1.12	2.75	5.19	8.43
1.00	1.17	2.80	5.24	8.47
3.00	1.31	2.94	5.38	8.62

DRVT4xFS | DRVT4xFS | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

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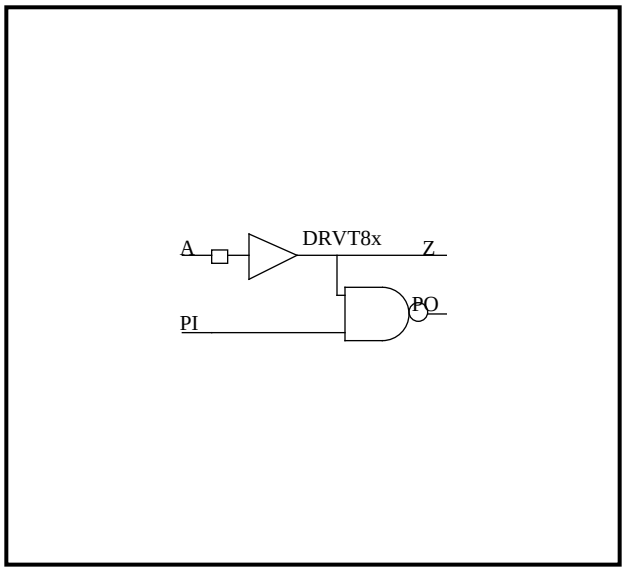
DRVT8x	DRVT8x	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
DRVT8x	CLOCK DRIVER with LVTTL LEVEL INPUT BUFFER (equal 8mA DRIVER)	1	2	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN	PULL-UP
DRVT8	DRVT8D	DRVT8U

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	L	H
L	H	L	H
H	L	H	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
DRVT8x  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:DRVT8x
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	17240.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	1126.8	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.28

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	266.67	800.00	1600.00	2666.67
0.01	0.87	1.36	2.07	3.01
0.38	0.87	1.35	2.06	3.00
1.00	0.88	1.36	2.07	3.01
3.00	0.95	1.44	2.15	3.09

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0026	0.28

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	266.67	800.00	1600.00	2666.67
0.01	1.01	1.81	2.99	4.56
0.38	1.03	1.83	3.01	4.58
1.00	1.07	1.87	3.05	4.62
3.00	1.24	2.04	3.22	4.79

DRVT8x | DRVT8x | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

Rev.1.01.10

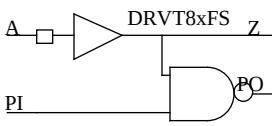
DRVT8xFS	DRVT8xFS	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
DRVT8xFS	CLOCK DRIVER with LVTTL LEVEL INPUT BUFFER (equal 8mA DRIVER) with FAILSAFE	1	2	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN
DRVT8FS	DRVT8DFS

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	L	H
L	H	L	H
H	L	H	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
DRVT8xFS  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:DRVT8xFS
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	17240.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	1126.8	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0025	0.28

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	266.67	800.00	1600.00	2666.67
0.01	0.87	1.36	2.07	3.01
0.38	0.87	1.35	2.06	3.00
1.00	0.88	1.36	2.07	3.01
3.00	0.95	1.44	2.15	3.09

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0026	0.28

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	266.67	800.00	1600.00	2666.67
0.01	1.01	1.81	2.99	4.56
0.38	1.03	1.83	3.01	4.58
1.00	1.07	1.87	3.05	4.62
3.00	1.24	2.04	3.22	4.79

DRVT8xFS | DRVT8xFS | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

Rev.1.01.10

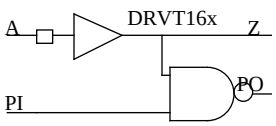
DRVT16x	DRVT16x	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
DRVT16x	CLOCK DRIVER with LVTTL LEVEL INPUT BUFFER (equal 16mA DRIVER)	1	2	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN	PULL-UP
DRVT16	DRVT16D	DRVT16U

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	L	H
L	H	L	H
H	L	H	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
DRVT16x  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:DRVT16x
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	17240.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	2285.1	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	400.00	1333.33	2666.67	4000.00
0.01	1.02	1.47	2.08	2.67
0.38	1.02	1.47	2.07	2.66
1.00	1.02	1.47	2.07	2.66
3.00	1.09	1.54	2.14	2.73

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0013	0.28

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	400.00	1333.33	2666.67	4000.00
0.01	1.07	1.79	2.79	3.78
0.38	1.09	1.81	2.80	3.79
1.00	1.13	1.85	2.84	3.83
3.00	1.30	2.02	3.01	4.00

DRVT16x | DRVT16x | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

Rev.1.01.10

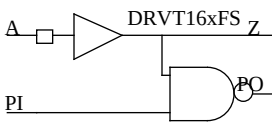
DRVT16xFS	DRVT16xFS	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
DRVT16xFS	CLOCK DRIVER with LVTTL LEVEL INPUT BUFFER (equal 16mA DRIVER) with FAILSAFE	1	2	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN
DRVT16FS	DRVT16DFS

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	L	H
L	H	L	H
H	L	H	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
DRVT16xFS  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:DRVT16xFS
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	17240.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	2285.1	34.3

Rev.1.01.10

DRVT16xFS | DRVT16xFS | 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0012	0.29

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	400.00	1333.33	2666.67	4000.00
0.01	1.02	1.47	2.08	2.67
0.38	1.02	1.47	2.07	2.66
1.00	1.02	1.47	2.07	2.66
3.00	1.09	1.54	2.14	2.73

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0013	0.28

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	400.00	1333.33	2666.67	4000.00
0.01	1.07	1.79	2.79	3.78
0.38	1.09	1.81	2.80	3.79
1.00	1.13	1.85	2.84	3.83
3.00	1.30	2.02	3.01	4.00

DRVT16xFS | DRVT16xFS | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

Rev.1.01.10

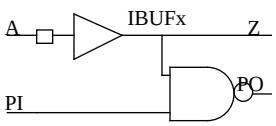
IBUFx	IBUFx	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
IBUFx	CMOS LEVEL INPUT BUFFER	1	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN	PULL-UP
IBUF	IBUFD	IBUFU

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	L	H
L	H	L	H
H	L	H	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
IBUFx  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:IBUFx
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	312.6	34.3

Rev.1.01.10

IBUFx IBUFx 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0115	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.22	0.29	0.36	0.53
0.38	0.28	0.35	0.42	0.59
1.00	0.35	0.42	0.49	0.66
3.00	0.48	0.56	0.63	0.81

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0080	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.23	0.32	0.41	0.61
0.38	0.28	0.37	0.45	0.65
1.00	0.35	0.44	0.53	0.73
3.00	0.51	0.61	0.69	0.90

IBUFx | IBUFx | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

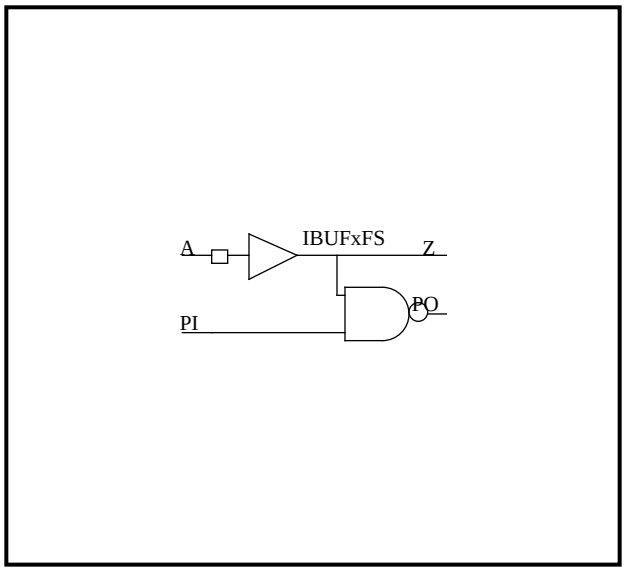
IBUFxFS	IBUFxFS	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
IBUFxFS	CMOS LEVEL INPUT BUFFER with FAILSAFE	1	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN
IBUFFS	IBUFDFS

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	L	H
L	H	L	H
H	L	H	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
IBUFxFS  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:IBUFxFS
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	312.6	34.3

Rev.1.01.10

IBUFxFS | IBUFxFS | 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0115	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.22	0.29	0.36	0.53
0.38	0.28	0.35	0.42	0.59
1.00	0.35	0.42	0.49	0.66
3.00	0.48	0.56	0.63	0.81

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0080	0.12

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.23	0.32	0.41	0.61
0.38	0.28	0.37	0.45	0.65
1.00	0.35	0.44	0.53	0.73
3.00	0.51	0.61	0.69	0.90

IBUFxFS | IBUFxFS | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

Rev.1.01.10

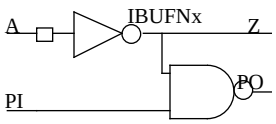
IBUFNx	IBUFNx	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
IBUFNx	CMOS LEVEL INVERTED INPUT BUFFER	1	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN	PULL-UP
IBUFN	IBUFND	IBUFNU

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	H	H
L	H	H	L
H	L	L	H
H	H	L	H

Verilog-HDL DESCRIPTION

```
IBUFNx  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:IBUFNx
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	183.5	34.3

Rev.1.01.10

IBUFNx | IBUFNx | 2/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0206	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.27	0.38	0.49	0.78
0.38	0.31	0.42	0.53	0.82
1.00	0.36	0.47	0.58	0.87
3.00	0.45	0.57	0.68	0.97

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0121	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.34	0.47	0.59	0.89
0.38	0.39	0.52	0.64	0.94
1.00	0.44	0.57	0.69	0.99
3.00	0.53	0.66	0.78	1.08

IBUFNx | IBUFNx | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

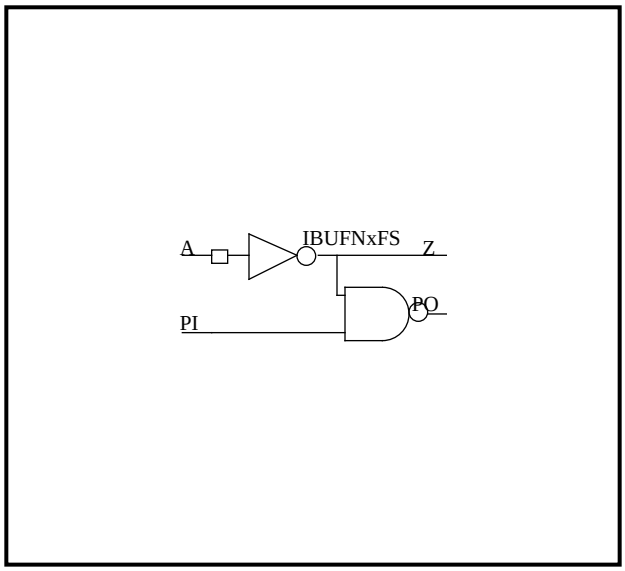
IBUFNxFS	IBUFNxFS	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
IBUFNxFS	CMOS LEVEL INVERTED INPUT BUFFER with FAILSAFE	1	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN
IBUFNFS	IBUFNDFS

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	H	H
L	H	H	L
H	L	L	H
H	H	L	H

Verilog-HDL DESCRIPTION

```
IBUFNxFS  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:IBUFNxFS
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	183.5	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0206	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.27	0.38	0.49	0.78
0.38	0.31	0.42	0.53	0.82
1.00	0.36	0.47	0.58	0.87
3.00	0.45	0.57	0.68	0.97

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0121	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.34	0.47	0.59	0.89
0.38	0.39	0.52	0.64	0.94
1.00	0.44	0.57	0.69	0.99
3.00	0.53	0.66	0.78	1.08

IBUFNxFS | IBUFNxFS | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

Rev.1.01.10

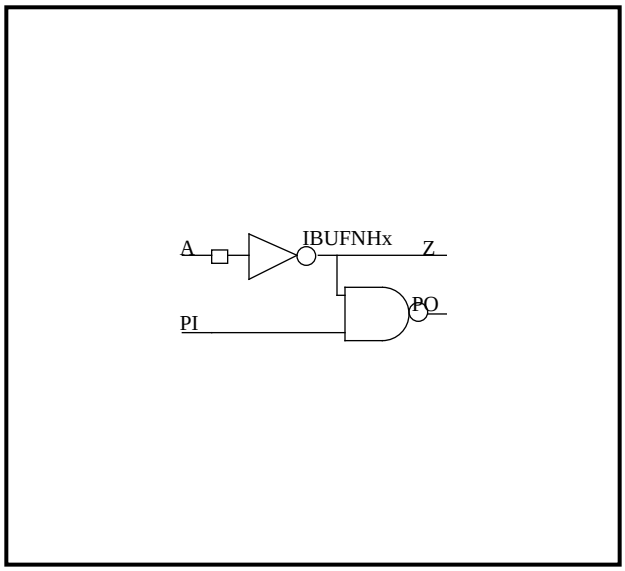
IBUFNHx	IBUFNHx	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
IBUFNHx	CMOS LEVEL INVERTED INPUT BUFFER HIGH-SPEED	1	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN	PULL-UP
IBUFNH	IBUFNHD	IBUFNHU

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	H	H
L	H	H	L
H	L	L	H
H	H	L	H

Verilog-HDL DESCRIPTION

```
IBUFNHx  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:IBUFNHx
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	202.4	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0133	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.09	0.17	0.24	0.44
0.38	0.12	0.20	0.28	0.48
1.00	0.15	0.26	0.35	0.57
3.00	0.21	0.37	0.50	0.77

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0105	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.10	0.20	0.30	0.56
0.38	0.14	0.25	0.35	0.62
1.00	0.18	0.32	0.44	0.72
3.00	0.23	0.44	0.61	0.98

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

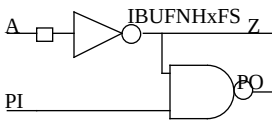
IBUFNHxFS	IBUFNHxFS	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
IBUFNHxFS	CMOS LEVEL INVERTED INPUT BUFFER HIGH-SPEED with FAILSAFE	1	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN
IBUFNHFS	IBUFNHDFS

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	H	H
L	H	H	L
H	L	L	H
H	H	L	H

Verilog-HDL DESCRIPTION

```
IBUFNHxFS  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:IBUFNHxFS
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	202.4	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0133	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.09	0.17	0.24	0.44
0.38	0.12	0.20	0.28	0.48
1.00	0.15	0.26	0.35	0.57
3.00	0.21	0.37	0.50	0.77

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0105	0.11

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.10	0.20	0.30	0.56
0.38	0.14	0.25	0.35	0.62
1.00	0.18	0.32	0.44	0.72
3.00	0.23	0.44	0.61	0.98

IBUFNHxFS | IBUFNHxFS | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

Rev.1.01.10

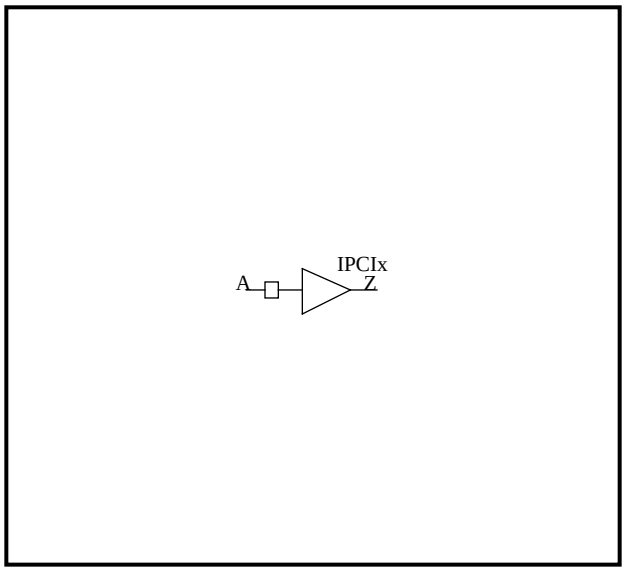
IPCIx	IPCIx	1/2

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
IPCIx	PCI (Peripheral Component Interconnect) BUS RECEIVER	0	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN	PULL-UP
IPCI	IPCID	IPCIU

LOGIC SYMBOL



TRUTH TABLE

INPUT	OUTPUT
A	Z
L	L
H	H

Verilog-HDL DESCRIPTION

```
IPCIx  inst(Z,A);
```

VHDL DESCRIPTION

```
inst:IPCIx
   port   map(Z,A);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z
ELECTRO MIGRATION DRIVE	12064.0

OUTPUT DRIVE (LU)

PIN NAME	Z
DRIVE	411.4

Rev.1.01.08

IPCIx IPCIx 2/2

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0114	0.09

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.25	0.32	0.38	0.55
0.38	0.25	0.31	0.38	0.55
1.00	0.26	0.32	0.39	0.55
3.00	0.26	0.33	0.39	0.56

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0037	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.29	0.35	0.40	0.51
0.38	0.31	0.37	0.43	0.54
1.00	0.38	0.44	0.49	0.60
3.00	0.62	0.68	0.73	0.85

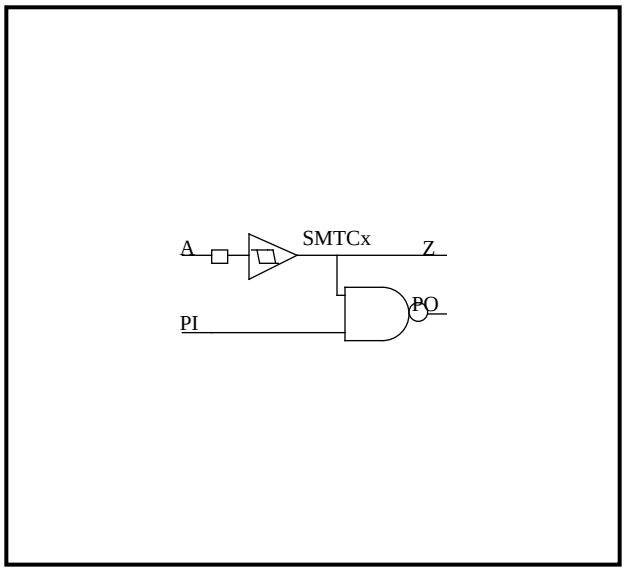
SMTCx	SMTCx	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
SMTCx	SCHMITT TRIGGER CMOS LEVEL INPUT BUFFER	1	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN	PULL-UP
SMTC	SMTCD	SMTCU

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	L	H
L	H	L	H
H	L	H	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
SMTCx  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:SMTCx
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	80.1	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0387	0.32

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.35	0.56	0.77	1.33
0.38	0.42	0.63	0.84	1.40
1.00	0.55	0.76	0.98	1.53
3.00	0.85	1.06	1.28	1.84

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0318	0.27

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.53	0.82	1.10	1.84
0.38	0.56	0.85	1.13	1.87
1.00	0.67	0.96	1.24	1.98
3.00	1.01	1.30	1.59	2.32

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

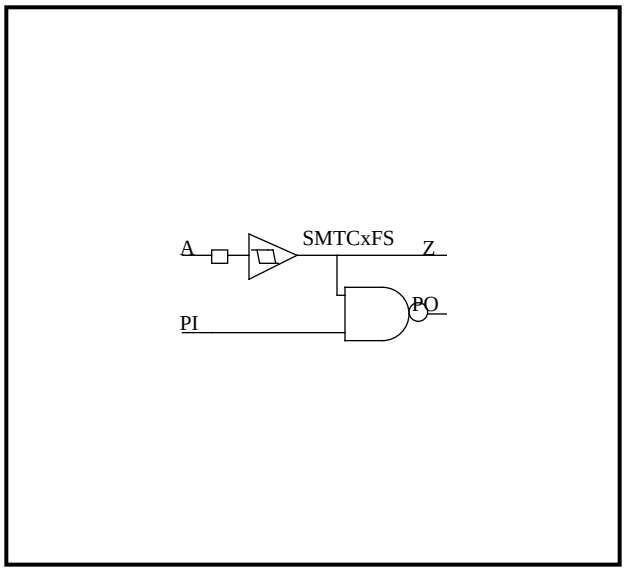
SMTCxFS	SMTCxFS	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
SMTCxFS	SCHMITT TRIGGER CMOS LEVEL INPUT BUFFER with FAILSAFE	1	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN
SMTCFS	SMTCDFS

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	L	H
L	H	L	H
H	L	H	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
SMTCxFS  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:SMTCxFS
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	80.1	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0387	0.32

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.35	0.56	0.77	1.33
0.38	0.42	0.63	0.84	1.40
1.00	0.55	0.76	0.98	1.53
3.00	0.85	1.06	1.28	1.84

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0318	0.27

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.53	0.82	1.10	1.84
0.38	0.56	0.85	1.13	1.87
1.00	0.67	0.96	1.24	1.98
3.00	1.01	1.30	1.59	2.32

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

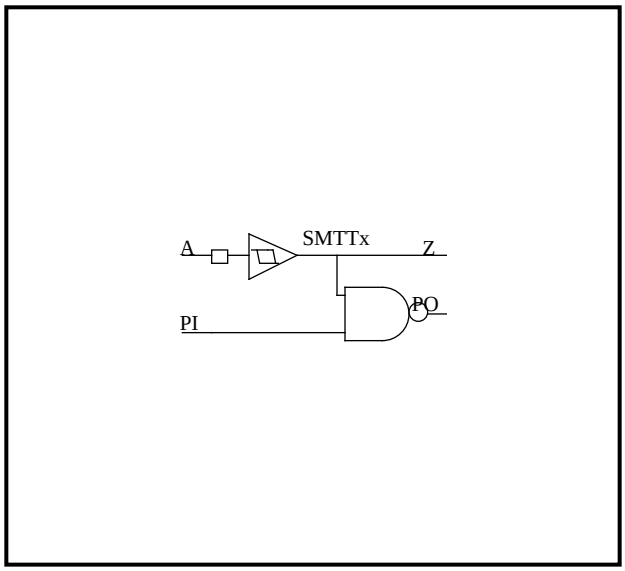
SMTTx	SMTTx	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
SMTTx	SCHMITT TRIGGER LVTTL LEVEL INPUT BUFFER	1	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN	PULL-UP
SMTT	SMTTD	SMTTU

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	L	H
L	H	L	H
H	L	H	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
SMTTx  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:SMTTx
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	76.8	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0395	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.73	0.96	1.18	1.78
0.38	0.73	0.96	1.18	1.78
1.00	0.75	0.98	1.21	1.81
3.00	0.92	1.15	1.38	1.98

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0322	0.34

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.73	1.03	1.33	2.10
0.38	0.74	1.04	1.34	2.11
1.00	0.79	1.09	1.39	2.16
3.00	1.04	1.34	1.64	2.41

SMTTx SMTTx 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

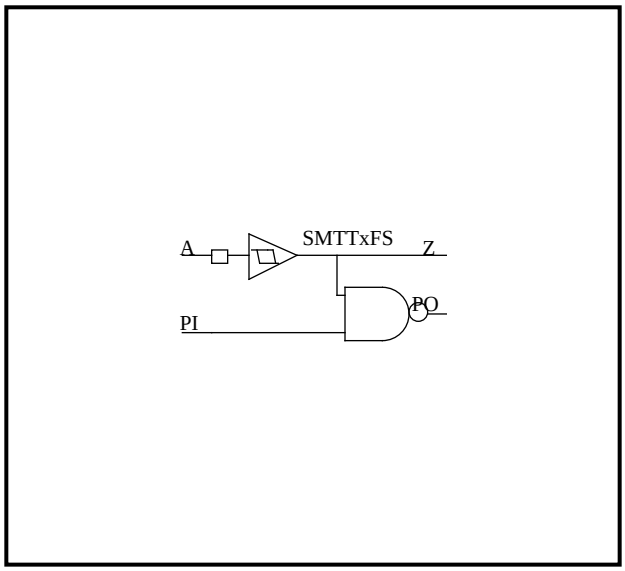
SMTTxFS	SMTTxFS	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
SMTTxFS	SCHMITT TRIGGER LVTTL LEVEL INPUT BUFFER with FAILSAFE	1	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN
SMTTFS	SMTTDFS

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	L	H
L	H	L	H
H	L	H	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
SMTTxFS  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:SMTTxFS
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	76.8	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0395	0.40

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.73	0.96	1.18	1.78
0.38	0.73	0.96	1.18	1.78
1.00	0.75	0.98	1.21	1.81
3.00	0.92	1.15	1.38	1.98

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0322	0.34

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.73	1.03	1.33	2.10
0.38	0.74	1.04	1.34	2.11
1.00	0.79	1.09	1.39	2.16
3.00	1.04	1.34	1.64	2.41

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

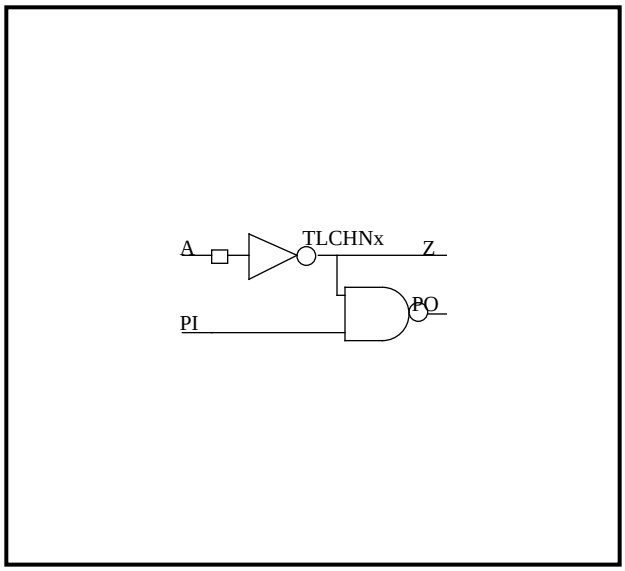
TLCHNx	TLCHNx	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
TLCHNx	LVTTL LEVEL INVERTED INPUT BUFFER	1	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN	PULL-UP
TLCHN	TLCHND	TLCHNU

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	H	H
L	H	H	L
H	L	L	H
H	H	L	H

Verilog-HDL DESCRIPTION

```
TLCHNx  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:TLCHNx
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	182.9	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0206	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.29	0.40	0.52	0.81
0.38	0.31	0.43	0.54	0.83
1.00	0.36	0.47	0.58	0.87
3.00	0.45	0.57	0.68	0.97

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0121	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.42	0.55	0.67	0.98
0.38	0.42	0.55	0.68	0.98
1.00	0.45	0.58	0.70	1.00
3.00	0.53	0.66	0.78	1.08

TLCHNx | TLCHNx | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

Rev.1.01.10

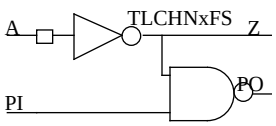
TLCHNxFS	TLCHNxFS	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
TLCHNxFS	LVTTL LEVEL INVERTED INPUT BUFFER with FAILSAFE	1	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN
TLCHNFS	TLCHNDFS

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	H	H
L	H	H	L
H	L	L	H
H	H	L	H

Verilog-HDL DESCRIPTION

```
TLCHNxFS  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:TLCHNxFS
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	182.9	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0206	0.13

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.29	0.40	0.52	0.81
0.38	0.31	0.43	0.54	0.83
1.00	0.36	0.47	0.58	0.87
3.00	0.45	0.57	0.68	0.97

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0121	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.42	0.55	0.67	0.98
0.38	0.42	0.55	0.68	0.98
1.00	0.45	0.58	0.70	1.00
3.00	0.53	0.66	0.78	1.08

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

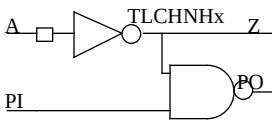
TLCHNHx	TLCHNHx	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
TLCHNHx	LVTTL LEVEL INVERTED INPUT BUFFER HIGH-SPEED	1	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN	PULL-UP
TLCHNH	TLCHNHD	TLCHNHU

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	H	H
L	H	H	L
H	L	L	H
H	H	L	H

Verilog-HDL DESCRIPTION

```
TLCHNHx  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:TLCHNHx
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	127.9	34.3

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TLCHNHx

TLCHNHx

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

TLCHNHx | TLCHNHx | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

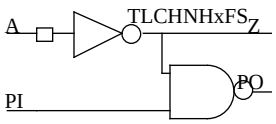
Rev.1.01.10

TLCHNHxFS			TLCHNHxFS	1/3
CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
TLCHNHxFS	LVTTL LEVEL INVERTED INPUT BUFFER HIGH-SPEED with FAILSAFE	1	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN
TLCHNHFS	TLCHNHDFS

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	H	H
L	H	H	L
H	L	L	H
H	H	L	H

Verilog-HDL DESCRIPTION

```
TLCHNHxFS  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:TLCHNHxFS
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	127.9	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0228	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.10	0.22	0.34	0.64
0.38	0.12	0.24	0.35	0.66
1.00	0.15	0.28	0.39	0.69
3.00	0.21	0.37	0.50	0.83

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0267	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.17	0.39	0.62	1.22
0.38	0.17	0.38	0.61	1.22
1.00	0.18	0.39	0.62	1.22
3.00	0.23	0.45	0.67	1.25

TLCHNHxFS | TLCHNHxFS | 3/3

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

Rev.1.01.10

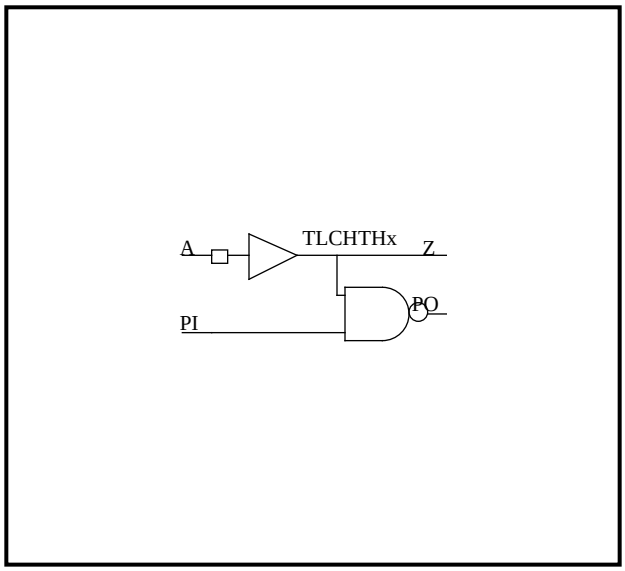
TLCHTHx	TLCHTHx	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
TLCHTHx	LVTTL LEVEL INPUT BUFFER	1	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN	PULL-UP
TLCHTH	TLCHTHD	TLCHTHU

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	L	H
L	H	L	H
H	L	H	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
TLCHTHx  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:TLCHTHx
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	299.5	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0121	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.37	0.45	0.53	0.71
0.38	0.37	0.45	0.52	0.71
1.00	0.38	0.46	0.54	0.73
3.00	0.48	0.56	0.63	0.82

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0081	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.29	0.38	0.47	0.68
0.38	0.31	0.40	0.49	0.70
1.00	0.36	0.45	0.54	0.75
3.00	0.51	0.61	0.69	0.90

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35

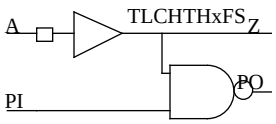
TLCHTHxFS	TLCHTHxFS	1/3

CELL NAME	FUNCTION	CELL COUNT		CONDITION
		GATE	I/O	
TLCHTHxFS	LVTTL LEVEL INPUT BUFFER with FAILSAFE	1	1	VDD=3.3V, Ta=25°C, Typ.

CELL NAME

no resister	PULL-DOWN
TLCHTHFS	TLCHTHDFS

LOGIC SYMBOL



TRUTH TABLE

INPUT		OUTPUT	
A	PI	Z	PO
L	L	L	H
L	H	L	H
H	L	H	H
H	H	H	L

Verilog-HDL DESCRIPTION

```
TLCHTHxFS  inst(Z,PO,A,PI);
```

VHDL DESCRIPTION

```
inst:TLCHTHxFS
   port   map(Z,PO,A,PI);
```

ELECTRO MIGRATION (LU*MHz)

PIN NAME	Z	PO
ELECTRO MIGRATION DRIVE	12064.0	12928.0

INPUT LOAD (LU)

PIN NAME	LOAD
PI	1.03

OUTPUT DRIVE (LU)

PIN NAME	Z	PO
DRIVE	299.5	34.3

Rev.1.01.10

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.11	0.25	0.42	1.11
0.38	0.13	0.28	0.45	1.13
1.00	0.17	0.33	0.51	1.19
3.00	0.23	0.43	0.64	1.38

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
Z->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.10	0.25	0.44	1.18
0.38	0.15	0.31	0.49	1.24
1.00	0.19	0.38	0.58	1.33
3.00	0.26	0.52	0.77	1.60

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0121	0.17

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.37	0.45	0.53	0.71
0.38	0.37	0.45	0.52	0.71
1.00	0.38	0.46	0.54	0.73
3.00	0.48	0.56	0.63	0.82

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
A->Z	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
Z	0.0081	0.14

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	15.00	30.00	70.00
0.01	0.29	0.38	0.47	0.68
0.38	0.31	0.40	0.49	0.70
1.00	0.36	0.45	0.54	0.75
3.00	0.51	0.61	0.69	0.90

CONDITION:VDD=3.3V, Ta=25°C, Typ.

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	FALL	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0653	0.10

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.24	0.43	1.17
0.38	0.15	0.32	0.51	1.25
1.00	0.21	0.42	0.63	1.39
3.00	0.32	0.62	0.90	1.78

PATH CONDITION

PATH	CONDITION	FUNCTION	IO LEVEL
PI->PO	---	RISE	---

SLEW FACTOR

PIN NAME	FACTOR (ns/LU)	CONSTANT (ns)
PO	0.0996	0.16

PATH DELAY (ns)				
LOAD (LU) SLEW (ns)	1.00	5.00	10.00	30.00
0.01	0.09	0.23	0.40	1.08
0.38	0.11	0.26	0.43	1.11
1.00	0.13	0.30	0.48	1.17
3.00	0.15	0.37	0.60	1.35