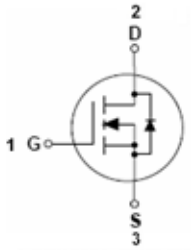
N-Channel Enhancement Mode MOSFET

TBL450N15D

Features

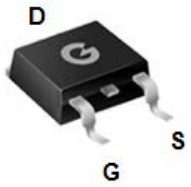
HF

- Super low gate charge
- Green device available
- Excellent C_{dv} / d_t effect decline
- Advanced high cell density trench technology
- Halogen free
- Qualified to AEC-Q101 standards for high reliability



Application

- Power switching application
- Hard swiched and high frequency circuits
- Uninterruptible power supply



TO-252

Mechanical Data

- Case: TO-252
- Molding Compound: UL Flammability Classification Rating 94V-0
- Terminals: Matte tin-plated leads; solderability-per MIL-STD-202, Method 208

Ordering Information

Part Number	Package	Shipping Quantity	Marking Code
TBL450N15D	TO-252	80pcs / Tube or 2500pcs / Tape & Reel	450N15D

Maximum Ratings (@ T_A = 25℃ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	150	V
Gate-to-Source Voltage	V_{GSS}	±20	V
Continuous Drain Current (T_C = 25°C,V_{GS} = 10V) *1	I_D	30	A
Continuous Drain Current (T_C = 100°C,V_{GS} = 10V) *1		22	A
Pulsed Drain Current *2	I_{DM}	60	A
Single Pulse Avalanche Energy *3	E_{AS}	216	mJ

Thermal Characteristics

Parameter	Symbol	Value	Unit
Power Dissipation (T_C = 25°C)	P_D	115	W
Thermal Resistance Junction-to-Case *1	$R_{\theta JC}$	1.09	°C/W
Operating Junction Temperature Range	T_J	-55 ~ +150	°C
Storage Temperature Range	T_{STG}	-55 ~ +150	°C

Electrical Characteristics (@ T_A = 25℃ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
V_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	150	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 120V, V_{GS} = 0V, T_J = 25°C	-	-	1	μA
		V_{DS} = 120V, V_{GS} = 0V, T_J = 55°C	-	-	5	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA
On Characteristics						
$R_{DS(ON)}$	Static Drain-Source On-resistance *2	V_{GS} = 10V,I_D = 20A	-	-	46	mΩ
		V_{GS} = 4.5V,I_D = 20A	-	-	50	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	1.2	-	2.5	V
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0V V_{DS} = 25V f = 1.0MHz	-	3755	-	pF
C_{OSS}	Output Capacitance		-	207	-	
C_{RSS}	Reverse Transfer Capacitance		-	160	-	
Switching Characteristics						
$t_{d(ON)}$	Turn-on Delay Time	V_{DD} = 50V V_{GS} = 4.5V R_G = 3.3Ω I_D = 10A	-	18	-	ns
t_r	Turn-on Rise Time		-	20	-	
$t_{d(OFF)}$	Turn-Off Delay Time		-	65	-	
t_f	Turn-Off Fall Time		-	15	-	
Q_G	Total Gate-Charge	V_{DD} = 75V V_{GS} = 4.5V I_D = 10A	-	40	-	nC
Q_{GS}	Gate to Source Charge		-	10	-	
Q_{GD}	Gate to Drain (Miller) Charge		-	21	-	
Source-Drain Diode Characteristics						
V_{SD}	Diode Forward Voltage *2	I_{SD} = 18A, V_{GS} = 0V, T_J = 25°C	-	-	1.2	V
I_S	Diode Continuous Forward Current *1		-	-	30	A

Notes:

1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper
2. The data tested by pulsed, pulse width ≤ 300μs, duty cycle ≤ 2%
3. The EAS data shows Max. rating. The test condition is V_{DD} = 25V, V_{GS} = 10V, L = 0.5mH

Ratings and Characteristics Curves (@ T_A = 25°C unless otherwise specified)

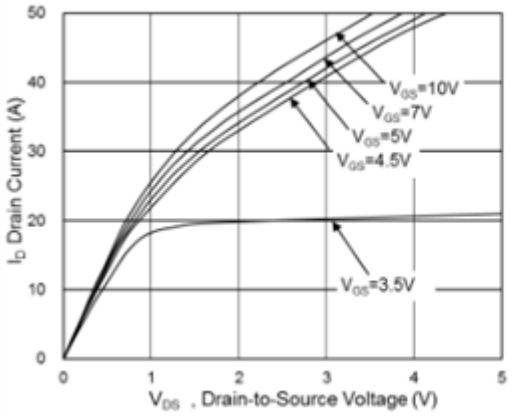


Fig 1 Typical Output Characteristics

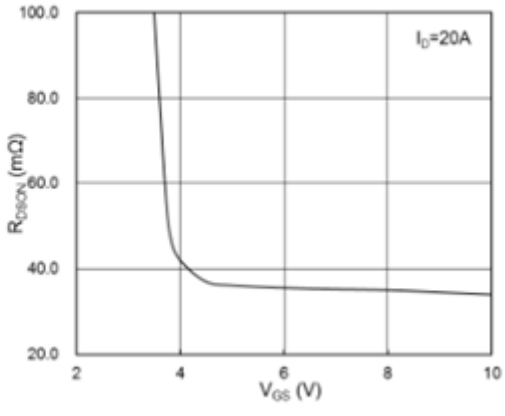


Fig 2 On-Resistance vs. Gate-Source

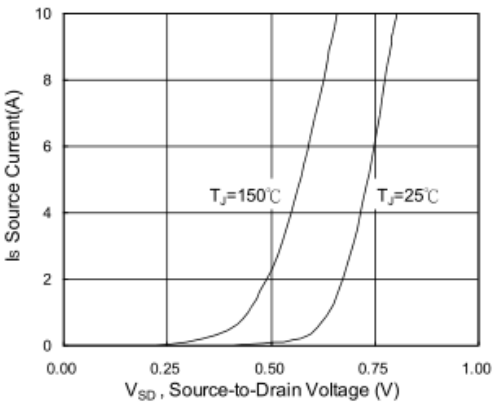


Fig 3 Forward Characteristics Of Reverse diode

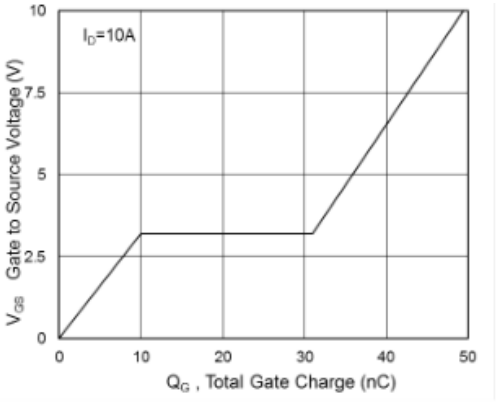


Fig 4 Gate-Charge Characteristics

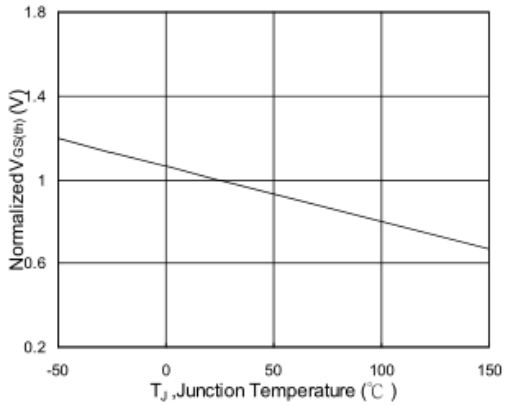


Fig 5 Normalized $V_{GS(th)}$ vs. T_J

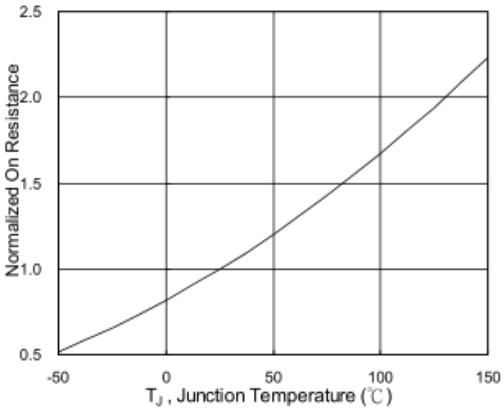


Fig 6 Normalized $R_{DS(ON)}$ vs. T_J

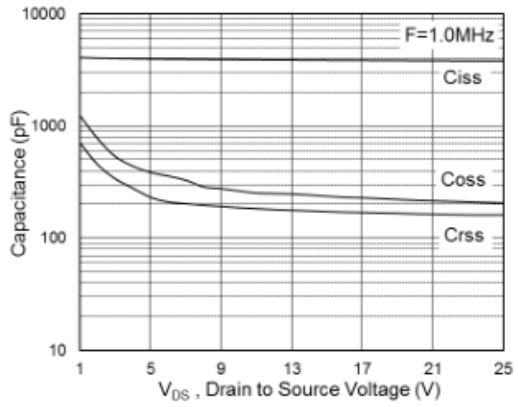


Fig 7 Capacitance

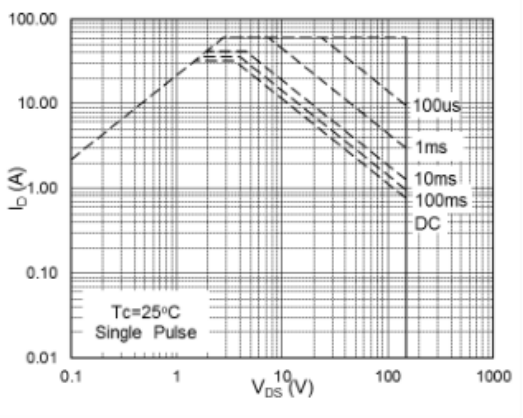


Fig 8 Safe Operating Area

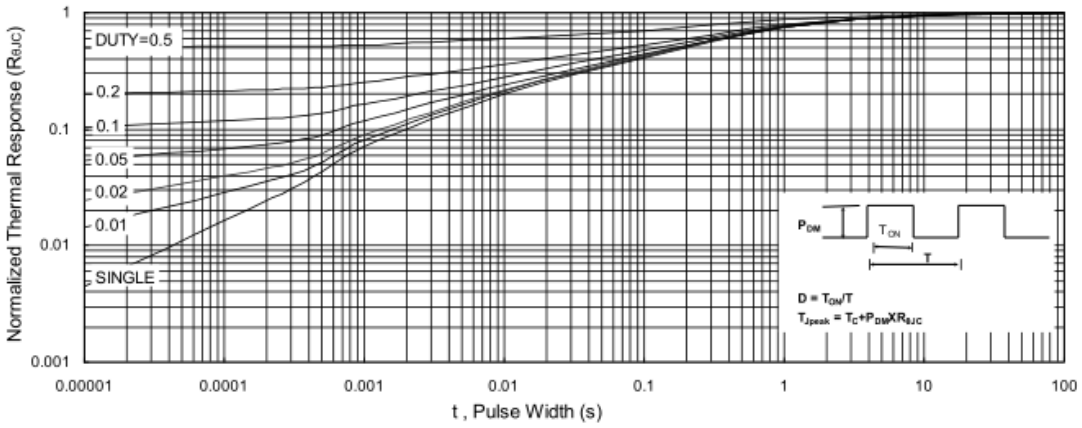
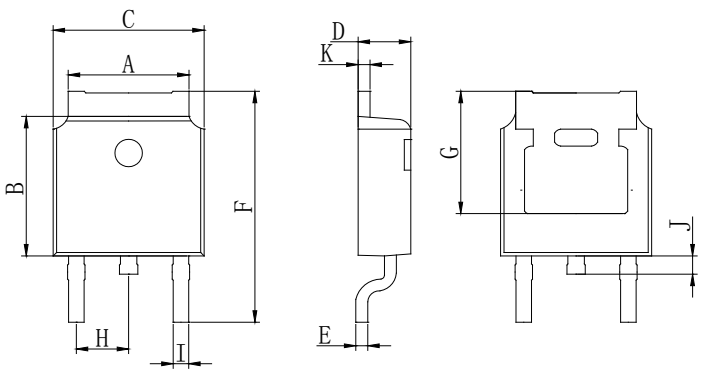


Fig9 Normalized Maximum Transient Thermal Impedance

Package Outline Dimensions (Unit: mm)



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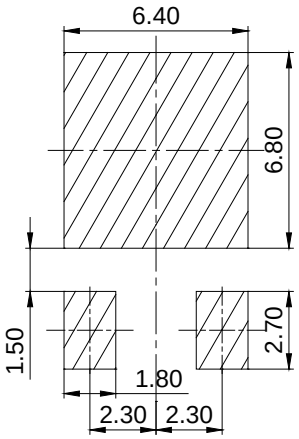
Dimension	**Min.**	**Max.**
A	5.05	5.65
B	5.80	6.40
C	6.25	6.85
D	2.20	2.40
E	0.40	0.60
F	9.71	10.31
G	5.05	5.65
H	2.10	2.50
I	0.70	0.90
J	0.50	0.70
K	0.40	0.60

Mounting Pad Layout (Unit: mm)

TO-252



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