P-Channel Enhancement Mode MOSFET

TBL250P06-3DL8

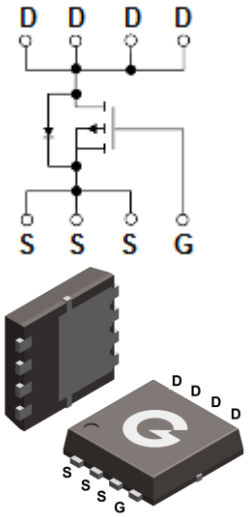
Features

HF

- Super low gate charge
- 100% E_{AS} guaranteed
- Excellent C_{dv}/d_t effect decline
- Advanced high cell density Trench technology
- Halogen free
- Qualified to AEC-Q101 standards for high reliability

Mechanical Data

- Case: PDFN3×3-8L
- Molding Compound: UL Flammability Classification Rating 94V-0
- Terminals: Matte tin-plated leads; solderability-per MIL-STD-202, Method 208



PDFN3×3-8L

Ordering Information

Part Number	Package	Shipping Quantity	Marking Code
TBL250P06-3DL8	PDFN3×3-8L	5000 pcs / Tape & Reel	250P06

Maximum Ratings (@ T_A = 25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	-60	V
Gate-to-Source Voltage	V_{GSS}	±20	V
Continuous Drain Current (T_A = 25°C) *1	I_D	-7.7	A
Continuous Drain Current (T_A = 70°C) *1		-6.2	A
Pulsed Drain Current *2	I_{DM}	-55	A
Avalanche Energy, Single Pulsed *3	E_{AS}	62.9	mJ

Thermal Characteristics

Parameter	Symbol	Value	Unit
Power Dissipation (T_A = 25°C) *4	P_D	1	W
Thermal Resistance Junction-to-Air *4	$R_{\theta JA}$	125	°C/W
Operating Junction Temperature Range	T_J	-55 ~ +150	°C
Storage Temperature Range	T_{STG}	-55 ~ +150	°C

Electrical Characteristics (@ T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
V_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = -250μA	-60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -48V, V_{GS} = 0V, T_C = 25°C	-	-	-1	μA
		V_{DS} = -48V, V_{GS} = 0V, T_C = 55°C	-	-	-5	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA
On Characteristics						
$R_{DS(ON)}$	Static Drain-Source On-resistance *5	V_{GS} = -10V, I_D = -18A	-	-	25	mΩ
		V_{GS} = -4.5V, I_D = -12A	-	-	33	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250μA	-1	-	-2.5	V
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0V V_{DS} = -15V f = 1.0MHz	-	3635	-	pF
C_{OSS}	Output Capacitance		-	224	-	
C_{RSS}	Reverse Transfer Capacitance		-	141	-	
Switching Characteristics						
$t_{d(ON)}$	Turn-on Delay Time	V_{GS} = -10V V_{DD} = -15V I_D = -1A R_G = 3.3Ω	-	38	-	ns
t_r	Turn-on Rise Time		-	23.6	-	
$t_{d(OFF)}$	Turn-Off Delay Time		-	100	-	
t_f	Turn-Off Fall Time		-	6.8	-	
Q_G	Total Gate-Charge	V_{GS} = -4.5V V_{DD} = -12V I_D = -12A	-	25	-	nC
Q_{GS}	Gate to Source Charge		-	6.7	-	
Q_{GD}	Gate to Drain (Miller) Charge		-	5.5	-	
Source-Drain Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{SD} = -1A, V_{GS} = 0V	-	-	-1.2	V

Notes:

1. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1-inch square copper plate
2. 10μs pulse, duty cycle = 1%
3. The E_{AS} data shows Max. rating. The test condition is V_{DD} = -30V, V_{GS} = -10V, L = 0.1mH
4. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided
5. Pulse width≤380μs; duty cycle≤2%

Ratings and Characteristics Curves (@ T_A = 25°C unless otherwise specified)

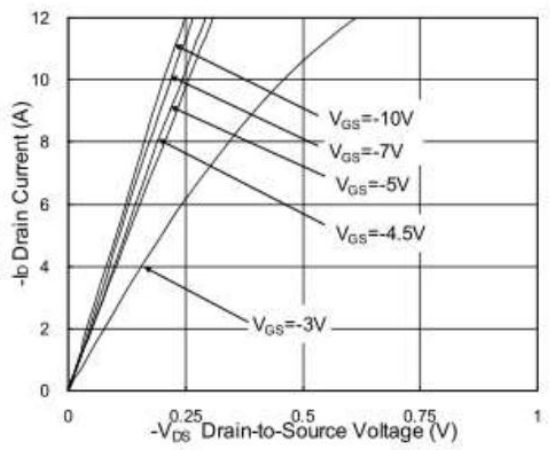


Fig.1 Typical Output Characteristics

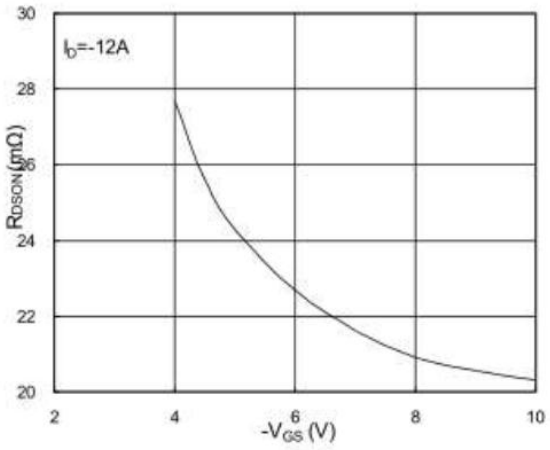


Fig.2 On-Resistance vs. G-S Voltage

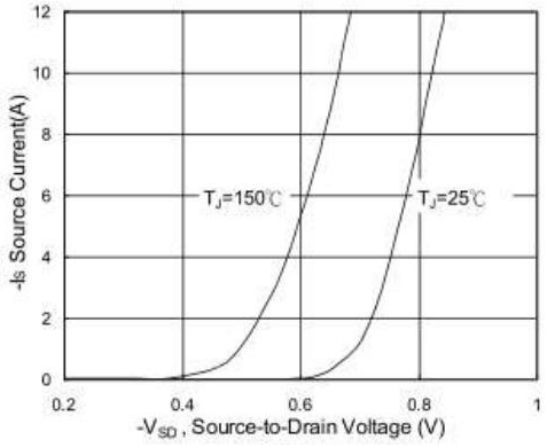


Fig.3 Forward Characteristics of Reverse

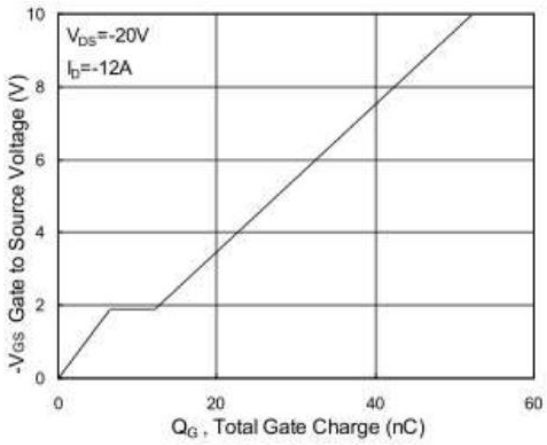


Fig.4 Gate-Charge Characteristics

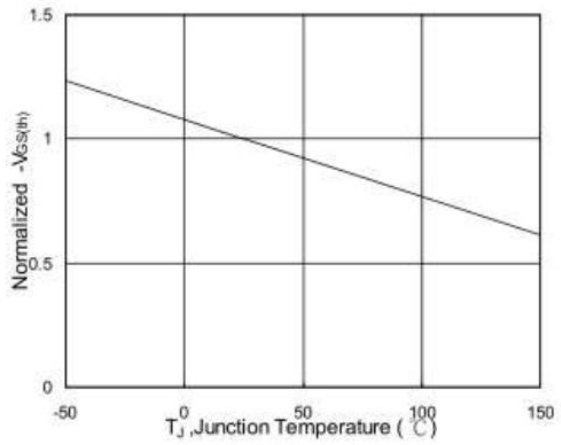


Fig.5 Normalized -$VG_{S(th)}$ vs. T_J

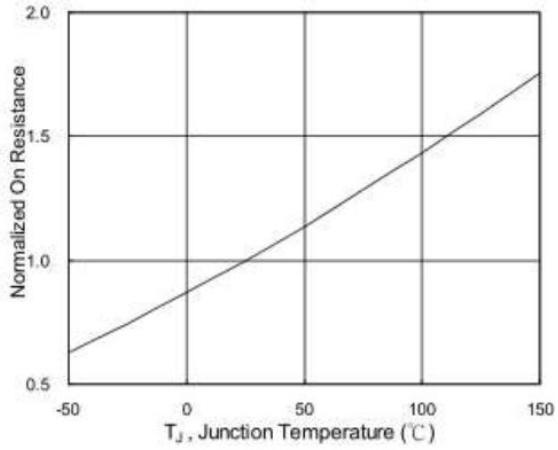
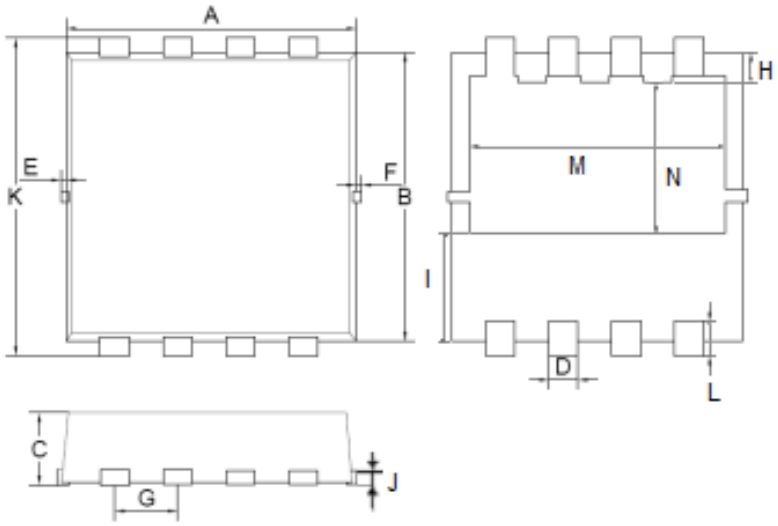


Fig.6 Normalized RD_{SON} vs. T_J

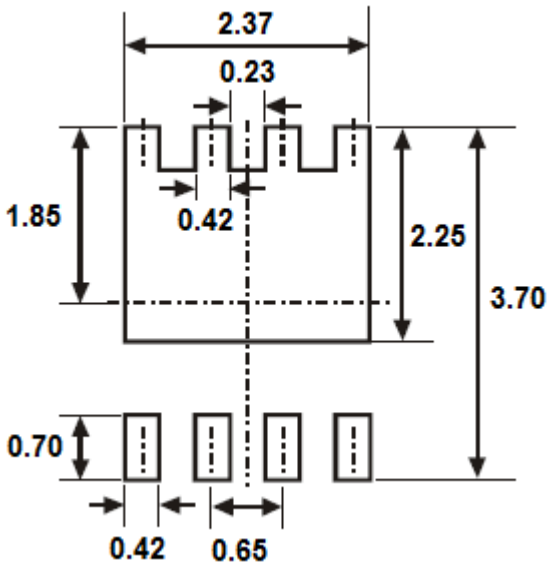
Package Outline Dimensions (Unit: mm)



PDFN3×3-8L		
Dimension	**Min.**	**Max.**
A	2.90	3.10
B	2.90	3.10
C	0.65	0.85
D	0.20	0.40
E	0.00	0.10
F	0.00	0.10
G	0.55	0.75
H	0.20	0.40
I	0.70	1.10
J	0.10	0.20
K	3.15	3.45
L	0.20	0.40
M	2.35	2.55
N	1.500	1.900

Mounting Pad Layout (Unit: mm)

PDFN3×3-8L



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