TOSHIBA BI-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

# **TB6524FN**

### DC MOTOR DUAL FULL BRIDGE DRIVER (H-SWITCH)

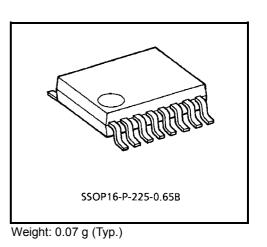
The TB6524FN is a bridge driver most suitable for switching between normal rotation and reverse rotation and can control three modes, normal rotation, reverse rotation, and stop. The driver is capable of handling output current of 100 mA. Fixed current operation is also available as the control method.

#### FEATURES

- Operating voltage range  $: V_{CC} = 1.5 \sim 7.0 V$ 
  - (normal operation)  $V_{CC} = 2.0 \sim 7.0 V$ (fixed current operation)

: IOUT = 100 mA

- Output current
- Built-in diode for absorbing counter electromotive force
- Built-in enable terminal



#### (16) Vca ĺ٩. Vr (4) OUTA1 Control circuit INA (2 **⑦**Ουτα2 Ch-A 6 RFA2 5 RFA1 ENABLE (1 3) GND ٩٧cc 13 OUTB1 Control circuit INB (15 Ch-B 1) RFB2 12 RFB1 14) GND

#### **BLOCK DIAGRAM**

### **PIN FUNCTION**

PIN No.	SYMBOL	DESCRIPTION			
1	ENABLE	nable signal input, Hi : Enabled, Low : All output OFF			
2	INA	annel A input signal terminal			
3	GND	round terminal			
4	OUTA1	annel A output terminal			
5	RFA1	nannel A : Output current is set by external resistance.			
6	RFA2	Channel A : Output current is set by external resistance.			
7	OUTA2	Channel A output terminal			
8	V <sub>CC</sub>	ower supply			
9	V <sub>CC</sub>	Power supply			
10	OUTB2	Channel B output terminal			
11	RFB2	Channel B : Output current is set by external resistance.			
12	RFB1	Channel B : Output current is set by external resistance.			
13	OUTB1	Channel B output terminal			
14	GND	Ground terminal			
15	INB	Channel B input signal terminal			
16	V <sub>CC</sub>	Logic power supply			

(8) V<sub>CC</sub>, (9) V<sub>CC</sub>, (16) V<sub>CC</sub>, (3) GND and (14) GND must be connected to V<sub>CC</sub> or GND.

#### FUNCTION

INPUT			OUTPUT				
INA	NA INB ENABLE		OUTA1	OUTA2	OUTB1	OUTB2	
Н	Н	Н	Н	L	Н	L	
L	L	Н	L	Н	L	Н	
Н	L	Н	Н	L	L	Н	
L	Н	Н	L	Н	Н	L	
H/L	H/L	L	8	8	8	8	

∞: High impedance

Note: Before you change "Enable" to Low from High on the operating, change to Low both "INA" and "INB".

#### MAXIMUM RATING (Ta = 25°C)

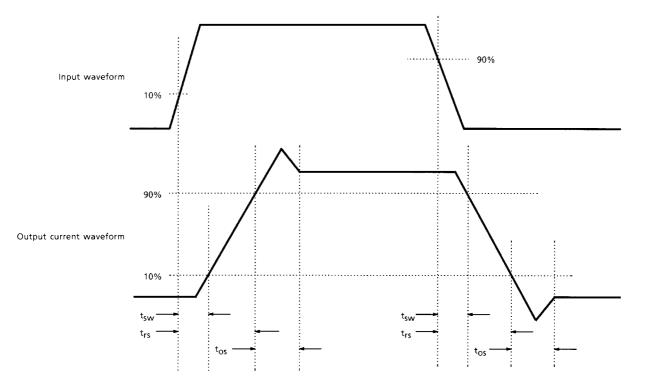
CHARACTERISTIC	SYMBOL	RATING	UNIT	
Power Supply Voltage	V <sub>CC</sub> (Max)	8	V	
Output Current	I <sub>OUT</sub>	0.1	А	
Power Dissipation (Tc = 25°C)	PD	0.5 (Note)	W	
Operating Temperature	T <sub>opr</sub>	-30 ~ 75	°C	
Storage Temperature	T <sub>stg</sub>	<b>−</b> 55 ~ 150	°C	

Note: IC single unit

# ELECTRICAL CHARACTERISTICS (Ta = $25^{\circ}$ C, V<sub>CC</sub> = 5 V)

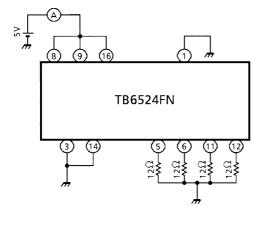
CHARACTERISTIC	SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
	I <sub>CC1</sub>	1	Standby (ENABLE OFF)	_	0.1	1.0	μA
Power Supply Current	I <sub>CC2</sub>	2	Normal / reverse (for 2 channels) output OPEN	_	32	45	mA
	Upper V <sub>SAT U-1</sub>	- 3	I <sub>OUT</sub> = 100 mA at normal / reverse	_	0.2	0.3	V
Output Saturation Voltage	Lower V <sub>SAT L-1</sub>		I <sub>OUT</sub> = 100 mA at normal / reverse	_	0.2	0.3	
Output Saturation Voltage	Upper V <sub>SAT U-2</sub>		I <sub>OUT</sub> = 50 mA at normal / reverse	_	0.1	0.25	
	Lower V <sub>SAT L-2</sub>		I <sub>OUT</sub> = 50 mA at normal / reverse	_	0.1	0.25	
Setting Output Current I <sub>OUT C</sub> 4		12 $\Omega$ between RFA1, 2 / RFB1, and 2–GND Load 7.5 $\Omega$	55	65	75	mA	
Output Current V <sub>CC</sub> Dependency	$\frac{\Delta I_{OUTC}}{\Delta V_{CC}}$	5	I <sub>OUT C</sub> = 10 ~ 100 mA (R <sub>f</sub> : 8 Ω, 80 Ω) V <sub>CC</sub> = 2.0 ~ 7.0 V Load 5 Ω	-8		5	%
Output Current Switching	t <sub>sw</sub>		560 μH (7.5 Ω) R <sub>f</sub> = 16 Ω	_	1.0	_	μs
Duration	t <sub>rs</sub>			_	6.0	—	
Overshoot Duration	t <sub>os</sub>			_	2.0	—	
Input Voltage	VIH	- 6	INA, INB, ENABLE	1.5	—	V <sub>CC</sub>	V
input voltage	VIL			0	—	0.3	
Input Current	l <sub>in</sub>	7	Sync V <sub>IN</sub> = 5.0 V Input terminal 4.7 kΩ	_	430	550	μA
Output Transistor Leak	Upper I <sub>LU</sub>	- 8	V <sub>L</sub> = 7 V	_	_	30	μA
Current	Lower I <sub>LL</sub>			_	_	30	μη

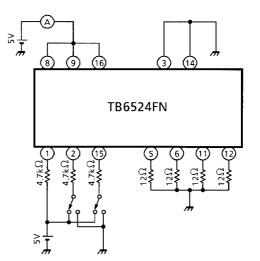
### $t_{sw}, t_{rs}, t_{os}$



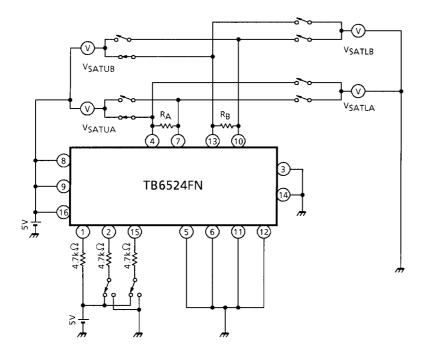
## TEST CIRCUIT 1 I<sub>CC1</sub>

TEST CIRCUIT 2 I<sub>CC2</sub>





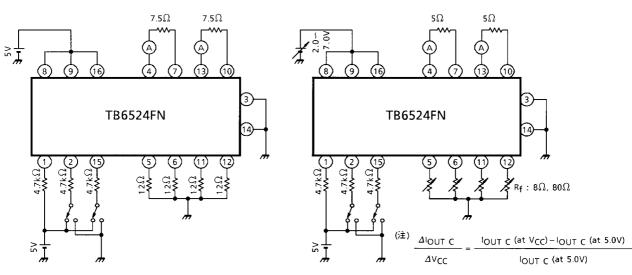
TEST CIRCUIT 3 VSAT U-1,2 / VSAT L-1,2



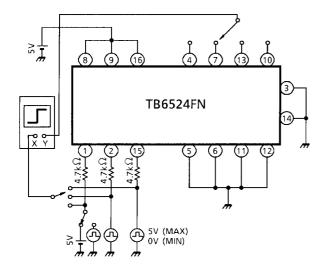
Note: Set  $R_A$  and  $R_B$  so that  $I_{OUT}$  = 50mA and 100mA is satisfied.

# TEST CIRCUIT 4 IOUT C

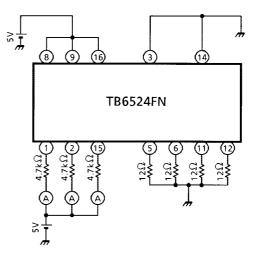
TEST CIRCUIT 5 ΔI<sub>OUT C</sub>



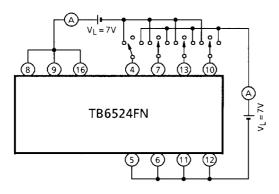
## TEST CIRCUIT 6 VIH / VIL

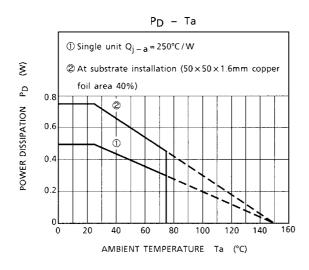


TEST CIRCUIT 7 Iin

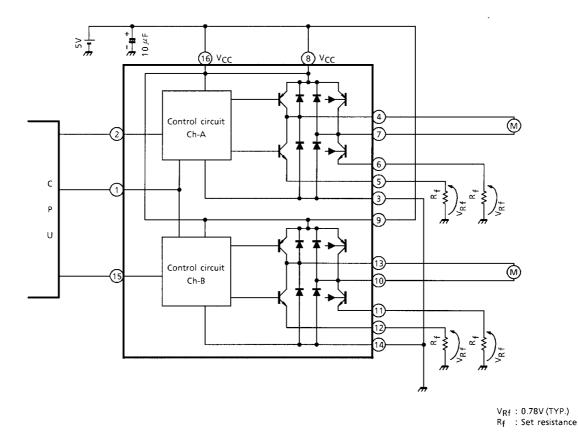


#### TEST CIRCUIT 8 ILU / ILL





### **APPLICATION CIRCUIT**

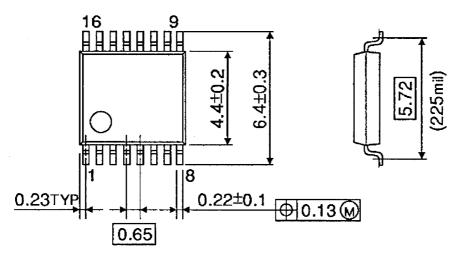


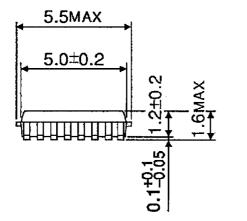
Note: Utmost care is necessary in the design of the output line, V<sub>CC</sub> and GND line since IC may be destroyed due to short–circuit between outputs, air contamination fault, or fault by improper grounding.

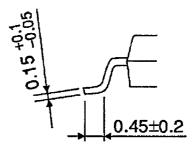
### PACKAGE DIMENSIONS

SSOP16-P-225-0.65B

Unit: mm







Weight: 0.07 g (Typ.)

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Handbook" etc..

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