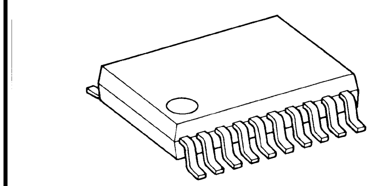
TOSHIBA Bi−CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB62715FN

8 BIT SHIFT REGISTER, LATCHES & CONSTANT CURRENT DRIVERS

The TB62715FN is specifically designed for LED and LED DISPLAY constant current drivers.
This constant current output circuits is able to set up external resistor (I_{OUT} = 2~150 mA).
This IC is monolithic integrated circuit designed to be used together with Bi−CMOS process.
The devices consist of 8 bit shift register, latch, AND−GATE & Constant Current Drivers.



Weight: 0.14 g (typ.)

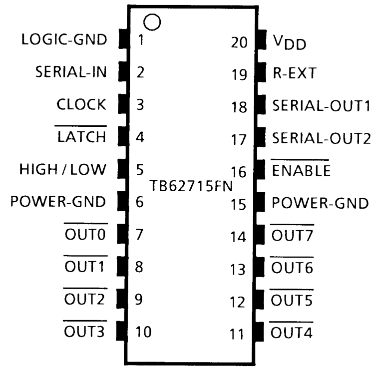
FEATURES

- Constant Current Output: Can set up all output current with one resistor for 80 to 150 mA.
- Constant Output Current Matching :

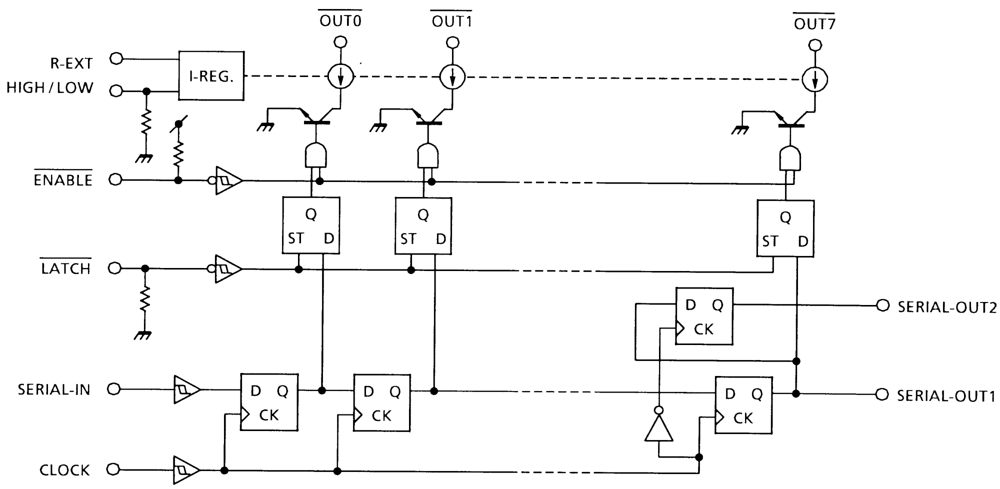
HIGH / LOW	OUTPUT−GND VOLTAGE	CURRENT MATCHING (BIT)	CURRENT MATCHING (LOT)	OUTPUT CURRENT (MAX.)
"L"	≥0.7 V	±6.0 %	±15.0 %	2~70 mA
"H"	≥1.0 V	±6.0 %	±15.0 %	50~150 mA

- Maximum Clock Frequency: f_{CLK} = 15 MHz (Cascade Connected Operate, T_{opr} = 25°C)
- 5 V C−MOS Compatible Input
- Package: SSOP20−P−225−0.65A

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM

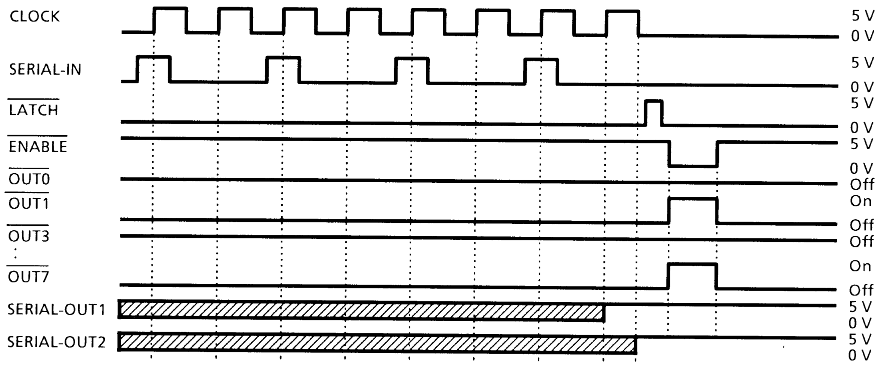


TRUTH TABLE

CLOCK	$\overline{LATCH}$	$\overline{ENABLE}$	SERIAL-IN	$\overline{OUT0}$ ··· $\overline{OUT5}$ ··· $\overline{OUT7}$	SERIAL-OUT
UP	H	L	D_n	D_n ··· D_{n-5} ··· D_{n-7}	D_{n-7}
UP	L	L	D_{n+1}	No Change	D_{n-6}
UP	H	L	D_{n+2}	D_{n+2} ··· D_{n-3} ··· D_{n-5}	D_{n-5}
DOWN	X	L	D_{n+3}	D_{n+2} ··· D_{n-3} ··· D_{n-5}	D_{n-5}
DOWN	X	H	D_{n+3}	Off	D_{n-5}

Note: $\overline{OUT0 \sim 7}$ = on in case of D_n = H level and $\overline{OUT0 \sim 7}$ = off in case of D_n = level.
A resistor is connected with R−EXT and GND accompanied with outside, and it is necessary that a correct power supply voltage is supplied.

TIMING DIAGRAM



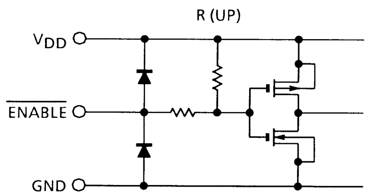
Note: Latches are level sensitive, not rising edge sensitive and not syncronus CLOCK.
Input of LATCH −terminal to H Level, data passes latches, and input to L level, data hold latches.
Input of ENABLE −terminal to H level, all output (OUT0 ~ 7) do off.

TERMINAL DISCRIPTION

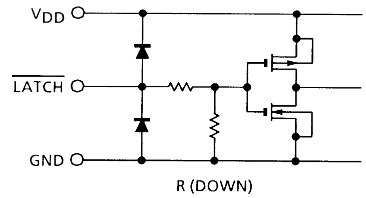
PIN No.	PIN NAME	FUNCTION
5	HIGH / LOW	It is the terminal which does switching for the big current / low current.
6, 15	POWER−GND	GND terminal for current output.
1	LOGIC−GND	GND terminal for control logic.
2	SERIAL−IN	Input terminal of a serial−data for shift−register.
3	CLOCK	Input terminal of a clock for data shift to up−edge.
4	LATCH	Input terminal of a data strobe. Latches passes data with “H” level input of LATCH−terminal, and hold data with “L” level input.
7~10, 11~14	OUT0 ~ 7	Output terminals.
16	ENABLE	Input terminal of output enable. All outputs (OUT0~7) do off with “H” level input of ENABLE−terminal, and do on with “L” level input.
18	SERIAL−OUT1	Output terminal of serial-data
17	SERIAL−OUT2	Output terminal of a serial−data for next SERIAL−IN terminal.
19	R−EXT	Input terminal of connects with a resister for to set up all output current.
20	V_{DD}	5 V Supply voltage terminal.

EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS

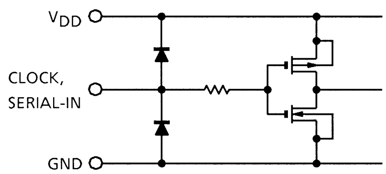
1. $\overline{\text{ENABLE}}$ terminal



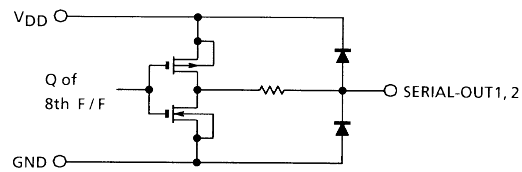
2. $\overline{\text{LATCH}}$ terminal



3. CLOCK, SERIAL−IN terminal



4. SERIAL−OUT terminal



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	0 ~ +7.0	V
Input Voltage	V_{IN}	−0.4 ~ V_{DD} +0.4	V
Output Current	I_{OUT}	+150 (HIGH / LOW = "H")	mA / ch
		+70 (HIGH / LOW = "L")	
Output Voltage	V_{OUT}	−0.5 ~ +17.0	V
Clock Frequency	f_{CLK}	15	MHz
GND Terminal Current	I_{GND}	1200	mA
Power Dissipation	P_{D1}	FN−type : 0.71 (FREE AIR, Ta = 25°C	W
	P_{D2}	FN−type : 0.96 (ON PCB, Ta = 25°C)	
Thermal Resistance	$R_{th\ (j\text{-}a)\ 1}$	175 (FREE AIR)	°C / W
	$R_{th\ (j\text{-}a)\ 2}$	130 (ON PCB)	
Operating Temperature	T_{opr}	−40 ~ +85	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

Note: FN type: Ambient temperature delated above 25°C in the proportion of 7.69 mW / °C
Condition = On PCB (50 × 50 × 1.6 mm Cu = 40%)

RECOMMENDED OPERATING CONDITION (Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Output Voltage	VOUT		—	—	15.0	V
Output Current	I_{OUT1}	DC 1 circuit (HIGH / LOW = "H")	50	—	130	mA / ch
	I_{OUT2}	DC 1 circuit (HIGH / LOW = "L")	2	—	60	
	I_{OH}	SERIAL−OUT1, 2	—	—	−1.0	mA
	I_{OL}	SERIAL−OUT1, 2	—	—	1.0	
Input Voltage	V_{IH}	VDD = 4.5~5.5 V	0.7 V_{DD}	—	V_{DD} + 0.3	V
	V_{IL}		−0.3	—	0.3 V_{DD}	
$\overline{\text{LATCH}}$ Pulse Width	$t_{w\ \overline{LAT}}$		100	—	—	ns
CLOCK Pulse Width	$t_{w\ CLK}$		50	—	—	ns
$\overline{\text{ENABLE}}$ Pulse Width	$t_{w\ \overline{EN}}$		1000	—	—	ns
Set−up Time for DATA	$t_{setup\ (D)}$		60	—	—	ns
Hold Time for DATA	$t_{hold\ (D)}$		20	—	—	ns
Set−up Time for $\overline{\text{LATCH}}$	$t_{setup\ (L)}$		100	—	—	ns
Hold Time for $\overline{\text{LATCH}}$	$t_{hold\ (L)}$		60	—	—	ns
Clock Frequency	f_{CLK}	V_{DD} = 4.5~5.5 V, Cascade Operation	10.0	—	—	MHz
Power Dissipation	P_D	Ta = 85°C (FN−type On PCB)	—	—	0.50	W

ELECTRICAL CHARACTERISTICS (Ta = 25°C unless otherwise noted)

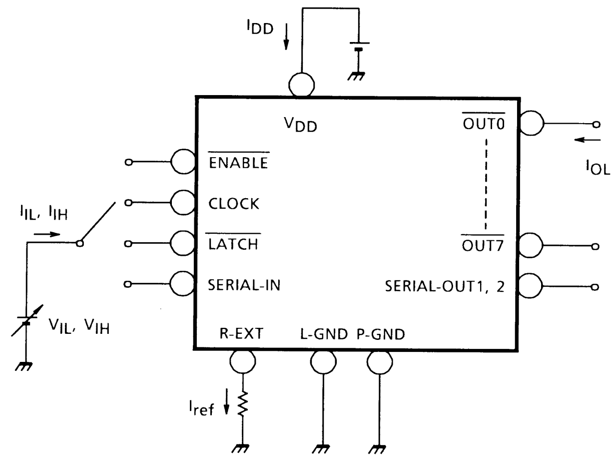
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	CONDITION		MIN	TYP.	MAX	UNIT
Input Voltage	"H" Level	V_{IH}	1	—		0.7 V_{DD}	—	V_{DD}	V
	"L" Level	V_{IL}		—		GND	—	0.3 V_{DD}	
Output Leakage Current		I_{OH}	1	V_{OH} = 15.0 V		—	—	10	μA
Output Voltage	SERIAL−OUT 1, 2	V_{OH}	1	I_{OL} = −1.0 mA		—	—	0.4	V
		V_{OL}		I_{OL} = +1.0 mA		4.6	—	—	
Output Current 1		I_{OL1}	1	V_{CE} = 0.7 V	R_{EXT} = 520 Ω, HIGH / LOW = "L"	31.7	37.5	43.1	mA
	Current Skew	dI_{OL1}				—	±1.5	±6.0	%
Output Current 2		I_{OL2}	1	V_{CE} = 1.0 V	R_{EXT} = 160 Ω, HIGH / LOW = "H"	104.0	123.0	141.4	mA
	Current Skew	dI_{OL2}				—	±1.5	±6.0	%
Supply Voltage Regulation		% / V_{DD}	1	Ta = −40~ +85°C		—	+1.5	+5.0	% / V
Pull−up Resistor		$R_{IN\ (up)}$	1			100	200	400	kΩ
Pull−down Resistor		$R_{IN\ (down)}$				100	200	400	
Supply Current	"OFF"	$I_{DD\ (off)\ 1}$	1	R_{EXT} = OPEN	$\overline{OUT0 \sim 7}$ = off	—	1.0	2.0	mA
		$I_{DD\ (off)\ 2}$		R_{EXT} = 260 Ω	$\overline{OUT0 \sim 7}$ = off	—	10.0	15.0	
		$I_{DD\ (off)\ 3}$		R_{EXT} = 160 Ω	$\overline{OUT0 \sim 7}$ = off	—	16.0	21.0	
	"ON"	$I_{DD\ (on)\ 1}$		R_{EXT} = 260 Ω	$\overline{OUT0 \sim 7}$ = on	—	23.1	40.5	
		$I_{DD\ (on)\ 2}$		R_{EXT} = 160 Ω	$\overline{OUT0 \sim 7}$ = on	—	33.0	62.1	

SWITCHING CHARACTERISTICS (Ta = 25°C unless otherwise noted)

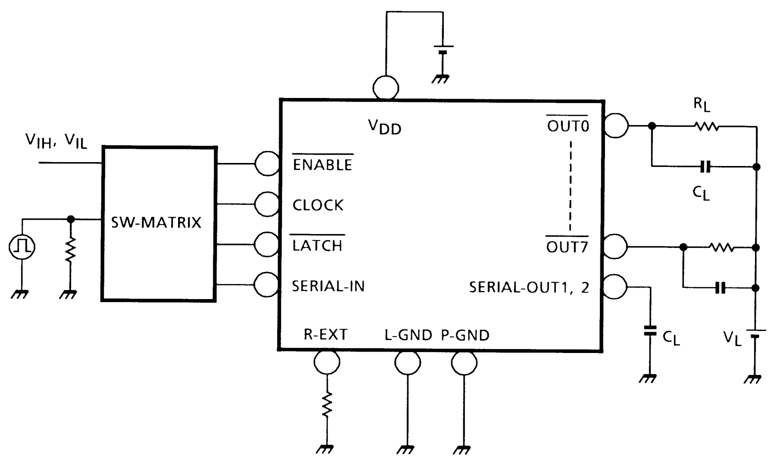
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	CONDITION	MIN	TYP.	MAX	UNIT
Propagation Delay Time ("L" To "H")	SIN− $\overline{OUTn}$	t_{pLH}	2	V_{DD} = 5.0 V V_{CE} = 1.0 V V_{IH} = V_{DD}, V_{IL} = GND R_{EXT} = 260 Ω, R_L = 32 Ω I_{OUT} = 125 mA, C_L = 10.5 pF t_{or} : 10% to 90% t_{or} : 90% to 10% t_{pLH} : 50% to 10% t_{pHL} : 50% to 90%	—	500	1000	ns
	$\overline{LATCH}$ − $\overline{OUTn}$				—	500	1000	
	$\overline{ENABLE}$ − $\overline{OUTn}$				—	500	1000	
	CLK−SOUTn				—	30	70	
Propagation Delay Time ("H" To "L")	SIN− $\overline{OUTn}$	t_{pHL}	2		—	500	1000	ns
	$\overline{LATCH}$ − $\overline{OUTn}$				—	500	1000	
	$\overline{ENABLE}$ − $\overline{OUTn}$				—	500	1000	
	CLK−SOUTn				—	30	70	
Pulse Width	CLK	$t_{w\ CLK,\ /\ CLK}$	2		—	20	30	ns
	$\overline{LATCH}$	$t_{w\ \overline{LAT}\ ,\ /\ LAT}$			—	10	25	
Set−Up Time for LATCH / SIN	L−H	$t_{setup\overline{LAT}}$ & SIN	2		—	25	50	ns
	H−L				—	25	50	
Hold Time for LATCH / SIN	L−H	t_{hold} $\overline{LAT}$ / SIN	2		—	0	15	ns
	H−L				—	0	15	
Maximum CLOCK Rise Time		t_r	2		—	—	10	μs
Maximum CLOCK Fall Time		t_f	2		—	—	10	μs
Output Rise Time		t_{or}	2		300	600	1000	ns
Output Fall Time		t_{of}	2		300	600	1000	ns

TEST CIRCUIT

DC characteristic

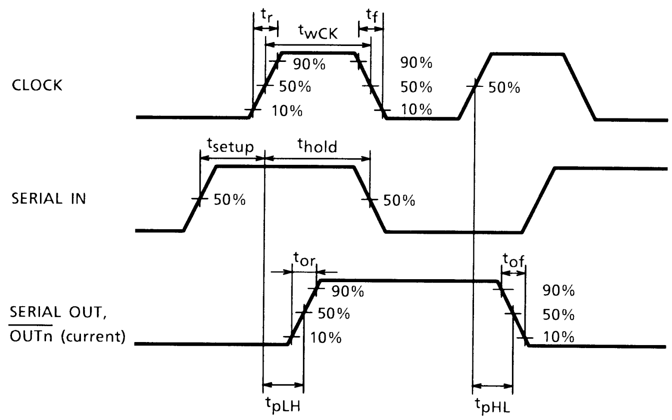


AC characteristic

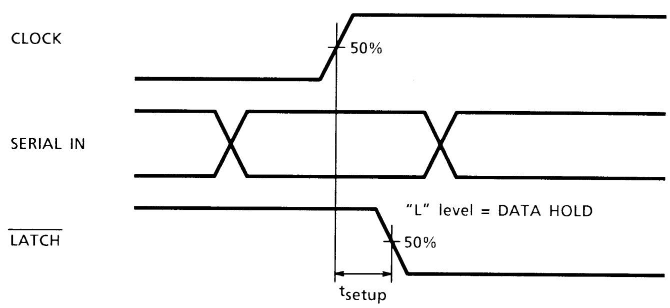


TIMING WAVEFORM

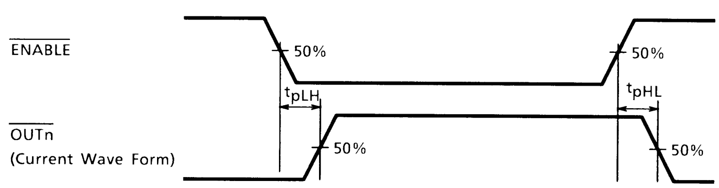
1. CLOCK−SERIAL OUT, $\overline{OUTn}$

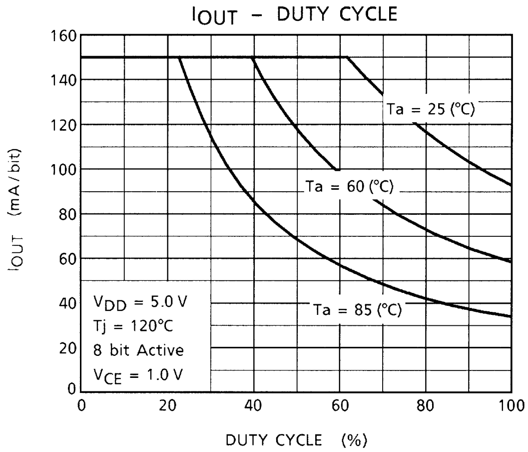


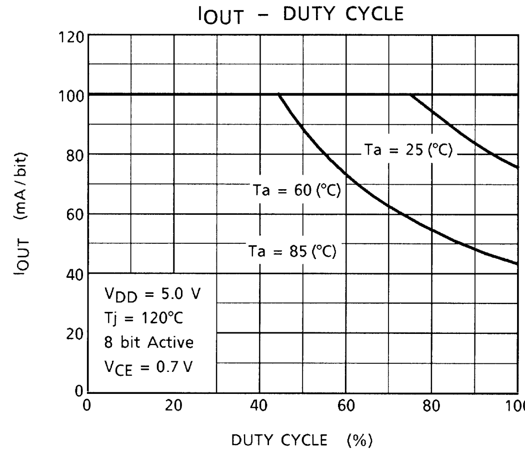
2. CLOCK−$\overline{LATCH}$

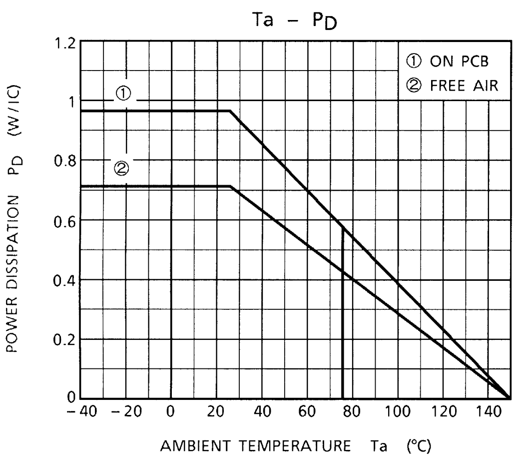


3. $\overline{ENABLE}$−OUTn

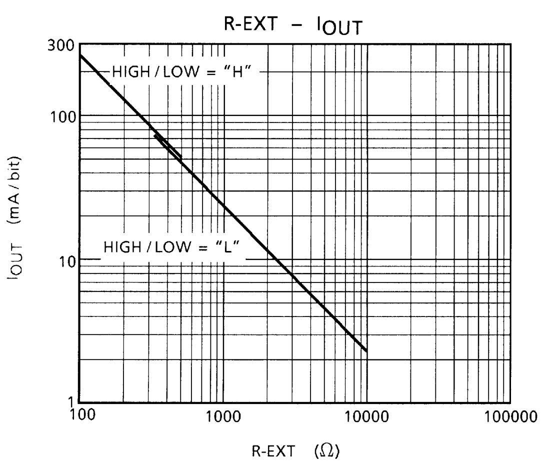


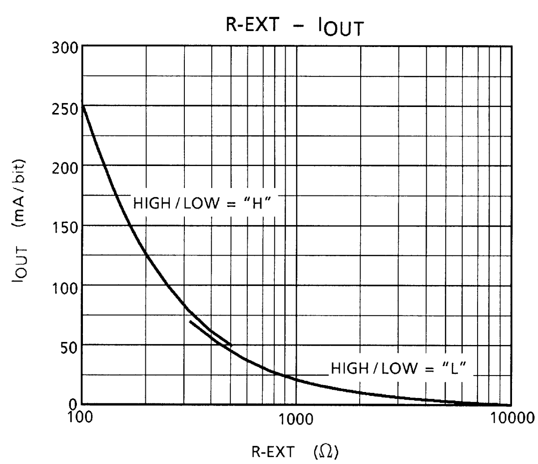






LED DRIVER TB6270X SERIES APPLICATION NOTE





I_{OUT} = {1.26 (V)/R_{EXT} (Ω)} × 15.5 (HIGH/LOW = "L")
I_{OUT} = {1.26 (V)/R_{EXT} (Ω)} × 15.6 (HIGH/LOW = "H")

TOTAL SUPPLY VOLTAGE (V_{LED})

This device can operate 0.7 V (V_O).
When a higher voltage is input to the device, the excess voltage is consumed inside the device, that leads to power dissipation.
In order to minimize power dissipation and loss, we would like to recommend to set the total supply voltage as shown below,

V_{LED} (total supply voltage) = V_{CE} (Tr V_{sat}) + V_f (LED Forward voltage) + V_O (IC supply voltage)

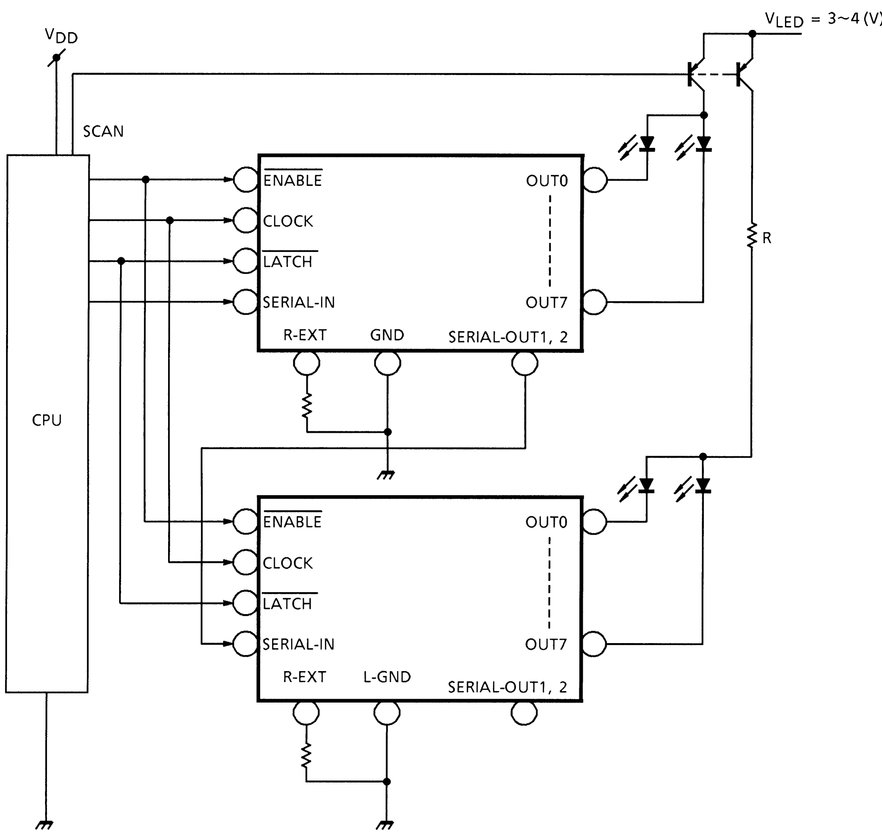
When the total supply is too high considering the power dissipation of this device, an additional R can decrease the supply voltage.

$$R = \frac{V_{LED} - V_{f\,(LED)} - V_{O\,(Min.)}}{I_{O\,(Max.)} \times BIT\ (Max.)}$$

PATTERN LAYOUT

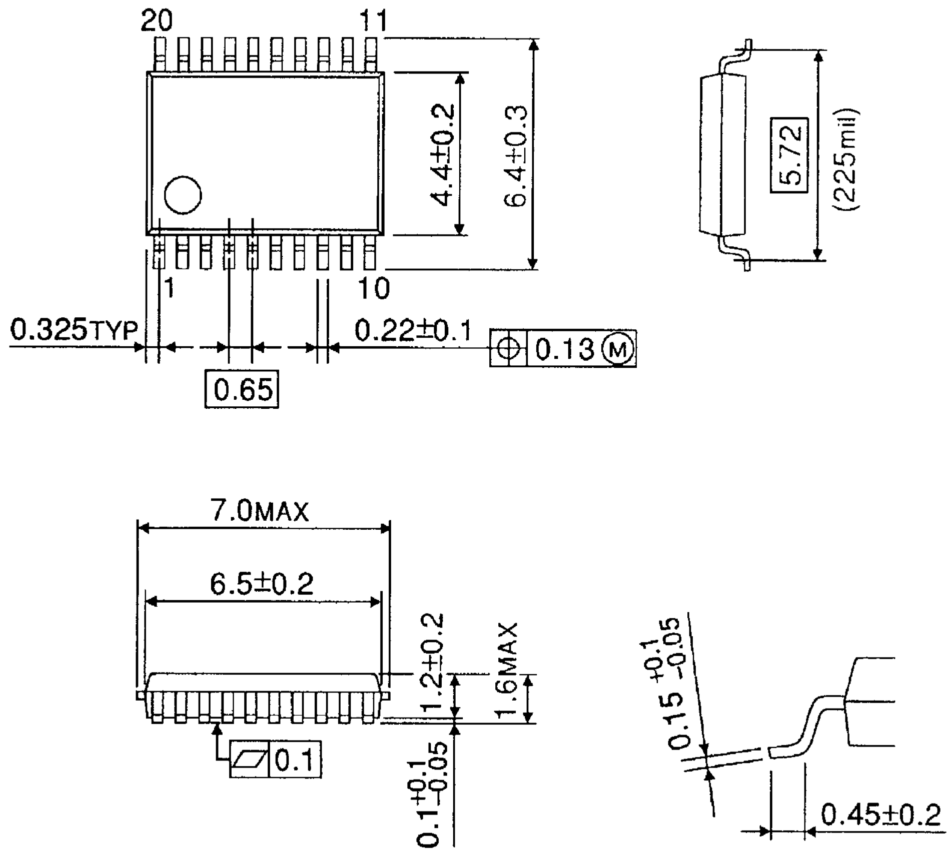
This device owns only one ground pin that means signal ground pin power ground pin are common. If ground pattern layout contains large inductance and impedance, and the voltage between ground and $\overline{\text{LATCH}}$, CLOCK terminals exceeds 2.5 V by switching noise in operation, this device may miss−operated.
So we would like you to pay attention to pattern layout to minimize inductance.

APPLICATION CIRCUIT



Package Dimensions

SSOP20-P-225-0.65A Unit : mm



Weight: 0.14 g (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only.
Thorough evaluation is required, especially at the mass production design stage.
Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

(5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to Remember on Handling of ICs

(1) Heat Radiation Design
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (Tj) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(2) Back-EMF
When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor’s power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device’s motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

RESTRICTIONS ON PRODUCT USE