

TB62710P, TB62710F, TB62710FN

8-Bit Constant-Current LED Driver for Cathode Common LED

The TB62710P, TB62710F and TB62710FN are specifically designed for use as LED and LED display (cathode-common) Constant-current drivers.

The constant-current output circuits can be set up using an external resistor ($I_{OUT} = -90 \text{ mA max}$).

These ICs are monolithic integrated circuits have been designed using the Bi-CMOS process.

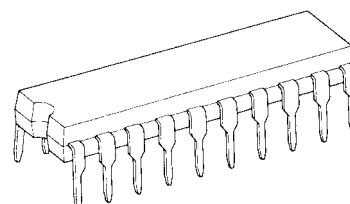
The devices consist of an 8-bit shift register, a latch, an ANDgate and constant-current drivers.

FEATURES

- Constant-current output:
A single resistor can be used to set any output current in the range $-5 \sim -90 \text{ mA}$.
- Maximum clock frequency: $f_{CLK} = 15 \text{ MHz}$
(operating while connected in cascade, $T_{opr} = 25^\circ\text{C}$)
- 5-V CMOS compatible input
- Packages:
P-type: DIP20-P-300-2.54A
F-type: SSOP24-P-300-1.00
FN-type: SSOP20-P-225-0.65A
- Constant-output-current accuracy:

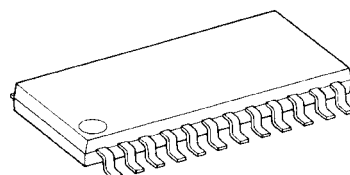
Output - GND Voltage	Current accuracy		Output Current (max)
	between bits	between ICs	
$\geq 2.0 \text{ V (min)}$	$\pm 6\%$	$\pm 15\%$	$-5 \sim -90 \text{ mA}$
$\geq 1.5 \text{ V (min)}$			$-5 \sim -40 \text{ mA}$

TB62710P



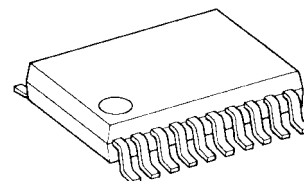
DIP20-P-300-2.54A

TB62710F



SSOP24-P-300-1.00

TB62710FN



SSOP20-P-225-0.65A

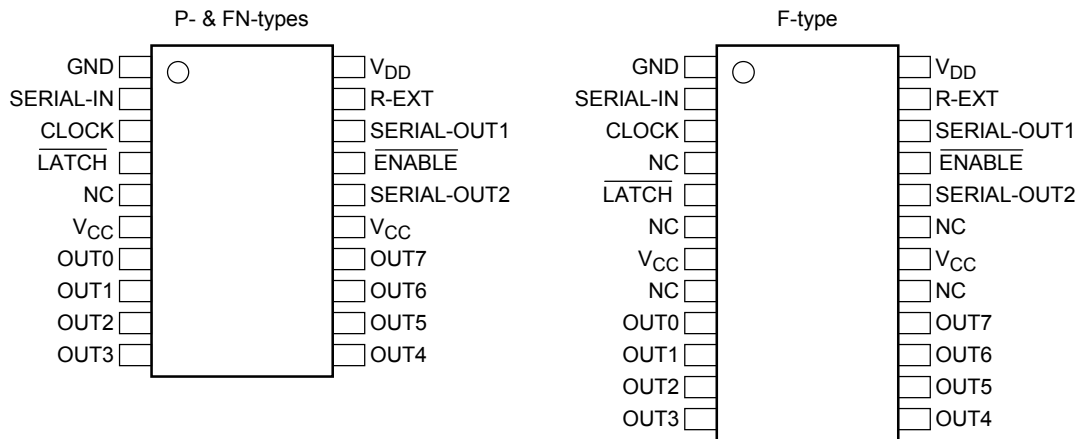
Weight

DIP20-P-300-2.54A: 2.25 g (Typ.)

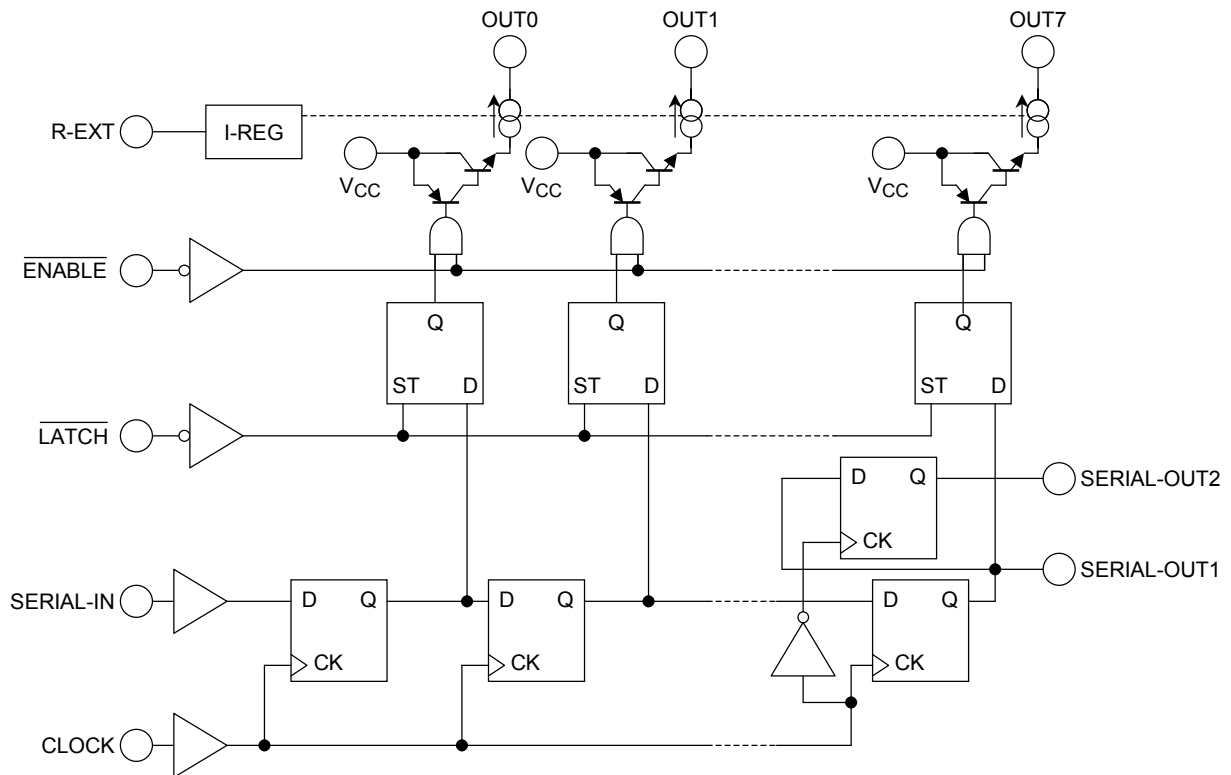
SSOP24-P-300-1.00: 0.33 g (Typ.)

SSOP20-P-225-0.65A: 0.10 g (Typ.)

Pin Assignment (top view)



Block Diagram



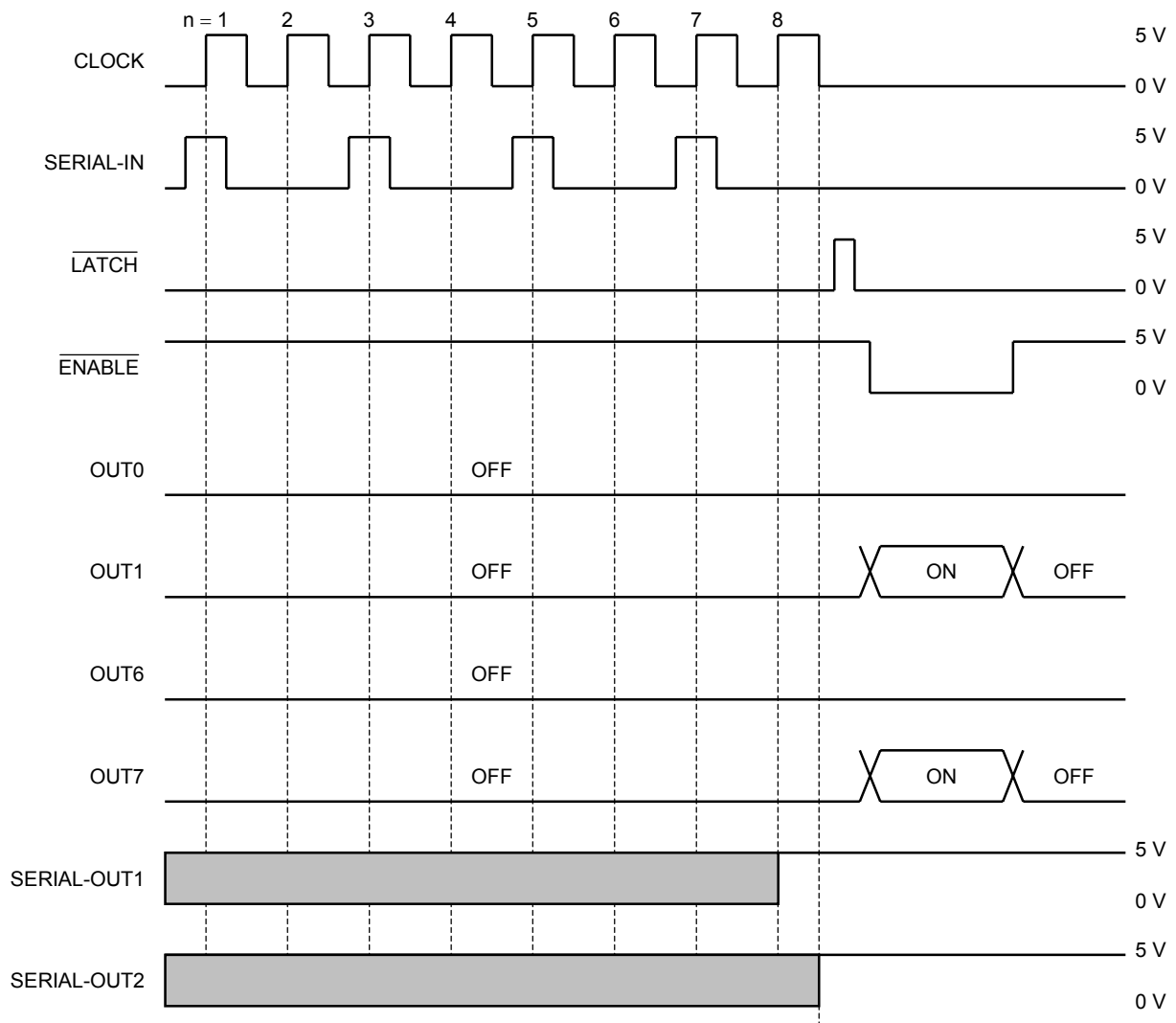
Truth Table

CLOCK	LATCH	ENABLE	SERIAL-IN	OUT0... OUT5 ... OUT7	SERIAL-OUT
	H	L	D _n	D _n ... D _{n-5} ... D _{n-7}	D _{n-7}
	L	L	D _{n+1}	No Change	D _{n-6}
	H	L	D _{n+2}	D _{n+2} ... D _{n-3} ... D _{n-5}	D _{n-5}
	X	L	D _{n+3}	D _{n+2} ... D _{n-3} ... D _{n-5}	D _{n-5}
	X	H	D _{n+3}	OFF	D _{n-5}

Note 1: OUT0~OUT7 = ON when D_n = "H"; OUT0~OUT7 = OFF when D_n = "L".

In order to ensure that the level of the power supply voltate is correct, an external resistor must be connected between R-EXT and GND.

Timing Diagram



Note 2: The latches circuit holds data by pulling the $\overline{\text{LATCH}}$ terminal Low.

And, when $\overline{\text{LATCH}}$ terminal is a "H" level, latch circuit doesn't hold data, and it passes from the input to the output.

When $\overline{\text{ENABLE}}$ terminal is a "L" level, output terminal OUT0~ OUT7 respond to the data, and on & off does.

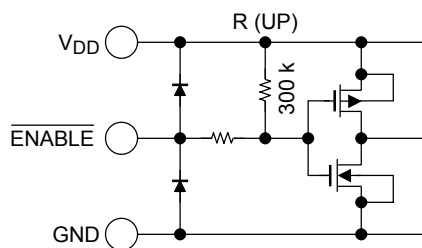
And, when $\overline{\text{ENABLE}}$ terminal is a "H" level, it offs with the output terminal regardless of the data.

Terminal Description

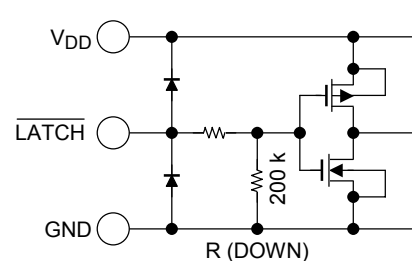
Pin No.		Pin Name	Function
P/FN-Type	F-Type		
1	1	GND	GND terminal for control logic
2	2	SERIAL-IN	Input terminal for serial data for data shift register
3	3	CLOCK	Input terminal for clock for data shift on rising edge
4	5	$\overline{\text{LATCH}}$	Input terminal for data strobe When the $\overline{\text{LATCH}}$ input is driven High, data is latched. When it is pulled Low, data is hold.
6, 15	7, 18	V _{CC}	0 V~17 V supply voltage terminal for LED
7~14	9~16	OUT0~OUT7	Output terminals
17	21	$\overline{\text{ENABLE}}$	Input terminal for output enable. All outputs (OUT0~OUT7) are turned off, when the $\overline{\text{ENABLE}}$ terminal is driven High. And are turned on, when the terminal is driven Low.
16	20	SERIAL-OUT2	Output terminal for serial data input on SERIAL-IN terminal
18	22	SERIAL-OUT1	Output terminal for serial data input on SERIAL-IN terminal
19	23	R-EXT	Input terminal used to connect an external resistor. This regulated the output current.
20	24	V _{DD}	5-V supply voltage terminal
5	4, 6, 8, 17, 19	NC	Not connected

Equivalent Circuits For Inputs and Outputs

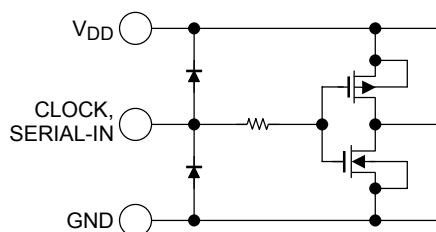
$\overline{\text{ENABLE}}$ terminal



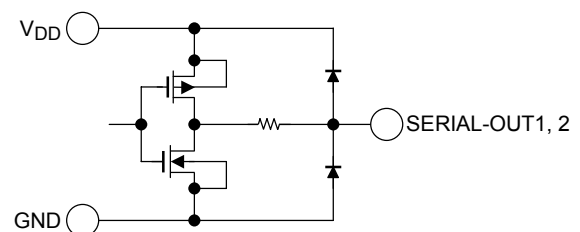
$\overline{\text{LATCH}}$ terminal



CLOCK, SERIAL-IN terminal



SERIAL-OUT1 and SERIAL-OUT2 terminals



Maximum Ratings (T_{opr} = 25°C)

Characteristic		Symbol	Rating	Unit
Supply voltage		V _{DD}	0~7.0	V
Supply voltage for LED		V _{LED}	0~17.0	V
Input voltage		V _{IN}	-0.4~V _{DD} + 0.4	V
Output current		I _{OUT}	-90	mA
Output voltage		V _{OUT}	-0.4~17	V
Clock frequency		f _{CLK}	15	MHz
V _{CC} terminal current		I _{VCC}	1440	mA
Power Dissipation (Note 3)	P-type (when not mounted)	P _{d1}	1.47	W
	F-type (when not mounted)	P _{d2}	0.59	
	F-type (on PCB)		0.83	
	FN-type (when not mounted)	P _{d3}	0.71	
	FN-type (on PCB)		0.96	
Thermal Resistance (Note 3)	P-type (when not mounted)	R _{th (j-a) 1}	85	°C/W
	F-type (when not mounted)	R _{th (j-a) 2}	210	
	F-type (on PCB)		150	
	FN-type (when not mounted)	R _{th (j-a) 3}	175	
	FN-type (on PCB)		130	
Operating Temperature		T _{opr}	-40~85	°C
Storage Temperature		T _{stg}	-55~150	°C

Note 3: P-Type: Power dissipation is derated by 12.5 mW/°C if device is mounted on PCB and ambient temperature is above 25°C.

F-Type: Power dissipation is derated by 6.7 mW/°C if device is mounted on PCB and ambient temperature is above 25°C.

With device mounted on PCB of 60% Cu and of dimensions 50 mm × 50 mm × 1.6 mm

FN-Type: Power dissipation is derated by 7.7 mW/°C if device is mounted on PCB and ambient temperature is above 25°C.

With device mounted on PCB of 40% Cu and of dimensions 50 mm × 50 mm × 1.6 mm

Recommended Operating Conditions ($T_{opr} = -40^{\circ}\text{C} \sim 85^{\circ}\text{C}$ unless otherwise specified)

Characteristic		Symbol	Conditions		Min	Typ.	Max	Unit
Supply voltage		V _{DD}	—		4.5	5.0	5.5	V
Supply voltage for LED		V _{CC1}	V _{CC} – V _{OUT} ≥ 2.0 V, I _{OUT} ≤ –90 mA		4	—	17	V
		V _{CC2}	V _{CC} – V _{OUT} ≥ 1.5 V, I _{OUT} ≤ –40 mA		3.5	—	17	
Output voltage		V _{OUT}	V _{CC} common		0	—	–17	V
Output current		I _{OUT}	DC1 circuit		–5	—	–78	mA
		I _{OH}	SERIAL-OUT1, 2		—	—	–1.0	
		I _{OL}	SERIAL-OUT1, 2		—	—	1.0	
Input voltage		V _{IH}	V _{DD} = 4.5~5.5 V		0.7 V _{DD}	—	V _{DD} + 0.3	V
		V _{IL}			–0.3	—	0.3 V _{DD}	
$\overline{\text{LATCH}}$ pulse width		t _{wLAT}	V _{DD} = 4.5~5.5 V		100	—	—	ns
CLOCK pulse width		t _{wCLK}	V _{DD} = 4.5~5.5 V		50	—	—	ns
$\overline{\text{ENABLE}}$ pulse width		t _{wENA}	V _{DD} = 4.5~5.5 V		1000	—	—	ns
Set-up time for DATA		t _{setup}	V _{DD} = 4.5~5.5 V		100	—	—	ns
Hold time for DATA		t _{hold}	V _{DD} = 4.5~5.5 V		100	—	—	ns
Clock frequency		t _{CLK}	V _{DD} = 4.5~5.5 V, Cascade operation		—	—	10.0	ns
Power Dissipation	P-type	P _{d1}	T _{opr} = 85°C	When not mounted	—	—	0.76	W
	F-type	P _{d2}		On PCB	—	—	0.43	
	FN-type	P _{d3}			—	—	0.50	

Electrical Characteristics ($T_{opr} = 25^{\circ}\text{C}$, $V_{DD} = 5\text{ V}$, $V_{CC} = 17\text{ V}$ unless otherwise specified)

Characteristic		Symbol	Test circuit	Conditions		Min	Typ.	Max	Unit
Output leakage current		I _{LEAK}	—	V _{CC} = 17.0 V		—	—	−10	μA
Output voltage	SERIAL-OUT 1, 2	V _{OH}	—	I _{OH} = −1.0 mA		—	—	0.4	V
		V _{OL}	—	I _{OL} = 1.0 mA		4.6	—	—	
Output current (including current skewing)		I _{OUT1}	—	V _{CC} = 4 V, V _{OUT} = V _{CC} − 2.0 V	R _{EXT} = 360 Ω	−62.1	−73.0	−83.9	mA
		I _{OUT2}	—	V _{CC} = 4 V, V _{OUT} = V _{CC} − 2.0 V	R _{EXT} = 620 Ω	−34.0	−40.0	−46.0	
		I _{OUT3}	—	V _{CC} = 3.5 V, V _{OUT} = V _{CC} − 1.5 V	R _{EXT} = 620 Ω	−32.3	−38.0	−43.7	
	Current skew	ΔI _{OUT}	—	Same as I _{OUT1} , I _{OUT2} and I _{OUT3}		—	±1.5	±6.0	%
Supply voltage regulation		%/V _{DD}	—	T _a = −40~85°C	R _{EXT} = 360 Ω	—	1.5	5.0	%/V
Pull-up resistor		R _{in} (Up)	—	—		150	300	600	kΩ
Pull-down resistor		R _{in} (Down)	—	—		100	200	400	kΩ
Supply current	V _{DD}	I _{DD} (OFF)	—	All outputs = OFF	R _{EXT} = OPEN	—	0.6	1.2	mA
		I _{DD} (ON) 1	—	DATA = ALL “H”, All outputs = ON (no load)	R _{EXT} = 360 Ω	—	7.5	10.0	
		I _{DD} (ON) 2	—	DATA = ALL “H”, All outputs = ON (no load)	R _{EXT} = 620 Ω	—	4.0	7.0	
	V _{CC}	I _{CC} (OFF)	—	DATA = ALL “L”, All outputs = OFF (no load)	R _{EXT} = 620 Ω	—	0.5	1.0	
		I _{CC} (ON)	—	DATA = ALL “H”, All outputs = ON (no load)	R _{EXT} = 360 Ω	—	42.0	52.0	

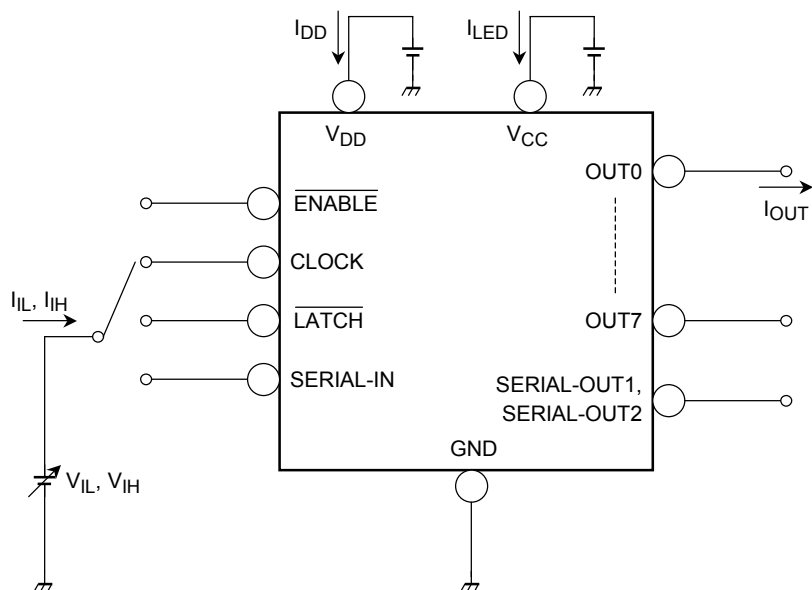
Switching Characteristics ($T_{opr} = 25^{\circ}\text{C}$ unless otherwise specified)

Characteristic		Symbol	Test circuit	Conditions	Min	Typ.	Max	Unit
Propagation delay time ("L" to "H")	CLK-OUTn	t_{pLH}	—	$V_{DD} = 5.0\text{ V}$, $V_{CC} = 17.0\text{ V}$ $V_{OUT} = V_{CC} - 2.0\text{ V}$ $V_{IH} = V_{DD}$, $V_{IL} = \text{GND}$ $R_{EXT} = 620\ \Omega$ $C_L = 10.5\text{ pF}$	—	200	450	ns
	$\overline{\text{LATCH}}$ -OUTn		—		—	20	70	
	$\overline{\text{ENABLE}}$ -OUTn		—		—	20	70	ns
	CLK-SOUTn		—		—	20	70	
Propagation delay time ("H" to "L")	CLK-OUTn	t_{pHL}	—		—	60	180	ns
	$\overline{\text{LATCH}}$ -OUTn		—		—	20	70	
	$\overline{\text{ENABLE}}$ -OUTn		—		—	20	70	ns
	CLK-SOUTn		—		—	20	70	
Pulse width	CLK	t_{wCLK}	—	t_{or} : 10~90%	—	20	30	ns
	$\overline{\text{LATCH}}$	t_{wLAT}	—	t_{of} : 90~10%	—	10	25	
Set-up time $\overline{\text{LATCH}}$ / SIN / CLOCK	DATA = "L" → "H"	t_{setup}	—	t_{pLH} : 50~10%	—	25	50	ns
			—	t_{pHL} : 50~90%	—	25	50	
Hold time $\overline{\text{LATCH}}$ / SIN / CLOCK	DATA = "H" → "L"	t_{hold}	—	Set the switching characteristics according to the result of measuring the voltage waveform.	—	0	30	ns
			—		—	0	30	
Slow clock	Rise time (Note 4)	t_r	—		—	—	10	μs
	Fall time (Note 4)	t_f	—		—	—	10	μs
Output rise time		t_{or}	—		25	55	110	ns
Output fall time		t_{of}	—		250	450	600	ns

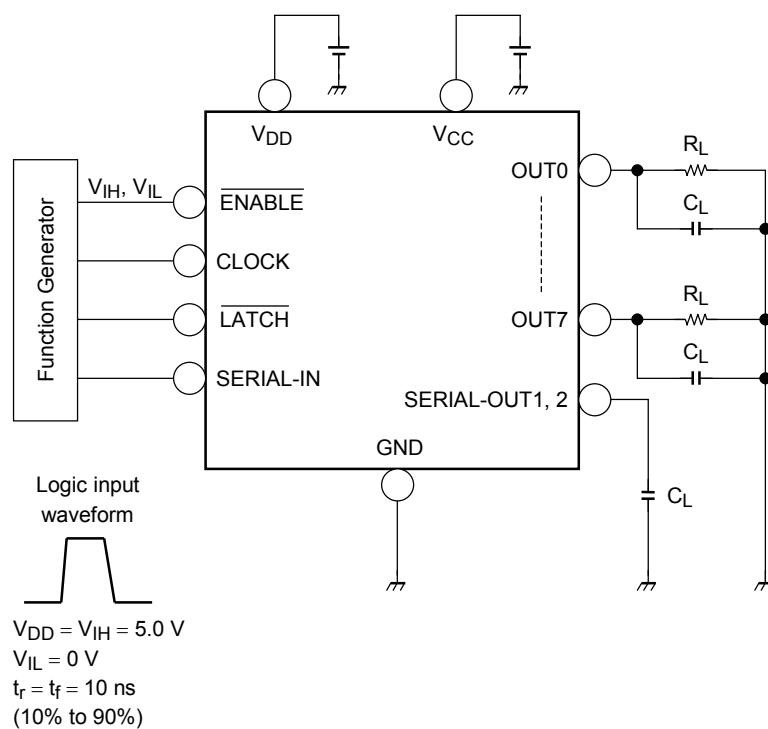
Note 4: If the device is connected in a cascade and t_r/t_f for the waveform is large, it may not be possible to achieve the timing required for data transfer. Please consider the timings carefully.

Test Circuit

DC Characteristic

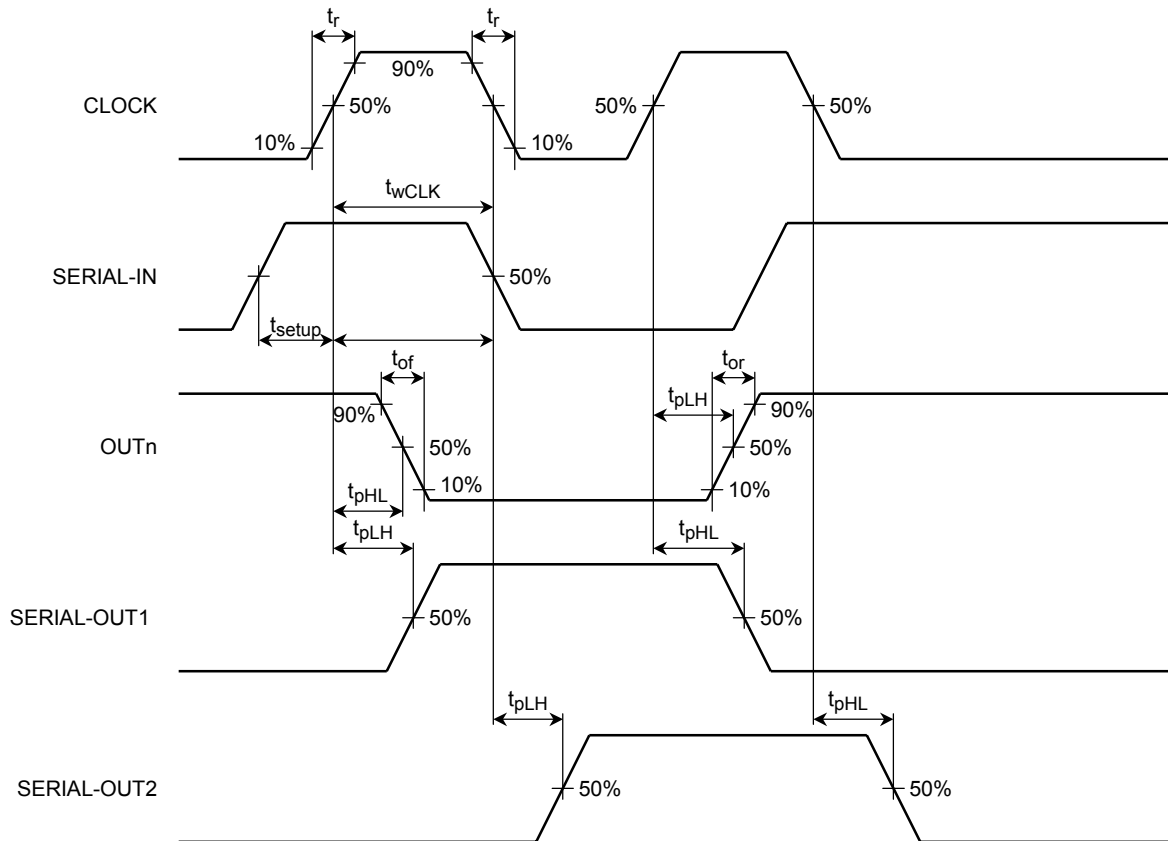


AC Characteristic

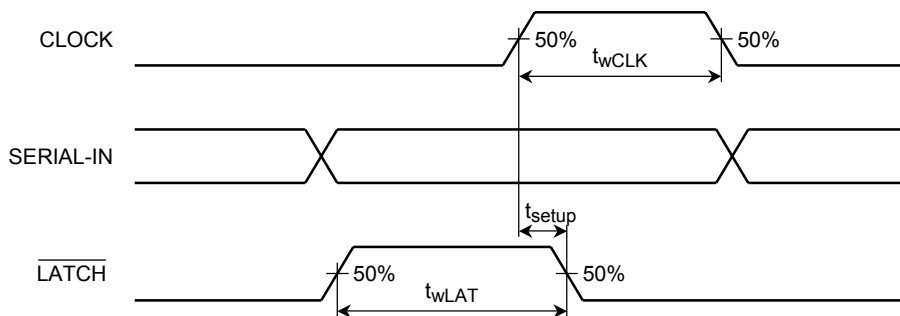


Timing Waveforms

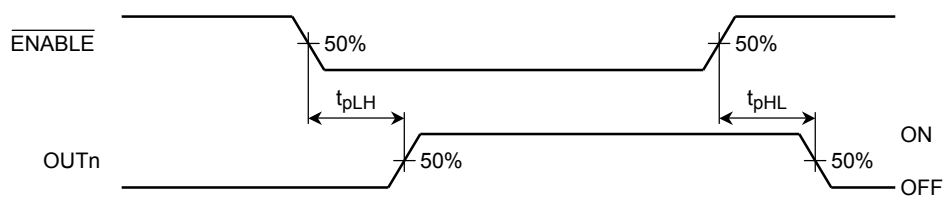
1. CLOCK, SERIAL OUTn



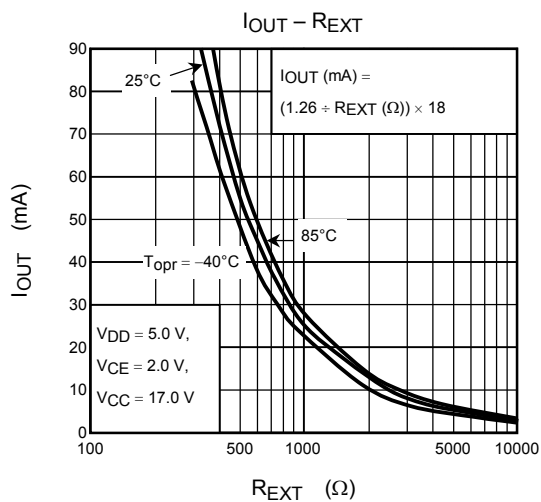
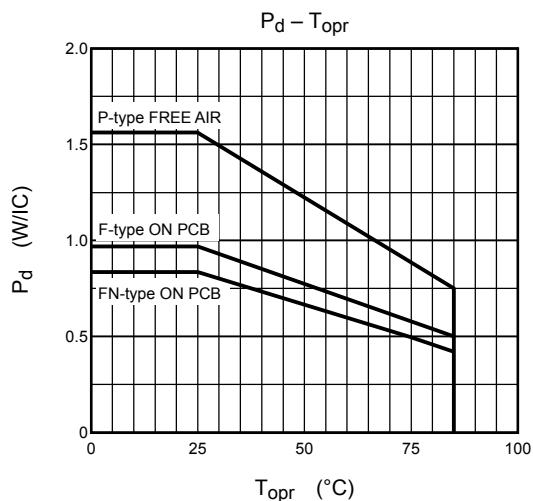
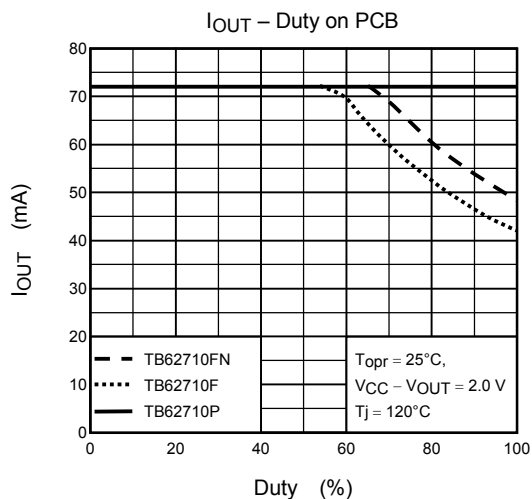
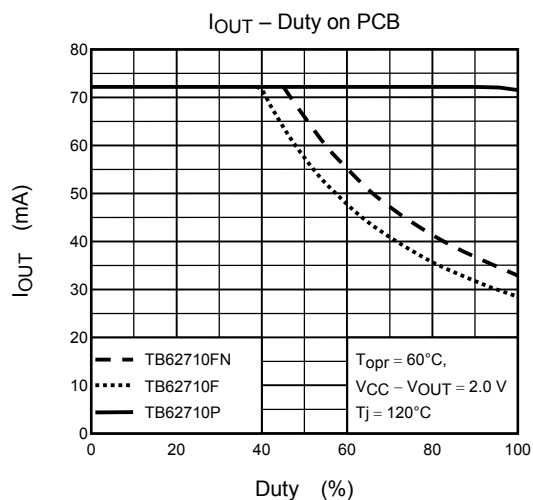
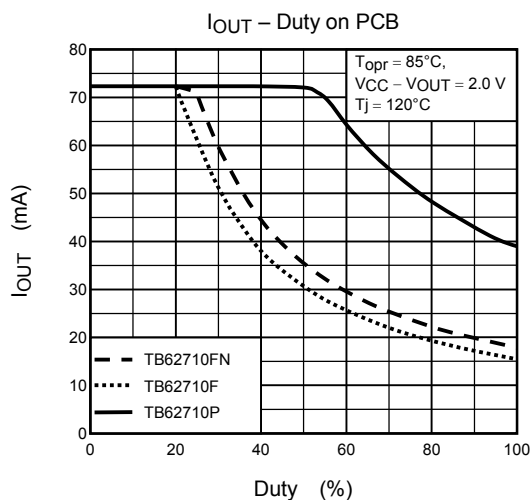
2. CLOCK, $\overline{\text{LATCH}}$

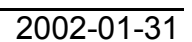


3. $\overline{\text{ENABLE}}$ - OUTn



Reference Data (duty curves + package power dissipation)





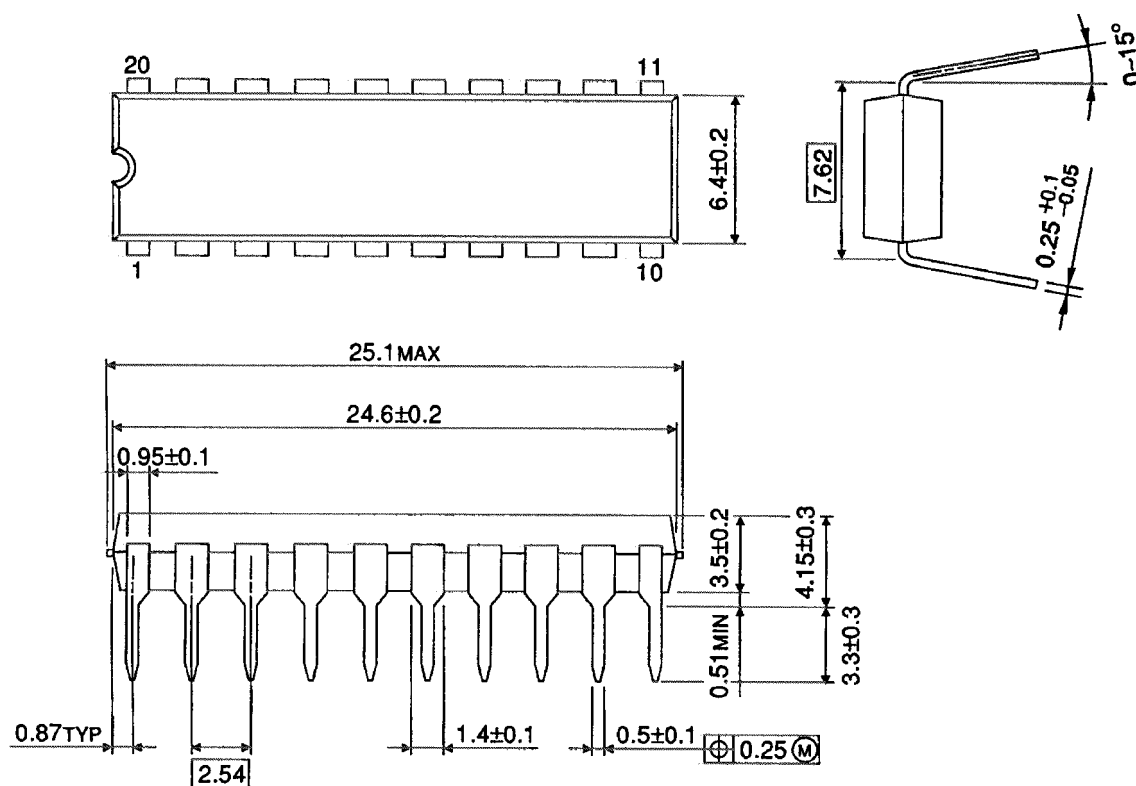
Notes

- Operation may become unstable due to the electromagnetic interference caused by the wiring and other phenomena.
To counter this, it is recommended that the IC be situated as close as possible to the LED module.
If overvoltage is caused by inductance between the LED and the output terminals, both the LED and the terminals may suffer damage as a result.
- There is only one GND terminal on this device when the inductance in the GND line and the resistor are large, the device may malfunction due to the GND noise when output switchings by the circuit board pattern and wiring.
To achieve stable operation, it is necessary to connect a resistor between the REXT terminal and the GND line. Fluctuation in the output waveform is likely to occur when the GND line is unstable or when a capacitor (of more than 50 pF) is used.
Therefore, take care when designing the circuit board pattern layout and the wiring from the controller.
- This application circuit is a reference example and is not guaranteed to work in all conditions.
Be sure to check the operation of your circuits.
- This device does not include protection circuits for overvoltage, overcurrent or overtemperature.
If protection is necessary, it must be incorporated into the control circuitry.
- The device is likely to be destroyed if a short-circuit occurs between either of the power supply pins and any of the output terminals when designing circuits, pay special attention to the positions of the output terminals and the power supply terminals (VDD and VLED), and to the design of the GND line.

Package Dimensions

DIP20-P-300-2.54A

Unit : mm

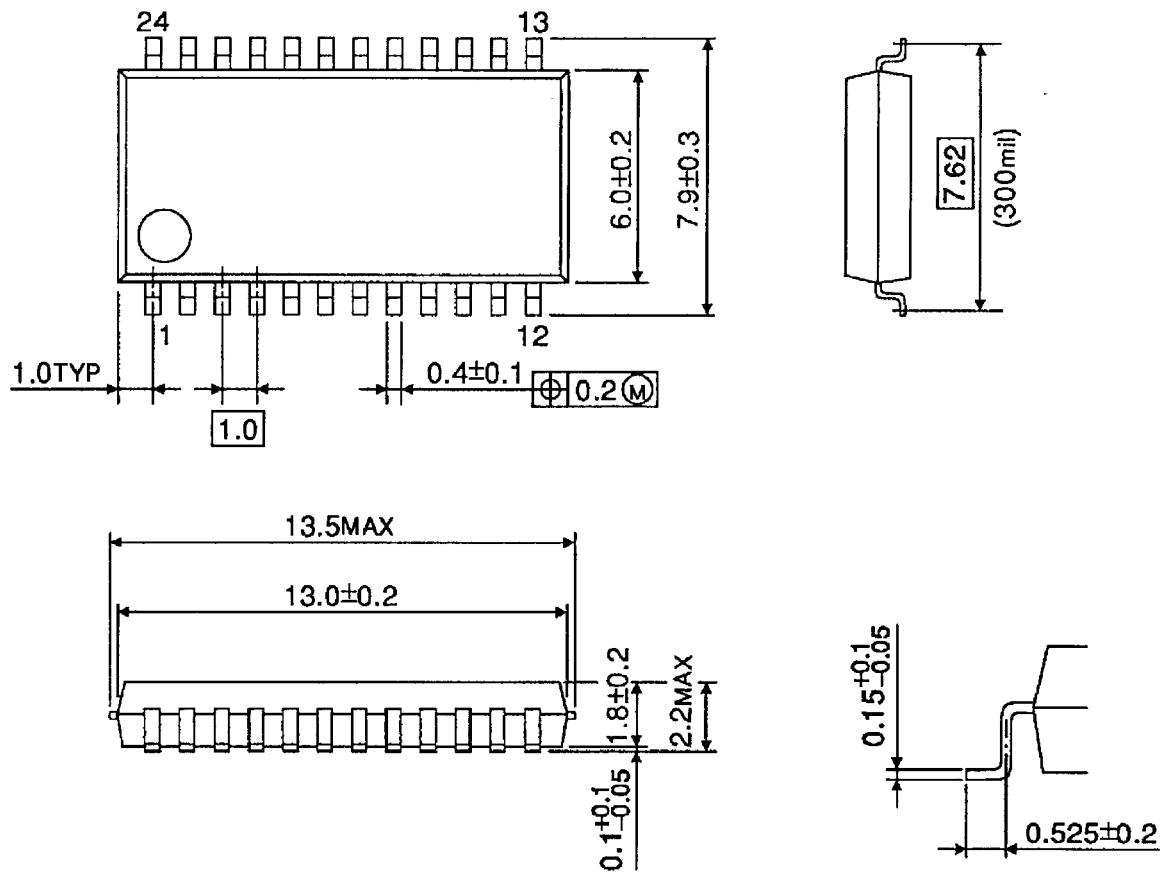


Weight: 2.25 g (typ.)

Package Dimensions

SSOP24-P-300-1.00

Unit : mm

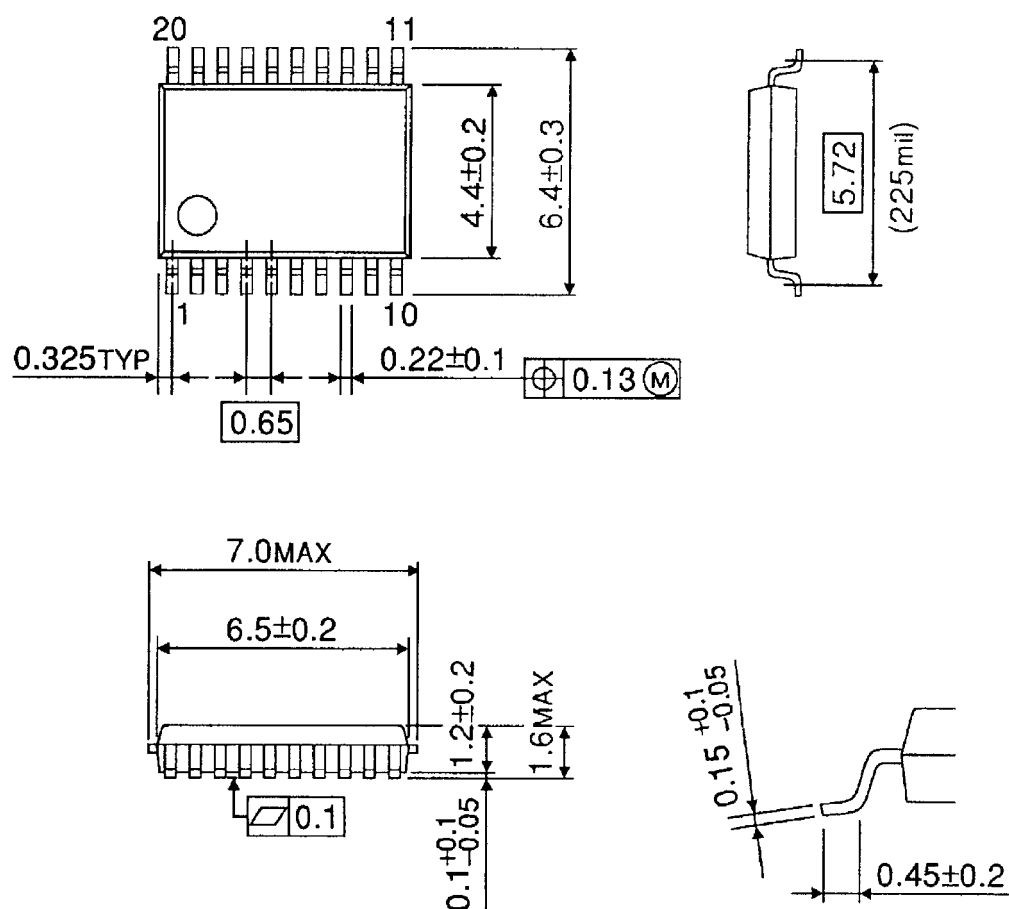


Weight: 0.33 g (typ.)

Package Dimensions

SSOP20-P-225-0.65A

Unit : mm



Weight: 0.10 g (typ.)

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