

TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

# TB62709NG, TB62709FG

## 7-SEGMENT DRIVERS WITH BUILT-IN DECODERS

(COMMON ANODE CAPABILITY, MAXIMUM 4-DIGIT CONTROL)

The TB62709NG and TB62709FG are multifunctional, compact, 7-segment LED display drivers.

These ICs can directly drive 7-segment displays and individual LEDs, and can control either a 4-digit display with decimal points, or 32 individual LEDs.

These ICs can also be used with common-anode displays. Their outputs are constant current, the ampere levels at which are set using an external resistor.

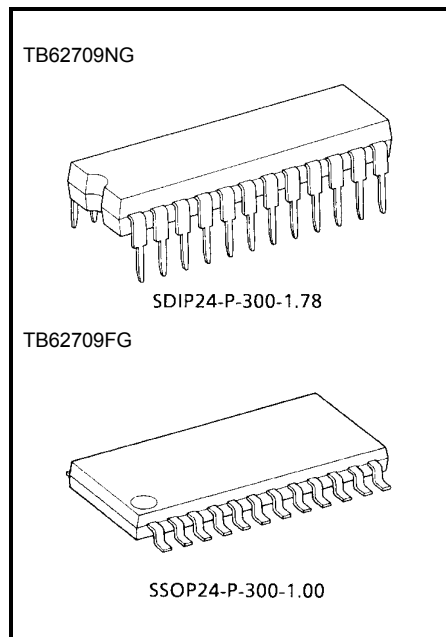
A synchronous serial port connects the IC to the CPU.

The different modes of control provided by this device including Duty Control Register Set, Digit Set, Decode Set and Standby Set, are all based on every 16-bit of serial data.

This devices are a product for the Pb free(Sn-Ag).

## FEATURES

- Control circuit power supply voltage  
:  $V_{DD} = 4.5$  to  $5.5$  V
- Digit output rating  
:  $17$  V /  $-400$  mA
- Decoder output rating  
:  $17$  V /  $50$  mA
- Built-in decoder  
: Decodes the numerals 0 to 9, certain alphabetic characters, and of course blanks code.
- Digit control function  
: Can scan digit outputs DIG-0 to DIG-3 when connected to the common anode pins of a 7-segment display.
- Maximum transmission frequency  
:  $f_{CLK} = 15$  MHz
- Decoder outputs (OUT-A to OUT-Dp)  
Output current can be set up to a 40mA maximum using an external resistor.
- Constant current tolerance ( $T_a = 25^\circ\text{C}$ ,  $V_{DD} = 5.0$  V)  
: Variation between bits =  $\pm 7\%$ , variation between devices (including variation between bits) =  $\pm 15\%$  at  $V_{CE} \geq 0.7$  V
- Package  
: 24-pin SDIP (SDIP24-P-300-1.78)  
24-pin SSOP (SSOP24-P-300-1.00)



Weight

SDIP24-P-300-1.78 : 1.62 g (typ.)

SSOP24-P-300-1.00 : 0.32 g (typ.)

[www.DataSheet4U.com](http://www.DataSheet4U.com)

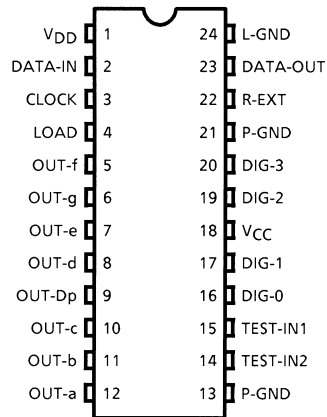
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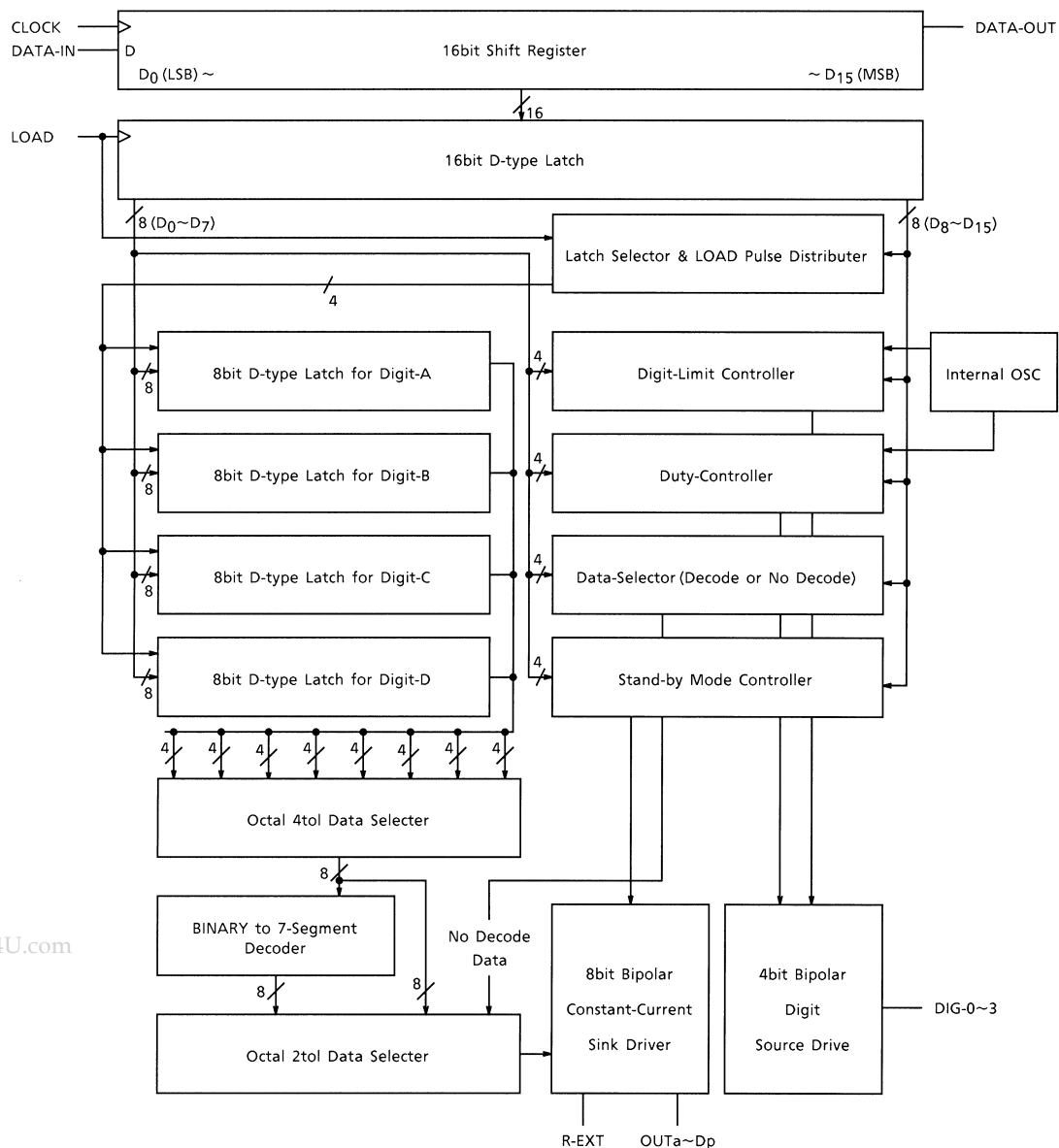
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## PIN ASSIGNMENT (Top view)



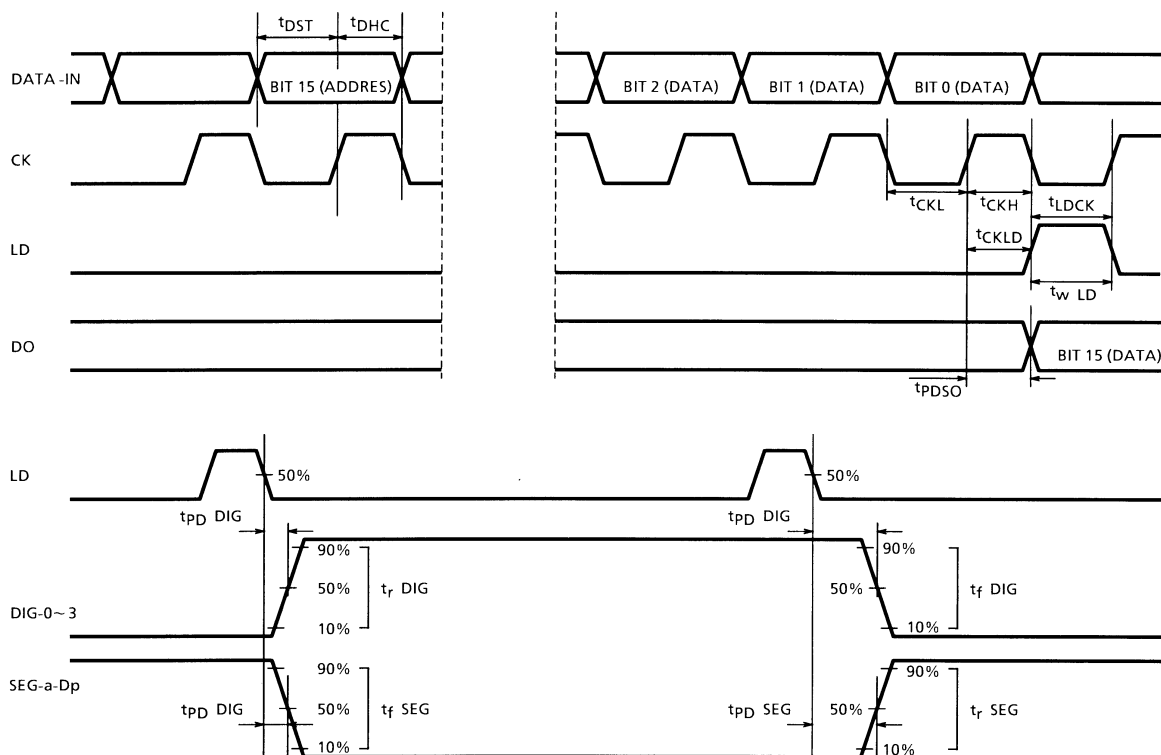
## BLOCK DIAGRAM



**PIN FUNCTIONS**

PIN NUMBER	PIN NAME	FUNCTION
1	V <sub>DD</sub>	5 V power pin.
2	DATA-IN (DI)	Serial data input pin.
3	CLOCK (CK)	Clock input pin. The shift register shifts data on the clock's rising edge.
4	LOAD (LD)	Load signal input pin. The data in the D <sub>8</sub> to D <sub>15</sub> are read on the rising edge and the current load register the is selected from among the Duty Register, the Decode & Digit Register, or Data Registers 0 to 3. The D <sub>0</sub> to D <sub>7</sub> bits of the 16-bit shift register contain data corresponding to the same registers just described, which are read on the load signal's falling edge.
5~12	OUT-A to OUT-Dp	Segment drive output pins. The A to Dp outputs correspond to the seven segments. These pins output constant sink current. Connect each of these pins to the corresponding LED's cathode.
13, 21	P-GND	Ground pins, There are two which can be used to ground the output OUT-A to OUT-Dp pins.
14	TEST-IN2	Product test pin. In normal use, be sure to connect to ground.
15	TEST-IN1	Product test pin. In normal use, be sure to connect to ground.
16, 17, 19, 20	DIG-0 to DIG-3	Digit output pins. Each of these pins can control one of the four seven-segment digits in a display. These pins output the V <sub>CC</sub> pin voltage as a source current output. Connect these pins to the LED anodes.
18	V <sub>CC</sub>	Power pin for digit output.
22	R-EXT	Current setting pin for the OUT-A to OUT-Dp pins. Connect a resistor between this pin and ground when setting the current.
23	DATA-OUT (DO)	Serial data output pin. Use when TB62709N or TB62709F devices are used in cascade connections.
24	L-GND	Ground pin for logic and analog circuits.

## TIMING DIAGRAM



## DATA INPUT

- Transfer data to the DATA-IN pin on every 16-bit combining address (8bits) and data (8bits). After the 16<sup>th</sup> clock signal input following this data transfer input a load signal from the LD pin.
- Input the load signal using an Active High pulse. The register address is set on the rising edge of the load pulse. On the subsequent falling edge, the data are read as data of the mode of the register.

## DESCRIPTION OF OPERATION

- Data input (SERIAL-IN, CLOCK, LOAD)

The data are input serially using the SERIAL-IN pin. The data input interface consists of a total of three inputs : SERIAL-IN, LOAD, and CLOCK.

Binary code stored in the 16-bit shift register offers control modes including duty Control Register Set, Digitset, Decode Set, and Standby Set,

The data are shifted on the rising edge of the clock, starting from the MSB. Cascade-connecting TB62709NG or TB62709FG devices provides capability for controlling a larger number of digits.

The serial data in the 16-bit shift register are used as follows : the four bits D<sub>15</sub> (MSB) to D<sub>12</sub> select the IC operating mode (Table 1), while D<sub>11</sub> to D<sub>8</sub> select the register corresponding to the operating mode (Table 2). Bits D<sub>7</sub> to D<sub>0</sub> (LSB) of the 16-bit shift register are used for detail settings, such as number of digits in use, character settings in each digit, and light intensity.

The internal registers are loaded on the rising edge of the LOAD signal, which causes loading of data from an external source into the D<sub>15</sub> (MSB) to D<sub>8</sub> bits of the shift register, operating mode and the corresponding register selection data. On the subsequent falling edge, the detail setting data of D<sub>7</sub> to D<sub>0</sub> (LSB) are loaded.

Normally LOAD is Low. After a serial transfer of 16bits, the input of a High-level pulse loads the data.

Note the following caution : Use the D<sub>15</sub> to D<sub>8</sub> setting and the D<sub>7</sub> to D<sub>0</sub> detail data setting as a pair. If only the D<sub>7</sub> to D<sub>0</sub> data are input without setting D<sub>15</sub> to D<sub>8</sub> an error condition may result, in which the device will not operate normally. If the current mode is set again by a new signal, the data for D<sub>15</sub> to D<sub>8</sub> must also be re-input.

- Operating precautions

At power-on or after operation in Clear mode (in initial state), set the IC to Normal mode again. Otherwise, the IC will not drive the LED.

Operating the IC in Blank mode (all lights off) or in All On mode (all lights lit) does not affect the internal data. Setting the IC to Normal mode again continues the LED lighting in the state governed by the settings made immediately before mode change.

Normal mode (not Shut Down, Clear, Blank, or All On mode) continues the operations set in Load Register mode. In Normal mode, operations are governed by any new settings made in the Load Register, as soon as the changed setting values are loaded.

- Operating modes (Table 1.)

These ICs support the following five operating modes :

- Blank : Forcibly turns OFF the constant-current output both for data and for digit setting. This mode is not affected by the values in bits D<sub>11</sub> to D<sub>0</sub>.
- Normal Operate : Used for display operations after the settings of the digits are complete. Note that setting this mode without making any other settings will cause display of the numeral 0.
- Load Register : Used for the detail settings of the Duty Control Register, for setting Decode / No Decode, for inputting display data, and for setting the number of digits to drive. D<sub>11</sub> to D<sub>0</sub> of the shift register are used for the detail settings of the digits currently being driven (Table 2).
- All On : Forcibly turns ON the data-side constant-current output. This mode is not affected by D<sub>11</sub> to D<sub>0</sub>.  
The initial setting is four digits. When the digits must be changed, use Load Register mode to set the number of digits to drive.
- Standby : Used to set Standby state (in which internal data are not cleared) and to clear data (initialization). The settings in D<sub>3</sub> to D<sub>0</sub> of the shift register determine the choice between standby state or initialization.

**Table 1 Operating mode settings**

	REGISTER DATA								INITIAL SETTING
	D <sub>15</sub>	D <sub>14</sub>	D <sub>13</sub>	D <sub>12</sub>	D <sub>11</sub> ~D <sub>8</sub>	D <sub>7</sub> ~D <sub>4</sub>	D <sub>3</sub> ~D <sub>0</sub>	HEX CODE	
BLANK (OUT-n & DIG-0~3 ALL-OFF)	0	0	0	0	—	—	—	0---H	■
NORMAL (OPERATION)	0	0	0	1	—	—	—	1---H	
LOAD REGISTER (DUTY, DECODE, DIGIT & DATA)	0	0	1	0	X	X	X	2XXXH	
ALL ON (OUTn ALL-ON)	0	0	1	1	—	—	—	3---H	
STAND-BY	0	1	0	0	—	—	X	4--XH	

X = Input H or L. "—" = Are not affected by the truth table.

- Load Register Selection modes (Table 2)

These modes select the register to provide the data to control the IC operation. The Load Register selection mode is determined by the settings of D<sub>15</sub> to D<sub>12</sub> and D<sub>11</sub> to D<sub>8</sub> of the shift register.

1. Duty Register : The data in D<sub>7</sub> to D<sub>0</sub> of this register set the digit output duty cycle.  
Duty settings can be made in 16 steps from 0 / 16 to 15 / 16.  
(See Table 3)
2. Decode & Digit Register : Sets Decode / No Decode and the number of digits to drive. Decode can be set using D<sub>7</sub> to D<sub>4</sub>.  
The number of digits driven can be set using D<sub>3</sub> to D<sub>0</sub>. Decode / No Decode and the number of digits driven are set simultaneously.
3. Data registers 0 to 3 : Set the display data corresponding to DIG<sub>0</sub> to DIG<sub>3</sub> respectively.  
D<sub>7</sub> to D<sub>0</sub> of the shift register are used to set the display data.

**Table 2 Load register selection**

	REGISTER DATA							HEX CODE
	D <sub>15</sub> ~D <sub>12</sub>	D <sub>11</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub> ~D <sub>4</sub>	D <sub>3</sub> ~D <sub>0</sub>	
LOAD DUTY REGISTER	2H	0	0	0	0	X	X	20XXH
LOAD DECODE & DIGIT REGISTER	2H	0	0	0	1	X	X	21XXH
LOAD DATA REGISTER 0	2H	0	0	1	0	X	X	22XXH
LOAD DATA REGISTER 1	2H	0	0	1	1	X	X	23XXH
LOAD DATA REGISTER 2	2H	0	1	0	0	X	X	24XXH
LOAD DATA REGISTER 3	2H	0	1	0	1	X	X	25XXH

X = Input H or L.

## DUTY CONTROL REGISTER SETTINGS

- Duty Control Register detail settings and operation (Table 3)

Writing 20H to D15~D8 and writing 0~FH to D3~D0 sets the duty cycle shown in the following table for the digit-side source driver output. The duty cycle can be set in 16 steps.

The initial setting is 15 / 16. After Data Clear, the setting is also 15 / 16.

The current settings continue until changed (by reset execution, or to the initial state, Data Clear state, or standby state).

Table 3 Duty control register settings

DUTY CYCLE	REGISTER DATA							INITIAL SETTING
	D15~D8	D7~D4	D3	D2	D1	D0	HEX CODE	
0 / 16	20H	—	0	0	0	0	20X0H	
1 / 16	20H	—	0	0	0	1	20X1H	
2 / 16	20H	—	0	0	1	0	20X2H	
3 / 16	20H	—	0	0	1	1	20X3H	
4 / 16	20H	—	0	1	0	0	20X4H	
5 / 16	20H	—	0	1	0	1	20X5H	
6 / 16	20H	—	0	1	1	0	20X6H	
7 / 16	20H	—	0	1	1	1	20X7H	
8 / 16	20H	—	1	0	0	0	20X8H	
9 / 16	20H	—	1	0	0	1	20X9H	
10 / 16	20H	—	1	0	1	0	20XAH	
11 / 16	20H	—	1	0	1	1	20XBH	
12 / 16	20H	—	1	1	0	0	20XCH	
13 / 16	20H	—	1	1	0	1	20XDH	
14 / 16	20H	—	1	1	1	0	20XEH	
15 / 16	20H	—	1	1	1	1	20XFH	■

X = Input H or L. "—" = Are not affected by the truth table.



## DIGIT SETTINGS

- Setting the number of digits (Table 4)

Writing 21H to D<sub>15</sub>~D<sub>8</sub> and at the same step writing 0H~3H to D<sub>3</sub>~D<sub>0</sub> sets the number of digits to a maximum of four the display. The initial setting is four digits, and four will also be set by a Data Clear.

The current settings continue until changed (by reset execution, or to the initial state, Data Clear state, or standby state).

When changing the number of digits, also set D<sub>7</sub> to D<sub>4</sub>.

**Table 4 Digit settings**

	REGISTER DATA							INITIAL SETTING
	D <sub>15</sub> ~D <sub>8</sub>	D <sub>7</sub> ~D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	HEX CODE	
ACTIVATED DIG--0 ONLY	21H	X	0	0	0	0	21X0H	
ACTIVATED DIG--0~1	21H	X	0	0	0	1	21X1H	
ACTIVATED DIG--0~2	21H	X	0	0	1	0	21X2H	
ACTIVATED DIG--0~3	21H	X	0	0	1	1	21X3H	■

X = Input H or L.

## DECODE SETTINGS

- Decode settings (Table 5)

The settings for Decode are the same as the settings for the number of digits, described under setting, above. Writing 21H to D<sub>15</sub>~D<sub>8</sub> and writing 0~1H to D<sub>7</sub>~D<sub>4</sub> set Decode mode.

When using this IC for controlling the lighting on individual LEDs used for a dot matrix rather than a 7-segment display, set to No Decode.

As Table 6 shows, D<sub>0</sub> in the data register is used to turn OUT-a ON and OFF ; D<sub>1</sub> turns OUT-b ON and OFF.

The initial setting is Decode mode, and Decode mode will also be set by a Data Clear.

The current settings continue until changed (by reset execution, or to the initial state, Data Clear state, or standby state).

Since D<sub>3</sub> to D<sub>0</sub> are also used for setting the number of digits, when changing the Decode setting, also set D<sub>3</sub> to D<sub>0</sub>.

**Table 5 Decode settings**

	REGISTER DATA							INITIAL SETTING
	D <sub>15</sub> ~D <sub>8</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub> ~D <sub>0</sub>	HEX CODE	
PASS DECODER (NO DECODE)	21H	0	0	0	0	X	210XH	
DECODE	21H	0	0	0	1	X	211XH	■

X = Input H or L.

THE FOLLOWING TABLE SHOWS THE CORRESPONDENCE BETWEEN THE SERIAL DATA AND THE OUTPUT PINS WHEN NO DECODE IS SET

**Table 6 Correspondence between serial data and output pins in no decode mode**

REGISTER DATA	OUTPUT	INITIAL STATE	NOTE
D <sub>0</sub>	OUT-a	L	Output is ON when data = H and OFF when data = L.
D <sub>1</sub>	OUT-b	L	
D <sub>2</sub>	OUT-c	L	
D <sub>3</sub>	OUT-d	L	
D <sub>4</sub>	OUT-e	L	
D <sub>5</sub>	OUT-f	L	
D <sub>6</sub>	OUT-g	L	
D <sub>7</sub>	OUT-Dp	L	

## STANDBY SETTINGS

- Standby mode settings and operation (Table 7)

Writing 4H to D<sub>15</sub>~D<sub>12</sub> and writing 0H to D<sub>3</sub>~D<sub>0</sub> sets Standby mode. Writing 4H to D<sub>15</sub>~D<sub>12</sub> and writing 1H to D<sub>3</sub>~D<sub>0</sub> sets All Data Clear mode.

Standby mode maintains the settings made immediately before this mode came in force, turns the output current OFF, and controls the bias current flowing in the internal circuits. All Data Clear resets all settings to their initial states.

**Table 7 Standby settings**

	REGISTER DATA						HEX CODE
	D <sub>15</sub> ~D <sub>8</sub>	D <sub>7</sub> ~D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	
STANDBY (NO DATA CLEAR)	4-H	—	0	0	0	0	4XX0H
ALL DATA CLEAR	4-H	—	0	0	0	1	4XX1H

X = Input H or L. "—" Are not affected by the truth table.

## LIST OF CHARACTER GENERATOR DECODING DATA

- Character generator decoding (Table 8)

As the following table shows, the characters are decoded using combinations of the data in D<sub>0</sub> to D<sub>3</sub> and D<sub>5</sub> to D<sub>4</sub>. In decoding, D<sub>6</sub> is used exclusively for setting decimal points.

Spaces where (D<sub>0</sub>, D<sub>1</sub>, D<sub>2</sub>, D<sub>3</sub>) = (0000) and (D<sub>5</sub>, D<sub>4</sub>) = (01) are regarded as blank.

Table 8 List of character generator decoding data

		D <sub>0</sub>	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	
		D <sub>1</sub>	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	
		D <sub>2</sub>	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	
		D <sub>3</sub>	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	
D <sub>5</sub>	D <sub>4</sub>	HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	0	0	0	:	.	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	1	1		H	J	L	P	R	T	V	X	-	0	2	4	6	8	3	

D <sub>7</sub>	D <sub>6</sub>	
X	0	Dp OFF
X	1	Dp ON

## DATA INPUT

(Example 1: Displays and blinks characters a, b, c and d in digits 0, 1, 2 and 3 respectively. Period after "d" part of it, or a sentence-end marker?)

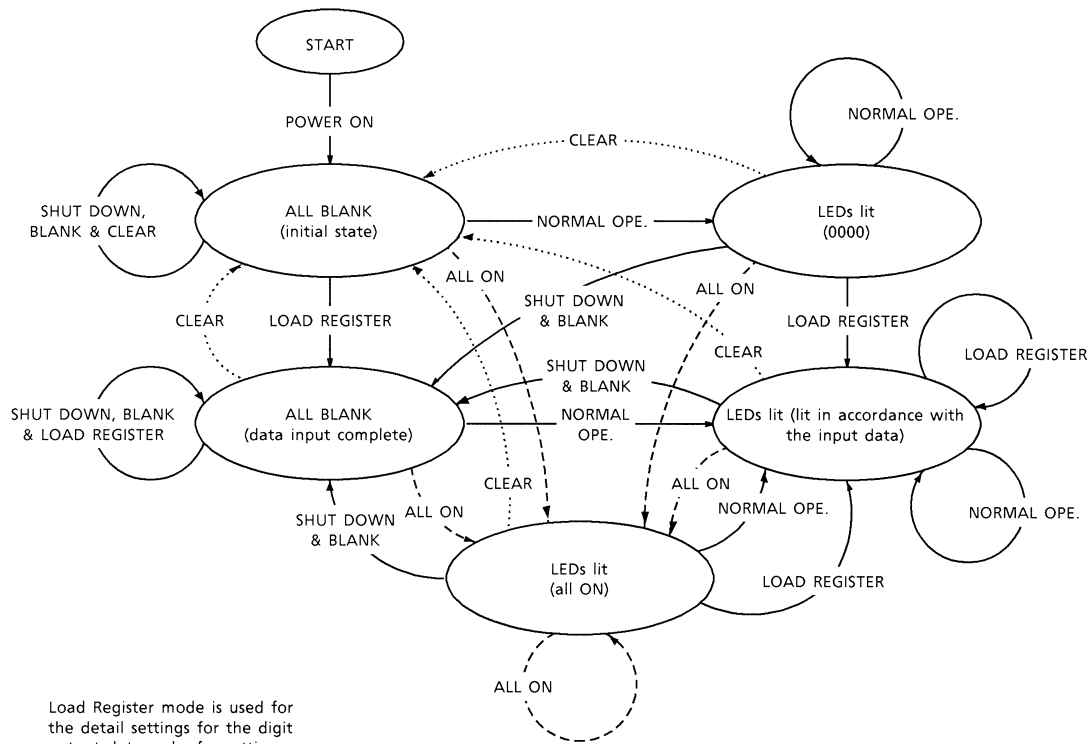
STEP	D15~ D12	D11~ D8	D7~ D4	D3~ D0	DIG -0~3	SEG -a, b, c, d, e, f, g	SEG -Dp	MODE	DISPLAY INDICATE
0	—	—	—	—	OFF	OFF	OFF	At power-on ( = CLEAR MODE)	ALL BLANK
1	0010	0000	XXXX	1111	OFF	OFF	OFF	DUTY = 15 / 16	ALL BLANK
2	0010	0001	0001	0011	OFF	OFF	OFF	DECODE, 4DIG	ALL BLANK
3	0010	0010	X000	1010	OFF	OFF	OFF	DIG-0 = a	ALL BLANK
4	0010	0011	X000	1011	OFF	OFF	OFF	DIG-1 = b	ALL BLANK
5	0010	0100	X000	1100	OFF	OFF	OFF	DIG-2 = c	ALL BLANK
6	0010	0101	X000	1101	OFF	OFF	OFF	DIG-3 = d	ALL BLANK
7	0001	XXXX	XXXX	XXXX	ON	ON	OFF	NORMAL	a-b-c-d
8	0010	0000	XXXX	1000	ON	ON	OFF	DUTY = 8 / 16	a-b-c-d
9	0000	XXXX	XXXX	XXXX	OFF	OFF	OFF	BLANK	ALL BLANK
10	0001	XXXX	XXXX	XXXX	ON	ON	OFF	NORMAL	a-b-c-d
11	0000	XXXX	XXXX	XXXX	OFF	OFF	OFF	BLANK	ALL BLANK
12	0001	XXXX	XXXX	XXXX	ON	ON	OFF	NORMAL	a-b-c-d
13	0000	XXXX	XXXX	XXXX	OFF	OFF	OFF	BLANK	ALL BLANK
14	0001	XXXX	XXXX	XXXX	ON	ON	OFF	NORMAL	a-b-c-d
15	0100	XXXX	XXXX	0000	OFF	OFF	OFF	STAND-BY (SHUT DOWN)	ALL BLANK

## DATA INPUT

(Example 2: Scroll-lights digits 0, 1, 2, 3 = a., -b., -c., -d. ?SEQ; and please explain the data on rhs? digit by digit (with decimal points))

STEP	D15~ D12	D11~D 8	D7~ D4	D3~ D0	DIG -0~3	SEG -a, b, c, d, e, f, g	SEG -Dp	MODE	DISPLAY INDICATE
0	—	—	—	—	OFF	OFF	OFF	At power-on ( = CLEAR MODE)	ALL BLANK
1	0010	0000	XXXX	1111	OFF	OFF	OFF	DUTY = 15 / 16	ALL BLANK
2	0010	0001	0001	0011	OFF	OFF	OFF	DECODE, 4DIG	ALL BLANK
3	0010	0010	X100	1010	OFF	OFF	OFF	DIG-0 = a.	ALL BLANK
4	0010	0011	X001	0000	OFF	OFF	OFF	DIG-1 = blank	ALL BLANK
5	0010	0100	X001	0000	OFF	OFF	OFF	DIG-2 = blank	ALL BLANK
6	0010	0101	X001	0000	OFF	OFF	OFF	DIG-3 = blank	ALL BLANK
7	0001	XXXX	XXXX	XXXX	ON	ON	ON	NORMAL	a.---
8	0010	0010	X001	0000	OFF	ON	OFF	DIG-0 = blank	ALL BLANK
9	0010	0011	X100	1011	ON	ON	ON	DIG-1 = b.	-b.--
10	0010	0011	X001	0000	OFF	ON	OFF	DIG-1 = blank	ALL BLANK
11	0010	0100	X100	1100	ON	ON	ON	DIG-2 = c.	--c.-
12	0010	0100	X001	0000	OFF	ON	OFF	DIG-2 = blank	ALL BLANK
13	0010	0101	X100	1101	ON	ON	ON	DIG-3 = d.	---d.
14	0100	XXXX	XXXX	0000	OFF	OFF	OFF	STAND-BY (SHUT DOWN)	ALL BLANK

## STATE TRANSITION DIAGRAM



Load Register mode is used for the detail settings for the digit output duty cycle, for setting Decode/No Decode, for inputting display data, and for setting the number of digits to use.

**MAXIMUM RATINGS (Ta = 25°C)**

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage for Logic Circuits	V <sub>DD</sub>	7.0	V
Supply Voltage	V <sub>CC</sub>	17	V
DIG-0 to DIG-3 Output Current	I <sub>DIG</sub>	-400	mA
OUT-a to Dp Output Current	I <sub>OUT</sub>	50	mA
Output Current for Logic Block	I <sub>OH</sub> / I <sub>OL</sub>	±5	mA
Input Voltage	V <sub>IN</sub>	-0.3~V <sub>DD</sub> + 0.3	V
Operating Frequency	f <sub>CK</sub>	15.0	MHz
Total Supply Current	I <sub>VDD</sub>	400	mA
Power Dissipation	TB62709NG	P <sub>D</sub> 1.78	W
	TB62709FG	0.62	
Operating Temperature	T <sub>opr</sub>	-40~85	°C
Storage Temperature	T <sub>stg</sub>	-55~150	°C

**ELECTRICAL CHARACTERISTICS**(Unless otherwise stated, V<sub>DD</sub> = 5.0 V, V<sub>CC</sub> = 5.0 V, R<sub>EXT</sub> = 760 Ω, Ta = -40~85°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Operating Power Supply Current for Output Block	I <sub>CC1</sub>	1	SET NORMAL OPE. MODE, R <sub>EXT</sub> = 760 Ω @OUT-a~Dp ALL ON, Ta = 25°C	—	300	—	mA
	I <sub>CC2</sub>	1	SET NORMAL OPE. MODE, R <sub>EXT</sub> = 760 Ω @OUT-a~Dp ALL ON V <sub>CC</sub> = 12 V, Ta = 25°C	—	320	—	
DIG-0 to DIG-3 Scan Frequency	f <sub>OSC</sub>	2	NORMAL OPE. MODE, V <sub>DD</sub> = 4.5~5.5 V	240	480	960	Hz
OUT-a to Dp Output Sink Current	I <sub>SEG</sub>	3	NORMAL OPE. MODE, V <sub>CE</sub> = 0.7 V, R <sub>EXT</sub> = 760 Ω	29	34	40	mA
DIG-0 to 3 Output Leakage Current	I <sub>leak1</sub>	4	ALL OFF MODE, V <sub>CC</sub> = 17 V	—	—	-20	μA
OUT-a to Dp Output Leakage Current	I <sub>leak2</sub>	4	ALL OFF MODE, V <sub>CC</sub> = 17 V	—	—	20	μA
DIG-0 to 3 Output Voltage	V <sub>OUT</sub>	5	NORMAL OPE. MODE, I <sub>DIG</sub> = -320 mA	3.0	—	—	V

**Logic block**

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Static Power Supply Current for Logic Circuits	I <sub>DD1</sub>	6	STANDBY MODE, Ta = 25°C	—	—	200	μA
	I <sub>DD2</sub>	6	BLANK MODE, Ta = 25°C	—	—	12.5	mA
Operating Power Supply Current for Logic Circuits	I <sub>DD3</sub>	6	NORMAL OPE. MODE, f <sub>CLK</sub> = 10MHz, DATA-IN : OUT-a~Dp = ON, Ta = 25°C	—	—	20.5	mA
High Input Current for Logic Circuits	I <sub>IH</sub>	—	DATA-IN, LOAD & CLOCK : V <sub>IN</sub> = 5 V	—	—	1	μA
Low Input Current for Logic Circuits	I <sub>IL</sub>	—	DATA-IN, LOAD & CLOCK : V <sub>IN</sub> = 0 V	—	—	-1	μA
High Output Voltage for Logic Circuits	V <sub>OH1</sub>	6	DATA-OUT, I <sub>OH</sub> = -1.0 mA	4.6	—	—	V
	V <sub>OH2</sub>	6	DATA-OUT, I <sub>OH</sub> = -1.0 μA	—	V <sub>DD</sub>	—	
Low Output Voltage for Logic Circuits	V <sub>OL1</sub>	6	DATA-OUT, I <sub>OL</sub> = 1.0 mA	—	—	0.4	V
	V <sub>OL2</sub>	6	DATA-OUT, I <sub>OH</sub> = 1.0 μA	—	0.1	—	
Clock Frequency	f <sub>CLK</sub>	6	CASCADE CONNECTED, Ta = -40~85°C	10	—	—	MHz

**SWITCHING CHARACTERISTICS**

 (Unless otherwise stated,  $V_{DD} = 5.0\text{ V}$ ,  $V_{CC} = 5.0\text{ V}$ ,  $T_a = 25^\circ\text{C}$ )

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Data Hold Time (D-IN-CLOCK)	$t_{DHO}$	—	—	—	10	—	ns
Data Setup Time (D-IN-CLOCK)	$t_{DST}$	—	—	—	20	—	ns
Serial Output Delay Time (CLOCK-D-OUT)	$t_{pHL-SO}$	—	$C_L = 10\text{ pF}$	—	25	—	ns
	$t_{pLH-SO}$		$C_L = 10\text{ pF}$	—	25	—	
High Clock Pulse Width	$t_{CKH}$	—	—	—	30	—	ns
Low Clock Pulse Width	$t_{CKL}$	—	—	—	30	—	ns
Load Pulse Width	$t_{WLD}$	—	—	—	100	—	ns
Load Clock Time (CLOCK-LOAD)	$t_{CLK-LD}$	—	—	—	50	—	ns
Clock Load Time (LOAD-CLOCK)	$t_{LD-CLK}$	—	—	—	50	—	ns
OUT-a to Dp Output Delay Time (LOAD-OUTn)	$t_{pHL-SEG}$	—	$C_L = 10\text{ pF}$	—	—	5.0	$\mu\text{s}$
	$t_{pLH-SEG}$		$C_L = 10\text{ pF}$	—	—	5.0	
OUT-a to Dp Output Rise Time (OUTn)	$t_r\text{ SEG}$	—	$C_L = 10\text{ pF}$	0.2	1.0	—	$\mu\text{s}$
OUT-a to Dp Output Fall Time (OUTn)	$t_f\text{ SEG}$	—	$C_L = 10\text{ pF}$	0.2	1.0	—	$\mu\text{s}$
DIG-0~DIG-3 Output Delay Time (LOAD-DIGn)	$t_{pHL-DIG}$	—	$C_L = 10\text{ pF}$	—	—	10.0	$\mu\text{s}$
	$t_{pLH-DIG}$		$C_L = 10\text{ pF}$	—	—	10.0	
DIG-0~DIG-3 Output Rise Time (DIGn)	$t_r\text{ DIG}$	—	$C_L = 10\text{ pF}$	0.4	2.0	—	$\mu\text{s}$
DIG-0~DIG-3 Output Fall Time (DIGn)	$t_f\text{ DIG}$	—	$C_L = 10\text{ pF}$	0.4	2.0	—	$\mu\text{s}$



**RECOMMENDED OPERATING CONDITIONS**(Unless otherwise stated,  $V_{DD} = 5.0\text{ V}$ ,  $V_{CC} = 5.0\text{ V}$ ,  $T_a = -40\sim 85^\circ\text{C}$ )

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage for Output Block	$V_{CC}$	—	—	4.0	—	6.0	V
DIG-0 to DIG-3 Output Source Current	$I_{DIG}$	—	$V_{OUT} = 3.0\text{ V}$	—	—	-320	mA
OUT-a to OUT-Dp Output Sink Current	$I_{SEG}$	—	$V_{CE} = 0.7\text{ V}$	—	—	40	mA

**Logic block**

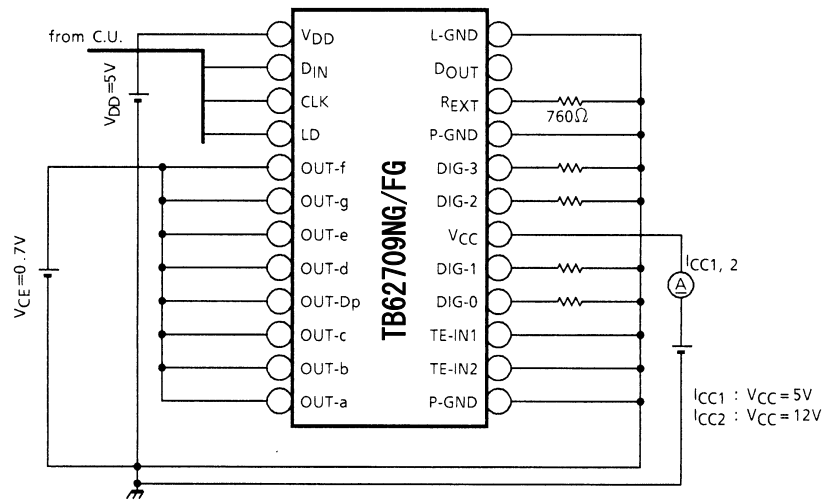
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage for Logic Block	$V_{DD}$	—	—	4.5	—	5.5	V
High Input Current for Logic Circuits	$I_{IH}$	—	DATA-IN, LOAD & CLOCK, $V_{IN} = V_{DD}$	—	—	1	$\mu\text{A}$
Low Input Current for Logic Circuits	$I_{IL}$	—	DATA-IN, LOAD & CLOCK, $V_{IN} = 0\text{V}$	—	—	-1	$\mu\text{A}$
High Input Voltage for Logic Circuits	$V_{IH}$	—	—	0.7 $V_{DD}$	—	—	V
Low Input Voltage for Logic Circuits	$V_{IL}$	—	—	—	—	0.3 $V_{DD}$	V

**SWITCHING CONDITIONS**

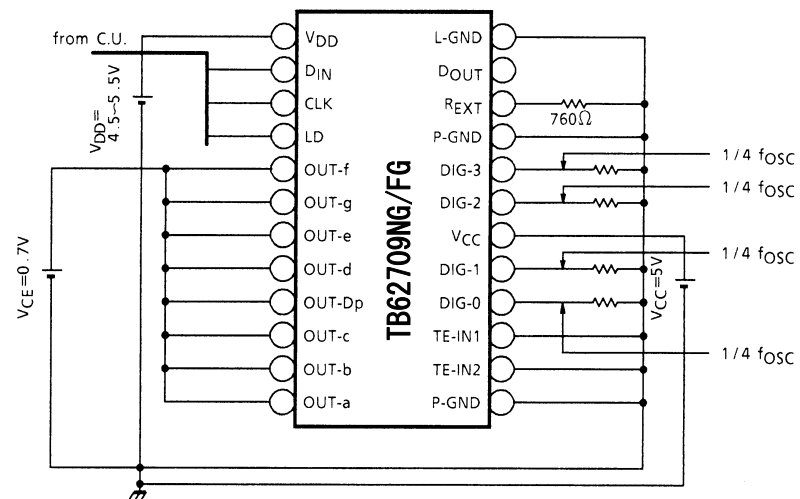
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Data Hold Time (D-IN-CLOCK)	$t_{DHO}$	—	—	30	—	—	ns
Data Setup Time (D-IN-CLOCK)	$t_{DST}$	—	—	50	—	—	ns
Serial Output Delay Time (CLOCK-D-OUT)	$t_{PDSO}$	—	$C_L = 10\text{ pF}$	50	—	—	ns
High Clock Pulse Width	$t_{CKH}$	—	—	30	—	—	ns
Low Clock Pulse Width	$t_{CKL}$	—	—	30	—	—	ns
Load Pulse Width	$t_{WLD}$	—	—	150	—	—	ns
Load Clock Time (CLOCK-LOAD)	$t_{CLKLD}$	—	—	100	—	—	ns
Clock Load Time (LOAD-CLOCK)	$t_{LDCLK}$	—	—	100	—	—	ns

## TEST CIRCUITS

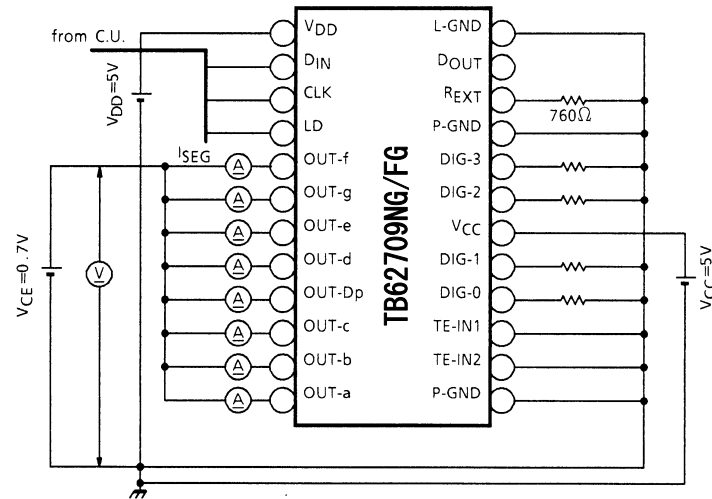
### (1) $I_{CC1}$ , $I_{CC2}$



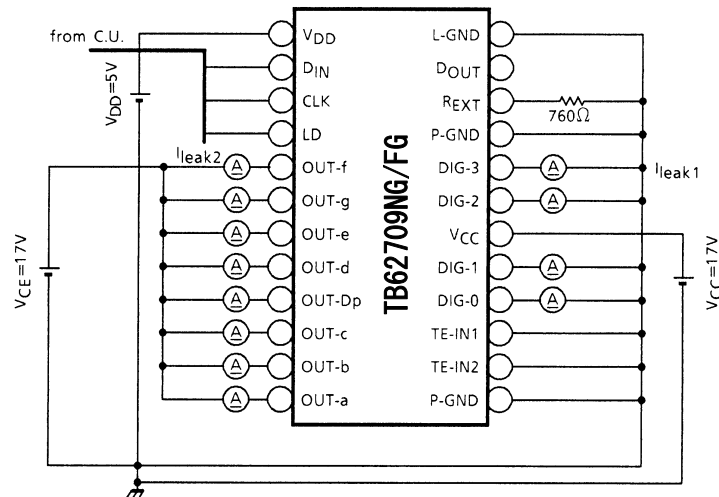
### (2) $f_{OSC}$



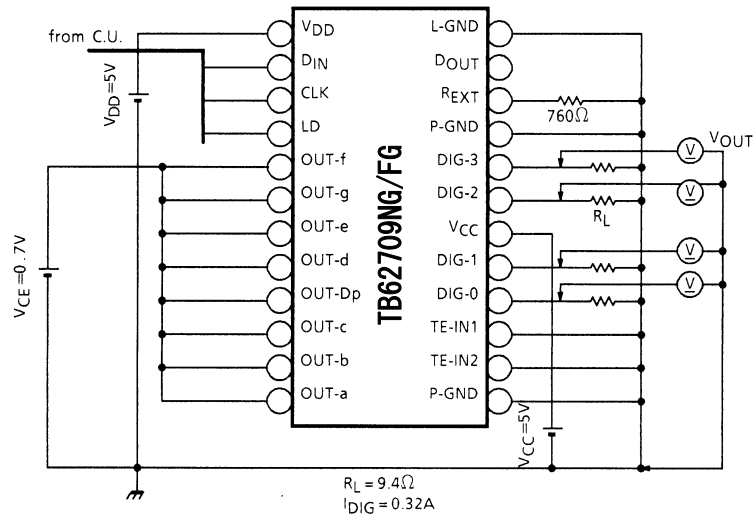
**(3)  $I_{SEG}$**



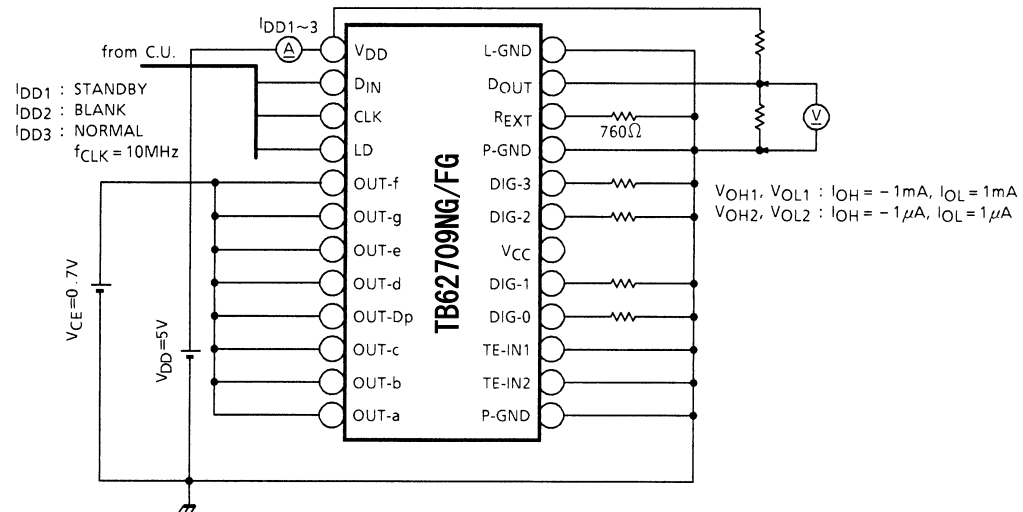
**(4)  $I_{leak1}$ ,  $I_{leak2}$**



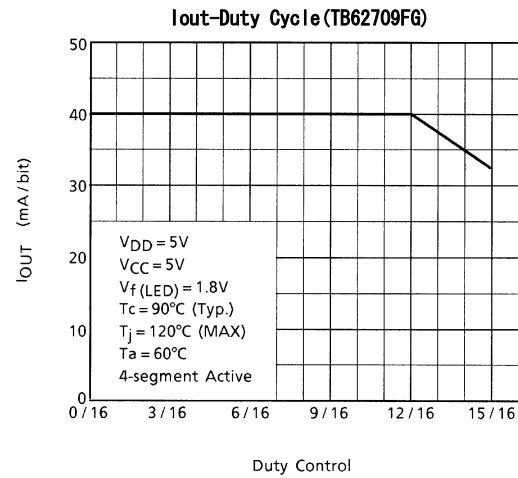
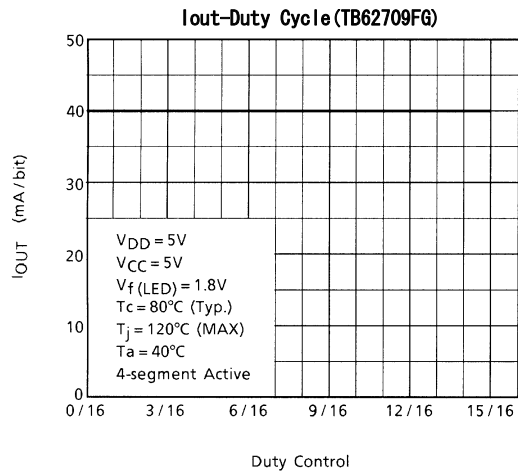
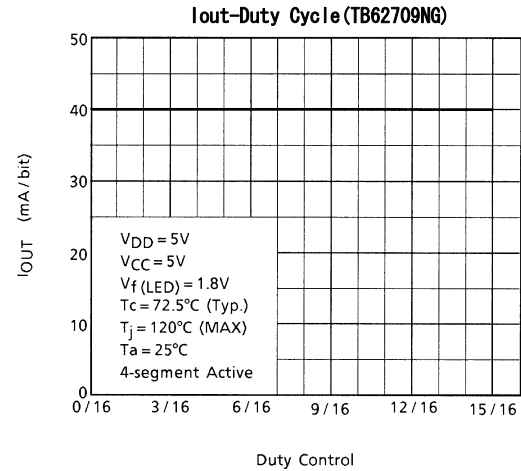
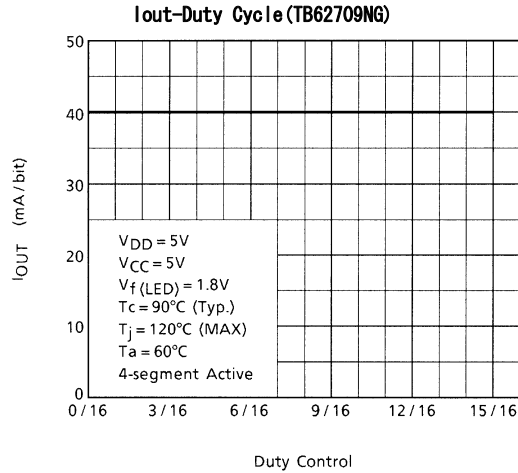
**(5)  $V_{OUT}$**



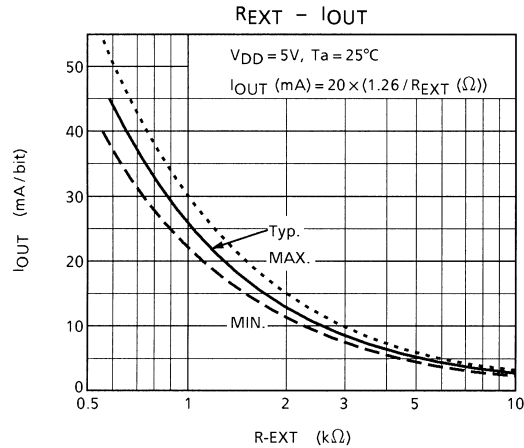
**(6)  $I_{DD1}$ ,  $I_{DD2}$ ,  $I_{DD3}$ ,  $V_{OH1}$ ,  $V_{OH2}$ ,  $V_{OL1}$ ,  $V_{OL2}$ ,  $f_{CLK}$**



**DUTY CYCLE SETTINGS AND OUTPUT CURRENT VALUES**



**EXTERNAL RESISTANCE AND OUTPUT CURRENT VALUES**



The following diagram shows application circuits.

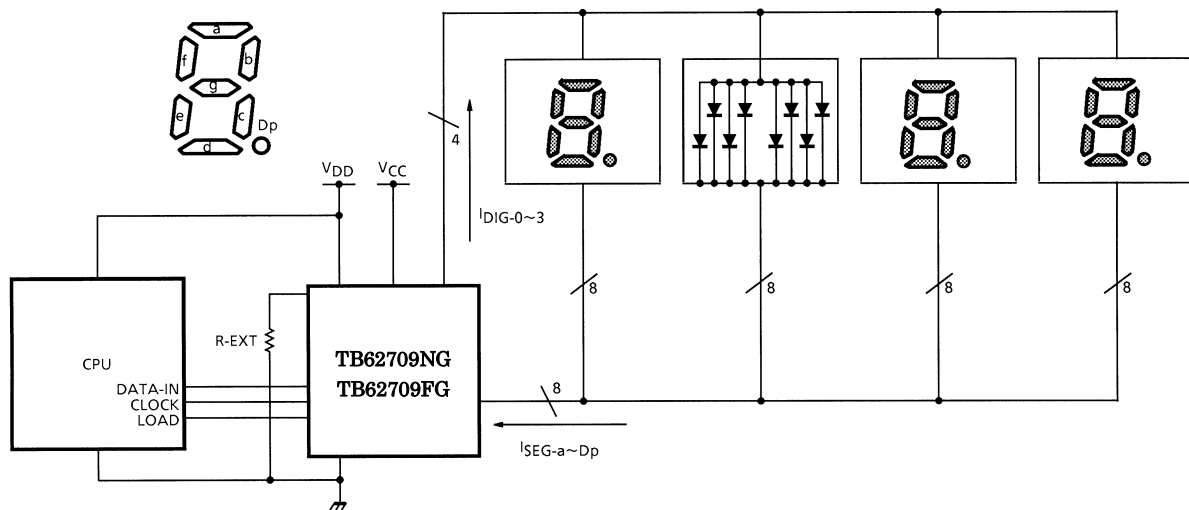
Because operation may be unstable due to influences such as the electromagnetic induction of the wiring, the IC should be located as close as possible to the LED.

The L-GND and P-GND of the IC are connected to the substrate in the IC.

Take care to avoid a potential difference exceeding 0.4V at two pins.

When executing the pattern layout, Toshiba recommends not including inductance components in the GND or output pin lines, and not inserting capacitance components exceeding 50pF between the  $R_{EXT}$  and GND.

## APPLICATION CIRCUIT EXAMPLE (Connection example)



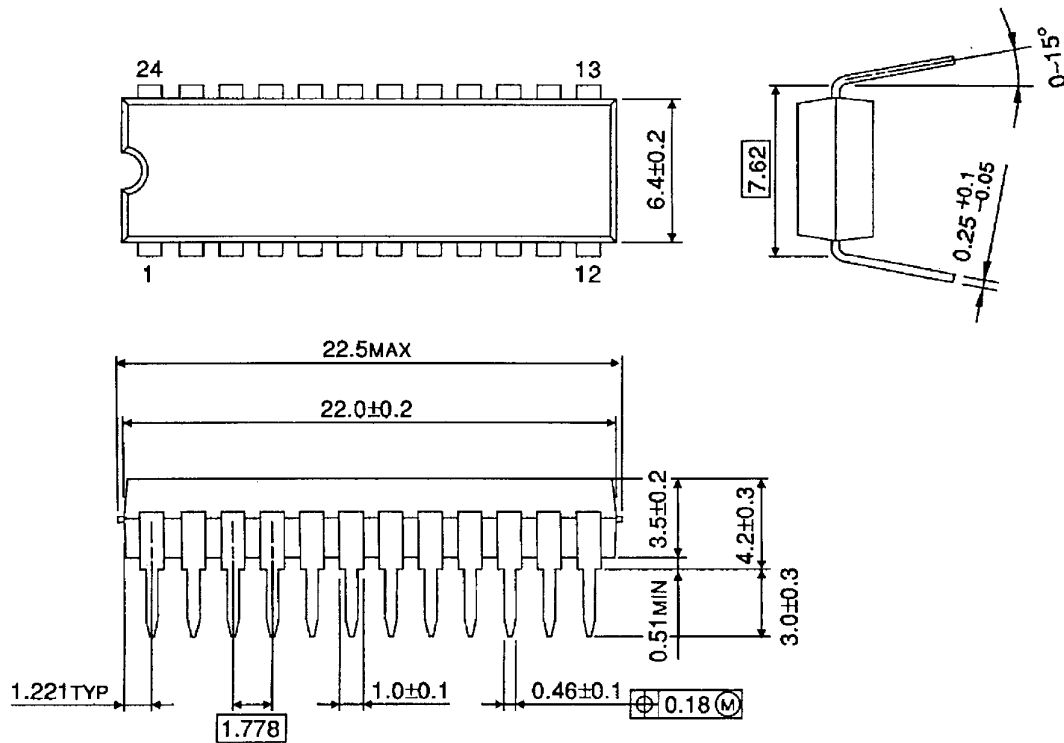
### PRECAUTIONS for USING

Utmost care is necessary in the design of the output line, VCC (VDD) and (L-GND, P-GND) line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

## Package Dimensions

SDIP24-P-300-1.78

Unit : mm



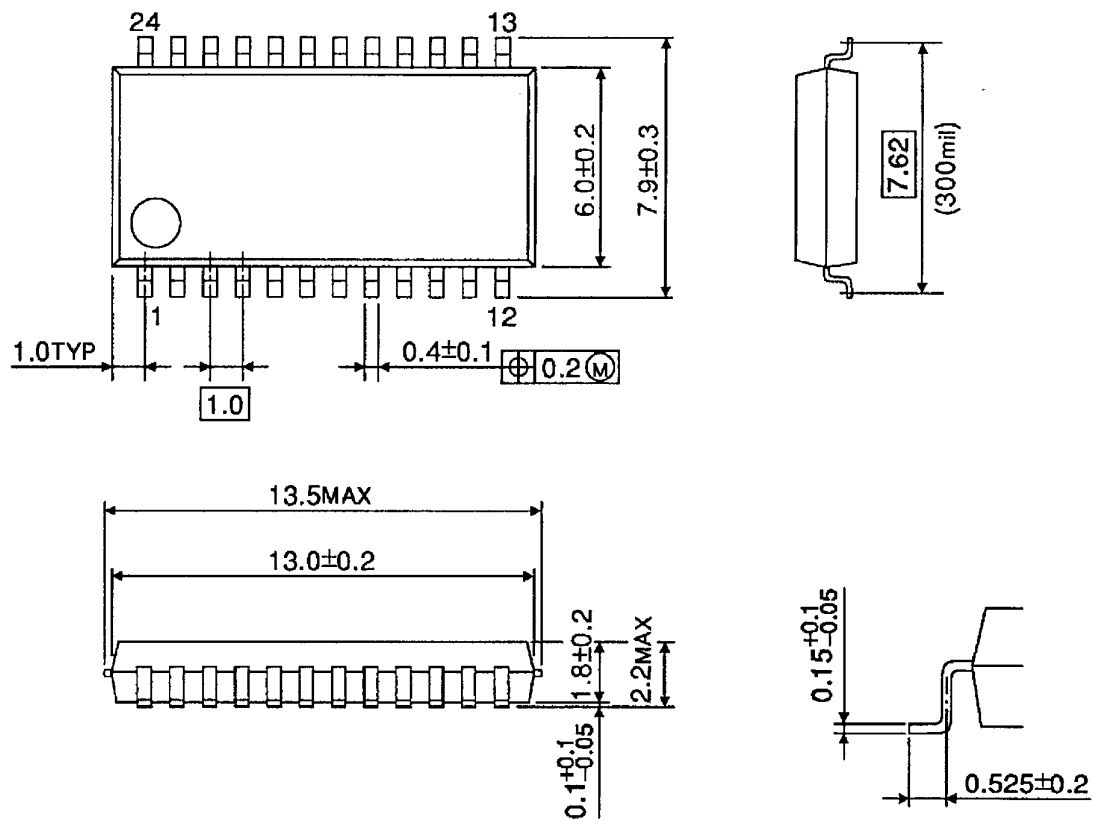
Weight: 1.62 g (typ.)



## Package Dimensions

SSOP24-P-300-1.00

Unit : mm



Weight: 0.32 g (typ.)

About solderability, following conditions were confirmed

- Solderability

- (1) Use of Sn-63Pb solder Bath

- solder bath temperature = 230°C
    - dipping time = 5 seconds
    - the number of times = once
    - use of R-type flux

- (2) Use of Sn-3.0Ag-0.5Cu solder Bath

- solder bath temperature = 245°C
    - dipping time = 5 seconds
    - the number of times = once
    - use of R-type flux

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030619EBA

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