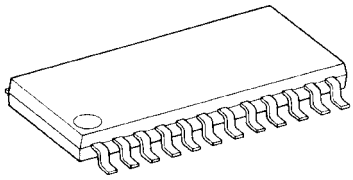
TOSHIBA Bi−CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB62707F

8BIT LATCHES & CONSTANT CURRENT DRIVERS

The TB62707F is specifically designed for LED and LED DISPLAY constant current drivers.
This constant current output is able to set up external resistor (I_{OUT} = 90 mA MAX.).
This IC is monolithic integrated circuit designed to be used together with Bi−CMOS process.
The devices consist of 8bit latches, AND−GATE and Constant Current Drivers.



SSOP24-P-300-1.00

Weight: 0.32 g (typ.)

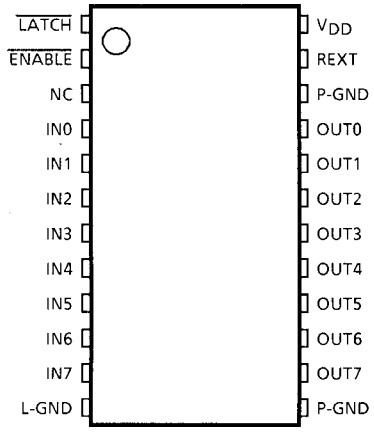
FEATURES

- Constant Current Output:
  Can set up all output current with one resistor for 5 to 90mA.
- Constant Output Current Matching:

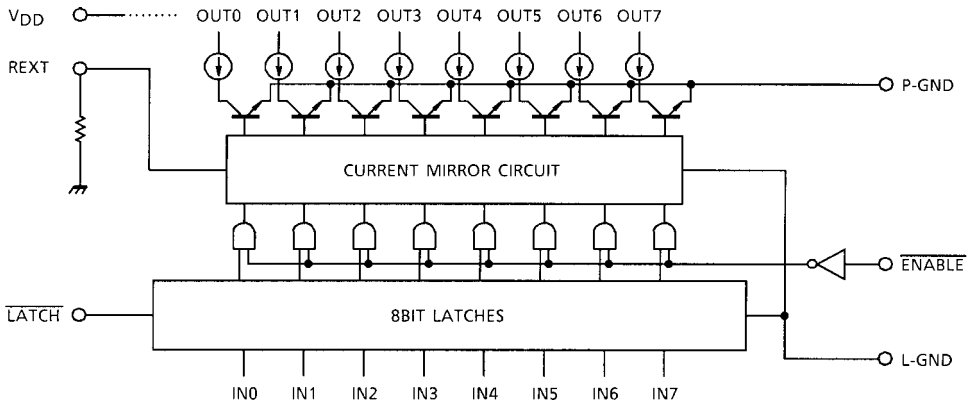
OUTPUT−GND VOLTAGE	CURRENT MATCHING	OUTPUT CURRENT
≥ 0.4 [V]	±6.0 [%]	5~40 mA
≥ 0.7 [V]	±6.0 [%]	40~90 mA

- 5 V CMOS Compatible Input
- Package: SSOP24−P−300

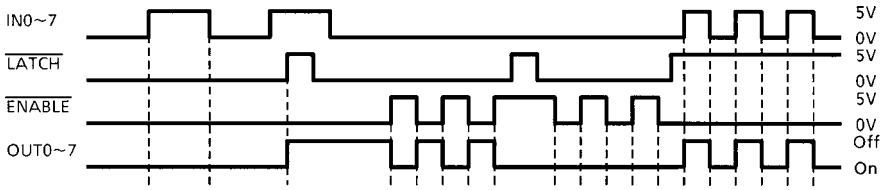
PIN CONNECTION (Top view)



BLOCK DIAGRAM



TIMING DIAGRAM



Note: Latches are level sensitive, not rising edge sensitive and not synchronous CLOCK.
Input of $\overline{\text{LATCH}}$ −terminal to "H" level, data passes latches, and input to "L" level, data hold latches.
Input of $\overline{\text{ENABLE}}$ −terminal to "H" level, all output (OUT0~7) do off.

TERMINAL DESCRIPTION

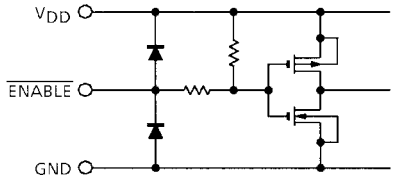
PIN No.	PIN NAME	FUNCTION
1	$\overline{\text{LATCH}}$	Input terminal of a data strobe. Latches passes data with "H" level input of $\overline{\text{LATCH}}$ −terminal, and hold data with "L" level input.
2	$\overline{\text{ENABLE}}$	Input terminal of output enable. All outputs (OUT0~7) do off with "H" level input of $\overline{\text{ENABLE}}$ −terminal, and do on with "L" level input.
4~11	IN0~7	Input terminal of a parallel−data for latches.
3	NC	No connection.
12	L−GND	GND terminal for controll logic.
13	P−GND	GND terminal for output constant current drivers.
14~21	OUT0~7	Output terminals.
22	P−GND	GND terminal for output constant current drivers.
23	REXT	Input terminal of connects with a resister for to set up all output current.
24	V_{DD}	5V Supply voltage terminal

TRUTH TABLE

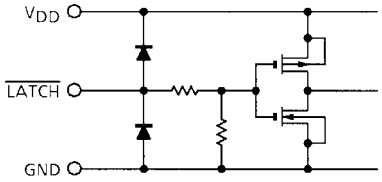
IN0~7	$\overline{\text{LATCH}}$	$\overline{\text{ENABLE}}$	OUT0~7
L	L	L	OFF
H	L	L	OFF
L	H	L	OFF
H	H	L	ON
L	↓	L	OFF
H	↓	L	ON
H	↓	H	OFF

EQUIVALENT CIRCUIT OF INPUTS

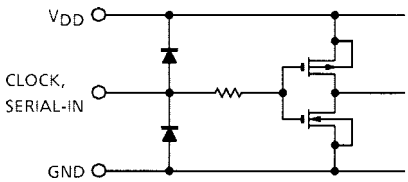
1. $\overline{\text{ENABLE}}$ terminal



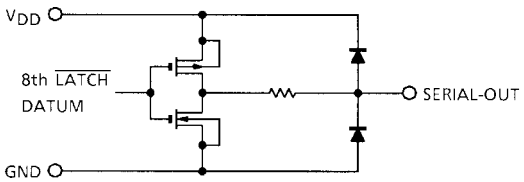
2. $\overline{\text{LATCH}}$ terminal



3. CLOCK, SERIAL−IN terminal



4. SERIAL−OUT terminal



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	7.0	V
Input Voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Output Current	I_O	90.0	mA
Output Voltage	V_O	−0.3~17.0	V
GND Terminal Current	IGND	720	mA
Power Dissipation	P_D	780 (Note)	mW
Operating Temperature	T_{opr}	−40~85	°C
Storage Temperature	T_{stg}	−55~150	°C

Note: On PCB (50 × 50 × 1.6 mm Cu 30% Glass Epoxy PCB)
Ambient temperature delated above 25°C in the proportion of 6.66 mW / °C

RECOMMENDED OPERATING CONDITION (Ta = −40~85°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage	V_{DD}	—	4.5	5.0	5.5	V
Output Voltage	V_O	—	—	—	15.0	V
Output Current	I_{OUT}	DC 1 circuit	5.0	—	88	mA
	I_{OH}	SERIAL−OUT	—	—	1.0	mA
	I_{OL}	SERIAL−OUT	—	—	−1.0	mA
Input Voltage	V_{IH}	—	0.7 V_{DD}	—	V_{DD} +0.3	V
	V_{IL}	—	−0.3	—	0.3 V_{DD}	
$\overline{\text{LATCH}}$ Pulse Width	$t_{w\ LAT}$	V_{DD} = 4.5 V	100	—	—	ns
	$t_{w\ \overline{LAT}}$		100	—	—	
INPUT Pulse Width	$t_{w\ IN}$		4500	—	—	ns
	$t_{w\ \overline{IN}}$		4500	—	—	
$\overline{\text{ENABLE}}$ Pulse Width	$t_{w\ EN}$		4500	—	—	ns
	$t_{w\ \overline{EN}}$		4500	—	—	
Set−Up Time for $\overline{\text{LATCH}}$	$t_{setup\ (L)}$		100	—	—	ns
Hold Time for $\overline{\text{LATCH}}$	$t_{hold\ (L)}$		100	—	—	ns
Power Dissipation	P_D	ON PCB, Ta = 85°C	—	—	0.60	W

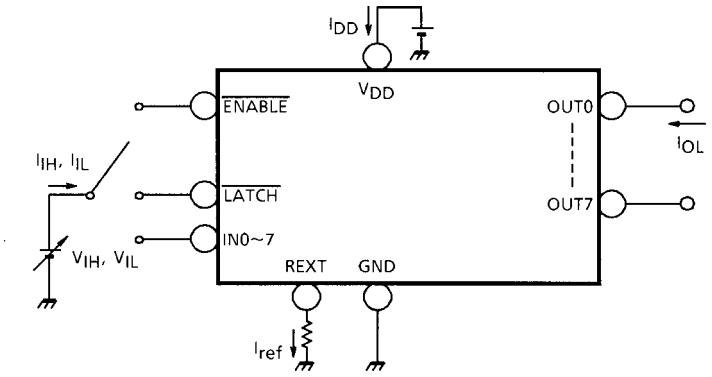
ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN	TYP.	MAX	UNIT
Input Voltage	"H" Level	V_{IH}	—	—		0.7 V_{DD}	—	V_{DD}	V
	"L" Level	V_{IL}	—	—		GND	—	0.3 V_{DD}	
Output Leakage Current		I_{OH}	—	V_{OH} = 15.0 V		—	—	10	μA
Output Voltage	SERIAL−OUT	V_{OL}	—	I_{OL} = 1.0 mA		—	—	0.4	V
		V_{OH}	—	I_{OL} = −1.0 mA		4.6	—	—	
Output Current 1		I_{OL1}	—	V_{CE} = 0.7 V	R_{EXT} = 620 Ω (Include skew)	35.7	42.0	48.3	mA
		I_{OL2}	—	V_{CE} = 0.4 V		68.0	80.0	92.0	mA
	Current Skew	ΔI_{OL1}	—	I_O = 40 mA, V_{CE} = 0.4 V	R_{EXT} = 620 Ω	—	±1.5	±6.0	%
Output Current 2		I_{OL3}	—	V_{CE} = 1.0 V	R_{EXT} = 330 Ω (Include skew)	64.2	75.5	86.8	mA
		I_{OL4}	—	V_{CE} = 0.7 V		63.8	75.0	86.2	mA
	Current Skew	ΔI_{OL2}	—	I_O = 75 mA V_{CE} = 0.7 V	R_{EXT} = 330 Ω	—	±1.5	±6.0	%
Supply Voltage Regulation		% / V_{DD}	—	R_{EXT} = 470 Ω, Ta = −40~85°C		—	+5.0	—	% / V
Reference Voltage		V_{ref}	—	—		—	1.26	—	V
Supply Current "OFF"		$I_{DD\ (off)\ 1}$	—	R_{EXT} = OPEN, OUT0~7 = off V_{DD} = 4.5 V, ENABLE = "H"		—	0.6	1.2	mA
		$I_{DD\ (off)\ 2}$	—	R_{EXT} = 500 Ω, OUT0~7 = off V_{DD} = 4.5V , ENABLE = "H"		6.0	8.0	10.0	
		$I_{DD\ (off)\ 3}$	—	R_{EXT} = 280 Ω, OUT0~7 = off V_{DD} = 4.5V, ENABLE = "H"		12.0	15.0	18.0	
Supply Current "ON"		$I_{DD\ (on)\ 1}$	—	R_{EXT} = 500 Ω, OUT0~7 = on V_{DD} = 4.5 V, ENABLE = "L"		8.0	13.0	20.0	mA
		$I_{DD\ (on)\ 2}$	—	R_{EXT} = 280 Ω, OUT0~7 = on V_{DD} = 4.5 V, ENABLE = "L"		18.0	25.0	35.0	

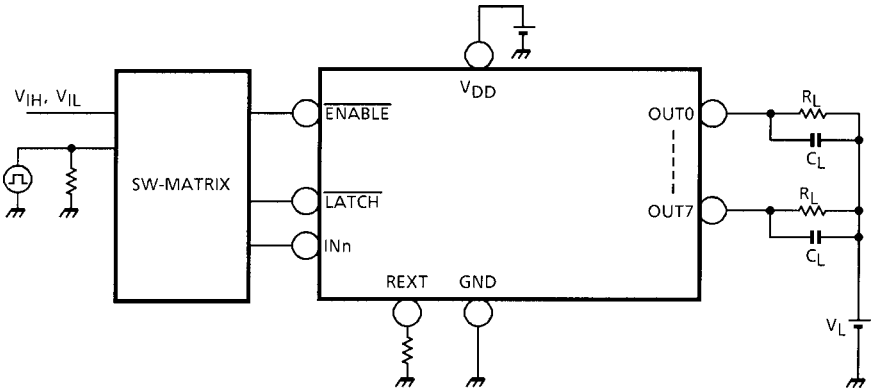
SWITCHING CHARACTERISTICS (Ta = 25°C, unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	CONDITION	MIN	TYP.	MAX	UNIT
Propagation Delay Time ("L" to "H")	IN−OUTn	t_{pLH}	—	V_{DD} = 5.0 V V_{CE} = 0.4 V V_{IH} = VDD V_{IL} = GND R_{EXT} = 500 Ω I_{OUT} = 40 Ma V_L = 3.0 V R_L = 65 Ω C_L = 10.5 pF	—	600	1200	ns
	$\overline{\text{LATCH}}$ −OUTn				—	600	1200	
	$\overline{\text{ENABLE}}$ −OUTn				—	600	1200	
Propagation Delay Time ("H" to "L")	IN−OUTn	t_{pHL}	—		—	300	1200	ns
	$\overline{\text{LATCH}}$ −OUTn				—	300	1200	
	$\overline{\text{ENABLE}}$ −OUTn				—	300	1200	
Pulse Width	IN	$t_{w\ IN}$, $\overline{\text{IN}}$	—		—	2000	3500	ns
	$\overline{\text{LATCH}}$	$t_{w\ LAT}$, $\overline{\text{LAT}}$	—		—	25	50	
	$\overline{\text{ENABLE}}$	$t_{w\ ENA}$, $\overline{\text{EN}}$			—	2000	3500	
Set−up Time for LATCH & CLOCK	L−H	t_{setup} $\overline{\text{LAT}}$	—		—	25	50	ns
	H−L		—		—	25	50	
Hold Time for LATCH & CLOCK	L−H	t_{hold} $\overline{\text{LAT}}$	—		—	0	30	ns
	H−L		—		—	0	30	
Output Rise Time		t_{or}	—		200	1000	1200	ns
Output Fall Time		t_{of}	—		200	1000	1200	ns

DC CHARACTERISTICS TEST CIRCUIT



AC CHARACTERISTICS TEST CIRCUIT

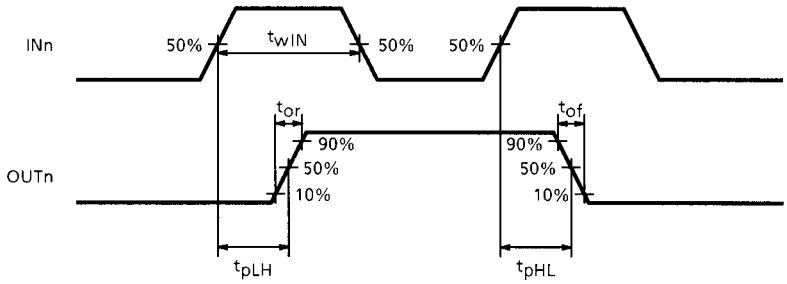


PRECAUTIONS for USING

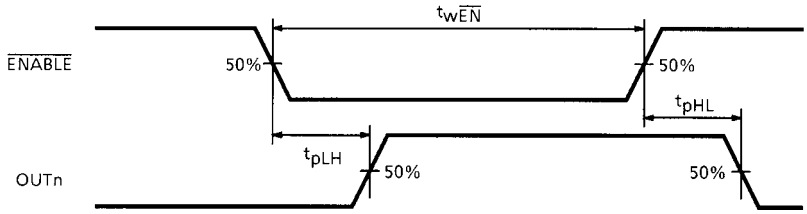
Utmost care is necessary in the design of the output line, V_{CC} (V_{DD}) and GND (L−GND, P−GND) line since IC may be destroyed due to short−circuit between outputs, air contamination fault, or fault by improper grounding.

TIMING WAVEFORM

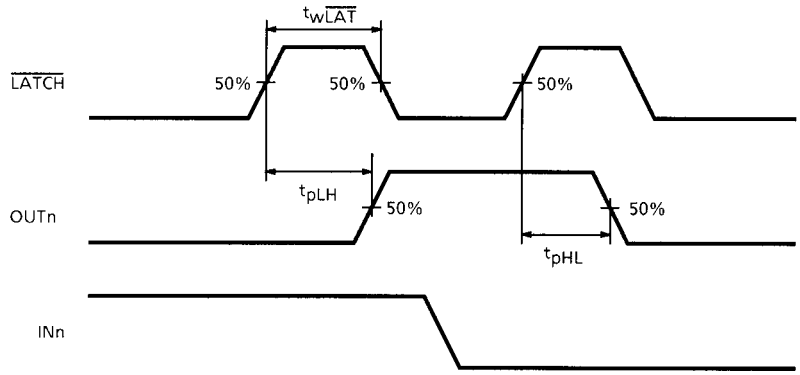
1. INn−OUTn

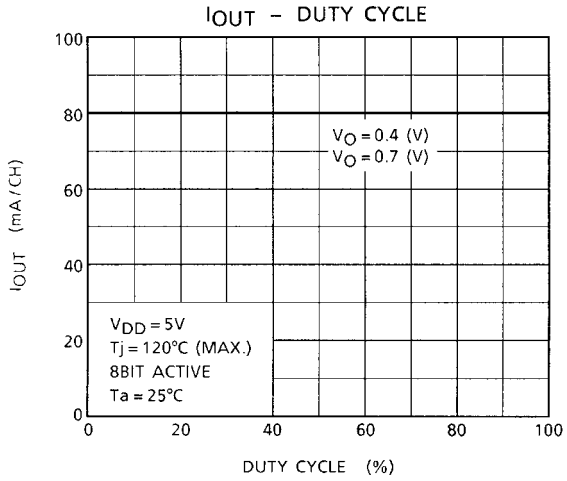


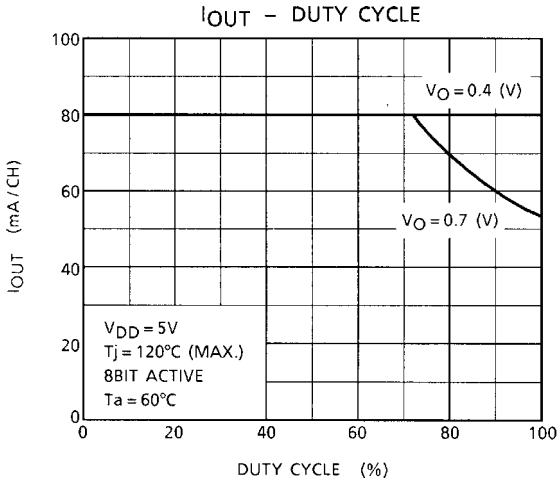
2. $\overline{\text{ENABLE}}$ −OUTn

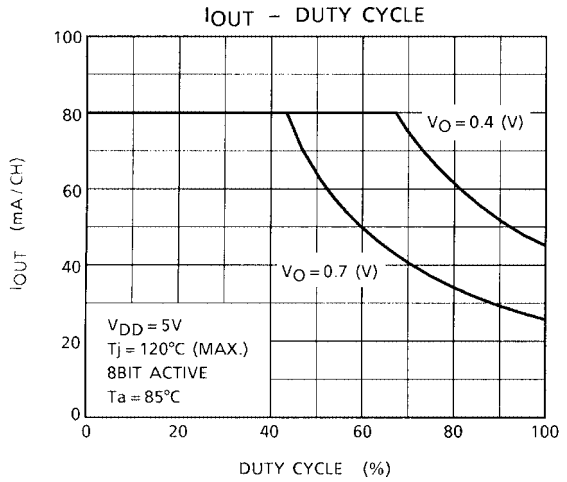


3. $\overline{\text{LATCH}}$ −OUTn



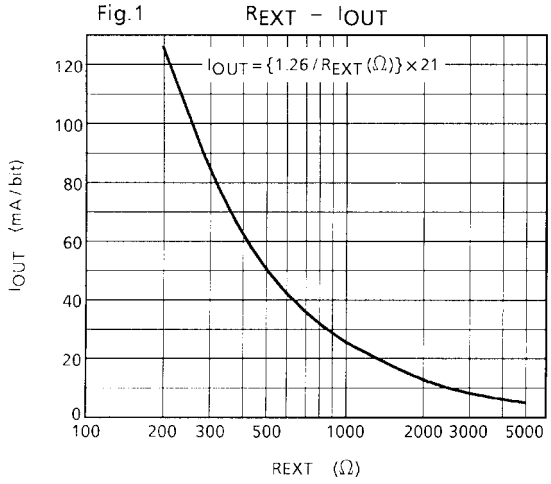






LED DRIVER TB6270X SERIES APPLICATION NOTE

Fig.1 R_{EXT} – I_{OUT}



[1] Output current (IOUT)

I_{OUT} is set by the enternal resistor (R−EXT) as shown in Fig.1.

[2] Total supply voltage (VLED)

This device can operate 0.4~0.7V (V_O).

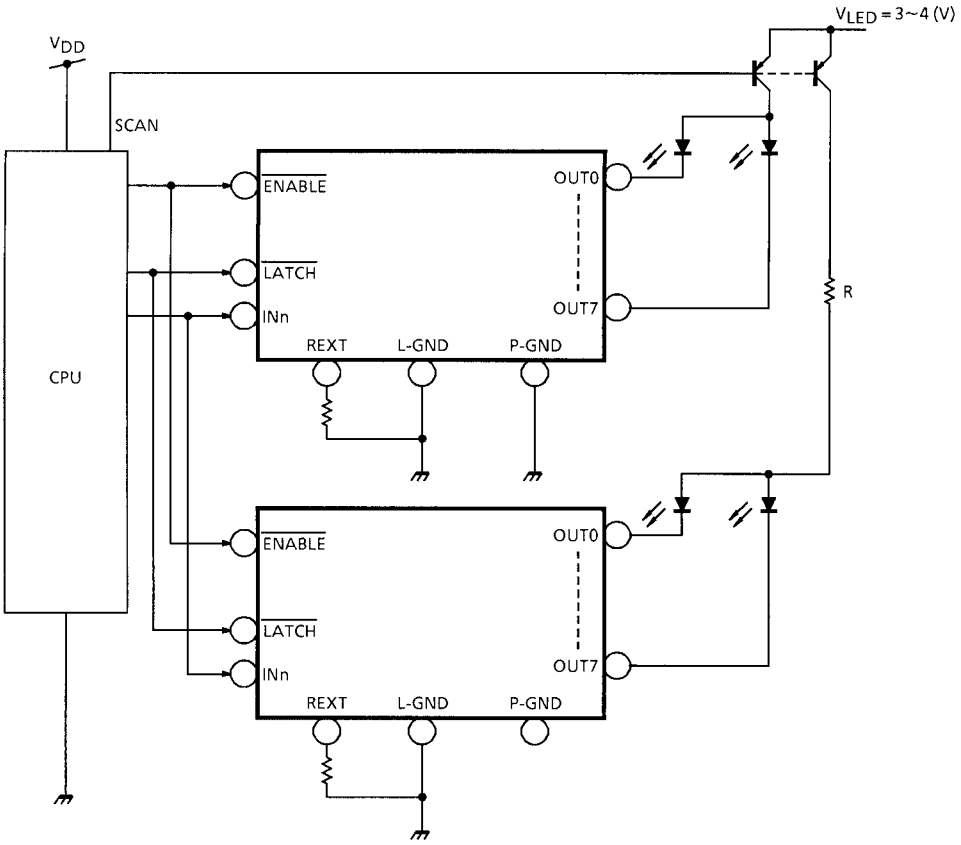
When a higher voltage is input to the devide, the excess voltage is consumed inside the device, that leads to power dissipation.

In order to minimize power dissipation and loss, we would like to recommended to set the total supply voltage as shown below.

V_{LED} (Total supply voltage)
= V_{CE} (Tr V_{sat}) + V_f (LED Forward voltage) + V_O (IC supply voltage)

When the total supply is too high considering the power dissipation of this devide, an additional R can decrease the supply voltage (V_O).

APPLICATION



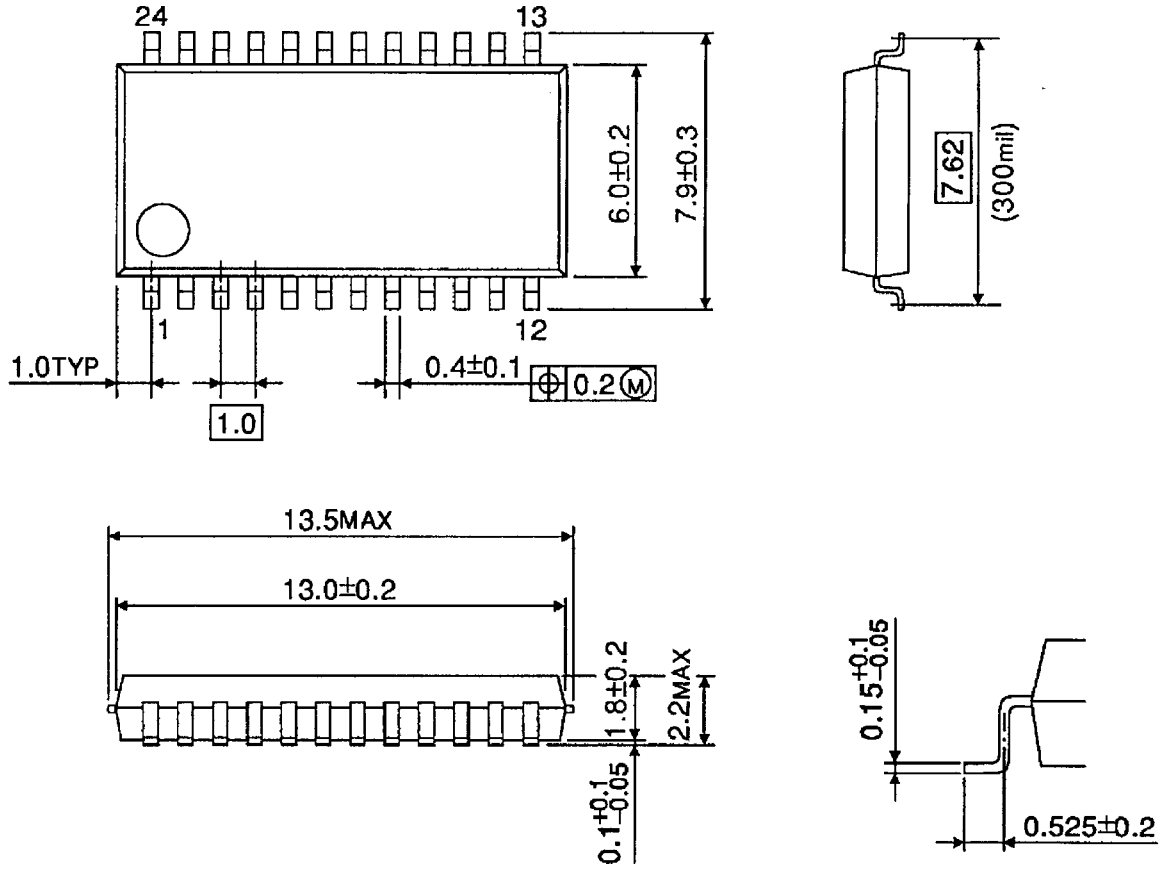
[3] Pattern layout

This device owns only one ground pin that means signal ground pin and power ground pin are common.

If ground pattern layout contains large inductance and impedance and the voltage between ground and $\overline{LATCH}$, CLOCK terminals exceeds 2.5V by switching noise in operation, this device may miss−operate. So we would life you to pay attention to pattern layout to minimize inductance.

Package Dimensions

SSOP24-P-300-1.00 Unit : mm



Weight: 0.32 g (typ.)

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