

TRUE DIGITAL AUDIO AMPLIFIER

TAS5010 DIGITAL AUDIO PWM PROCESSOR

FEATURES

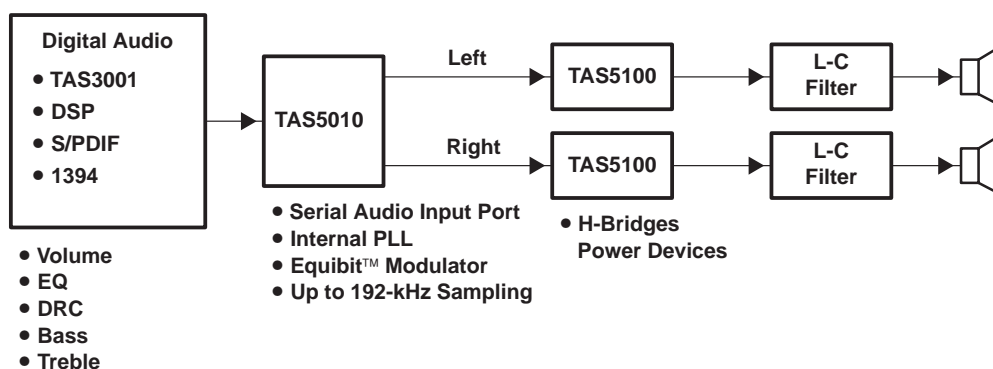
- **TAS5010 + TAS5100 TDAA System – High Quality Digital Audio Amplification**
- **96-dB Dynamic Range (TAS5010 Device)**
- **93-dB Dynamic Range (TAS5010 & TAS5100 System Measured at Speaker Terminals)**
- **THD+N < 0.08% (1 kHz, 1 to 30W RMS into 6 Ω)**
- **Power Efficiency Is 90% Into 8- Ω Load**
- **16-, 20-, or 24-Bit Input Data**
- **44.1-kHz, 48-kHz, 88.2-kHz, 96-kHz, 176.4-kHz, 192-kHz Sampling Rates**
- **Economical 48-Pin TQFP Package**
- **Lower-Jitter Internal PLL**
- **3.3-V Power Supply**
- **Mute**
- **Clicks and Pops Reduction (Patent Pending)**

APPLICATIONS

- **DVD-Audio**
- **Home Theater**
- **Car Audio Amplifiers and Head Units**
- **Internet Music Appliance**
- **Mini/Micro Component Systems**

DESCRIPTION

The true digital audio amplifier (TDAA) is a new paradigm in digital audio. One TDAA system consists of the TAS5010 PCM-PWM modulator device + a TAS5100 PWM power output device. This system accepts a serial PCM digital audio stream and converts it to a 3.3-V PWM audio stream (TAS5010). The TAS5100 device then provides a large-signal PWM output. This digital PWM signal is then demodulated providing power output for driving loudspeakers. This patented technology provides low-cost, high-quality, high-efficiency digital audio applicable to many audio systems developed for the digital age. The TAS5010 is an innovative, cost-effective, high-performance 24-bit stereo PCM-PWM modulator based on Equibit™ technology. It has a wide variety of serial input options including right-justified (16, 20, or 24 bits), IIS (16, 20, or 24 bits), left-justified (16 bits), or DSP (16 bits) data formats. It is fully compatible with AES standard sampling rates of 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz. The TAS5010 also provides a de-emphasis function for 44.1-kHz and 48-kHz sampling rates.

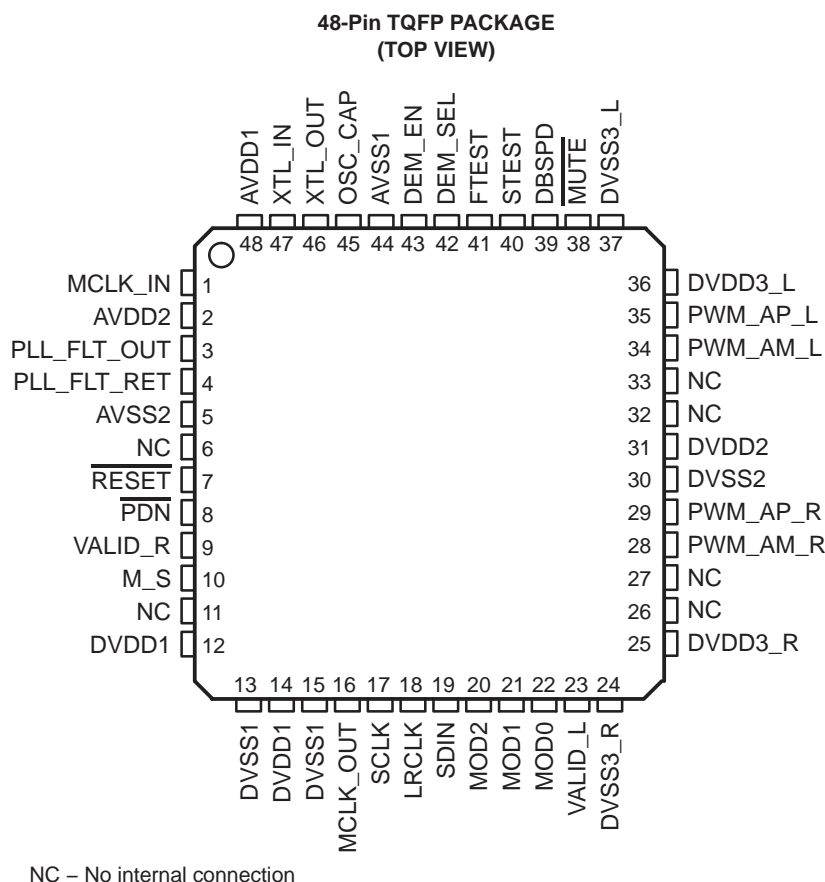


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Equibit is a trademark of Toccata Technology ApS, Denmark.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

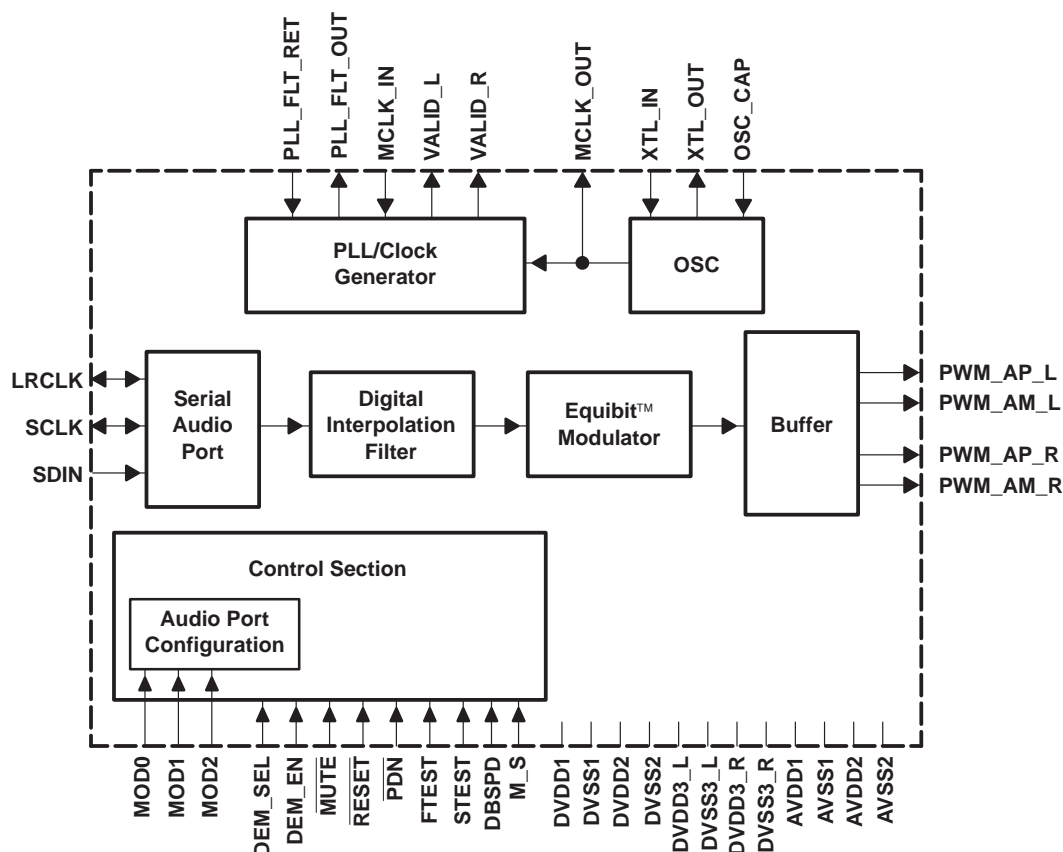
terminal assignments



references

- *True Digital Audio Amplifier TAS5100 Power Output Stage* – Texas Instruments publication SLLS419A
- *Design Considerations for TAS5000/TAS5100 True Digital Audio Power Amplifiers* – Texas Instruments publication SLAA117
- *Digital Audio Measurements* – Texas Instruments publication SLAA114
- *PowerPAD™ Thermally Enhanced Package* – Texas Instruments publication SLMA002

functional block diagram



AVAILABLE OPTIONS

T _A	PACKAGE†
0°C to 70°C	TAS5010PFB
-40°C to 85°C	TAS5010IPFB

† These packages are available taped and reeled. Add an R suffix to device type (e.g., TAS5010PFBR).

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AVDD1	48	I	Analog supply for oscillator
AVDD2	2	I	Analog supply for PLL
AVSS1	44	I	Analog ground for oscillator
AVSS2	5	I	Analog ground for PLL
DBSPD	39	I	Indicates sample rate is double speed (88.2 kHz or 96 kHz), active high
DEM_EN	43	I	De-emphasis enable, active high
DEM_SEL	42	I	De-emphasis select (0 = 44.1 kHz, 1 = 48 kHz)
DVDD1	12, 14	I	Digital voltage supply for logic
DVDD2	31	I	Digital voltage supply for PWM reclocking
DVDD3_L	36	I	Digital voltage supply for PWM output (left)
DVDD3_R	25	I	Digital voltage supply for PWM output (right)
DVSS1	13, 15	I	Digital ground for logic
DVSS2	30	I	Digital ground for PWM reclocking
DVSS3_L	37	I	Digital ground for PWM output (left)
DVSS3_R	24	I	Digital ground for PWM output (right)
FTEST	41	I	Tied to DVSS1 for normal operation
LRCLK	18	I/O	Left/right clock (input when M_S = 0; output when M_S = 1)
MCLK_IN	1	I	MCLK input
MCLK_OUT	16	O	Buffered system clock output if M_S = 1; otherwise set to 0
MOD0	22	I	Serial interface selection pin, bit 0
MOD1	21	I	Serial interface selection pin, bit 1
MOD2	20	I	Serial interface selection pin, bit 2 (MSB)
M_S	10	I	Master/slave, master=1, slave=0
MUTE	38	I	Muted signal = 0, normal mode = 1
NC	6, 11, 26, 27, 32, 33		No connection
OSC_CAP	45	I	Oscillator cap return
PDN	8	I	Power down, active low
PLL_FLT_OUT	3	O	Output terminal for external PLL filter
PLL_FLT_RET	4	I	Return for external PLL filter
PWM_AM_L	34	O	PWM left output (differential –)
PWM_AM_R	28	O	PWM right output (differential –)
PWM_AP_L	35	O	PWM left output (differential +)
PWM_AP_R	29	O	PWM right output (differential +)
RESET	7	I	Reset (active low)
SCLK	17	I/O	Shift clock (input when M_S = 0, output when M_S = 1)
SDIN	19	I	Stereo serial audio data input
STEST	40	I	Tied to DVSS1 for normal operation
VALID_L	23	O	PWM left outputs valid (active high)
VALID_R	9	O	PWM right outputs valid (active high)
XTL_IN	47	I	Crystal or clock input (MCLK input)
XTL_OUT	46	O	Crystal output (not for external usage).NC when XTL_IN is MCLK input

functional description

serial audio port

The serial audio port consists of a shift clock (SCLK pin), a left/right frame synchronization clock (LRCLK pin), and a data input (SDIN pin). The serial audio port supports standard serial PCM formats (Fs = 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4kHz, or 192kHz) stereo. See serial interface formats section.

system clocks—master mode and slave mode

The TAS5010 allows multiple system clocking schemes. In this document, master mode indicates that the TAS5010 provides system clocks to other parts of the system (M_S=1). Audio system clocks of frequency 256Fs MCLK_OUT, 64 Fs SCLK, and Fs LRCLK are output from this device when it is configured in master mode. Slave mode indicates that a system master other than the TAS5010 provides system clocks (LRCLK, SCLK, and MCLK_IN) to the TAS5010 (M_S = 0). The TAS5010 operates with LRCLK and SCLK synchronized to MCLK. TAS5010 does not require any specific phase relationship between LRCLK and MCLK, but there must be synchronization. In the slave mode MCLK_OUT is driven low. Table 1 shows all the possible master and slave modes. When operating in quad mode (Fs = 176.4kHz or 192 kHz), the device works in slave mode only with MCLK_IN = 128 Fs.

oscillator/sampling frequency

The sampling frequency is determined by the crystal (master mode) or master clock in (slave mode) which should be either 11.2896 MHz (Fs = 44.1 kHz) or 12.288 MHz (Fs = 48 kHz). Twice the normal sampling frequency can be selected by using the DBSPD pin which allows usage of Fs = 88.2 kHz or Fs = 96 kHz. In the double-speed slave mode (DBSPD = 1, M_S = 0), the external clock input is either 22.5796 MHz (Fs = 88.2 kHz) or 24.576 MHz (Fs = 96 kHz). Table 1 explains the proper clock selection.

Table 1. Oscillator, External Clock, and PLL Functions

DESCRIPTION	M_S	DBSPD	XTL_IN (MHz) [†]	MCLK_IN (MHz) [‡]	SCLK (MHz) [¶]	LRCLK (kHz) [¶]	MCLK_OUT (MHz) [#]
Master, normal speed	1	0	11.2896	—	2.8224	44.1	11.2896
Master, normal speed	1	0	12.288	—	3.072	48	12.288
Master, double speed	1	1	—	22.5792 [§]	5.6448	88.2	22.5792
Master, double speed	1	1	—	24.576 [§]	6.144	96	24.576
Slave, normal speed	0	0	—	11.2896 [§]	2.8224	44.1	Digital GND
Slave, normal speed	0	0	—	12.288 [§]	3.072	48	Digital GND
Slave, double speed	0	1	—	22.5792 [§]	5.6448	88.2	Digital GND
Slave, double speed	0	1	—	24.576 [§]	6.144	96	Digital GND
Slave, quad speed	0	0	—	22.5792 [§]	11.2896	176.4	Digital GND
Slave, quad speed	0	0	—	24.576 [§]	12.288	192	Digital GND

[†] Either a crystal oscillator or an external clock of the specified frequency can be connected to XTL_IN.

[‡] MCLK_IN tied low when input to XTL_IN is provided; XTL_IN tied low when MCLK_IN is provided.

[§] External MCLK connected to MCLK_IN input

[¶] SCLK and LRCLK are outputs when M_S=1, inputs when M_S=0.

[#] MCLK_OUT is driven low when M_S=0.

^{||} Quad speed mode is detected automatically.

phase-locked loop (PLL)/clock generation

A low jitter PLL is incorporated for internal use. Connections for the PLL external loop filter are provided as PLL_FLT_RET and PLL_FLT_OUT. If the PLL loses lock, the PWM output status pins (VALID_L and VALID_R) go low. Note that VALID_L and VALID_R can go low for other conditions as well. See error status reporting section.

functional description (continued)

digital interpolation filter

The 24-bit high-performance linear phase FIR interpolation filter up-samples the input digital data at a rate of 2 times (quad speed mode = 176.4kHz or 192kHz), 4 times (double speed mode = 88.2 kHz or 96 kHz), or 8 times (normal mode = 44.1 kHz or 48 kHz) the incoming sample rate. This filter provides very low pass-band ripple and optimized time domain transient response for accurate music reproduction.

digital PWM modulator

The interpolation filter output is sent to the modulator. This modulator consists of a high performance fourth order digital noise shaper and a PCM-to-PWM converter. Following the noise shaper, the PCM signal is fed into a very low distortion PCM-to-PWM conversion block, buffered, and output from the chip. The modulation scheme is based on a 2-state control of the H-bridge output.

control, status, and operational modes

The TAS5010 control section consists of several control-input pins. Three serial mode pins (MOD0, MOD1, and MOD2) are provided to select various serial data formats. During normal operating conditions if any of the MOD0, MOD1, or MOD2 pins changes state, a reset sequence is initiated. Also provided are separate power-down (PDN), reset ($\overline{\text{RESET}}$), and mute ($\overline{\text{MUTE}}$) pins.

power up

At power up the VALID_L and VALID_R pins are asserted low and the PWM outputs go to the hard mute state in which the P outputs are held low and the M outputs are held high. Following initialization, the TAS5010 comes up in the operational state (differential PWM audio). There are two cases of power-up timing. The first case is shown in Figure 1 with $\overline{\text{RESET}}$ preceding PDN. The second case is shown in Figure 2 with PDN preceding $\overline{\text{RESET}}$.

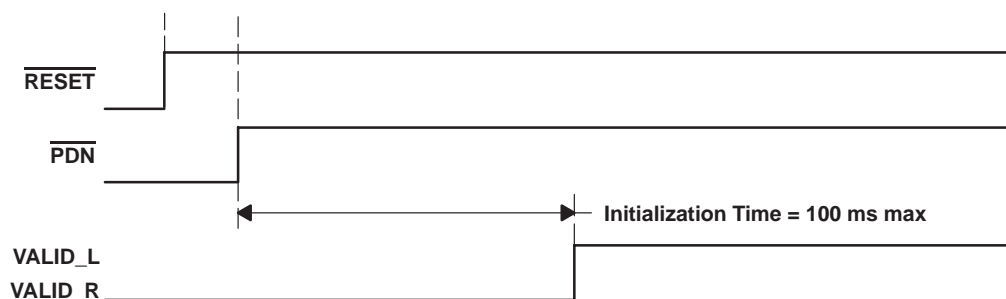


Figure 1. Power-Up Timing ($\overline{\text{RESET}}$ Preceding PDN)

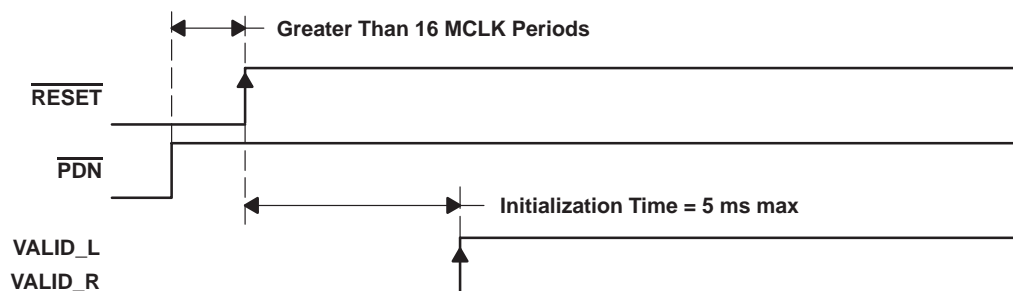


Figure 2. Power-Up Timing (PDN Preceding $\overline{\text{RESET}}$)

functional description (continued)

reset

The reset signal for the TAS5010 must be applied whenever toggling the M_S, DBSPD signal. This reset is asynchronous. See Figure 3 for reset timing. To initiate the reset sequence the $\overline{\text{RESET}}$ pin is asserted low. As long as the pin is held low the chip is in the reset state. During this reset time the PWM outputs are hard-muted (P-outputs held low and M-outputs held high) and the PWM outputs valid pins (VALID_L, VALID_R) are held low. Assuming $\overline{\text{PDN}}$ is high, the rising edge of the reset pulse begins chip initialization. After the initialization time, the TAS5010 begins normal operation.

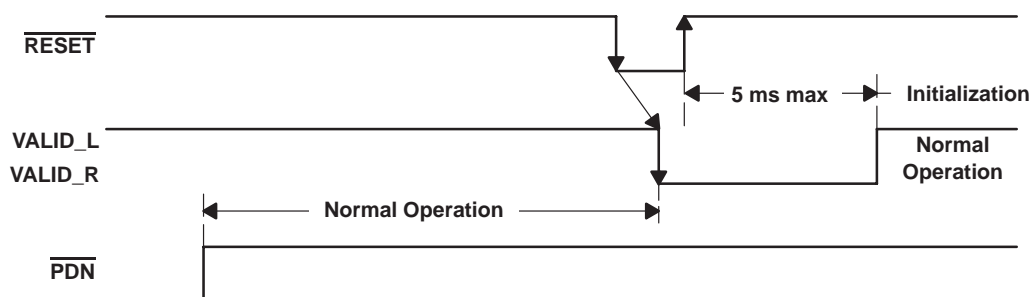


Figure 3. Reset Timing

power down

When PDN is low (see Figure 4), both the PLL and the oscillator are shut down. Note that power down is an asynchronous operation. To place the device in total power-down mode, both $\overline{\text{RESET}}$ and $\overline{\text{PDN}}$ must be held low. As long as these pins are held low, the chip is in the power-down state and the PWM outputs are hard muted with the P outputs held low and the M outputs held high. To place the device back into normal mode, see the power up section.

NOTE:

In order for the dynamic logic to be properly powered down, the clocks should not be stopped before the PDN pin goes low. Otherwise, the device may drain additional supply current.

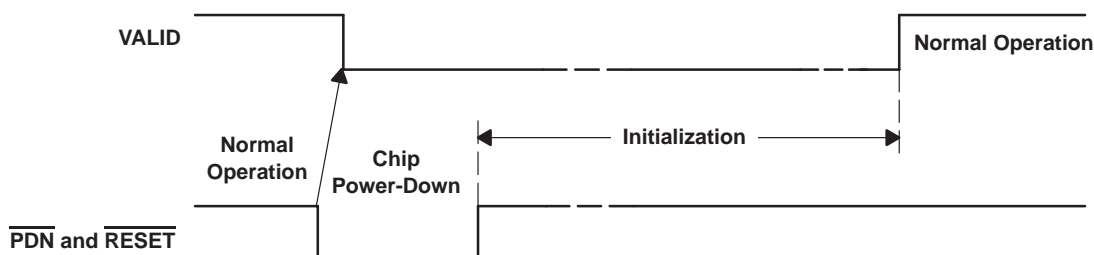


Figure 4. Power-Down Timing

mute

The TAS5010 provides a mute function that is used when the $\overline{\text{MUTE}}$ pin is asserted low. See Table 2 for mute description. This mute is a quiet mute; that is, the mute is accomplished by outputting a zero value waveform in which both sides of the differential PWM outputs have a 50% duty cycle (see Figure 5 for mute timing).

Table 2. Mute Description

$\overline{\text{MUTE}}$	P OUTPUTS	M OUTPUTS	DESCRIPTION
0	50% duty cycle	50% duty cycle	Mute
1	DATA	DATA	Normal operation

functional description (continued)

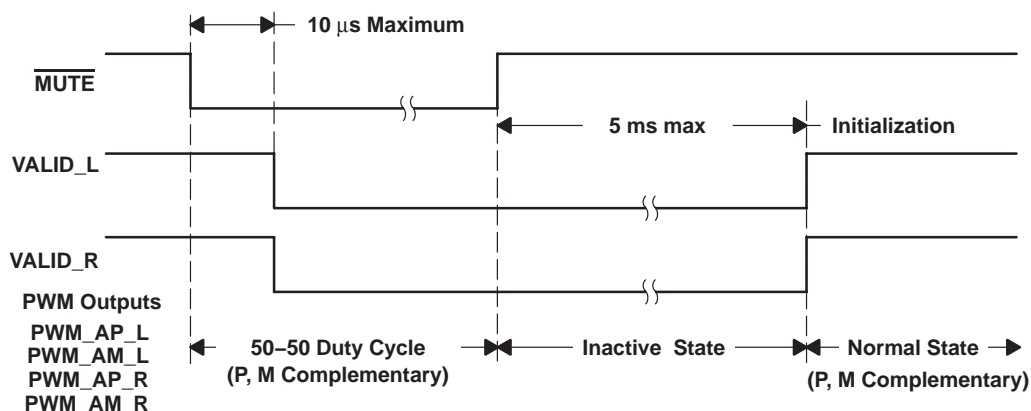


Figure 5. Mute Timing

double speed

Double-speed mode is used to support sampling rates of 88.2 kHz and 96 kHz. In order to put the TAS5010 in double-speed mode with the device in normal operating conditions, the **RESET** pin must be held low while switching the **DBSPD** pin high. After the **RESET** pin is brought high again, a reset sequence takes place. If the change is at power up, a power-up sequence is originated.

quad speed

Quad-speed mode is used to support sampling rates of 176.4 kHz and 192 kHz. It is supported in slave mode only. In order to put the TAS5010 in quad-speed mode, **M_S** and **DBPSB** pins are brought low. Quad-speed mode is then automatically detected due to the fact that it is the only mode in which **MCLK_IN** is 128Fs.

de-emphasis filter

For audio sources that have been preemphasized, a precision 50 μs/15 μs de-emphasis filter is provided to support the sampling rates of 44.1 kHz and 48 kHz. Pins **DEM_SEL** and **DEM_EN** select the de-emphasis functions. See Figure 6 for a graph showing the de-emphasis filtering characteristics. See Table 3 for de-emphasis selection.

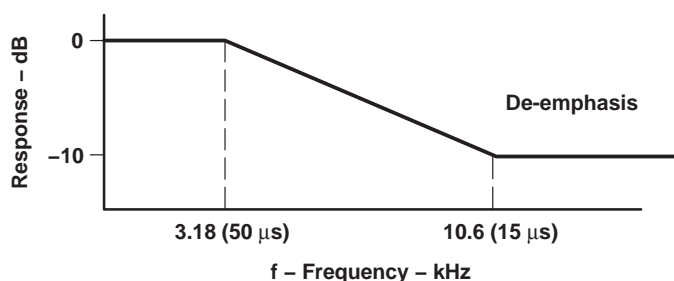


Figure 6. De-Emphasis Filter Characteristics

functional description (continued)**de-emphasis selection**

De-emphasis selection is accomplished by using the DEM_SEL and DEM_EN pins. See Table 3 for de-emphasis selection description.

Table 3. De-Emphasis Selection

DEM_SEL	DEM_EN	DESCRIPTION
0	0	De-emphasis disabled
0	1	De-emphasis enabled for $F_s = 44.1$ kHz
1	1	De-emphasis enabled for $F_s = 48$ kHz
1	0	Forbidden mode. Do not use.

error status reporting (VALID_L and VALID_R)

The following is a list of the error conditions that will cause the VALID_L and VALID_R pins to be asserted low:

- No clocks
- Clock phase errors

When either of the above conditions is met, the VALID_L and VALID_R goes low and the PWM outputs go to the hard mute state. If the error condition is removed, the TAS5010 is reinitialized and the VALID_L and VALID_R pins are asserted high.

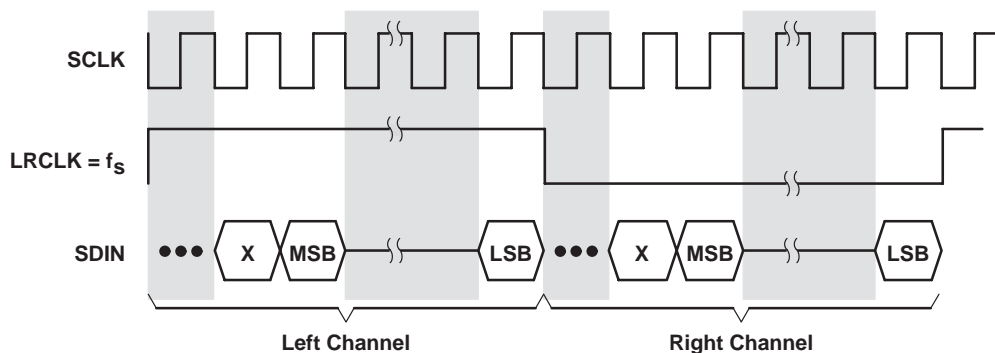
serial interface formats

The TAS5010 is compatible with eight different serial interfaces. Available interface options are IIS, right justified, left justified, and DSP frame. Table 4 indicates how these options are selected using the MOD0, MOD1, and MOD2 pins.

Table 4. Hardware Selection of Serial Audio Modes

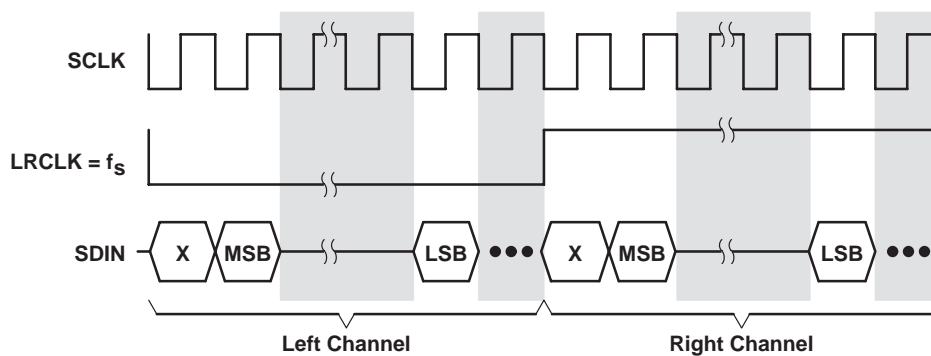
MODE	MOD2 PIN	MOD1 PIN	MOD0 PIN	SERIAL INTERFACE SDIN
0	0	0	0	16 bit, MSB first; right justified
1	0	0	1	20 bit, MSB first; right justified
2	0	1	0	24 bit, MSB first; right justified
3	0	1	1	16 bit IIS
4	1	0	0	20 bit IIS
5	1	0	1	24 bit IIS
6	1	1	0	16 bit MSB first, left justified
7	1	1	1	16 bit DSP frame

The following figures illustrate the relationship between the SCLK, LRCLK and the serial data I/O for the different interface protocols. Note that there are always 64 SCLKs per LRCLK. The nondata bits are padded with binary 0s.

functional description (continued)**MSB first, right-justified (for 16, 20, 24 bits)****Figure 7. MSB First Right Justified**

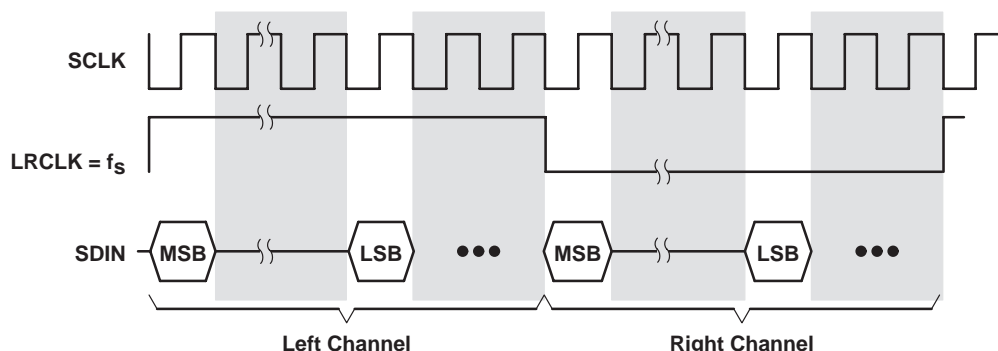
Note the following characteristics of this protocol:

- Left channel is received when LRCLK is high.
- Right channel is received when LRCLK is low.
- SDIN is sampled at the rising edge of SCLK.

IIS compatible serial format (for 16, 20, 24 bits)**Figure 8. IIS Compatible Serial Format**

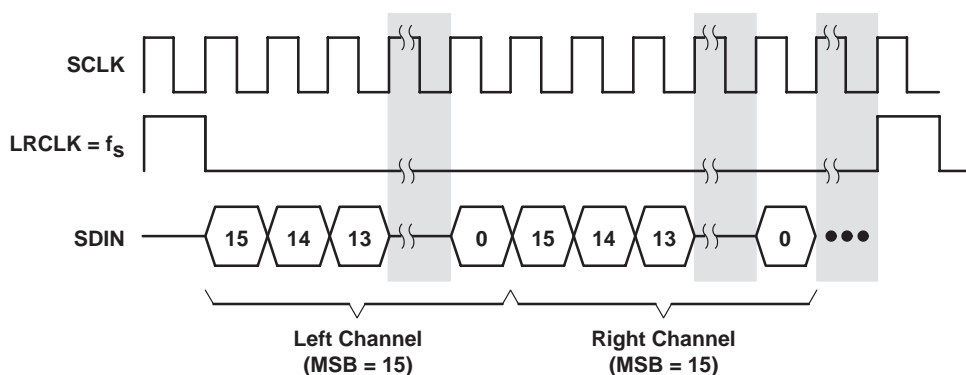
Note the following characteristics of this protocol:

- Left channel is received when LRCLK is low.
- Right channel is received when LRCLK is high.
- SDIN is sampled with the rising edge of the SCLK.

functional description (continued)**MSB left-justified serial interface format (for 16 bits)****Figure 9. MSB Left-Justified Serial Interface Format**

Note the following characteristics of this protocol:

- Left channel is received when LRCLK is high.
- Right channel is received when LRCLK is low.
- SDIN is sampled at the rising edge of SCLK.

DSP compatible serial interface format (for 16 bits)**Figure 10. DSP Compatible Serial Interface Format**

Note the following characteristics of this protocol:

- Serial data is sampled with the falling edge of SCLK.

PWM Outputs

Designed to be used with the TAS5100 family of H-Bridges, the PWM outputs provide differential 3.3 V square-wave signals. During normal operation these outputs represent the input PCM audio in the pulse-width modulation scheme. In the hard-mute state the P outputs (PWM_AP_L and PWM_AP_R) are held low and the M outputs (PWM_AM_L and PWM_AM_R) are held high. In the quiet-mute state the differential PWM outputs have a 50% duty cycle.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Analog supply voltage range, AV_{DD1} , AV_{DD2}	–0.3 V to 4.2 V
Digital power supply voltage, DV_{DD1} , DV_{DD2} , DV_{DD3_L} , DV_{DD3_R}	–0.3 V to 4.2 V
Digital input voltage, V_I (see Note 1)	–0.3 V to $DV_{DDX}+0.3$ V
Operating free-air temperature, T_A	0°C to 70°C
Storage temperature, T_{stg}	–65°C to 150°C
ESD	2000 V

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: DV_{DD1} , DV_{DD2} , DV_{DD3_L} , DV_{DD3_R} .

recommended operating conditions, $T_A = 25^\circ\text{C}$, $DV_{DD1} = DV_{DD2} = DV_{DD3_L} = DV_{DD3_R} = 3.3\text{ V} \pm 10\%$, $AV_{DD1} = AV_{DD2} = 3.3\text{ V} \pm 10\%$, $F_s = 44.1\text{ kHz}$

			MIN	TYP	MAX	UNIT
Supply voltage	Digital	DV_{DDX}^\ddagger	3	3.3	3.6	V
Supply current	Digital	Operating		22		mA
		Power down§		10	20	µA
Power dissipation	Digital	Operating		59.4		mW
		Power down§		6.6	72	µW
Supply voltage	Analog	AV_{DDX}^\P	3	3.3	3.6	V
Supply current	Analog	Operating		8		mA
		Power down§		10	100	µA
Power dissipation	Analog	Operating		26.4		mW
		Power down§		33	360	µW

‡ DV_{DD1} , DV_{DD2} , DV_{DD3_L} , DV_{DD3_R}

§ If the clocks are turned off

¶ AV_{DD1} , AV_{DD2}

electrical characteristics, $T_A = 25^\circ\text{C}$, $DV_{DD1} = DV_{DD2} = DV_{DD3_L} = DV_{DD3_R} = 3.3\text{ V} \pm 10\%$, $AV_{DD1} = AV_{DD2} = 3.3\text{ V} \pm 10\%$ **static digital specifications**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH} High-level input voltage		2		DV_{DD1}	V
V_{IL} Low-level input voltage		0		0.8	V
V_{OH} High-level output voltage	$I_O = -1\text{ mA}$	2.4			V
V_{OL} Low-level output voltage	$I_O = 4\text{ mA}$			0.4	V
Input leakage current		–10		10	µA

digital interpolation filter and PWM modulator, $F_s = 44.1\text{ kHz}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass band		0		20	kHz
Pass band ripple			± 0.012		dB
Stop band			24.1		kHz
Stop band attenuation	24.1 kHz to 152.3 kHz	50			dB
Group delay			700		µS
PWM modulation index (gain)			0.93		

TAS5010/TAS5100 system performance measured at the speaker terminals

See application note, literature number SLAA117.

switching characteristics,

$T_A = 25^\circ\text{C}$, $DV_{DD1} = DV_{DD2} = DV_{DD3_L} = DV_{DD3_R} = AV_{DD1} = AV_{DD2} = 10\% \ 3.3 \text{ V} \pm 10\%$

serial audio ports slave mode

PARAMETER		MIN	TYP	MAX	UNIT
f(SCLK)	SCLK frequency			12.288	MHz
t _{su} (SDIN)	SDIN setup time before SCLK rising edge	20			ns
t _h (SDIN)	SDIN hold time from SCLK rising edge	10			ns
F(LRCLK)	LRCLK frequency	44.1	48	192	kHz
	MCLK duty cycle		50%		
	SCLK duty cycle		50%		
	LRCLK duty cycle		50%		
t _{su} (LRCLK)	LRCLK edge setup before SCLK rising edge	20			ns

serial audio ports master mode, load conditions: 50 pF

PARAMETER		MIN	TYP	MAX	UNIT
t(MSD)	MCLK to SCLK	0		5	ns
t(MLRD)	MLCK to LRCLK	0		5	ns

DSP serial interface mode

PARAMETER		MIN	TYP	MAX	UNIT
f(SCLK)	SCLK frequency			12.288	MHz
t _W (FSHIGH)	Pulse duration, sync		$1/(64 \times f_s)$		ns
t _{su} (SDIN), t _{su} (LRCLK)	SDIN and LRCLK setup time before SCLK falling edge	20			ns
t _h (SDIN), t _h (LRCLK)	SDIN and LRCLK hold time from SCLK falling edge	10			ns
	SCLK duty cycle		50%		

PARAMETER MEASUREMENT INFORMATION

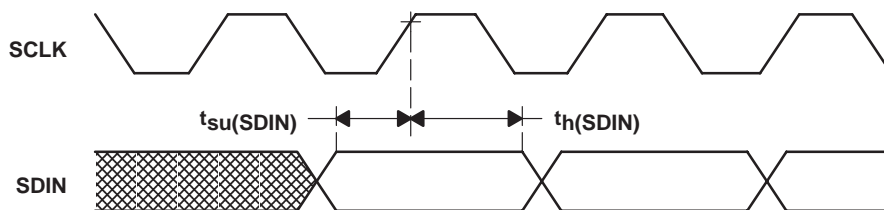
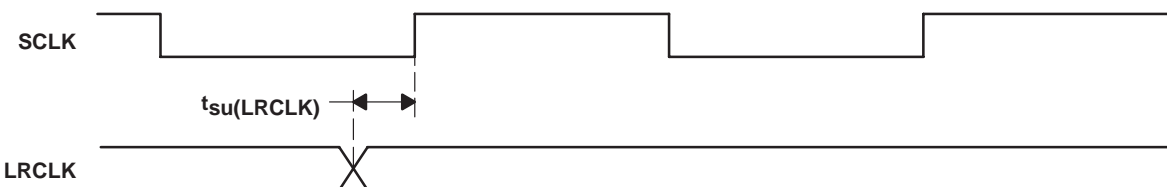


Figure 11. Right-Justified, IIS, Left-Justified Serial Protocol Timing



NOTE: Serial data is sampled with the rising edge of SCLK (setup time = 20 ns and hold time = 10 ns)

Figure 12. Right, Left, and IIS Serial Mode Timing Requirement

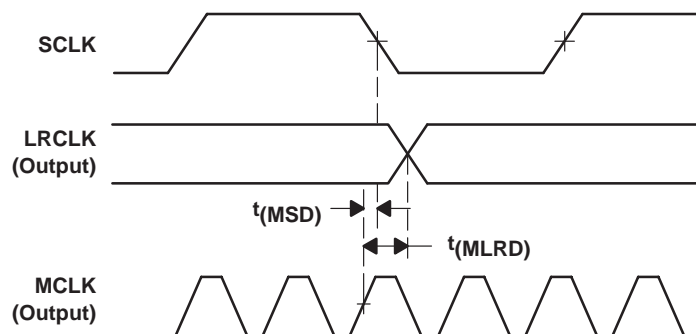


Figure 13. Serial Audio Ports Master Mode Timing

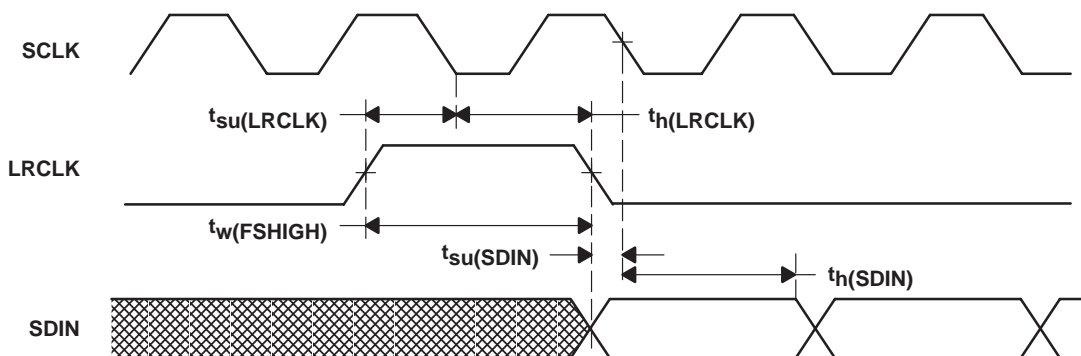


Figure 14. DSP Serial Port Timing

PARAMETER MEASUREMENT INFORMATION

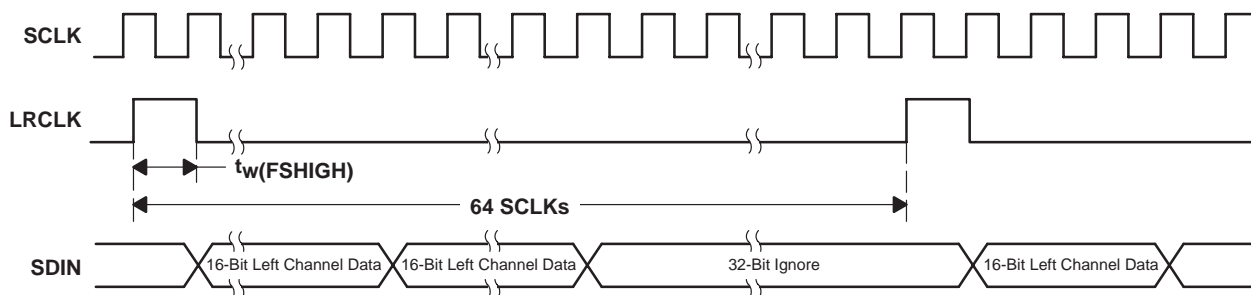
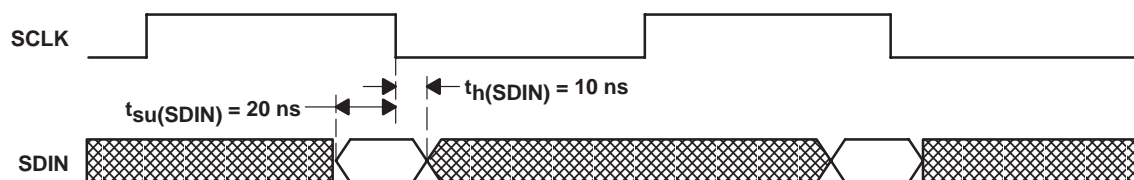


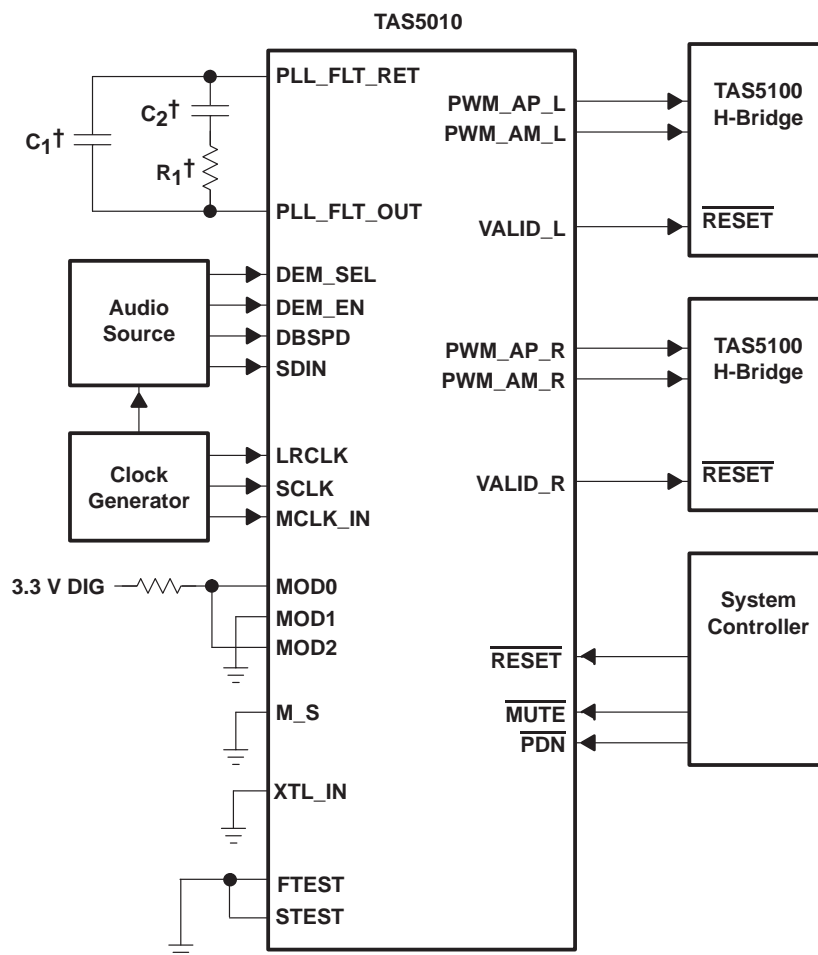
Figure 15. DSP Serial Port Expanded Timing



NOTE: Serial data is sampled with the falling edge of SCLK (setup time = 20 ns and hold time = 10 ns)

Figure 16. DSP Absolute Timing Requirement

APPLICATION INFORMATION

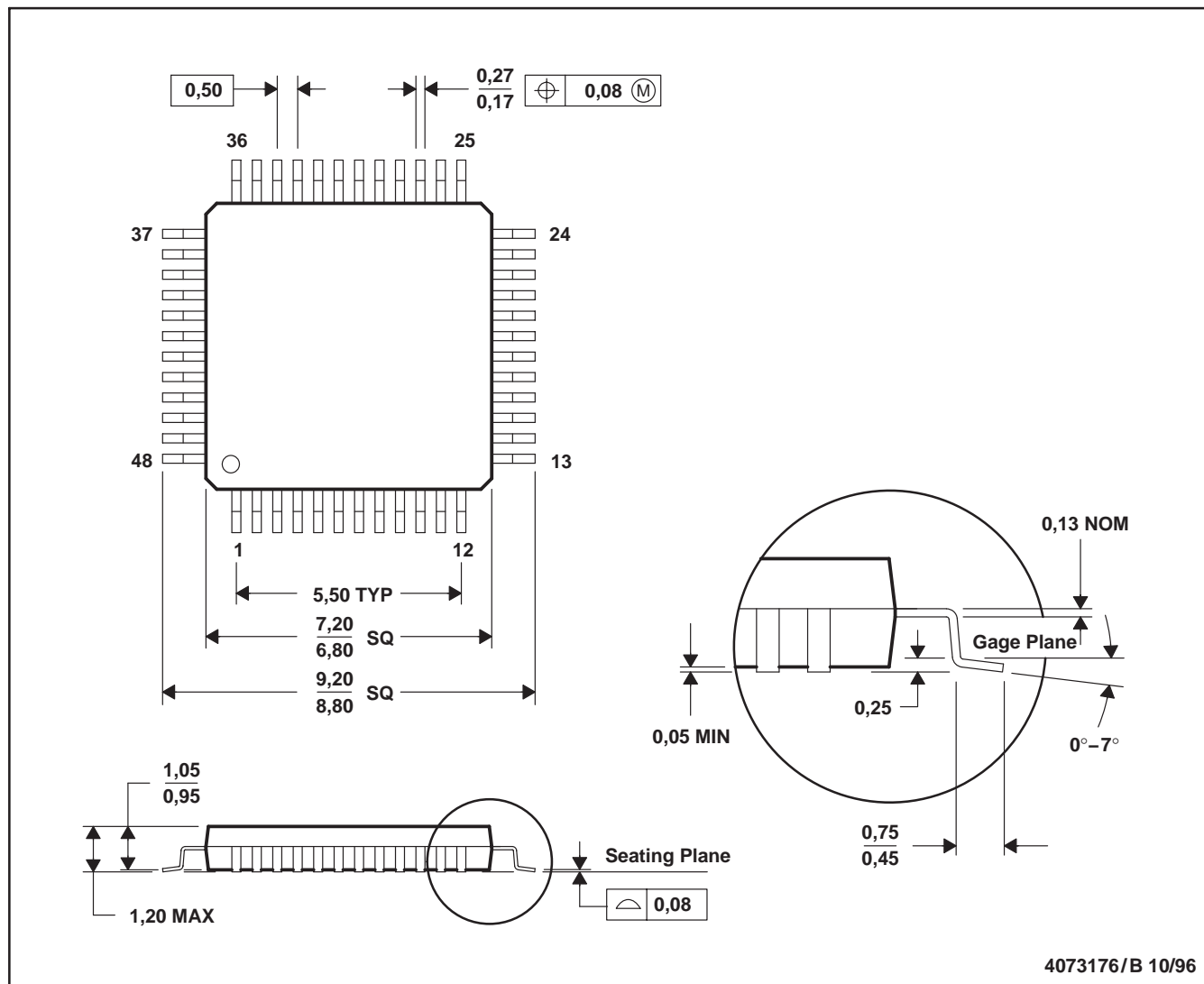


† See application note, literature number SLAA117 for values

MECHANICAL DATA

PFB (S-PQFP-G48)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-026

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated