TOSHIBA Bipolar Linear Integrated Circuit SiGe Monolithic

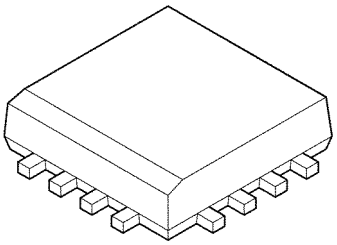
TA4500F

1.9 GHz Band RX Front-End IC

PHS, Digital Cordless Telecommunication Applications

Features

- Low-noise amplifier / down-conversion mixer
- Integrated local buffer amplifier
- Single positive power supply: V_{CC} = 3.0 V
- Large conversion gain: G_{LNA} = 17.5 dB (typ.)
  G_{MIX} = 5.0 dB (typ.)
- High input IP3: $IIP3_{LNA}$ = -7.5 dBmW (typ.)
  $IIP3_{MIX}$ = 7.0 dBmW (typ.)
- High 1/2 IF reduction ratio: $1/2IFR_{MIX}$ = 45 dB (typ.)
- Small package: QS16 (2.5 mm × 2.5 mm × 0.55 mm)



QS16

Weight: 0.0065 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Supply voltage	V_{CC} (Note 1)	4.5	V
Input power	P_{IN} (RF_IN)	10	dBmW
	P_{IN} (LO_IN)	0	dBmW
	P_{IN} (MIX_IN)	0	dBmW
Power dissipation	P_d (Note 2)	500	mW
Operating temperature range	Topr	−40 to +85	°C
Storage temperature range	Tstg	−55 to +150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: VCC = VCC1 = VCC2 = VCC3

Note 2: When mounted on a 30 mm × 35 mm × 0.6 mm FR4 substrate at Ta = 25°C (double-sided substrate: the reverse side is ground connection)

Caution

This device is sensitive to electrostatic discharge. When handling this product, ensure that the environment is protected against electrostatic discharge by using an earth strap, a conductive mat and an ionizer.

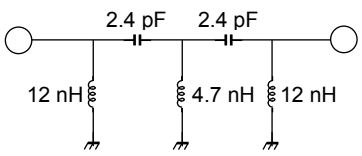
Electrical Characteristics

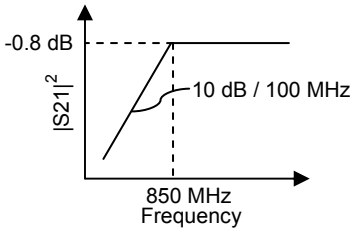
V_{CC} = 3.0 V, Ta = 25°C, Zg = Zl = 50 Ω

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Total						
Operating frequency	f	—	1.884	—	1.920	GHz
Operating supply voltage	V_{CC}	—	2.7	3.0	3.3	V
Supply current	I_{CC}	pRF_IN = pLO_IN = pMIX_IN = 0 mW (no signal)	—	15.0	22.0	mA
Low Noise Amplifier (LNA) Block						
Power gain	G_{LNA}	fRF_IN = 1.9 GHz, pRF_IN = -35 dBmW	15.0	17.5	22.0	dB
Noise figure	NF_{LNA}	Measured at 1.9 GHz	—	2.2	3.0	dB
Input IP3	$IIP3_{LNA}$	(Note 3)	-13.5	-7.5	—	dBmW
Down Conversion Mixer (MIX) Block						
Conversion gain	G_{MIX}	fMIX_IN = 1.9 GHz, pMIX_IN = -25 dBmW, fLO_IN = 1.66 GHz, pLO_IN = -15 dBmW, measured at IF_OUT1, IF_OUT2 terminated via 50 Ω and vice versa	2.8	5.0	7.0	dB
Noise figure	NF_{MIX}	fLO_IN = 1.66 GHz, pLO_IN = -15 dBmW, measured at IF_OUT1, IF_OUT2 terminated via 50 Ω and vice versa, fIF_OUT = 240 MHz, DSB (Note 4)	—	13.0	17.5	dB
Input IP3	$IIP3_{MIX}$	fLO_IN = 1.66 GHz, pLO_IN = -15 dBmW, measured at IF_OUT1, IF_OUT2 terminated via 50 Ω and vice versa (Note 5)	-1.0	7.0	—	dBmW
1/2 IF reduction ratio	$1/2IFR_{MIX}$	fMIX_IN = 1.9 GHz, 1.78 GHz, pMIX_IN = -25 dBmW, fLO_IN = 1.66 GHz, pLO_IN = -15 dBmW, measured at IF_OUT1, IF_OUT2 terminated via 50 Ω and vice versa, fIF_OUT = 240 MHz	—	45.0	—	dB
Local leak power	P_{LK}	fLO_IN = 1.66 GHz, pLO_IN = -15 dBmW, measured at MIX_IN, IF_OUT1, 2 terminated via 50 Ω	—	-40.0	—	dBmW

Note 3: IIP3 of the LNA block is converted from IM3 when RF1 = 1.900 GHz / −35 dBmW, RF2 = 1.9006 GHz / −35 dBmW are input to RF_IN.

Note 4: Measured with the high pass filter shown below connected to MIX_IN.

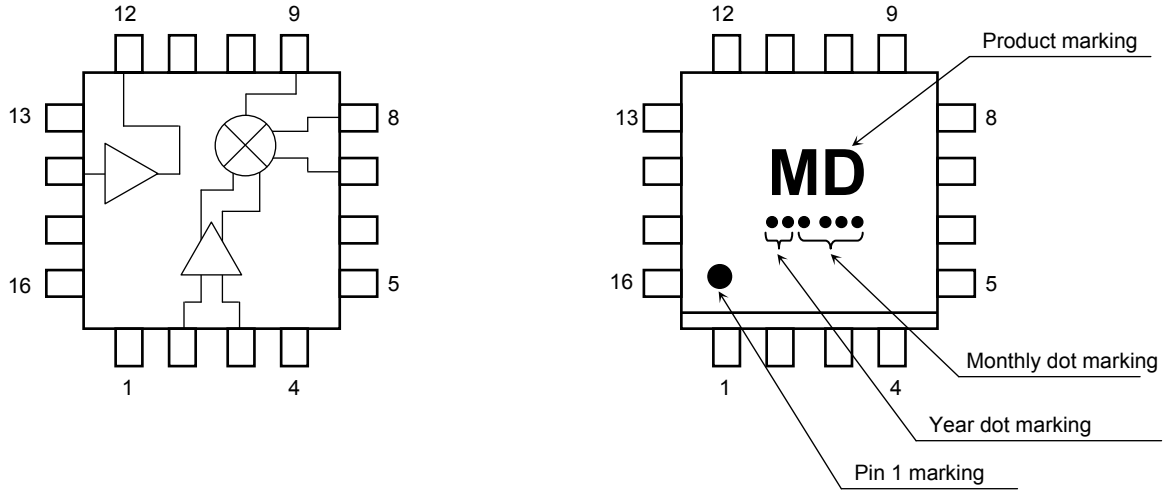




Note 5: IIP3 of the MIX block is converted from IM3 when RF1 = 1.900 GHz / −25 dBmW, RF2 = 1.9006 GHz / −25 dBmW are input to MIX_IN.

Note 6: All tests for electrical characteristics are performed using the test board shown on page 4.

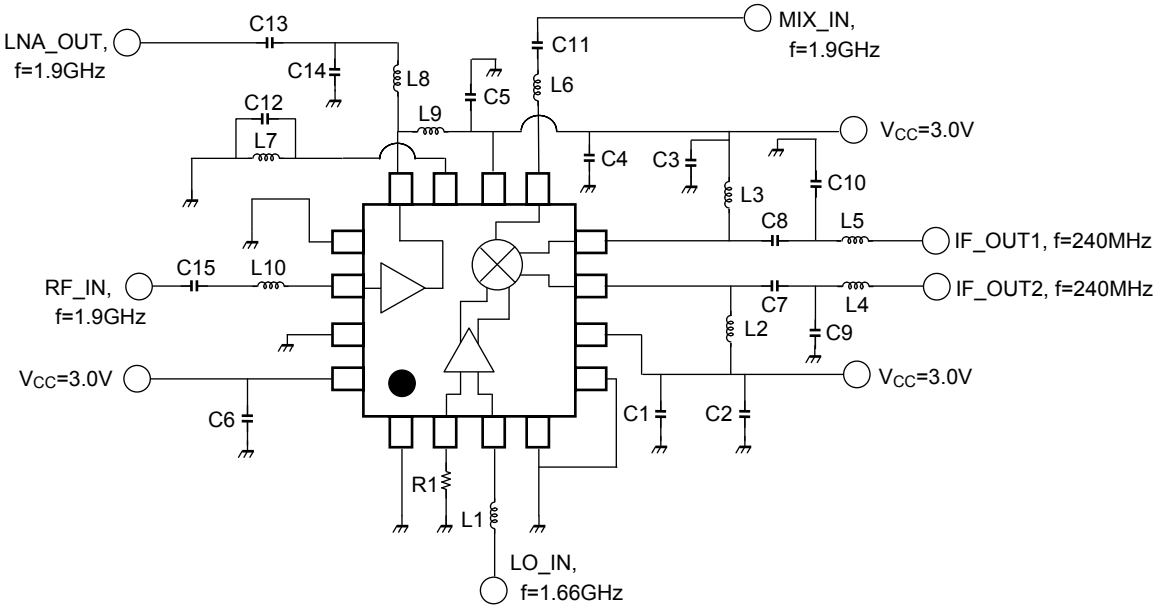
Block Diagram and Marking (Top View)



Pin Configuration

Pin number	Pin name	Description
1	N.C.	Not connected to the pellet. Connect to ground.
2	LO_term	MIX local input termination pin. To be terminated.
3	LO_IN	MIX local input
4	GND1	Ground.
5	GND2	Ground.
6	V_{CC2}	Supply pin for MIX.
7	IF_OUT2	MIX IF output. Biasing circuit is necessary.
8	IF_OUT1	MIX IF output. Biasing circuit is necessary.
9	MIX_IN	MIX RF input.
10	V_{CC1}	Supply pin for LNA and biasing circuits.
11	LNA_ind	LNA emitter. Connect to ground via 1 nH inductance // 1 pF capacitance.
12	LNA_OUT	LNA output. Biasing circuit is necessary.
13	GND3	Ground.
14	RF_IN	LNA input.
15	GND4	Ground.
16	V_{CC3}	Supply pin for MIX.

Circuit Diagram of Test Board

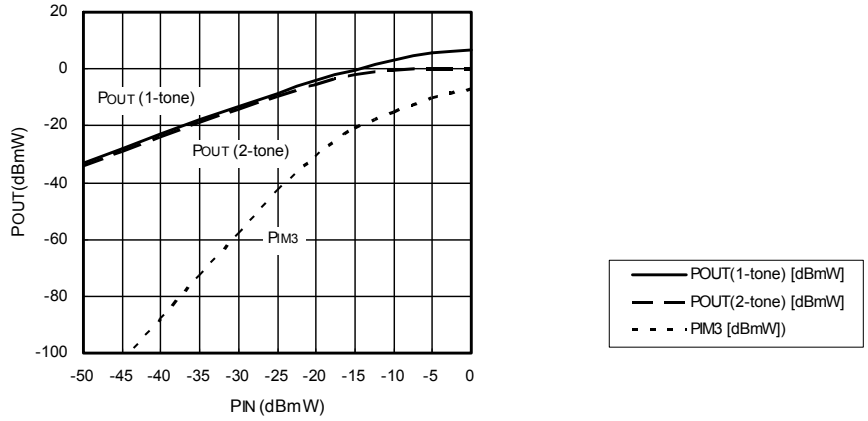


List of External Chip Components

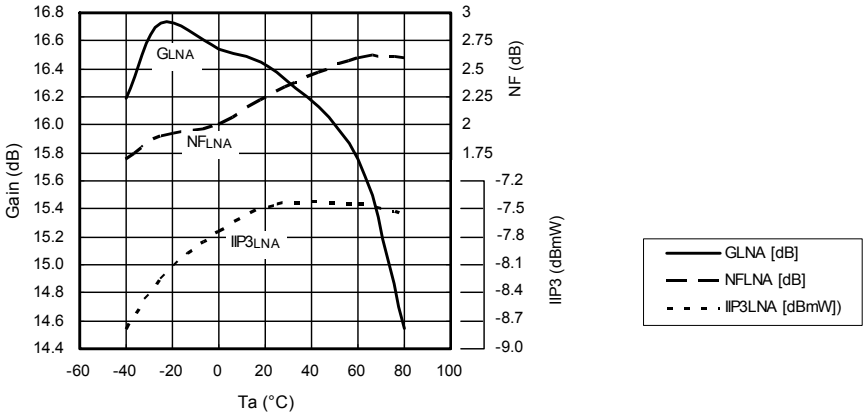
Part	Value	Chip Series	Description
C1	1000 pF	GRM15 series MURATA	Decoupling capacitor
C2	1000 pF	GRM15 series MURATA	Decoupling capacitor
C3	1000 pF	GRM15 series MURATA	Decoupling capacitor
C4	1000 pF	GRM15 series MURATA	Decoupling capacitor
C5	1000 pF	GRM15 series MURATA	Decoupling capacitor
C6	1000 pF	GRM15 series MURATA	Decoupling capacitor
C7	1000 pF	GRM15 series MURATA	DC blocking capacitor
C8	1000 pF	GRM15 series MURATA	DC blocking capacitor
C9	5 pF	GRM15 series MURATA	IF_OUT matching
C10	5 pF	GRM15 series MURATA	IF_OUT matching
C11	39 pF	GRM15 series MURATA	MIX_IN matching
C12	1 pF	GRM15 series MURATA	Determining LNA gain
C13	82 pF	GRM15 series MURATA	LNA_OUT matching
C14	1.2 pF	GRM15 series MURATA	LNA_OUT matching
C15	3 pF	GRM15 series MURATA	RF_IN matching
L1	8.2 nH	LQG15HN series MURATA	LO_IN matching
L2	120 nH	LQG15HN series MURATA	MIX output load
L3	120 nH	LQG15HN series MURATA	MIX output load
L4	120 nH	LQG15HN series MURATA	IF_OUT matching
L5	120 nH	LQG15HN series MURATA	IF_OUT matching
L6	8.2 nH	LQG15HN series MURATA	MIX_IN matching
L7	1 nH	LQG15HN series MURATA	Determining LNA gain
L8	10 nH	LQG15HN series MURATA	LNA_OUT matching
L9	15 nH	LQG15HN series MURATA	LNA output load
L10	6.8 nH	LQG15HN series MURATA	LNA_IN matching
R1	51 Ω	MCR01 series ROHM	LO termination load

Typical Operating Characteristics of Low-Noise Amplifier Block

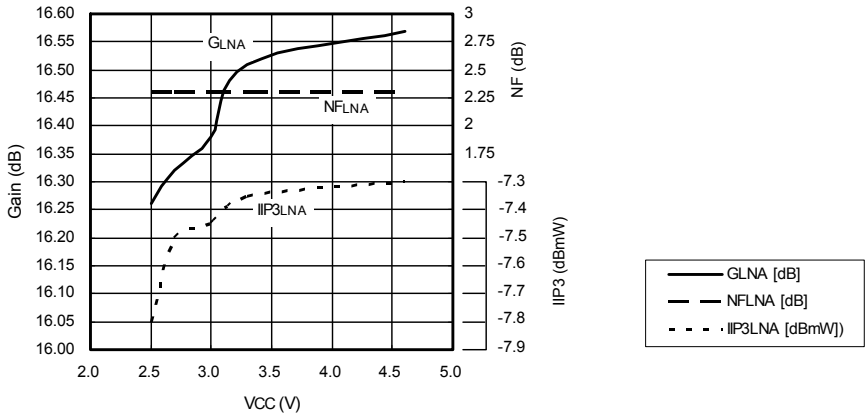
LNA Block
POUT(1-,2-tone),PIM3 vs PIN
VCC = 3 V, Ta = 25 °C,
RF1 = 1.9000 GHz,
RF2 = 1.9006 GHz for 2-tone, IM3 measurement



LNA Block
GLNA, IIP3LNA, NFLNA vs Temperature
VCC = 3 V,
RF1 = 1.9000 GHz/-35 dBmW,
RF2 = 1.9006 GHz/-35 dBmW for IIP3 measurement

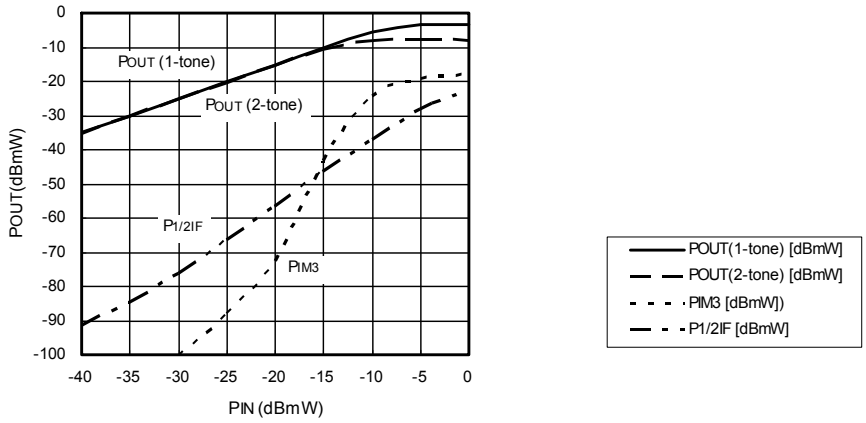


LNA Block
GLNA, IIP3LNA, NFLNA vs VCC
Ta = 25 °C,
RF1 = 1.9000 GHz/-35 dBmW,
RF2 = 1.9006 GHz/-35 dBmW for IIP3 measurement

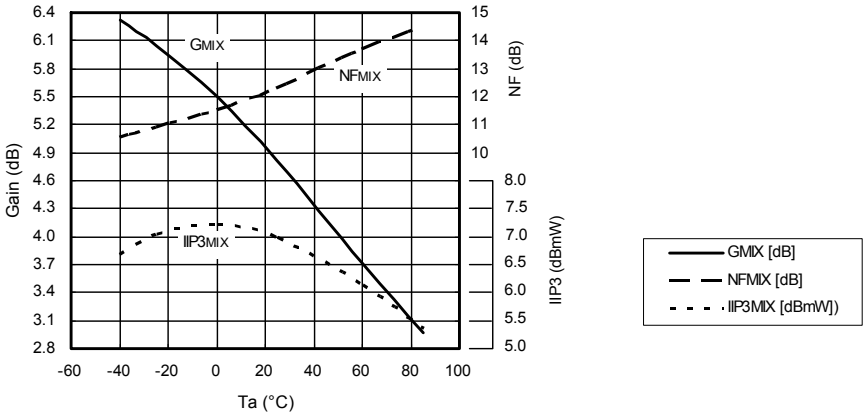


Typical Operating Characteristics of Down Conversion Mixer Block

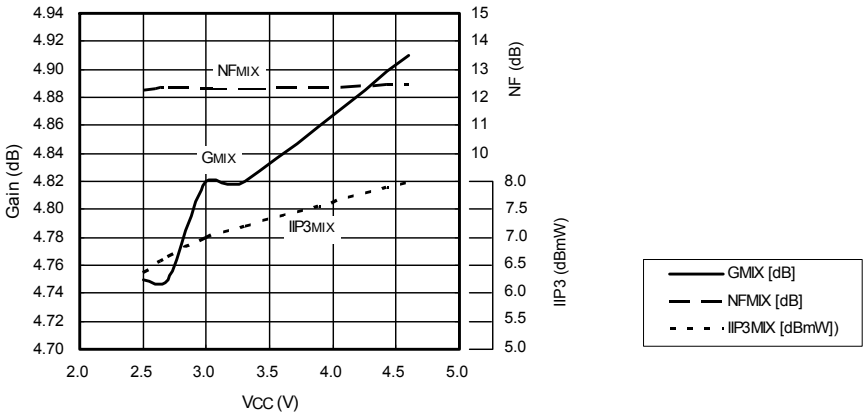
MIX Block
POUT(1-,2-tone),PIM3 , P1/2IF vs PIN
VCC = 3 V,Ta = 25 °C,
LO = 1.66 GHz/-15dBmW, RF1 = 1.9000 GHz, 1.7800 GHz,
RF2 = 1.9006 GHz for 2-tone, IM3 measurement



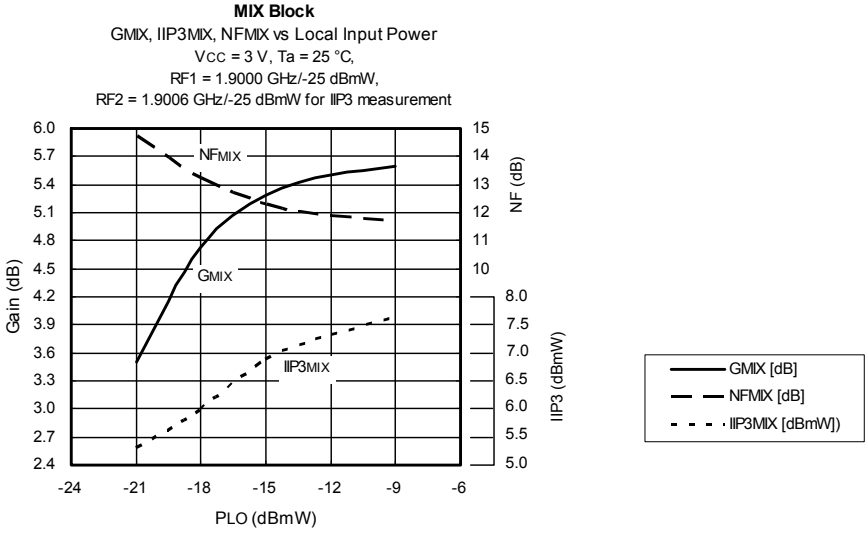
MIX Block
GMIX, IIP3MIX, NFMIX vs Temperature
VCC = 3 V,
LO = 1.66 GHz/-15 dBmW, RF1 = 1.9000 GHz/-25 dBmW,
RF2 = 1.9006 GHz/-25 dBmW for IIP3 measurement



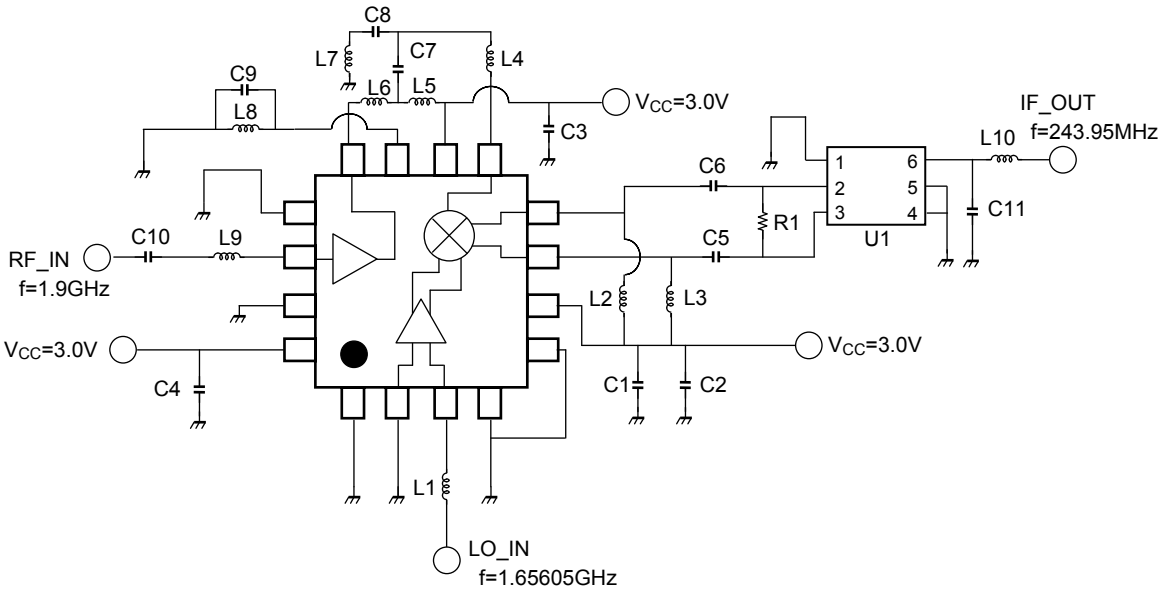
MIX Block
GMIX, IIP3MIX, NFMIX vs VCC
Ta = 25 °C,
LO = 1.66 GHz/-15 dBmW, RF1 = 1.9000 GHz/-25 dBmW,
RF2 = 1.9006 GHz/-25 dBmW for IIP3 measurement



Typical Operating Characteristics of Down Conversion Mixer Block (continued)



Circuit Diagram of Evaluation Board



List of External Chip Components on Evaluation Board

Part	Value	Chip Series	Part	Value	Chip Series
C1	1000 pF	GRM15 series MURATA	L2	120 nH	LQG15HN series MURATA
C2	1000 pF	GRM15 series MURATA	L3	120 nH	LQG15HN series MURATA
C3	1000 pF	GRM15 series MURATA	L4	5.6 nH	LQG15HN series MURATA
C4	1000 pF	GRM15 series MURATA	L5	2.2 nH	LQG15HN series MURATA
C5	1000 pF	GRM15 series MURATA	L6	3.3 nH	LQG15HN series MURATA
C6	1000 pF	GRM15 series MURATA	L7	5.6 nH	LQG15HN series MURATA
C7	1 pF	GRM15 series MURATA	L8	1 nH	LQG15HN series MURATA
C8	2 pF	GRM15 series MURATA	L9	6.8 nH	LQG15HN series MURATA
C9	1 pF	GRM15 series MURATA	L10	100 nH	LQG15HN series MURATA
C10	3 pF	GRM15 series MURATA	R1	1.2 kΩ	MCR01 series ROHM
C11	2.7 pF	GRM15 series MURATA	U1	243.95 MHz	SAFDA243MRD9X00R00 MURATA
L1	8.2 nH	LQG15HN series MURATA			

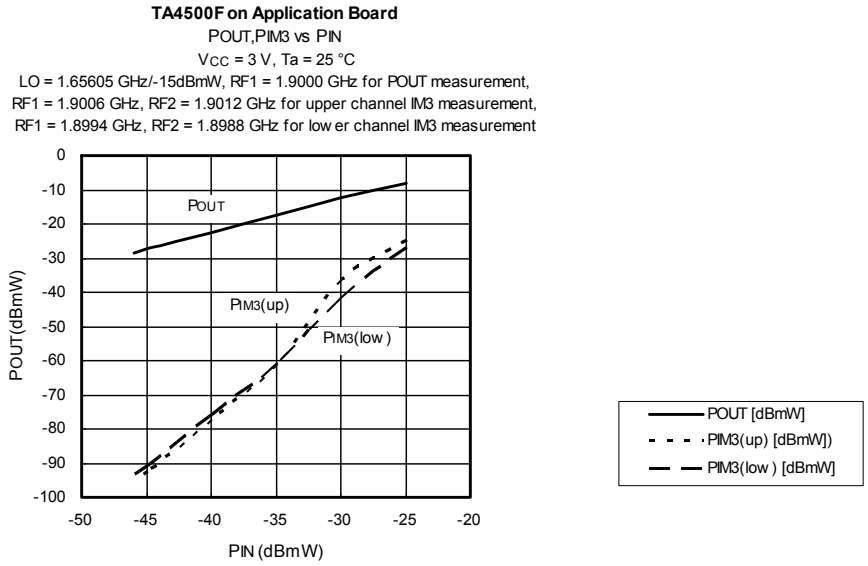
Typical Electrical Characteristics of Evaluation Board (for Reference Only)

V_{CC} = 3.0 V, Ta = 25°C, Zg = Zl = 50 Ω, fLO_IN = 1.65605 GHz, pLO_IN = -15 dBmW, fIF_OUT = 243.95 MHz

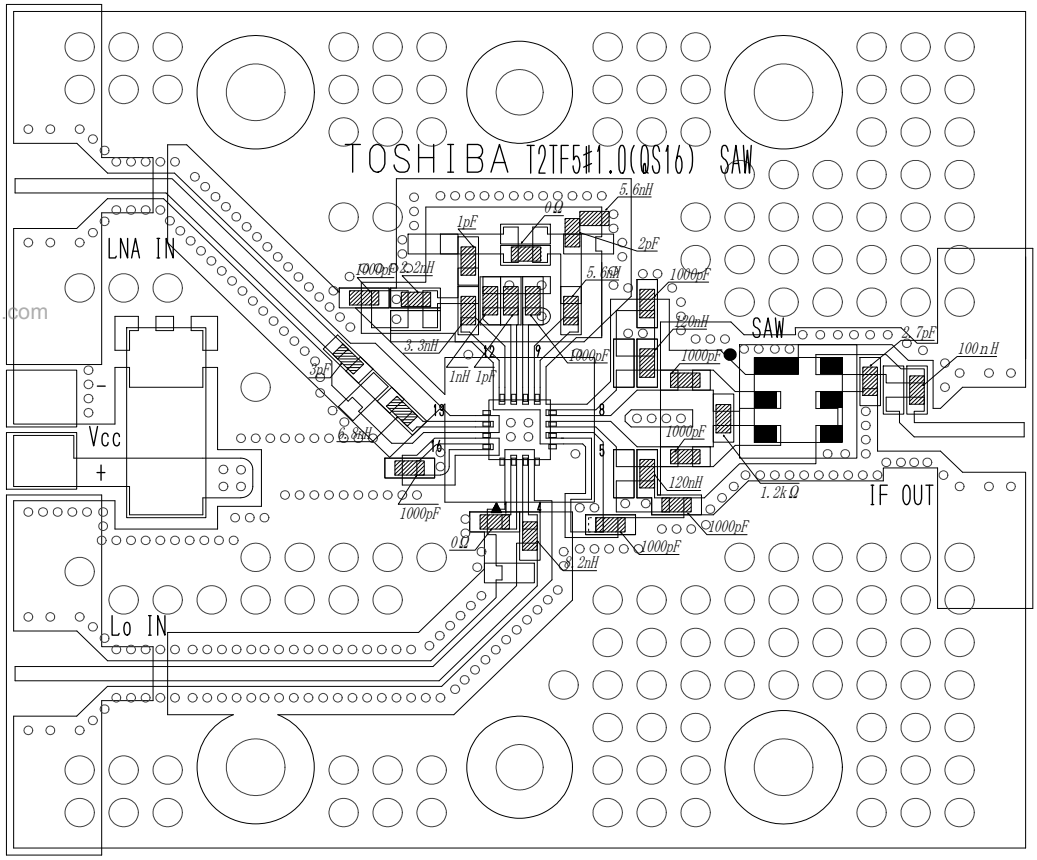
Characteristic	Symbol	Test Condition	Typ	Unit
Conversion gain	G_C	fRF_IN = 1.9 GHz, pRF_IN = -30 dBmW (Note 7)	17.5	dB
Noise figure	NF	DSB	3.8	dB
3rd order intermodulation distortion	IM3	IF output: fRF_IN = 1.9 GHz, pRF_IN = -46 dBmW, 3rd order: fRF_IN1 = 1.8994 GHz, fRF_IN2 = 1.8988 GHz, pRF_IN1 = pRF_IN2 = -46 dBmW	64.0	dB
Image reduction ratio	IMR	fRF_IN = 1.9 GHz,1.4121 GHz, pRF_IN = -46 dBmW	27.0	dB
1/2 IF reduction ratio	1/2IFR	fRF_IN = 1.9 GHz,1.778025 GHz, pRF_IN = -46 dBmW	48.0	dB

Note 7: Conversion gain in the above table includes the insertion loss (3.5 dB typical) of SAW filter, SAFDA243MRD 9X00R00.

Typical Operating Characteristics of Evaluation Board



Pattern Layout of Evaluation Board (Top Layer)



Notice

The circuits and measurements contained in this document are given in the context of example applications of the product only.

Moreover, these example application circuits are not intended for mass production since the high-frequency characteristics (i.e., the AC characteristics) of the device will be affected by the external components that the customer uses, by the design of the circuit and by various other conditions.

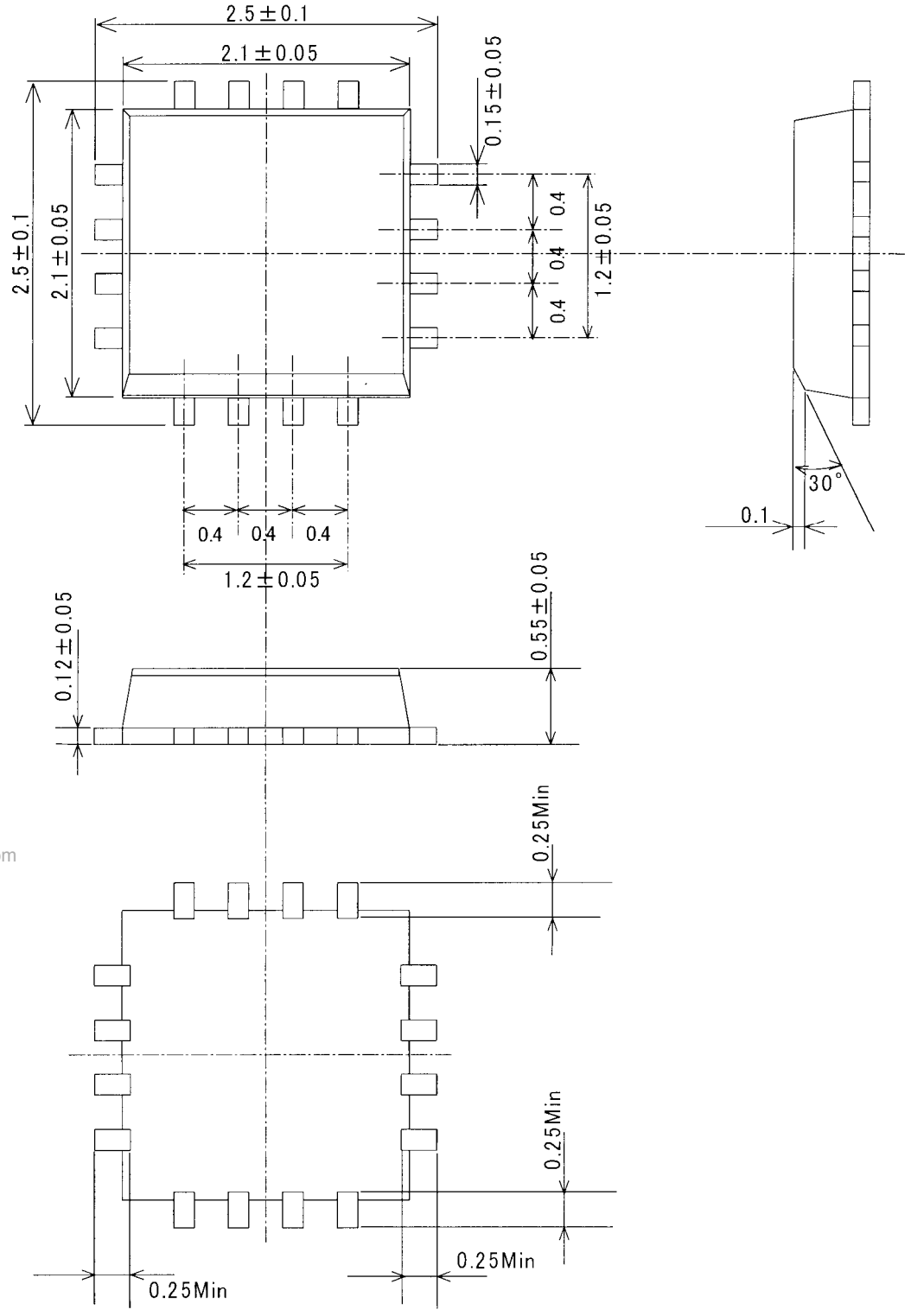
It is the responsibility of the customer to design external circuits that correctly implement the intended application and to check the characteristics of the design.

TOSHIBA assumes no responsibility for the integrity of customer circuit designs or applications.

Package Physical Dimensions

QS16

Unit: mm



Weight: 0.0065 g (typ.)

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20070701-EN GENERAL

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