# T54LS490
# T74LS490

# DUAL DECADE COUNTER

## DESCRIPTION

The T54LS490/T74LS490 contains a pair of high-speed 4-stage ripple counters. Each half of the T54LS/T74LS490 has individual Clock, Master Reset and Master Set (Preset 9) inputs. Each section counts in 8, 4, 2, 1 BCD code.

- DUAL VERSION OF 54LS/74LS90
- INDIVIDUAL ASYNCHRONOUS CLEAR AND PRESET TO 9 FOR EACH COUNTER
- COUNT FREQUENCY - TYPICALLY 65 MHz
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
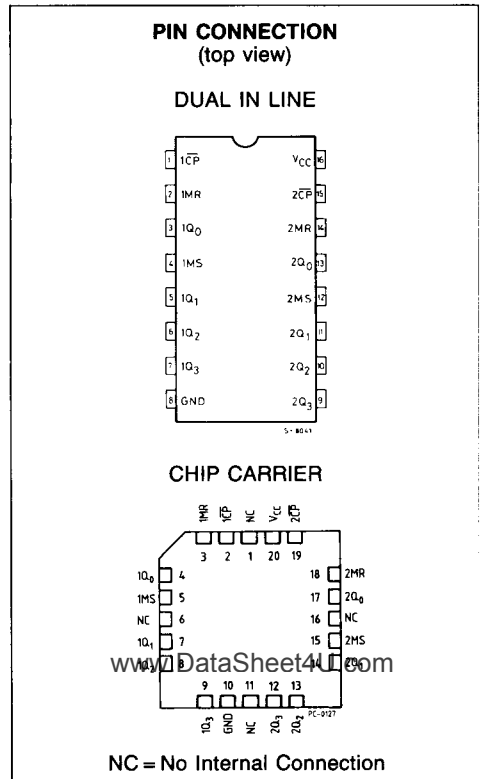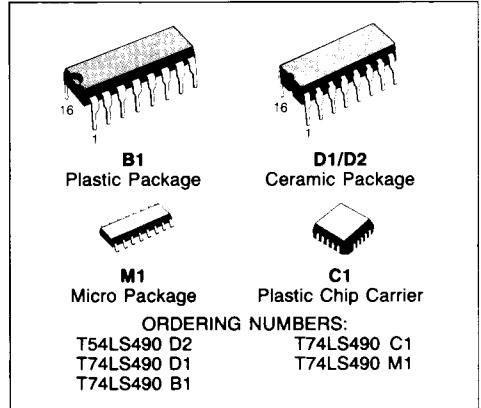- TTL AND CMOS COMPATIBLE

| | |
|---|---|
| **B1** Plastic Package | **D1/D2** Ceramic Package |
| **M1** Micro Package | **C1** Plastic Chip Carrier |

ORDERING NUMBERS:

| | |
|---|---|
| T54LS490 D2 | T74LS490 C1 |
| T74LS490 D1 | T74LS490 M1 |
| T74LS490 B1 | |

## TRUTH TABLE

| COUNT | OUTPUTS | | | |
|:---:|:---:|:---:|:---:|:---:|
| | $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

## PIN NAMES

| MS | Master Set (Set to 9) Input |
|---|---|
| MR | Master Reset |
| CP | Clock Input (Active HIGH Going Edge) |
| $Q_0$-$Q_3$ | Counter Outputs |

## PIN CONNECTION
### (top view)

### DUAL IN LINE

| Pin | | | Pin |
|---|---|---|---|
| 1 | 1CP | $V_{CC}$ | 16 |
| 2 | 1MR | 2CP | 15 |
| 3 | $1Q_0$ | 2MR | 14 |
| 4 | 1MS | $2Q_0$ | 13 |
| 5 | $1Q_1$ | 2MS | 12 |
| 6 | $1Q_2$ | $2Q_1$ | 11 |
| 7 | $1Q_3$ | $2Q_2$ | 10 |
| 8 | GND | $2Q_3$ | 9 |

### CHIP CARRIER

NC = No Internal Connection

## LOGIC SYMBOL AND LOGIC DIAGRAM



```
                        (4) 12
                         ┌──────────────┐
                         │  MS          │
              (1) 15 ──○─┤ CP           │
                         │ MR Q₀ Q₁ Q₂ Q₃│  LC-0110
                         └──────────────┘
                        (2)(3)(5)(6)(7)
                        14 13 11 10  9
```

$V_{CC}$ = Pin 16
GND = Pin 8
( ) = Pin numbers

LC-0098
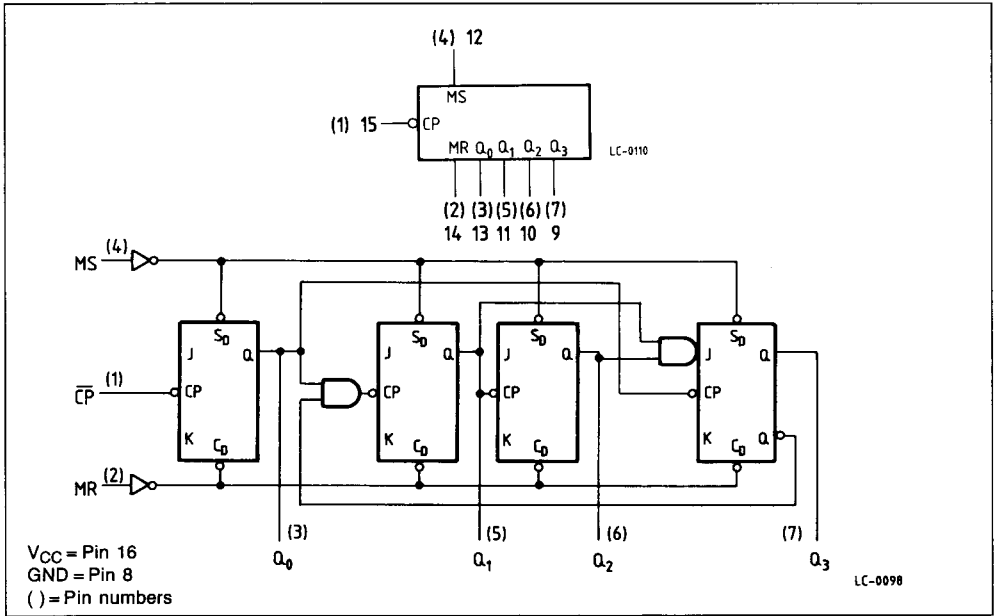
## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|--------|-----------|-------|------|
| $V_{CC}$ | Supply Voltage | − 0.5 to 7 | V |
| $V_I$ | Input Voltage, Applied to Input | − 0.5 to 5.5 | V |
| $V_O$ | Output Voltage, Applied to Output | − 0.5 to 10 | V |
| $I_I$ | Input Current, Into Inputs | − 30 to 5 | mA |
| $I_O$ | Output Current, Into Outputs | 50 | mA |

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## GUARANTEED OPERATING RANGES

| Part Numbers | Supply Voltage | | | Temperature |
|--------------|------|------|------|-------------|
| | Min | Typ | Max | |
| T54LS490D2 | 4.5  V | 5.0 V | 5.5  V | − 55°C to + 125°C |
| T74LS490XX | 4.75 V | 5.0 V | 5.25 V | 0°C to + 70°C |

XX = package type.
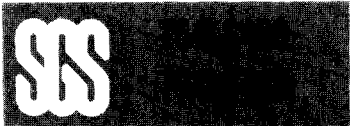
# DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

| Symbol | Parameter | | Limits | | | Test Conditions (Note 1) | Units |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | Guaranteed input HIGH Voltage for all Inputs | V |
| $V_{IL}$ | Input LOW Voltage | 54 | | | 0.7 | Guaranteed input LOW Voltage for all Inputs | V |
| | | 74 | | | 0.8 | | |
| $V_{CD}$ | Input Clamp Diode Voltage | | | $-0.65$ | $-1.5$ | $V_{CC} = MIN, I_{IN} = -18mA$ | V |
| $V_{OH}$ | Output HIGH Voltage | 54 | 2.5 | | | $V_{CC} = MIN, I_{OH} = -400\mu A, V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table | V |
| | | 74 | 2.7 | | | | |
| $V_{OL}$ | Output LOW Voltage | 54,74 | | 0.25 | 0.4 | $I_{OL} = 4.0mA$    $V_{CC} = MIN, V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table | V |
| | | 74 | | 0.35 | 0.5 | $I_{OL} = 8.0mA$ | |
| $I_{IH}$ | Input HIGH Current | | | | | | |
| | MR, MS | | | | 20 | $V_{CC} = MAX, V_{IN} = 2.7V$ | $\mu A$ |
| | $\overline{CP}$ | | | | 60 | | |
| | $\overline{CP}$ | | | | $-300$ | $V_{IN} = 5.5V$ $\overline{CP}$ only | $\mu A$ |
| | MR, MS | | | | 100 | $V_{CC} = MAX, V_{IN} = 7.0V$ | |
| $I_{IL}$ | Input LOW Current | | | | | | |
| | $\overline{CP}$ | | | | $-2.4$ | $V_{CC} = MAX, V_{IN} = 0.4V$ | mA |
| | MR, MS | | | | $-0.4$ | | |
| $I_{OS}$ | Output Short Circuit Current (Note 2) | | $-20$ | | $-100$ | $V_{CC} = MAX, V_{OUT} = 0V$ | mA |
| $I_{CC}$ | Power Supply Current | | | 19 | 30 | $V_{CC} = MAX$ | mA |

# AC CHARACTERISTICS: $T_A = 25°C$

| Symbol | Parameter | | Limits | | Test Conditions | | Units |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| $f_{MAX}$ | Maximum Input Count Frequency | 25 | 35 | | Fig. 1 | | MHz |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay, $\overline{CP}$ to $Q_0$ | | 12 13 | 20 20 | Fig. 1 | | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay, $\overline{CP}$ to $Q_1$ or $Q_3$ | | 24 26 | 39 39 | Fig. 3 | $V_{CC} = 5.0V$ $C_L = 15pF$ $R_L = 2$ k$\Omega$ | ns |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay, $\overline{CP}$ to $Q_2$ | | 32 36 | 54 54 | Fig. 2 | | ns |
| $t_{PHL}$ | Propagation Delay, MR to Output | | 24 | 39 | Fig. 2 | | ns |
| $t_{PLH}$ | Propagation Delay,    $Q_0, Q_3$ | | 24 | 39 | | | ns |
| $t_{PHL}$ | MS to Output    $Q_1, Q_2$ | | 20 | 36 | Fig. 2 | | |

**Notes:**
1) For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating conditions for the device type.
2) Not more than one output should be shorted at a time.
3) Typical values are at $V_{CC} = 5.0V$, $T_A = 25°C$

## AC SET-UP REQUIREMENTS: $T_A = 25°C$

| Symbol | Parameter | Limits | | | Test Conditions | | Units |
|--------|-----------|--------|--------|--------|-----------------|------|-------|
| | | Min. | Typ. | Max. | | | |
| $t_W$ | $\overline{CP}$, MR or MS Pulse Width | 20 | 14 | | Fig. 1 | $V_{CC} = 5.0V$ | ns |
| $t_{rec}$ | MR or MS to $\overline{CP}$ | 15 | 12 | | Fig. 1 | | ns |
| $t_s$ | Set-up time | 25 | 11 | | Fig. 1 | | ns |

RECOVERY TIME ($t_{rec}$) - is defined as the minimim time required between the end of the MS or MR pulse and the clock transition from HIGH to LOW in order to recognize and transfer HIGH Data to the Q outputs.

## AC WAVEFORMS



Fig. 1

Fig. 2

Fig. 3

\* The number of Clock Pulses required between the
$t_{PHL}$ and $t_{PLH}$ measurements can be determined from the Truth Table