LOW POWER SCHOTTKY INTEGRATED CIRCUITS

T54LS465
T74LS465

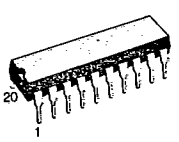
67C 16502 D T-52-09

OCTAL BUFFERS WITH 3-STATE OUTPUTS

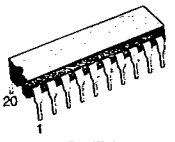
DESCRIPTION

The T54LS/T74LS465 is an Octal Buffer which utilizes the latest low-power Schottky technology. A two-input active low and enable gate controlling al eight data buffers is provided, a high level on any $\overline{G}$ places the affected outputs at high impedance.

- PNP INPUTS REDUCE BUS LOADING



B1
Plastic Package



D1/D2
Ceramic Package

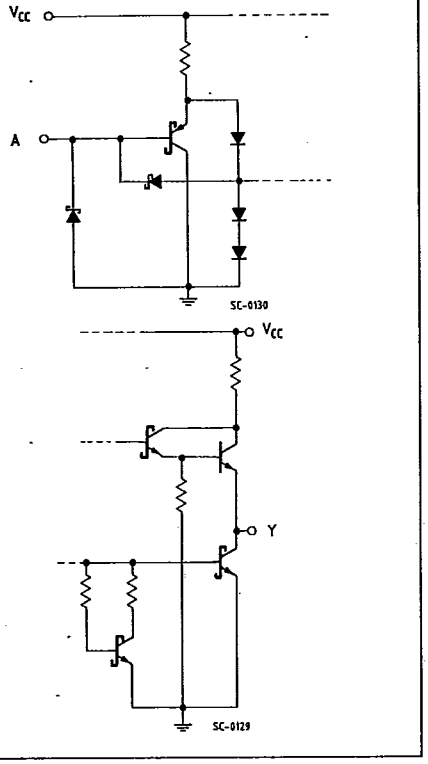
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

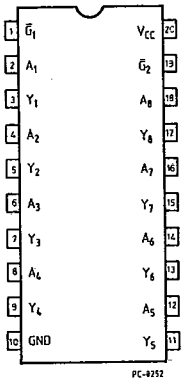
T54LS465 D2	T74LS465 C1
T74LS465 D1	T74LS465 M1
T74LS465 B1	

SCHEMATICS OF INPUT AND OUTPUT

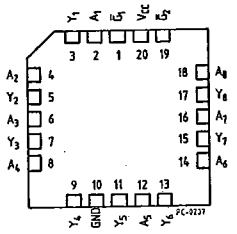


PIN CONNECTION
(top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

T54LS465
T74LS465

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	0 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS465D2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS465XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Conditions (Note 1)		Units
			Min.	Typ.	Max.			
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs		V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs		V
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA		V
V_{OH}	Output HIGH Voltage	54	2.4	3.3		I_{OH} = −1.0mA	V_{CC} = MIN, V_{IH} = 2.0V V_{IL} = V_{IL}MAX	V
		74	2.4	3.1		I_{OH} = −2.6mA		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 12mA	V_{CC} = MIN, V_{IH} = 2.0V V_{IL} = V_{IL}MAX	V
		74		0.35	0.5	I_{OL} = 24mA		
I_{OZH}	Output Off Current HIGH				20	V_{CC} = MAX, V_{OUT} = 2.4V		μA
I_{OZL}	Output Off Current LOW				−20	V_{CC} = MAX, V_{OUT} = 0.4V		μA
I_{IH}	Input HIGH Current				20 0.1	V_{CC} = MAX, V_{IN} = 2.7V V_{CC} = MAX, V_{IN} = 7.0V		μA mA
I_{IL}	Input LOW Current				−0.2	V_{CC} = MAX, V_{IN} = 0.4V		mA
I_{OS}	Output Short Circuit Current (Note 2)		−30		−130	V_{CC} = MAX		mA
I_{CC}	Power Supply Current Outputs Low Outputs High Outputs Hi-Z				 32 22 37	V_{CC} = MAX		mA

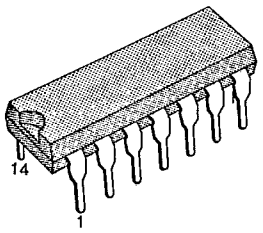
Notes:
1) For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

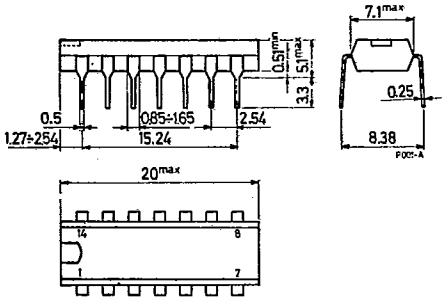
T54LS465
T74LS465

AC CHARACTERISTICS: $T_A = 25°C$

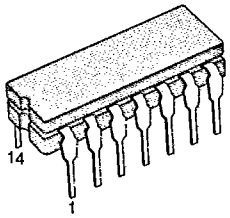
Symbol	From (Input)	To (Output)	Limits			Test Conditions	Units
			Min.	Typ.	Max.		
t_{PLH}	Ai	Yi		9	15	$C_L = 45pF$, $R_L = 667\ \Omega$	ns
t_{PHL}	Ai	Yi		12	18		ns
t_{PZH}	G	Y		25	40		ns
t_{PZL}	$\overline{G}$	Y		29	45		ns
t_{PHZ}	$\overline{G}$	Y		25	40	$C_L = 5.0pF$	ns
t_{PLZ}	$\overline{G}$	Y		30	45		ns

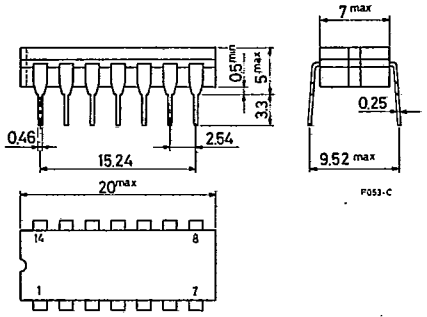
14-LEAD PLASTIC DIP



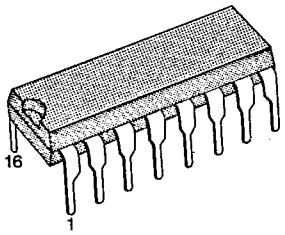


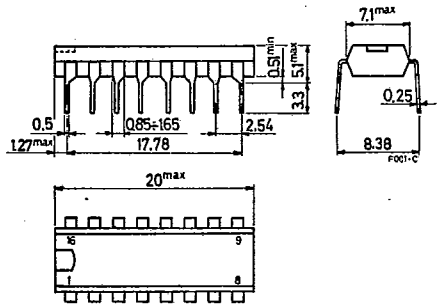
14-LEAD CERAMIC DIP





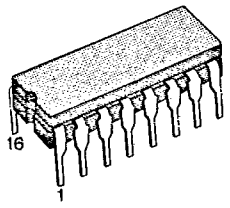
16-LEAD PLASTIC DIP

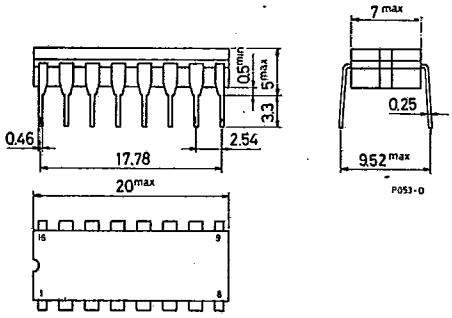




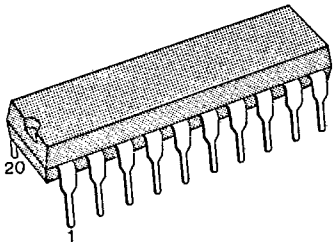
Packages

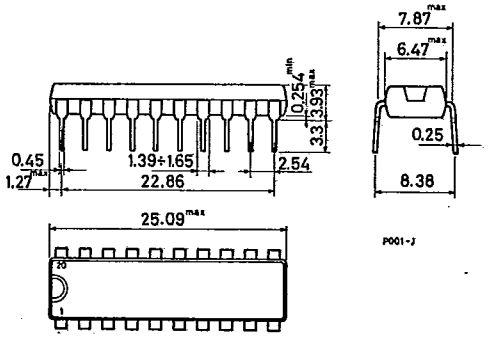
16-LEAD CERAMIC DIP



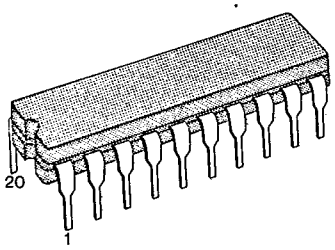


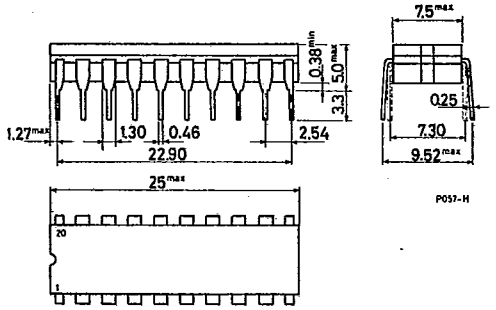
20-LEAD PLASTIC DIP





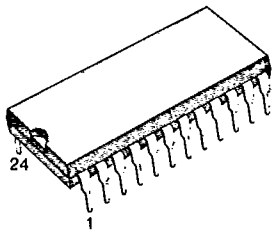
20-LEAD CERAMIC DIP

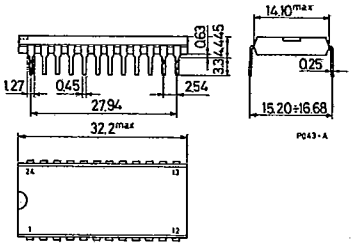




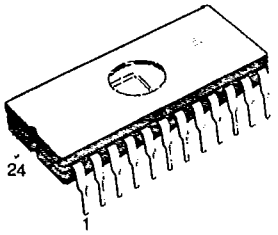
Packages

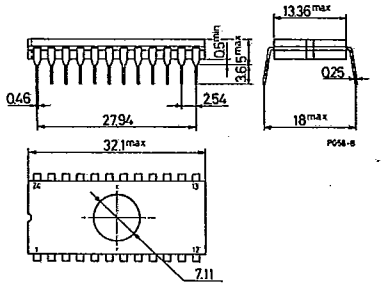
24-LEAD PLASTIC DIP



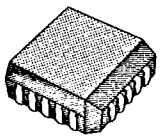


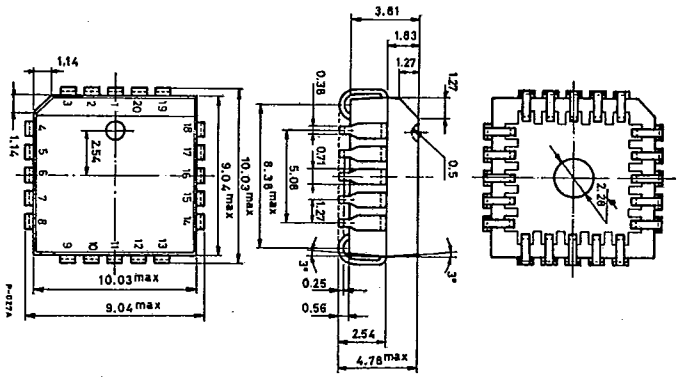
24-LEAD CERAMIC DIP





CHIP CARRIER 20 LEAD PLASTIC

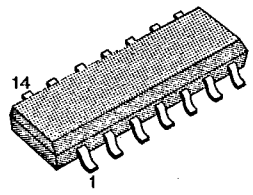


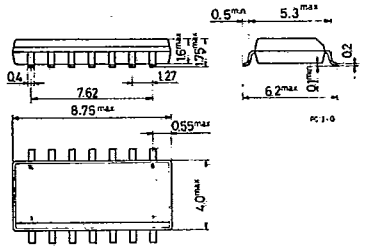


Packages

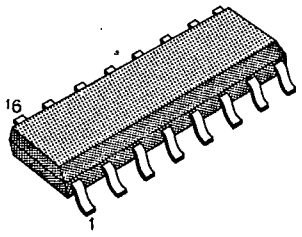
T-90-20

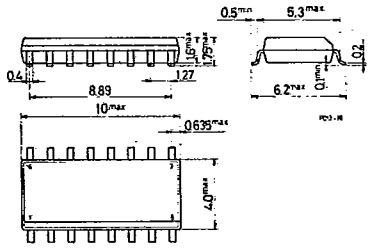
14-LEAD PLASTIC DIP MICROPACKAGE





16-LEAD PLASTIC DIP MICROPACKAGE





NOTE: FOR 20-LEAD PLASTIC DIP MICROPACKAGE CONTACT SGS

Surface Mounted

One possible solution to the important problem of PWB minimization, is that of using surface mounted components. Integrated circuits in SO (Small Outline) packages are made up of standard chips mounted in very small plastic packages.
The advantages given by using these devices are:

PWB Reduction

This is by far the most important advantage since the reduction of PWB size varies from 40 to 60% in comparison with standard board types. (See page 584 for package dimensions.)

Assembly Cost Reduction

SO Devices require no preliminary operation prior to mounting and can therefore be easily utilized in fully automatic equipment.

Increasing Reliability

The following characteristics lead to a higher level of reliability with respect to their standard packaged counter parts:

- The mounting system is fully automatic
- PWB number and the interconnections between them are reduced when the same number of devices are used.
- The high density of components on the board makes it thermally much more stable.

Noise Reduction and Improved Frequency Response

The reduction of the length of the connecting wires between the leads and the silicon guarantees a more homogeneous propogation delay between the external pins, with respect to the standard type.

Assembly Without Board Holes

The devices are placed on the board and soldered. This technology permits a higher level of tolerance in the positioning (automatic) of the device. For the standard DIP types this must be done with great accuracy due to the insertion of the leads into their holes.