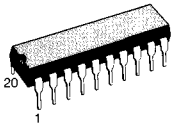
T54LS374
T74LS374

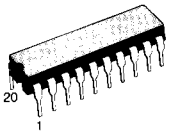
OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

DESCRIPTION

The T54LS374/T74LS374 is a high-speed, low-power Octal D-type Flip-Flop featuring separate D-type inputs for each flip-flop and 3-state outputs for oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.



B1
Plastic Package



D1/D2
Ceramic Package

M1
Micro Package

C1
Plastic Chip Carrier

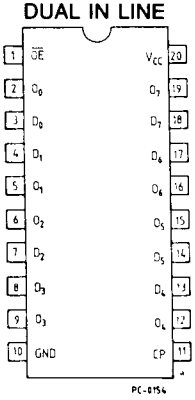
ORDERING NUMBERS:

T54LS374 D2	T74LS374 C1
T74LS374 D1	T74LS374 M1
T74LS374 B1	

- EDGE-TRIGGERED D-TYPE INPUTS
- BUFFERED POSITIVE EDGE-TRIGGERED CLOCK
- 3-STATE OUTPUTS FOR BUS ORIENTED APPLICATIONS
- HYSTERESIS ON OUTPUT ENABLE INPUT TO IMPROVE NOISE MARGIN
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

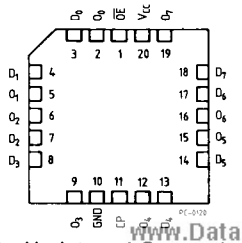
PIN CONNECTION
(top view)

DUAL IN LINE



PC-0154

CHIP CARRIER



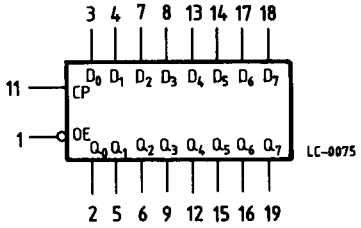
PC-0120

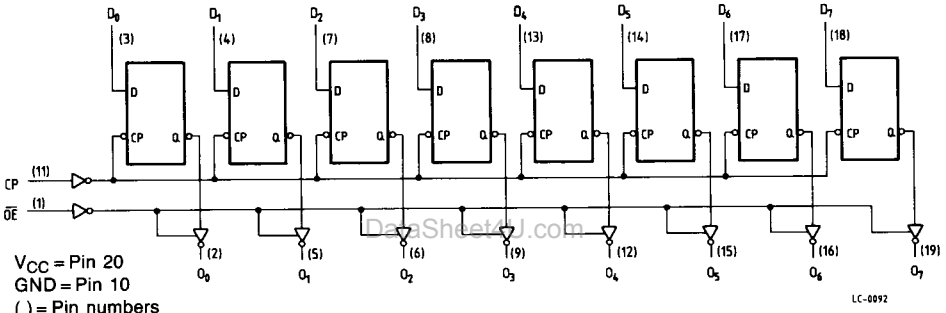
NC = No Internal Connection

PIN NAMES

D_0-D_7	Data Inputs
CP	Clock (Active HIGH Going Edge) Input
$\overline{OE}$	Output Enable (Active LOW) Input
O_0-O_7	Outputs

LOGIC SYMBOL AND LOGIC DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	−0.5 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS374D2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS374XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

TRUTH TABLE

D_n	CP	$\overline{OE}$	Q_n
H	I	L	H
L	I	L	L
X	X	H	Z*

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = HIGH Impedance

* Note: Contents of flip-flops unaffected by the state of the Output Enable input ($\overline{OE}$)

FUNCTIONAL DESCRIPTION

The LS374 consist of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The Clock and Output Enable are common. The eight flip-flops will store the state of their individual D inputs that meet the set-up and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are refected on the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits Min.	Typ.	Max.	Test Conditions (Note 1)		Units
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs		V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs		V
		74			0.8			
V_{CD}	Input Clamp Diode Voltage				−1.5	V_{CC} = MIN, I_{IN} = −18mA		V
V_{OH}	Output HIGH Voltage	54	2.4	3.4		I_{OH} = −1.0mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74	2.4	3.1		I_{OH} = −2.6mA		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 12mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74		0.35	0.5	I_{OL} = 24mA		
I_{OZH}	Output Off Current HIGH				20	V_{CC} = MAX, V_{OUT} = 2.7V, V_E = 2.0V		μA
I_{OZL}	Output Off Current LOW				−20	V_{CC} = MAX, V_{OUT} = 0.4V, V_E = 2.0V		μA
I_{IH}	Input HIGH Current				20	V_{CC} = MAX, V_{IN} = 2.7V		μA
	Input HIGH Current at MAX Input Voltage				0.1	V_{CC} = MAX, V_{IN} = 7.0V		mA
I_{IL}	Input LOW Current				−0.4	V_{CC} = MAX, V_{IN} = 0.4V		mA
I_{OS}	Output Short Circuit Current (Note 2)		−30		−130	V_{CC} = MAX, V_{OUT} = 0V		mA
I_{CC}	Power Supply Current Output Off			27	45	V_{CC} = MAX, V_{IN} = 0V, V_E = 4.5V		mA

Notes:
1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

AC CHARACTERISTICS: $T_A = 25°C$

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Propagation Delay, CP to Output		15 19	28 28	Fig. 1		ns
t_{PZH}	Output Enable Time to HIGH level		20	28	Figs. 3, 4	$C_L = 45pF$ $R_L = 667\Omega$	ns
t_{PZL}	Output Enable Time to LOW level		21	28	Figs. 2, 4		ns
t_{PLZ}	Output Disable Time from LOW level		15	25	Figs. 2, 4	$C_L = 5.0pF$ $R_L = 667\Omega$	ns
t_{PHZ}	Output Disable Time from HIGH level		12	20	Figs. 3, 4		ns
f_{MAX}	Maximum Input Frequency	35	50		Fig. 1		MHz

AC SET-UP REQUIREMENTS: $T_A = 25°C$

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
$t_W CP$	Minimum Clock Pulse Width HIGH or LOW	13	10		Fig. 1	$V_{CC} = 5.0V$	ns
t_s	Minimum Set-up Time, Data to CP	20	15				ns
t_h	Minimum Hold Time, Data to CP	0	−3				ns

DEFINITION OF TERMS:

SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) - is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

AC WAVEFORMS AND LOAD CIRCUIT

Fig. 1

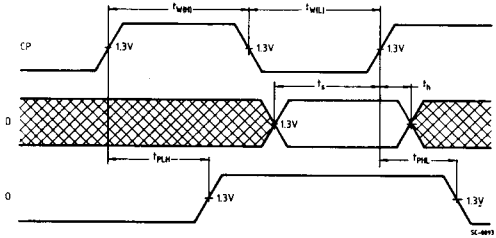


Fig. 2

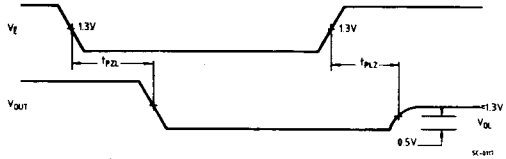
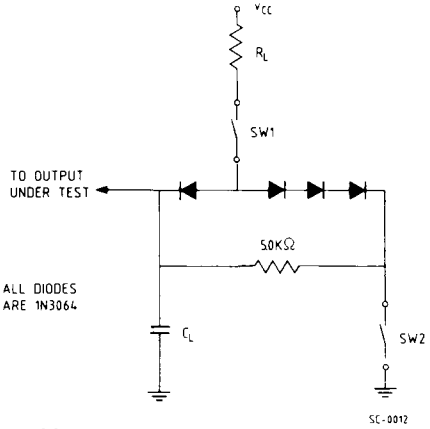


Fig. 3

Fig. 4



SWICTH POSITION

Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed