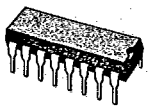
SGS-THOMSON MICROELECTRONICS

T-46-09-05

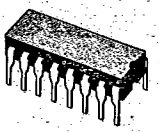
T74LS195A

UNIVERSAL 4-BIT SHIFT REGISTER

- TYPICAL SHIFT REGISTER FREQUENCY OF 40 MHz
- ASYNCHRONOUS MASTER RESET
- J, K INPUT TO FIRST STAGE
- FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

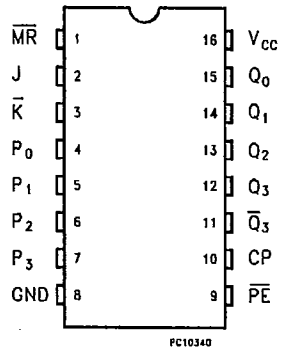
T74LS195A D1	T74LS195A C1
T74LS195A B1	T74LS195A M1

DESCRIPTION

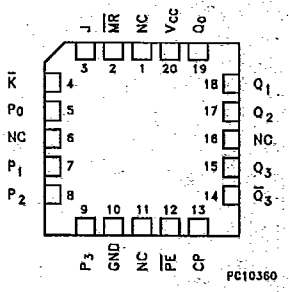
The T74LS194A is a High Speed Bidirectional Universal Shift Register. As a hgih spped multifuntional sequential bulding block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial and parallel-parallel data register transfers.

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER

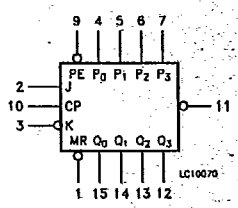


NC = No Internal Connection

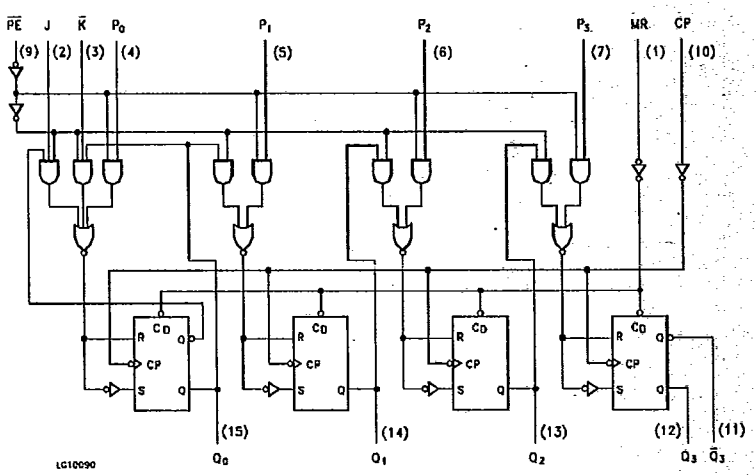
PIN NAMES

$\overline{PE}$	Parallel Enable (Active LOW) Input
P_0-P_3	Parallel Data Inputs
J	First Stage J (Active HIGH) Input
$\overline{K}$	First Stage K (Active LOW) Input
CP	Clock (Active HIGH Going Edge) Input
$\overline{MR}$	Master Reset (Active LOW) Input
Q_0-Q_3	Parallel Outputs
$\overline{Q}_3$	Complementary Last Stage Output

LOGIC SYMBOL



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

TRUTH TABLE

OPERATING	INPUTS					OUTPUTS				
	$\overline{MR}$	$\overline{PE}$	J	$\overline{K}$	P_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
Asynchronous Reset	L	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$
Shift, Reset First Stage	H	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$
Shift, Toggle First Stage	H	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
Shift, Retain First Stage	H	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
Paralled Load	H	l	X	X	p_n	p_0	p_1	p_2	p_3	$\overline{p}_3$

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
l = LOW voltage level one set-up time prior to the LOW to HIGH clock transition
h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transitio
Pn (qn) = Lower case letters indicate the state of the reference input (or output) one set-up time prior to the LOW to HIGH clock transition.

FUNCTIONAL DESCRIPTION

The Logic Diagram and Truth Table indicate the functional characteristics of the LS195A Shift register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The LS195A has not two primary modes of operation, shift right (Q_0 -> Q_1) and parallel load which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. When the PE input is HIGH, serial data enters the first flip-flop Q_0 via the J and $\overline{K}$ inputs and is shifted one bit in the direction Q_0 -> Q_1 -> Q_2 -> Q_3 following each LOW to HIGH clock transition. The J $\overline{K}$ inputs provide the flexibility of the J K type input for special applications, are the simple D type input for general applications by tying the two pins togheter. When the $\overline{PE}$ input is LOW, the LS195A appears as four common clocked D flip-flop. The data on the parallel inputs P_0, P_1, P_2, P_3 is transferred to the respective Q_0, Q_1, Q_2, Q_3 outputs to the P_{n-1} inputs and holding the $\overline{PE}$ input LOW. All serial and parallel data transfers are synchronous, occurring after each LOW to HIGH clock transition. Since the LS195A utilizes edge-triggering, there is no restriction on the activity of the J, K, P_n and $\overline{PE}$ inputs for logic operation - except for the set-up and release time requirements.

A LOW on the asynchronous Master Reser ($\overline{MR}$) input sets all Q outputs LOW, independent for any other input condition.

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	- 0.5 to 7	V
V_I	Input Voltage, Applied to Input	- 0.5 to 15	V
V_O	Output Voltage, Applied to Output	- 0.5 to 10	V
I_I	Input Current, Into Inputs	- 30 to 5	mA
I_O	Output Current, Into Outputs	30	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS195AXX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Input		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Input		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 12 mA	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 24 mA		V
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current		14	21	V_{CC} = MAX		mA

Notes : 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
f_{MAX}	Shift Frequency	30	40		Figures 1	V_{CC} = 5.0 V C_L = 15 pF	MHz
t_{PLH} t_{PHL}	Propagation Delay, Clock to Outputs		14 17	22 26	Figures 1		ns
t_{PHL}	Propagation Delay, $\overline{MR}$ to Outputs		19	30	Figures 3		ns

AC SET-UP REQUIREMENTS: T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_WCP	Clock Pulse Width	16	17		Figure 1	V_{CC} = 5.0 V C_L = 15 pF	ns
t_s(Data)	Set-Up Time Data to Clock	15	11		Figure 2		ns
t_h(Data)	Hold Time Data to Clock	0					ns
t_s(S)	Set-Up Time $\overline{PE}$ Control to Clock	25	18		Figure 4		ns
t_h(S)	Hold Time $\overline{PE}$ Control to Clock	0					ns
$t_W(\overline{MR})$	Master Reset Pulse Width	12	8		Figure 3		ns
$t_{rec}(\overline{MR})$	Recovery Time Mater Reset to Clock	25	6				ns
$t_{release}$	$\overline{PE}$			10			ns

DEFINITION OF TERMS:

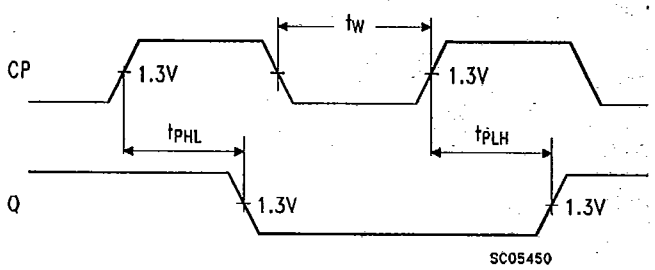
SET-UP TIME (t_s): is defined as the minimum time required for the corret logic level to be present at the logic input prior the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h): is defined as the minimum time following the clock transition from LOW to HIGH at which the logiclevel must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be relased prior to the clock transitio from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) : is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

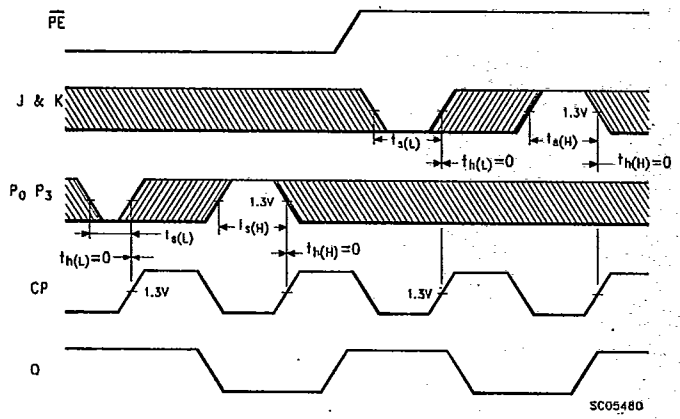
AC WAVEFORMS

Figure 1: Clock to Output Delays and Clock Pulse Width



Conditions: J = $\overline{PE}$ = $\overline{MR}$ = H = $\overline{K}$ = L

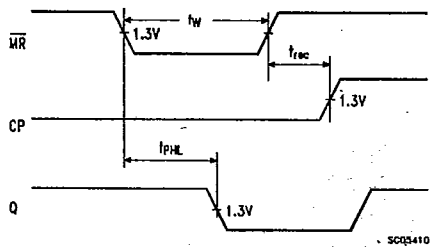
Figure 2: Set-up (ts) and Hold (th) Time for Serial Data (J & K) and Parallel Data (P_0, P_1, P_2, P_3)



Conditions: $\overline{MR}$ = H, J and K set-up time affects Q_0 only

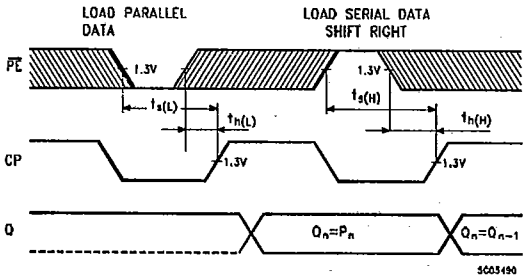
The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 3: Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Other Conditions: $\overline{PE}$ = L, $P_0 = P_1 = P_2 = P_3$ = H

Figure 4: Set-up (t_s) and Hold (t_h) Time for $\overline{PE}$ Input



Conditions: MR = H, Q_0 state will be determined by J and $\overline{K}$ input

The shaded areas indicate when the input is permitted to change for predictable output performance.