

T6A92

COLUMN DRIVER LSI FOR A DOT MATRIX LCD

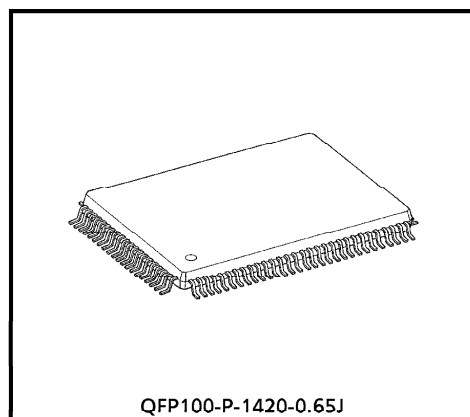
The T6A92 is a column driver with 80 output channels for a medium- or small-scale dot matrix LCD.

The T6A92 realizes low power LCD systems using the CMOS Si-Gate process.

The T6A92 has two types of data flow.

① $O_1 \rightarrow O_{80}$, ② $O_{80} \rightarrow O_1$

The T6A92 can be connected to extension drivers like the T6A39.



Weight: 1.6g (typ.)

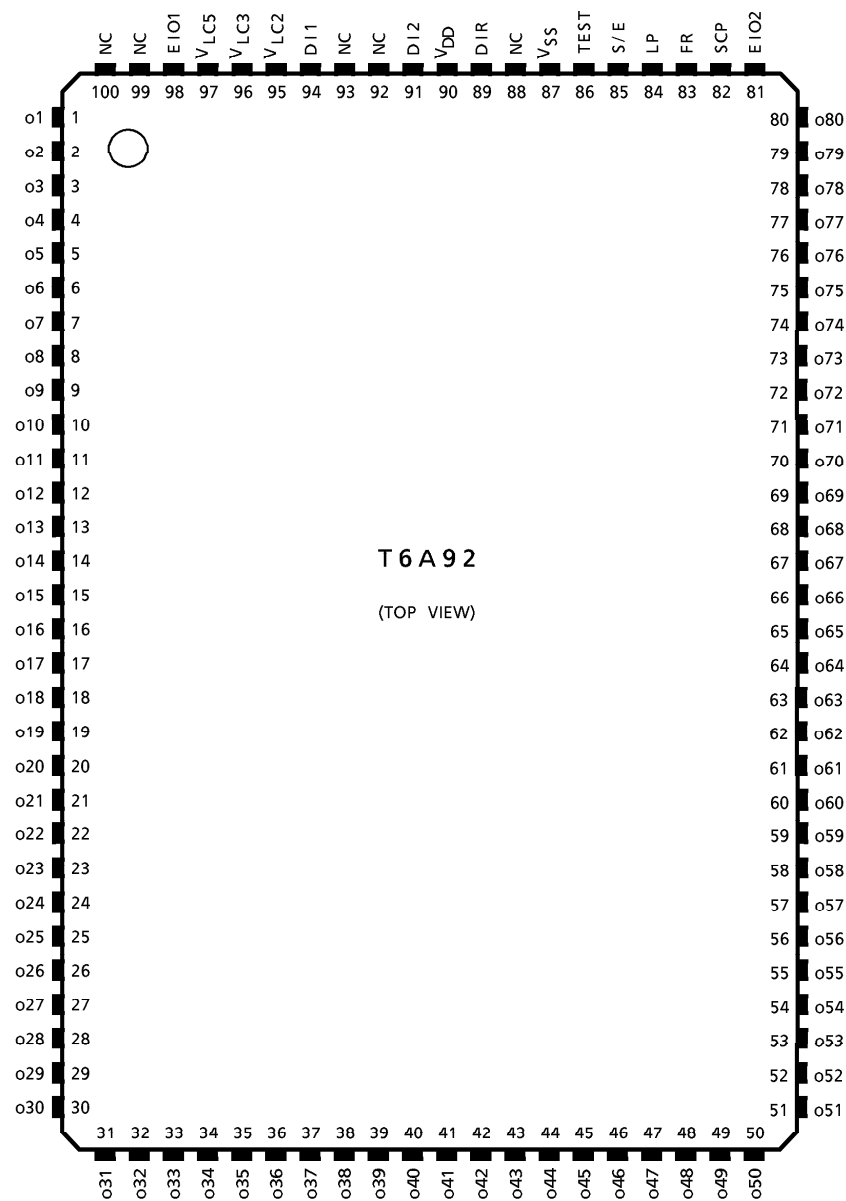
FEATURES

- 80-output column driver
- Data input format : 1-bit (ENABLE mode)
: 2-bit (SHIFT mode)
- Two types of data flow :
 - ① $O_1 \rightarrow O_{80}$
 - ② $O_{80} \rightarrow O_1$
- Low power consumption
- Power supply : $5\text{ V} \pm 10\%$
- 100-pin plastic flat package

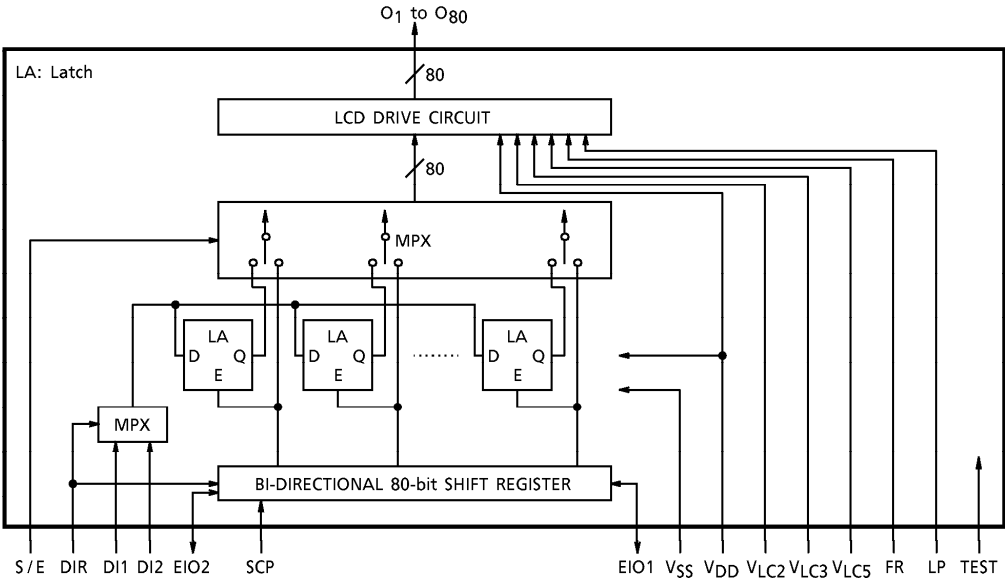
961001EBA2

- TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
- The products described in this document are subject to foreign exchange and foreign trade control laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

PIN ASSIGNMENT



BLOCK DIAGRAM



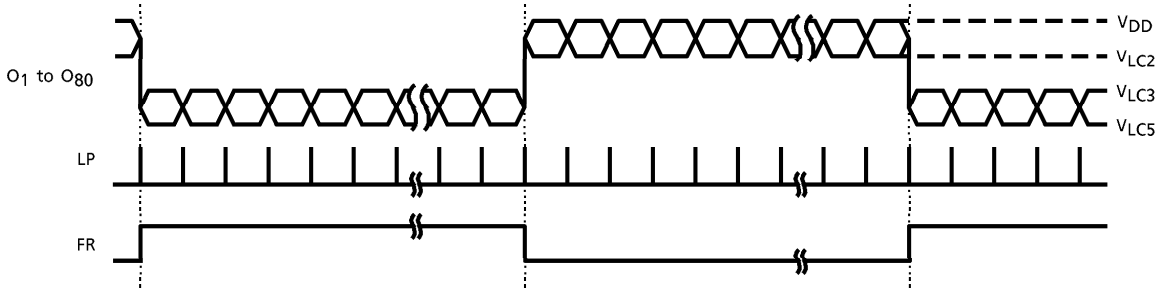
PIN FUNCTIONS

PIN NAME	I/O	FUNCTIONS	LEVEL
O1 to O80	Output	LCD drive signal output	V_{DD} to V_{LC5}
DI1, DI2	Input	Data signal input	V_{DD} to V_{SS}
EIO1, EIO2	I/O	ENABLE signal input/output When $S/E = H$, this pin is for input.	
SCP	Input	(Shift Clock Pulse) Shift clock pulse input	
FR	Input	(Frame) Frame signal input	
LP	Input	(Latch Pulse) Latch pulse signal input	
S/E	Input	Input for mode selection	
DIR	Input	Input data flow direction select	
TEST	Input	Test pin: usually connected to V_{SS} (0V)	
$V_{LC2, 3, 5}$	—	Power supply for LCD drive	—
V_{DD}	—	Power supply (5V)	
V_{SS}	—	Power supply (0V)	

FUNCTION OF DATA AND ENABLE PINS

S / E DIR		DI1	DI2	EIO1	EIO2	DATA FLOW	FIRST DATA	LAST DATA	MODE
L	L	Open	DATA INPUT	ENABLE signal input	ENABLE signal output	O ₈₀ →O ₁	O ₁	O ₈₀	ENABLE
L	H	DATA INPUT	Open	ENABLE signal output	ENABLE signal input	O ₁ →O ₈₀	O ₈₀	O ₁	
H	L	Open	Open	DATA INPUT	DATA OUTPUT	O ₁ →O ₈₀	O ₈₀	O ₁	SHIFT
H	H	Open	Open	DATA OUTPUT	DATA INPUT	O ₈₀ →O ₁	O ₁	O ₈₀	

TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

ITEM	SYMBOL	RATING	UNIT
Supply Voltage (1)	V _{DD} (Note 1)	- 0.3 to 7.0	V
Supply Voltage (2)	V _{LC2} , V _{LC3} , V _{LC5} (Note 1, 2)	- 0.3 to 7.0	V
Input Voltage	V _{IN} (Note 1)	- 0.3 to V _{DD} + 0.3	V
Operating Temperature	T _{opr}	- 20 to 75	°C
Storage Temperature	T _{stg}	- 55 to 125	°C

- (Note 1) Referenced to V_{SS} = 0V
(Note 2) Ensure that the following condition is always maintained.
 $V_{DD} \geq V_{LC2} \geq V_{LC3} \geq V_{LC5}$

ELECTRICAL CHARACTERISTICS

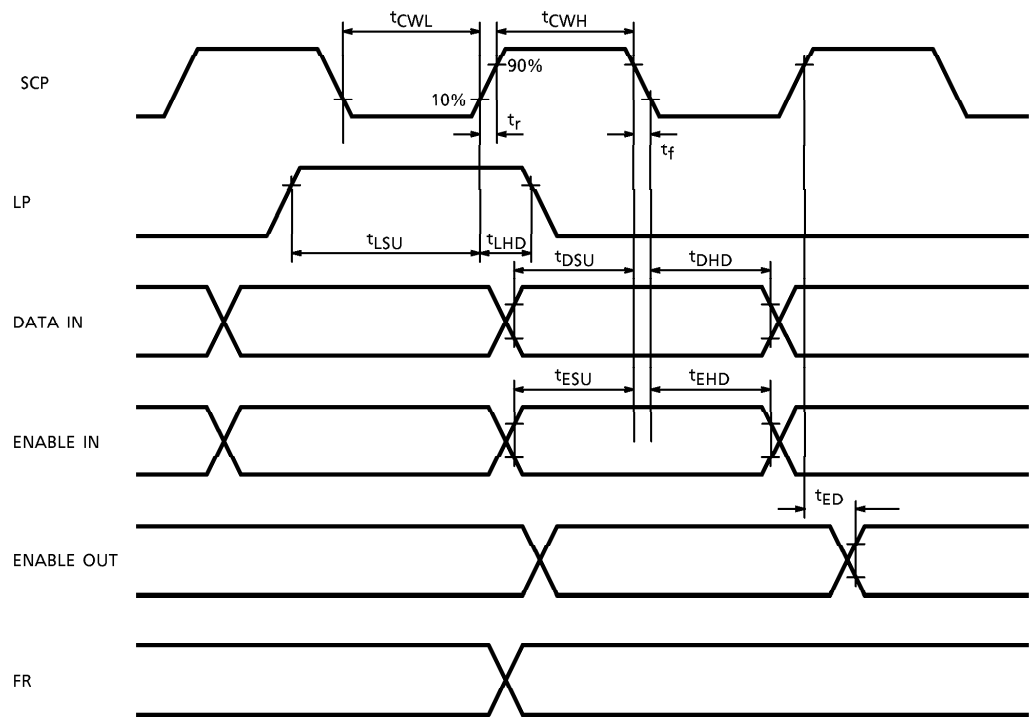
DC CHARACTERISTICS

TEST CONDITIONS (Unless otherwise noted, $V_{SS} = 0V$, $V_{DD} = 5.0V \pm 10\%$, $V_{LC5} = 0V$, $T_a = -20$ to $75^\circ C$)

ITEM		SYMBOL	TEST CIR- CUIT	TEST CONDITIONS	MIN	TYP.	MAX	UNIT	PIN NAME	
Operating Voltage (1)		—	—	—	4.5	5.0	5.5	V	V _{DD}	
Operating Voltage (2)		—	—	—	0	—	V _{DD} - 3.0	V	V _{LC5}	
Input Voltage	H Level	V _{IH}	—	—	V _{DD} - 1.0	—	V _{DD}	V	(*)	
	L Level	V _{IL}	—	—	0	—	1.0	V	(*)	
Output Voltage	H Level	V _{OH}	—	I _{OH} = - 0.4mA	V _{DD} - 0.4	—	V _{DD}	V	EIO1, EIO2	
	L Level	V _{OL}	—	I _{OH} = 0.4mA	0	—	0.4	V	EIO1, EIO2	
Output Resistance		R _{COL}	—	I _d = ± 50μA	—	—	30	kΩ	O ₁ to O ₈₀	
Operating Frequency		f _{scp}	—	Ta = - 20 to 75°C	—	—	400	kHz	SCP	
Current Consumption		I _{SS}	—	V _{DD} = 5.0V V _{LC2} = 3.0V V _{LC3} = 2.0V V _{LC5} = 0.0V f _{FR} = 39Hz f _{scp} = 250kHz O ₁ to O ₈₀ : No Load	Binary Data Input	—	—	1.0	mA	V _{SS}
				Input Data : LOW Constant	—	—	0.4	mA		

(*) SCP, LP, FR, EIO1, EIO2, DI1, DI2, DIR, S/E, TEST

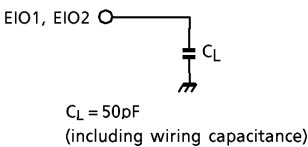
AC CHARACTERISTICS



TEST CONDITIONS ($V_{SS} = 0V$, $V_{DD} = 5V \pm 10\%$, $V_{LC5} = 0V$, $T_a = -20$ to $75^\circ C$)

ITEM	SYMBOL	MIN	MAX	UNIT
Operating Frequency	f_{scp}	—	400	kHz
SCP Pulse Width	t_{CWH} , t_{CWL}	800	—	ns
SCP Rise / Fall Time	t_r , t_f	—	200	ns
LP Set-up Time	t_{LSU}	500	—	ns
LP Hold Time	t_{LHD}	—	10	ns
Data Set-up Time	t_{DSU} (Note 1)	300	—	ns
Data Hold Time	t_{DHD} (Note 1)	300	—	ns
Enable Set-up Time	t_{ESU} (Note 2)	300	—	ns
Enable Hold Time	t_{EHD} (Note 2)	300	—	ns
Enable Delay Time	t_{ED} (Note 3)	—	500	ns

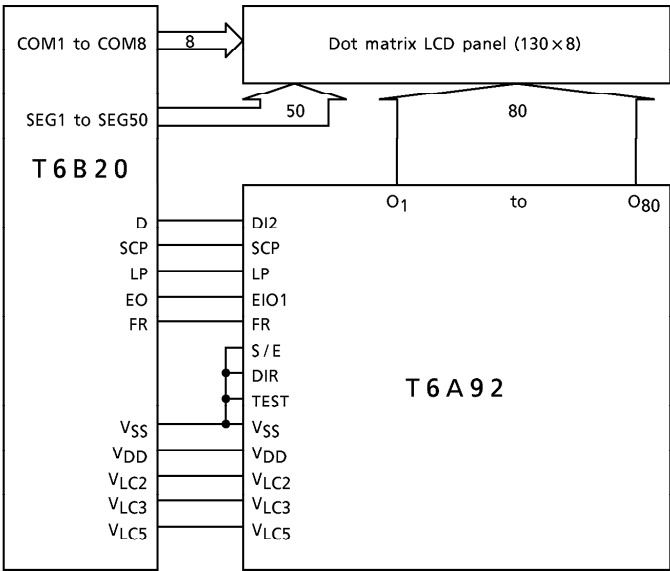
LOAD CIRCUIT



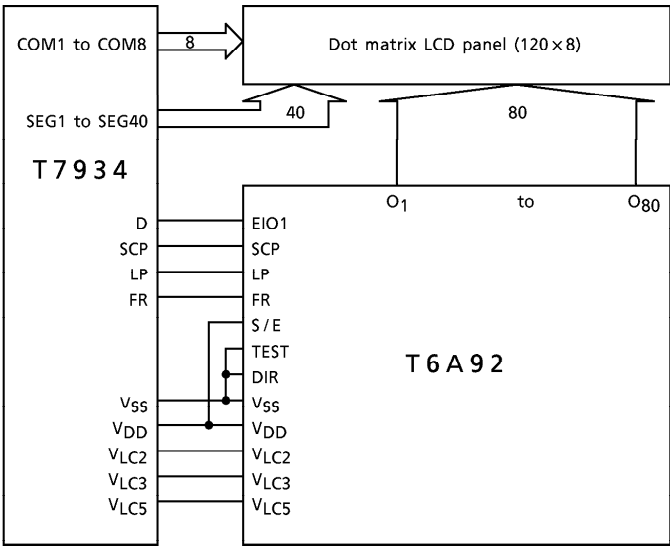
- (Note 1) Applies to DI1 and DI2
- (Note 2) Applies to EIO1 and EIO2
- (Note 3) With load circuit connected

APPLICATION CIRCUIT

- S/E = L (ENABLE mode)

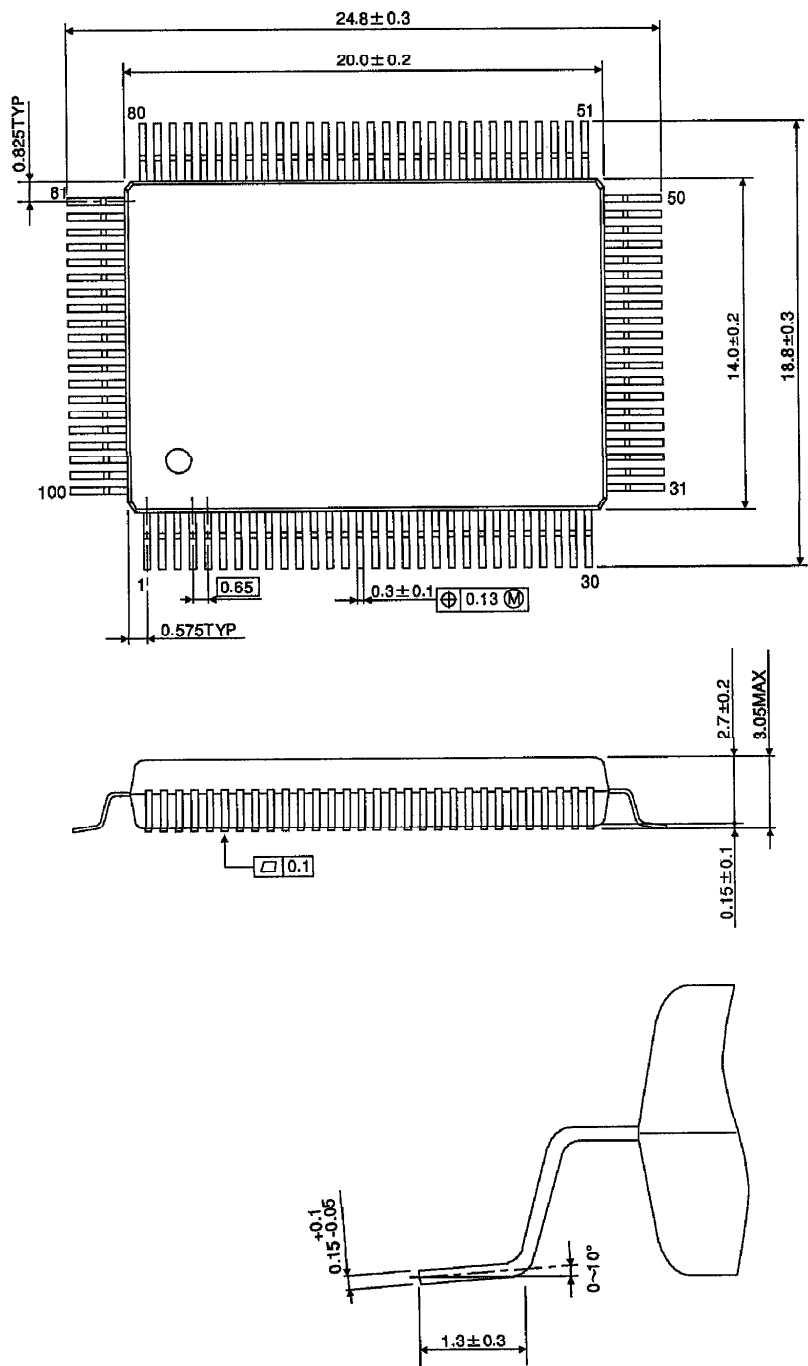


- S/E = H (SHIFT mode)



OUTLINE DRAWING
QFP100-P-1420-0.65J

Unit : mm



Weight : 1.6g (Typ.)