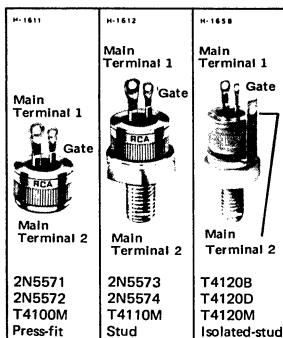


RCA
Solid State
Division

Thyristors

2N5571 - 2N5574

T4100 T4110 T4120 Series



15-A Silicon Triacs

Features:

- di/dt Capability = 150 A/ μ s
- Shorted-Emitter Center-Gate Design
- Low Switching Losses
- Low On-State Voltage at High Current Levels
- Low Thermal Resistance

Voltage Package	200 V	400 V	600 V
	Types	Types	Types
Press-Fit (T4100 Series)	2N5571	2N5572	T4100M (40797)
Stud (T4110 Series)	2N5573	2N5574	T4110M (40798)
Isolated-Stud (T4120 Series)	T4120B (40802)	T4120D (40803)	T4120M (40804)

Numbers in parentheses (e.g. 40802) are former RCA type numbers.

These RCA triacs are gate-controlled, full-wave silicon ac switches. They are designed to switch from an off-state to an on-state for either polarity of applied voltage with positive or negative gate triggering voltages.

These triacs are intended for control of ac loads in applications such as heating controls, motor controls, arc-welding equipment, light dimmers, and power switching systems.

MAXIMUM RATINGS, Absolute-Maximum Values:

For Operation with Sinusoidal Supply Voltage at Frequencies up to 50/60 Hz and with Resistive or Inductive Load.

*REPETITIVE PEAK OFF-STATE VOLTAGE:

Gate open, $T_J = -65$ to 100°C

*RMS ON-STATE CURRENT (Conduction angle = 360°):

Case temperature

$T_C = 80^\circ\text{C}$ (Press-fit & stud types)

$= 75^\circ\text{C}$ (Isolated-stud types)

For other conditions

PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT:

For one cycle of applied principal voltage, T_C as above

* 60 Hz (sinusoidal)

50 Hz (sinusoidal)

For more than one cycle of applied principal voltage

RATE-OF-CHANGE OF ON-STATE CURRENT:

$V_{DM} = V_{DROM}$, $I_{GT} = 160\text{ mA}$, $t_r = 0.1\ \mu\text{s}$ (See Fig. 13)

FUSING CURRENT (for Triac Protection):

$T_J = -65$ to 100°C , $t = 1.25$ to 10 ms

PEAK GATE-TRIGGER CURRENT:

For $1\ \mu\text{s}$ max., See Fig. 7

*GATE POWER DISSIPATION:

PEAK (For $1\ \mu\text{s}$ max., $I_{GTM} \leq 4\text{ A}$, See Fig. 7)

AVERAGE

*TEMPERATURE RANGE:

Storage

Operating (Case)

*TERMINAL TEMPERATURE (During soldering):

For 10 s max. (terminals and case)

STUD TORQUE:

Recommended

Maximum (DO NOT EXCEED)

* In accordance with JEDEC registration data format (JIS-14, RDF 2) filed for the JEDEC (2N-Series) types.

● For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.

■ For either polarity of gate voltage (V_G) with reference to main terminal 1.

▲ For temperature measurement reference point, see Dimensional Outline.

2N5571	2N5572	T4100M
2N5573	2N5574	T4110M
T4120B	T4120D	T4120M

V_{DROM}	200	400	600	V
$I_T(\text{RMS})$	_____	_____	_____	A
	_____	_____	_____	A
	_____	_____	_____	See Fig. 3
I_{TSM}	_____	_____	_____	A
	_____	_____	_____	A
	_____	_____	_____	See Fig. 4
di/dt	_____	150	_____	A/ μs
I^2_t	_____	50	_____	A ² s
I_{GTM}	_____	4	_____	A
P_{GM}	_____	16	_____	W
$P_G(\text{AV})$	_____	0.5	_____	W
T_{stg}	_____	-65 to 150	_____	$^\circ\text{C}$
T_C	_____	-65 to 100	_____	$^\circ\text{C}$
T_T	_____	225	_____	$^\circ\text{C}$
τ_s	_____	35	_____	in-lb
	_____	50	_____	in-lb

ELECTRICAL CHARACTERISTICS

At Maximum Ratings and at Indicated Case Temperature (T_C) Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	LIMITS			UNITS
		Min.	Typ.	Max.	
Peak Off-State Current: Gate open, $T_J = 100^\circ\text{C}$, $V_{DROM} = \text{Max. rated value}$	I_{DROM}	—	0.2	2*	mA
Maximum On-State Voltage: For $i_T = 21\text{ A (peak)}$, $T_C = 25^\circ\text{C}$	V_{TM}	—	1.4	1.8*	V
DC Holding Current: Gate open, Initial principal current = 500 mA (DC), $v_D = 12\text{V}$: $T_C = 25^\circ\text{C}$ $T_C = -65^\circ\text{C}$ For other case temperatures	I_{HO}	— —	20 75	75 300*	mA
			See Fig. 6		
Critical Rate-of-Rise of Commutation Voltage: For $v_D = V_{DROM}$, $I_T(\text{RMS}) = 15\text{ A}$, commutating $di/dt = 8\text{ A/ms}$, gate unenergized, (See Fig. 14): $T_C = 80^\circ\text{C}$ (Press-fit & stud types) $= 75^\circ\text{C}$ (Isolated-stud)	dv/dt	2* 2	10 10	— —	V/ μs
Critical Rate-of-Rise of Off-State Voltage: For $v_D = V_{DROM}$, exponential voltage rise, gate open, $T_C = 100^\circ\text{C}$: 2N5571, 2N5573, T4120B 2N5572, 2N5574, T4120D T4100M, T4110M, T4120M	dv/dt	30* 20* 10	150 100 75	— — —	V/ μs
DC Gate-Trigger Current: ♦♦ Mode V_{MT2} V_G For $v_D = 12\text{ V (DC)}$, I^+ positive positive $R_L = 30\ \Omega$, III^- negative negative $T_C = 25^\circ\text{C}$ I^- positive negative III^+ negative positive	I_{GT}	— — — —	20 20 35 35	50 50 80 80	mA
Mode V_{MT2} V_G For $v_D = 12\text{ V (DC)}$, I^+ positive positive $R_L = 30\ \Omega$, III^- negative negative $T_C = -65^\circ\text{C}$ I^- positive negative III^+ negative positive		— — — —	75 75 100 100	150* 150* 200* 200*	
For other case temperatures			See Figs. 8 & 9		
DC Gate-Trigger Voltage: ♦♦ For $v_D = 12\text{ V(DC)}$, $R_L = 30\ \Omega$, $T_C = 25^\circ\text{C}$ $T_C = -65^\circ\text{C}$ For other case temperatures	V_{GT}	— — 0.2	1 2 See Fig. 10 —	2.5 4* —	V
For $v_D = V_{DROM}$, $R_L = 125\ \Omega$, $T_C = 100^\circ\text{C}$					
Gate-Controlled Turn-On Time: (Delay Time + Rise Time) For $v_D = V_{DROM}$, $I_{GT} = 160\text{ mA}$, $t_r = 0.1\ \mu\text{s}$, $i_T = 25\text{ A (peak)}$, $T_C = 25^\circ\text{C}$ (See Figs. 11 & 15)	t_{gt}	—	1.6	2.5	μs
Thermal Resistance: Junction-to-Case: Steady-State Transient	$R_{\theta JC}$	—	—	1*	$^\circ\text{C/W}$
			See Fig. 12		
Junction-to-Isolated Hex (Stud, see Dim. Outline): Steady-State	$R_{\theta JH}$	—	—	1.1	

* In accordance with JEDEC registration data format (JS-14, RDF 2) filed for the JEDEC (2N-Series) types.

⚡ For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.

◆ For either polarity of gate voltage (V_G) with reference to main terminal 1.

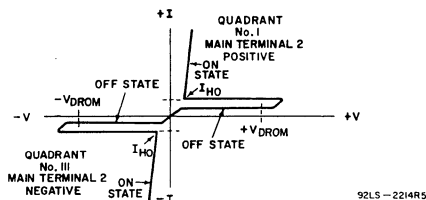


Fig. 1 - Principal voltage-current characteristic.

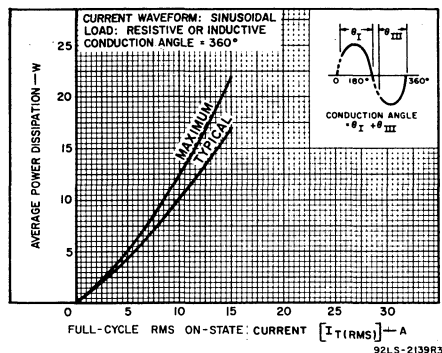


Fig. 2 - Power dissipation vs. on-state current.

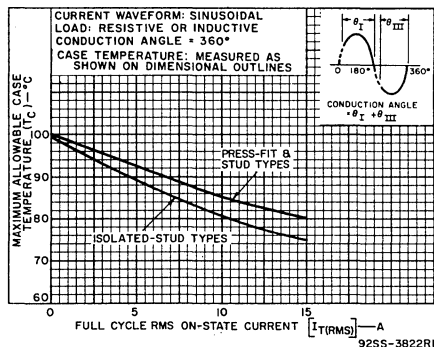


Fig. 3 - Maximum allowable case temperature vs. on-state current.

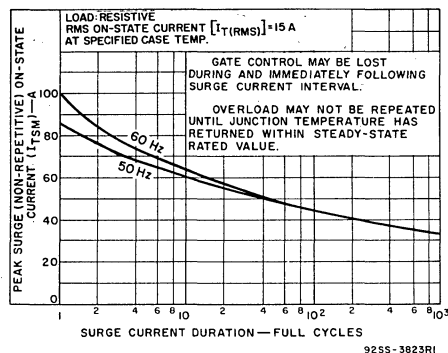


Fig. 4 - Peak surge on-state current vs. surge current duration.

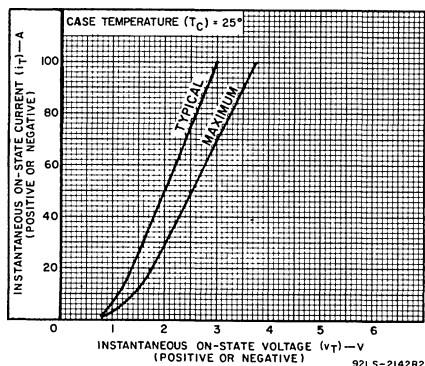


Fig. 5 - On-state current vs. on-state voltage.

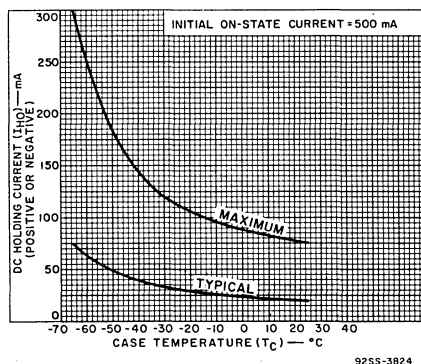


Fig. 6 - DC holding current vs. case temperature.

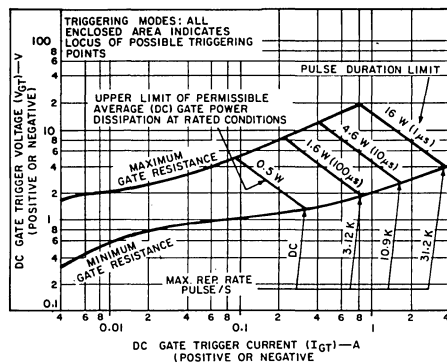


Fig. 7 - Gate trigger characteristics and limiting conditions for determination of permissible gate trigger pulses.

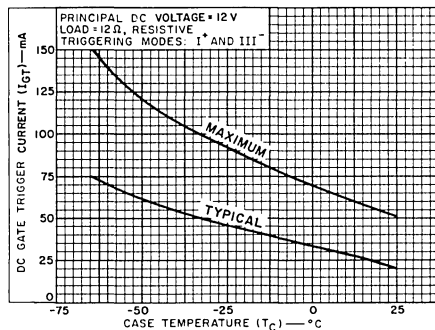


Fig. 8 - DC gate-trigger current vs. case temperature (I* and III* modes).

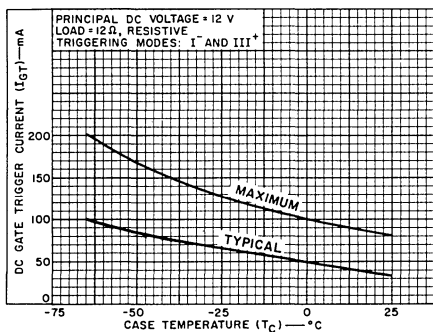


Fig. 9 - DC gate-trigger current vs. case temperature (I* and III* modes).

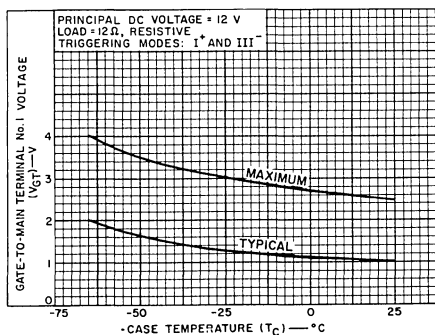


Fig. 10 - DC gate-trigger voltage vs. case temperature.

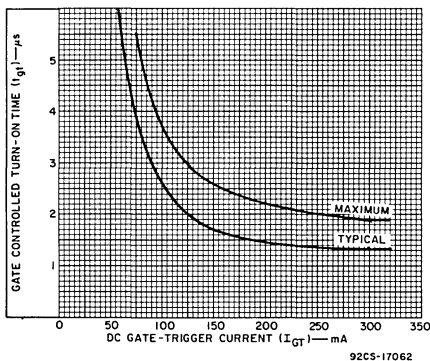


Fig. 11 - Turn-on time vs. gate trigger current.

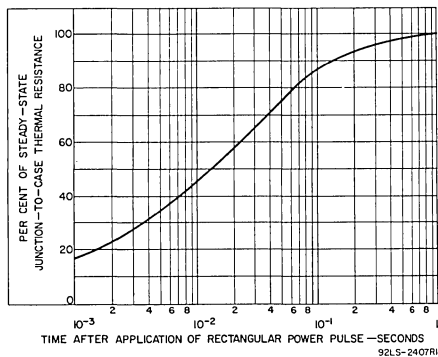


Fig. 12 - Transient junction-to-case thermal resistance vs. time.

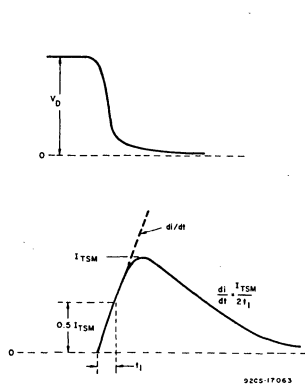


Fig. 13—Rate-of-change of on-state current with time (defining di/dt).

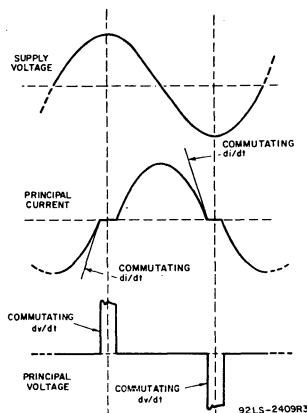


Fig. 14—Relationship between supply voltage and principal current (inductive load) showing reference points for definition of commutating voltage (dv/dt).

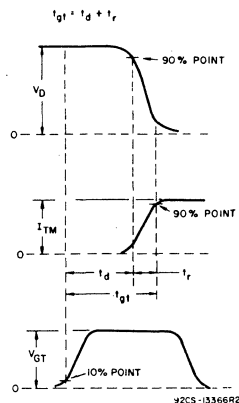


Fig. 15—Relationship between off-state voltage, on-state current, and gate-trigger voltage showing reference points for definition of turn-on time (t_{gt}).

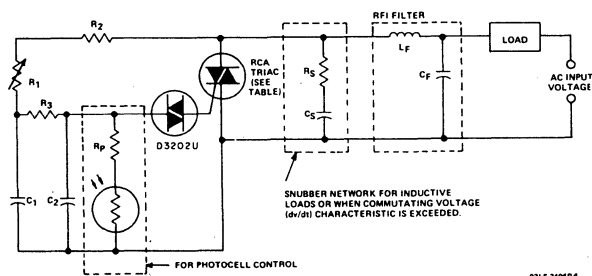


Fig. 16—Typical phase-control circuit for lamp dimming, heat control, and universal-motor speed control.

AC INPUT VOLTAGE		120V 60Hz	240V 50Hz	240V 50Hz
C ₁	C ₁	0.1μF 400V	0.1μF 400V	0.1μF 400V
	C ₂	0.1μF 100V	0.1μF 100V	0.1μF 400V
R ₁	R ₁	100kΩ 1/2W	20kΩ 1/2W	250kΩ 1W
	R ₂	2.2kΩ 1/2W	3.3kΩ 1/2W	3.3kΩ 1/2W
R ₃	R ₃	15kΩ 1/2W	15kΩ 1/2W	15kΩ 1/2W
	R _p	1.2kΩ 2W	1.2kΩ 2W	1.2kΩ 2W
PHOTOCELL CONTROL	C _s	0.1μF 200V	0.1μF 400V	0.1μF 400V
	R _s	100Ω 1/2W	100Ω 1/2W	100Ω 1/2W
SNUBBER NETWORK	C _F	0.1μF 200V	0.1μF 400V	0.1μF 400V
	L _F	100μH	200μH	200μH
RFI FILTER	C _F	0.1μF 200V	0.1μF 400V	0.1μF 400V
	L _F	100μH	200μH	200μH
RCA TRIACS		2N5567 2N5568 T4120B	2N5568 2N5570 T4120D	2N5568 2N5570 T4120D

*Typical values for lamp dimming circuits.

WARNING:

The RCA isolated-stud package thyristors should be handled with care. The ceramic portion of these thyristors contains BERYLLIUM OXIDE as a major ingredient. Do not crush, grind, or abrade these portions of the thyristors because the dust resulting from such action may be hazardous if inhaled.

TERMINAL CONNECTIONS

No.1—Gate
No.2—Main Terminal 1
No.3—Main Terminal 2