SYNCHRONOUS BURST SRAM

32K x 32 SRAM

Pipeline and Flow-Through Burst Mode

FEATURES

- ßb $\overline{FT}$ pin for user configurable pipeline or flow-through operation.
- ßb= Fast Access times:
  - Pipeline – 3.8 / 4 / 4.5 ns
  - Flow-through – 9 / 10 / 11ns
- ßbSingle 3.3V +0.3V/-0.165V power supply
- ßbCommon data inputs and data outputs
- ßbIndividual BYTE WRITE ENABLE and GLOBAL WRITE control
- ßb=Three chip enables for depth expansion and address pipelining
- ßb€lock-controlled and registered address, data I/Os and control signals
- ßbInternally self-timed WRITE CYCLE
- ßbBurst control pins (interleaved or linear burst sequence)
- ßbHigh 30pF output drive capability at rated access time
- ßbSNOOZE MODE for reduced power standby
- ßb=Burst Sequence :
  - Interleaved (MODE=NC or VCC)

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OPTIONS

MARKING		-3.8	-4	-4.5
Pipeline 3-1-1-1	Access time	3.8ns	4ns	4.5ns
	Cycle time	6.6ns	7.5ns	8.5ns
Flow-through 2-1-1-1	Access time	9ns	10ns	11ns
	Cycle time	10.5ns	15ns	15ns

Package

100-pin QFP	Q
100-pin TQFP	T

Part Number Examples

PART NO.	Pkg.
T35L3232B-3.8Q	Q
T35L3232B-4T	T

GENERAL DESCRIPTION

The Taiwan Memory Technology Synchronous Burst RAM family employs high-speed, low power CMOS design using advanced triple-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high valued resistors.

The T35L3232B SRAM integrates 32,768 x 32 bits SRAM cells with advanced synchronous peripheral circuitry and a 2-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining chip enable ($\overline{CE}$), depth-expansion chip enables ($\overline{CE2}$ and CE2), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), write enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$, and $\overline{BWE}$), and global write ($\overline{GW}$).

Asynchronous inputs include the output enable ($\overline{OE}$), Snooze enable (ZZ) and burst mode control (MODE). The data outputs (Q), enabled by $\overline{OE}$, are also asynchronous.

Addresses and chip enables are registered with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$).

Address and write controls are registered on-chip to initiate self-timed WRITE cycle. WRITE cycles can be one to four bytes wide as controlled by the write control inputs. Individual byte write allows individual byte to be written. $\overline{BW1}$ controls DQ1-DQ8. $\overline{BW2}$ controls DQ9-DQ16. $\overline{BW3}$ controls DQ17-DQ 24. $\overline{BW4}$ controls DQ25-DQ32. $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, and $\overline{BW4}$ can be active only with $\overline{BWE}$ being LOW. $\overline{GW}$ being LOW causes all bytes to be written. WRITE pass-through capability allows written data available at the output for the immediately next READ cycle. This device also incorporates pipelined enable circuit for easy depth expansion without penalizing system performance.

FUNCTIONAL BLOCK DIAGRAM

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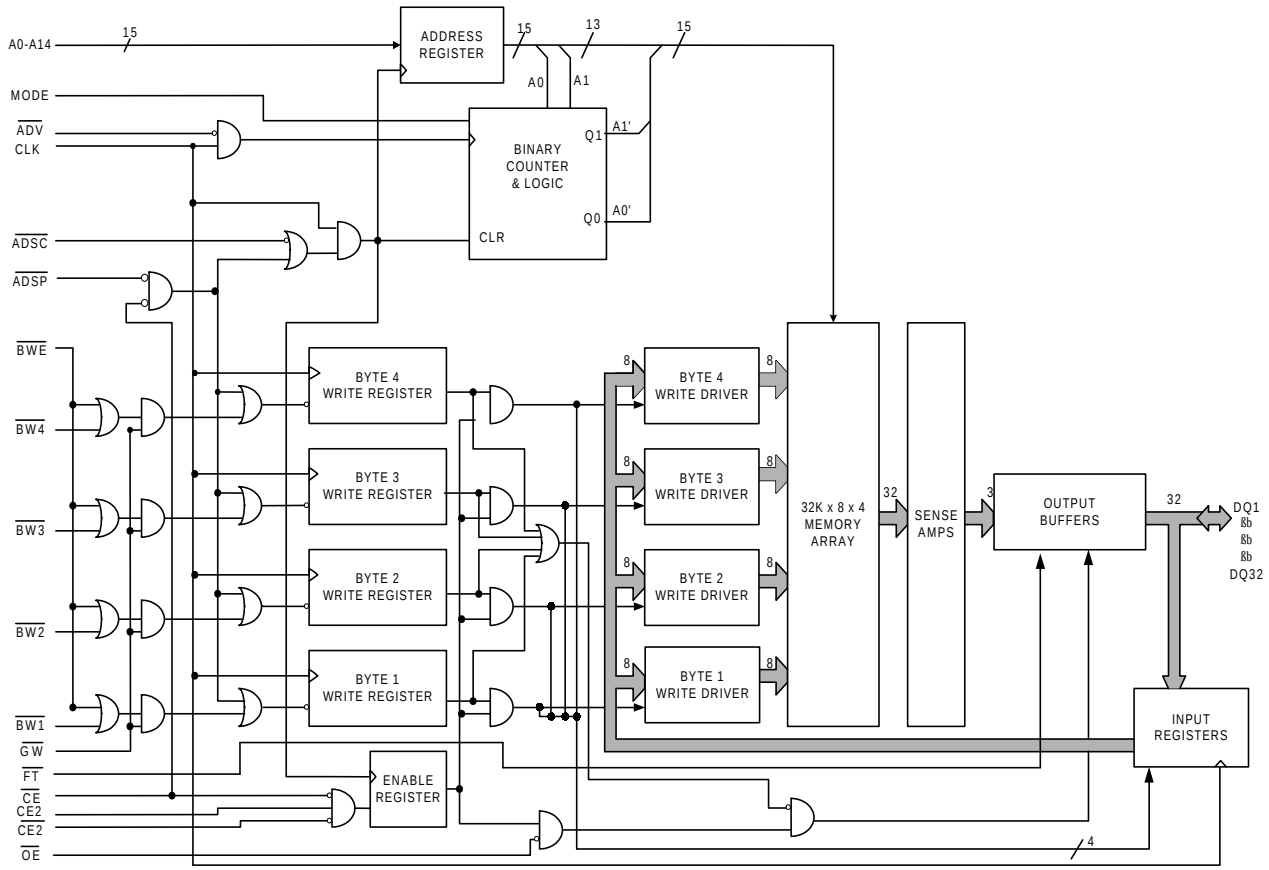

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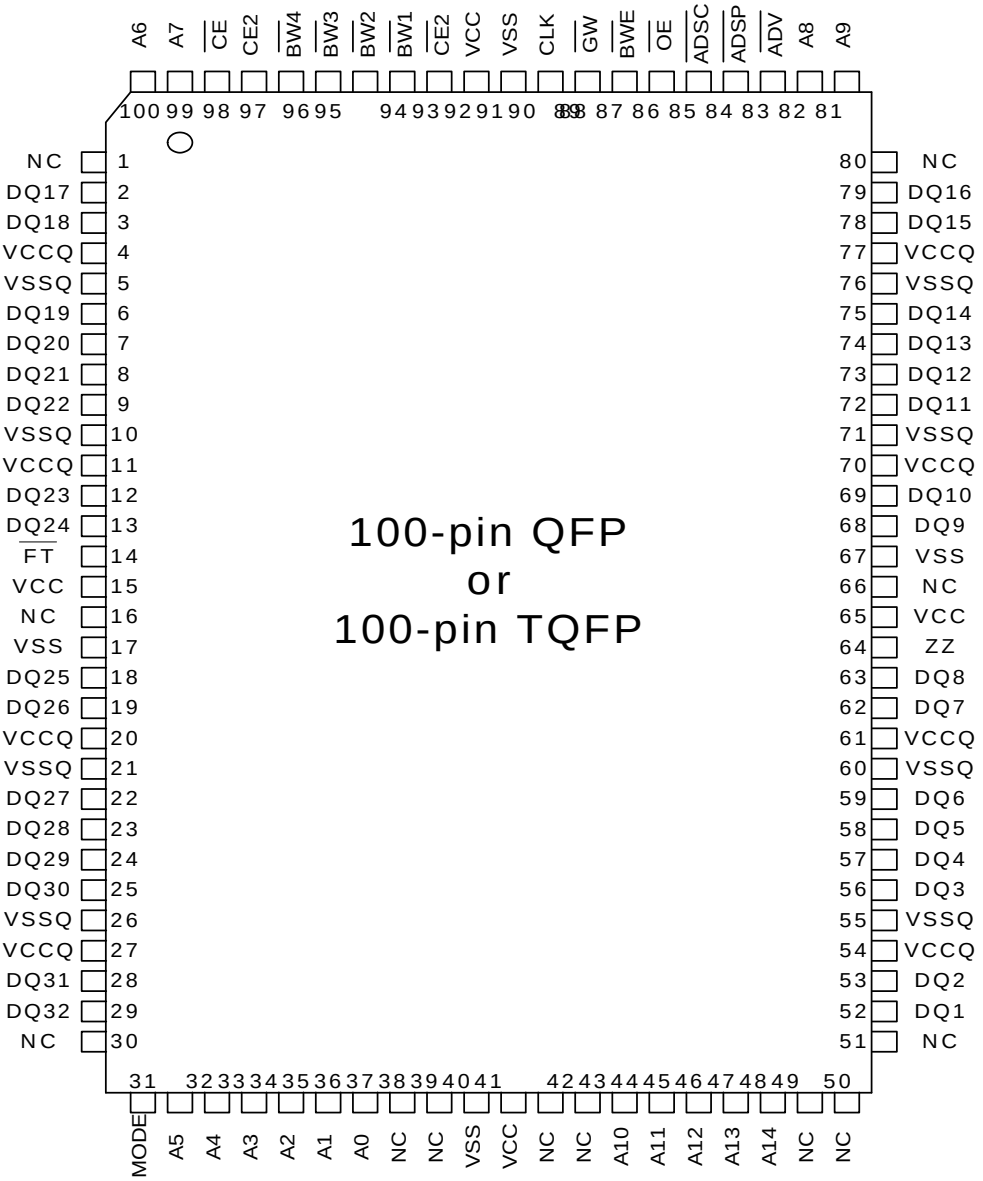
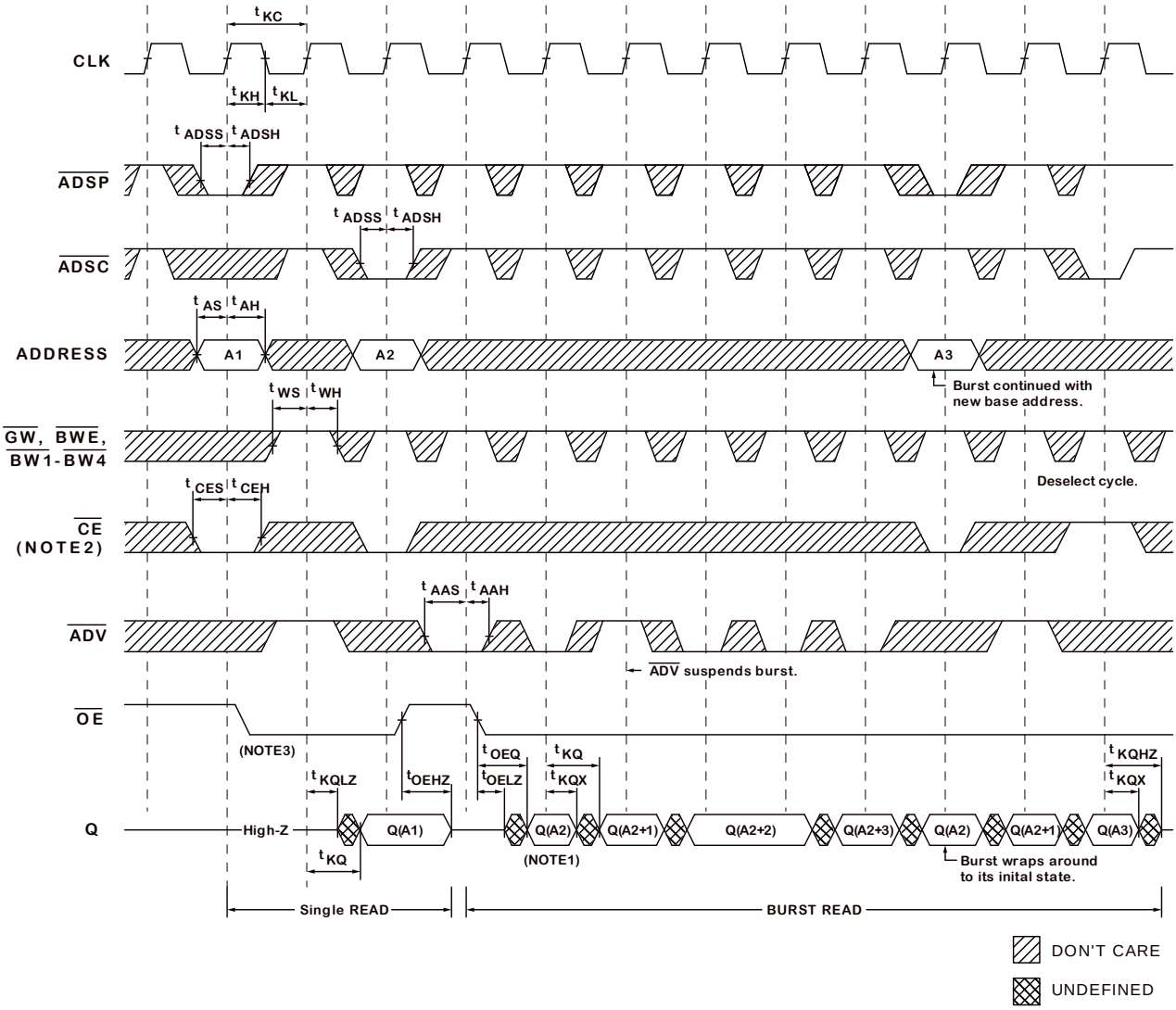
Note: The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

PIN ASSIGNMENT (Top View)



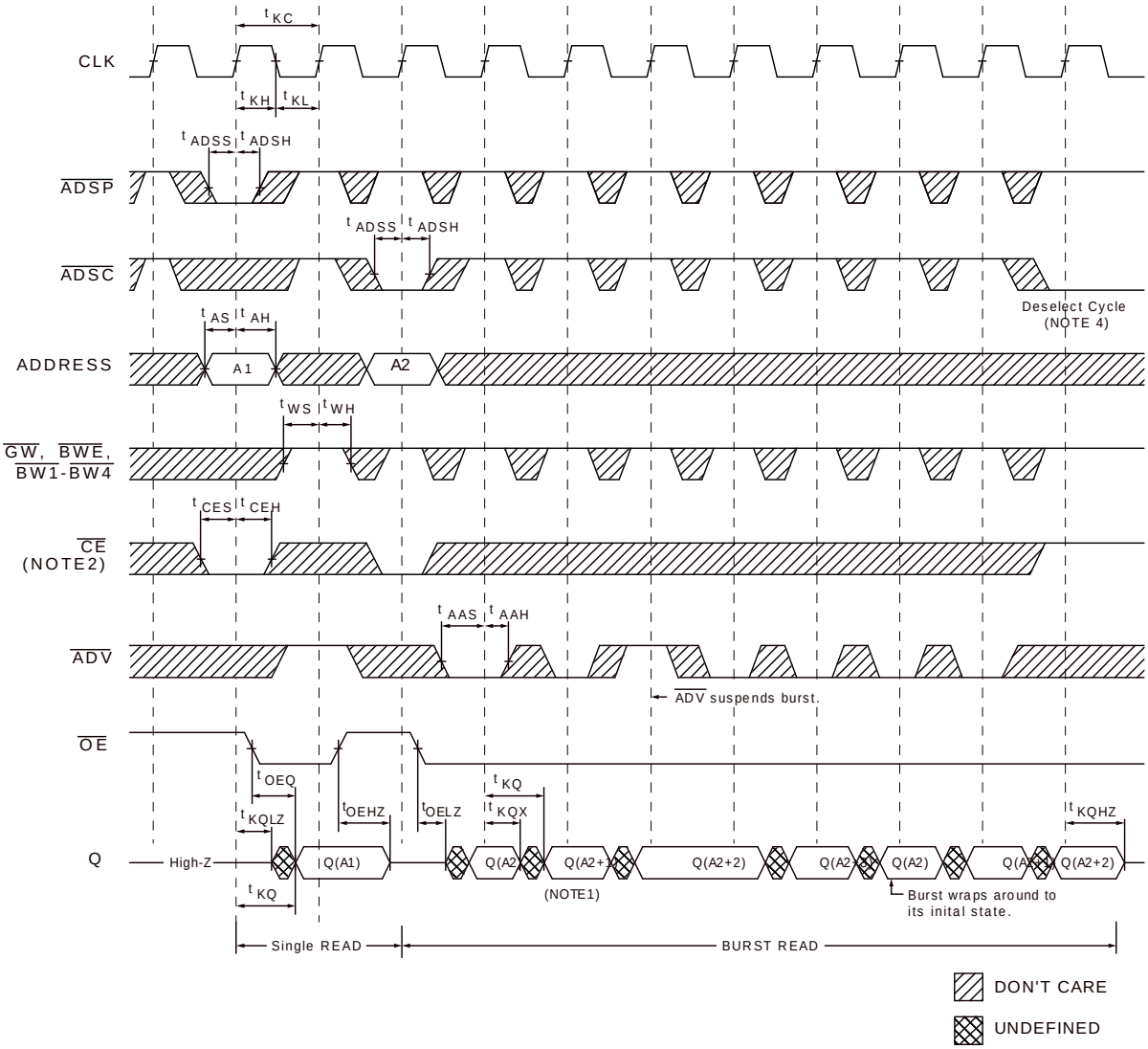
PIPELINE READ TIMING



Note: 1. Q(A2) refers to output from address A2. Q (A2 + 1) refers to output from the next internal burst address following A2.

2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. Timing is shown assuming that the device was not enabled before entering into this sequence. $\overline{OE}$ does not cause Q to be driven until after the following clock rising edge.

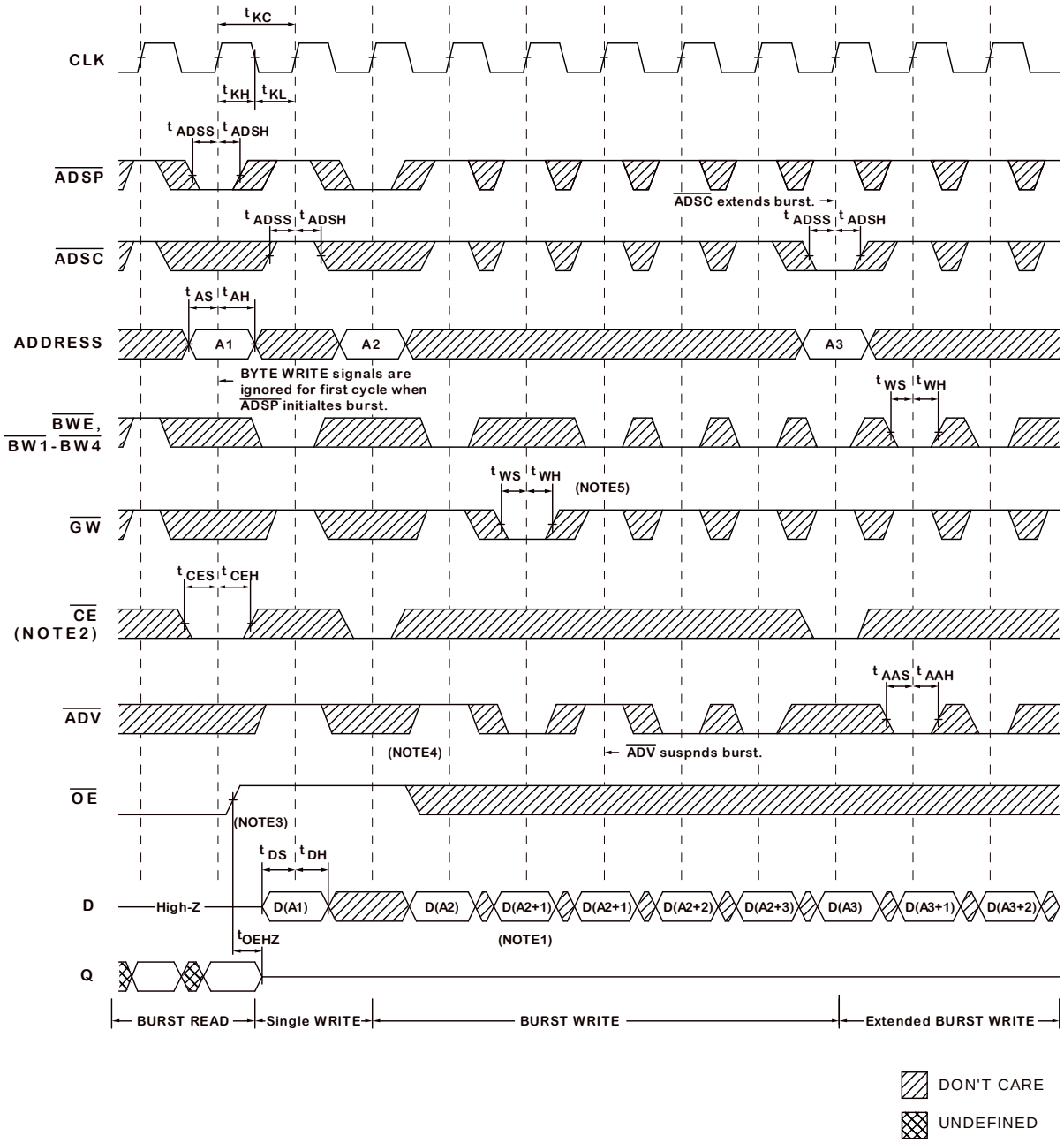
FLOW-THROUGH READ TIMING



Note: 1. Q(A2) refers to output from address A2. Q (A2 + 1) refers to output from the next internal burst address following A2.

2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. Timing is shown assuming that the device was not enabled before entering into this sequence. $\overline{OE}$ does not cause Q to be driven until after the following clock rising edge.
4. Output are disabled ^{t}KQHZ after diselect.

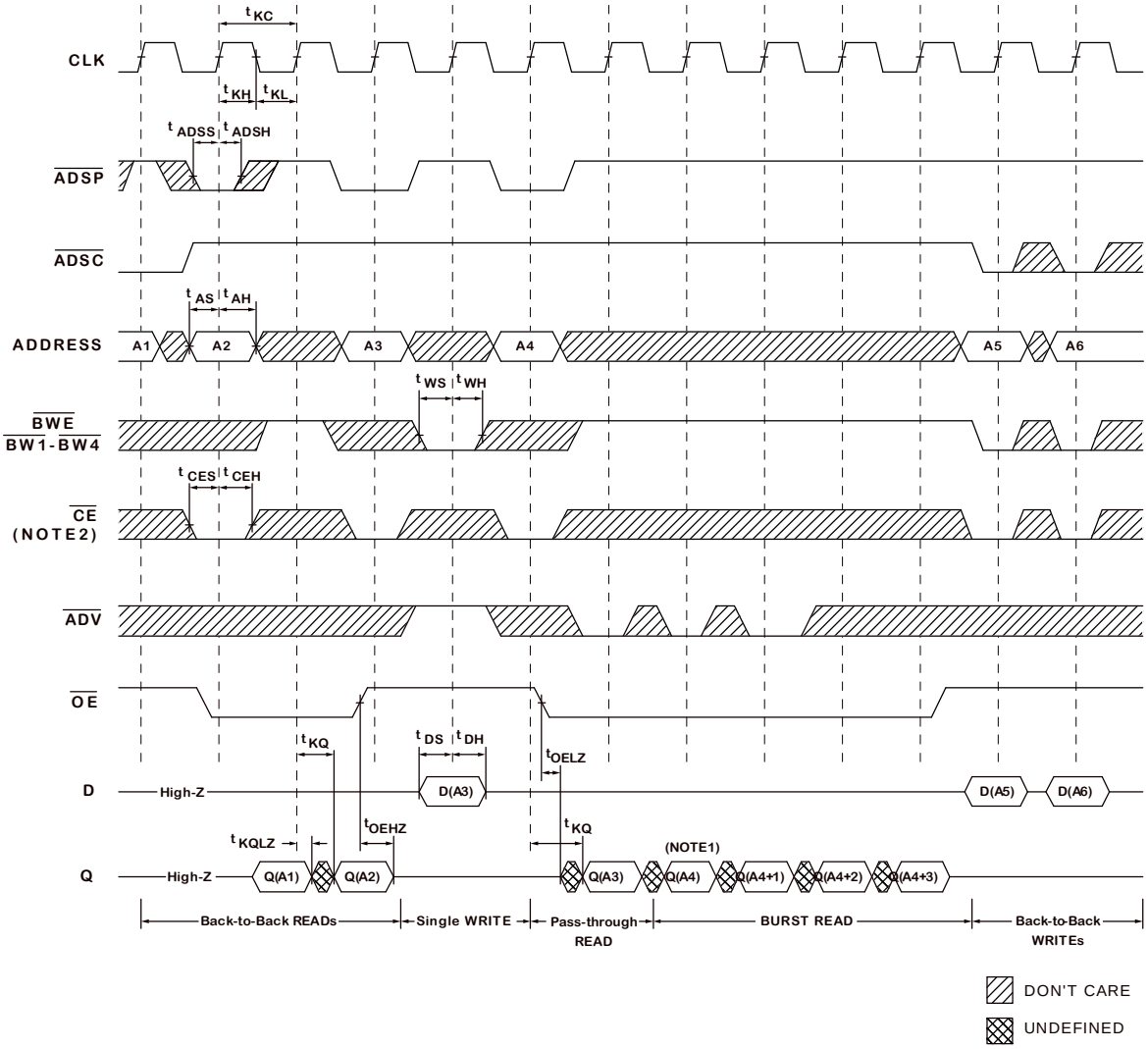
WRITE TIMING



Note: 1. Q(A2) refers to output from address A2. Q (A2 + 1) refers to output from the next internal burst address following A2.

2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW , $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH , $\overline{CE2}$ is HIGH and CE2 is LOW.
3. $\overline{OE}$ must be HIGH before the input data setup and hold HIGH throughout the data hold time. This prevents input/output data contention for the time period to the byte write enable inputs being sampled.
4. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.
5. Full width WRITE can be initiated by $\overline{GW}$ LOW or $\overline{GW}$ HIGH and $\overline{BWE}$, $\overline{BW1}$ - $\overline{BW4}$ LOW.

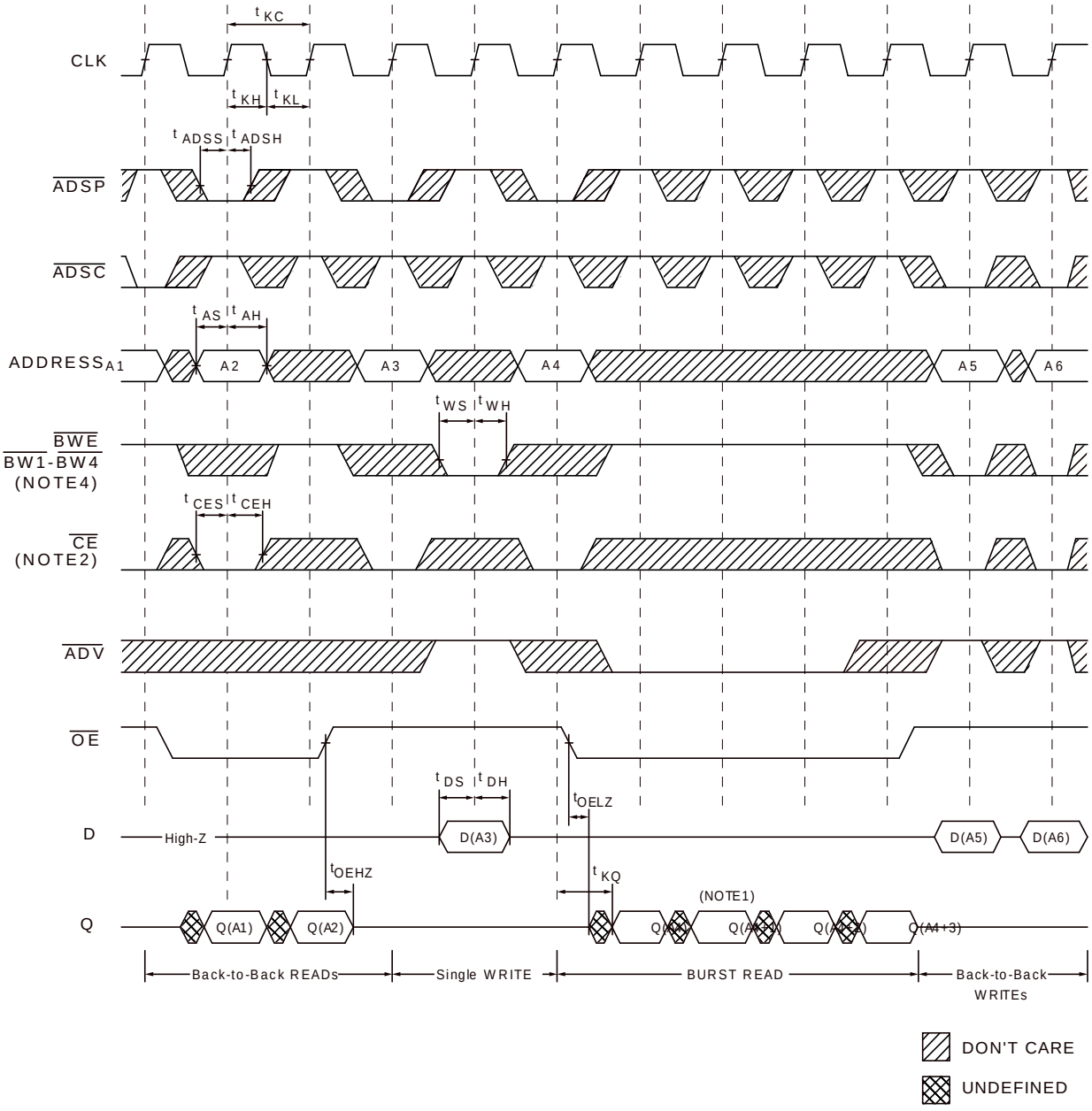
PIPELINE READ/WRITE TIMING



Note: 1. Q(A4) refers to output from address A4. Q (A4 + 1) refers to output from the next internal burst address following A4.

2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. The data bus (Q) remains in High-Z following a WRITE cycle unless an $\overline{ADSP}$, $\overline{ADSC}$ or $\overline{ADV}$ cycle is performed.
4. $\overline{GW}$ is HIGH.
5. Back-to-back READs may be controlled by either $\overline{ADSP}$ or $\overline{ADSC}$.

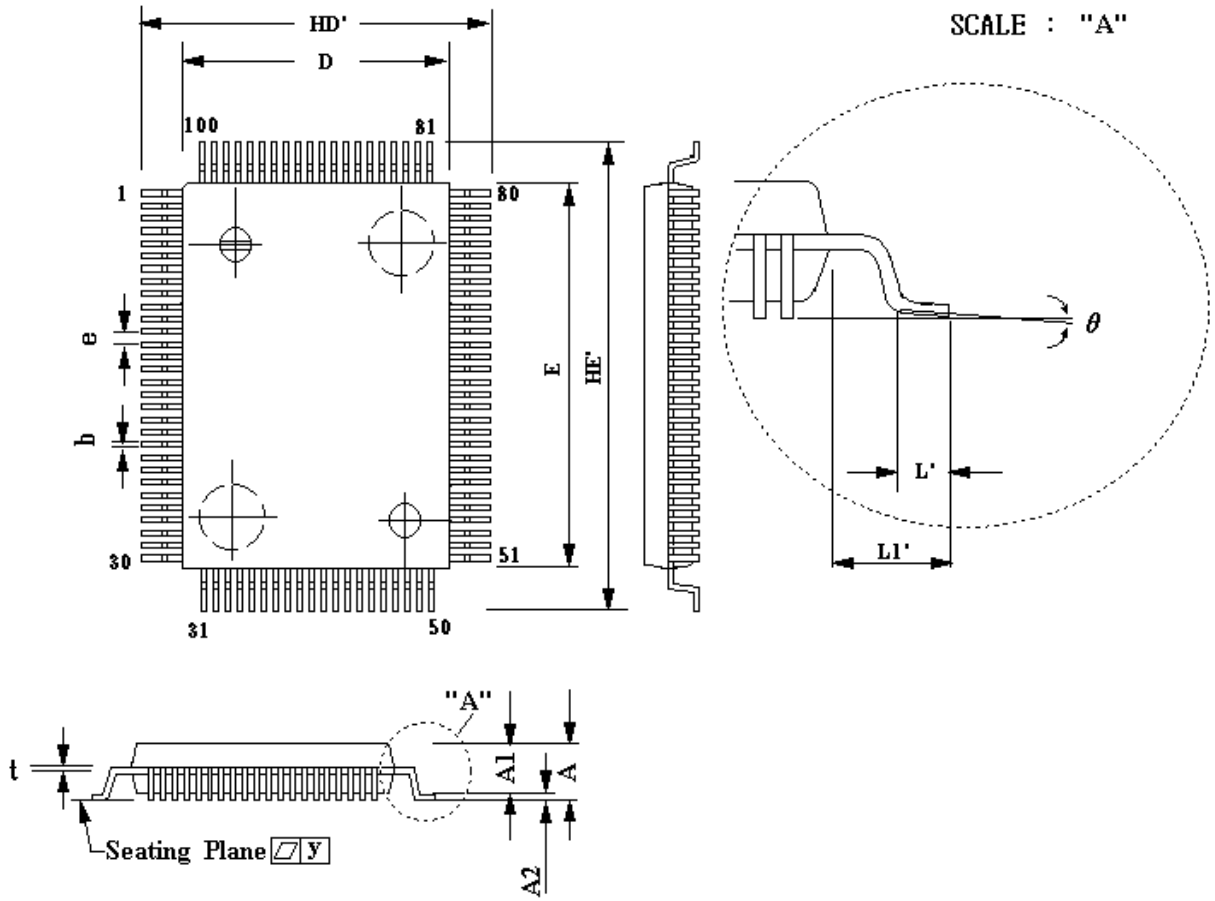
FLOW-THROUGH READ/WRITE TIMING



Note: 1. Q(A4) refers to output from address A4. Q (A4 + 1) refers to output from the next internal burst address following A4.

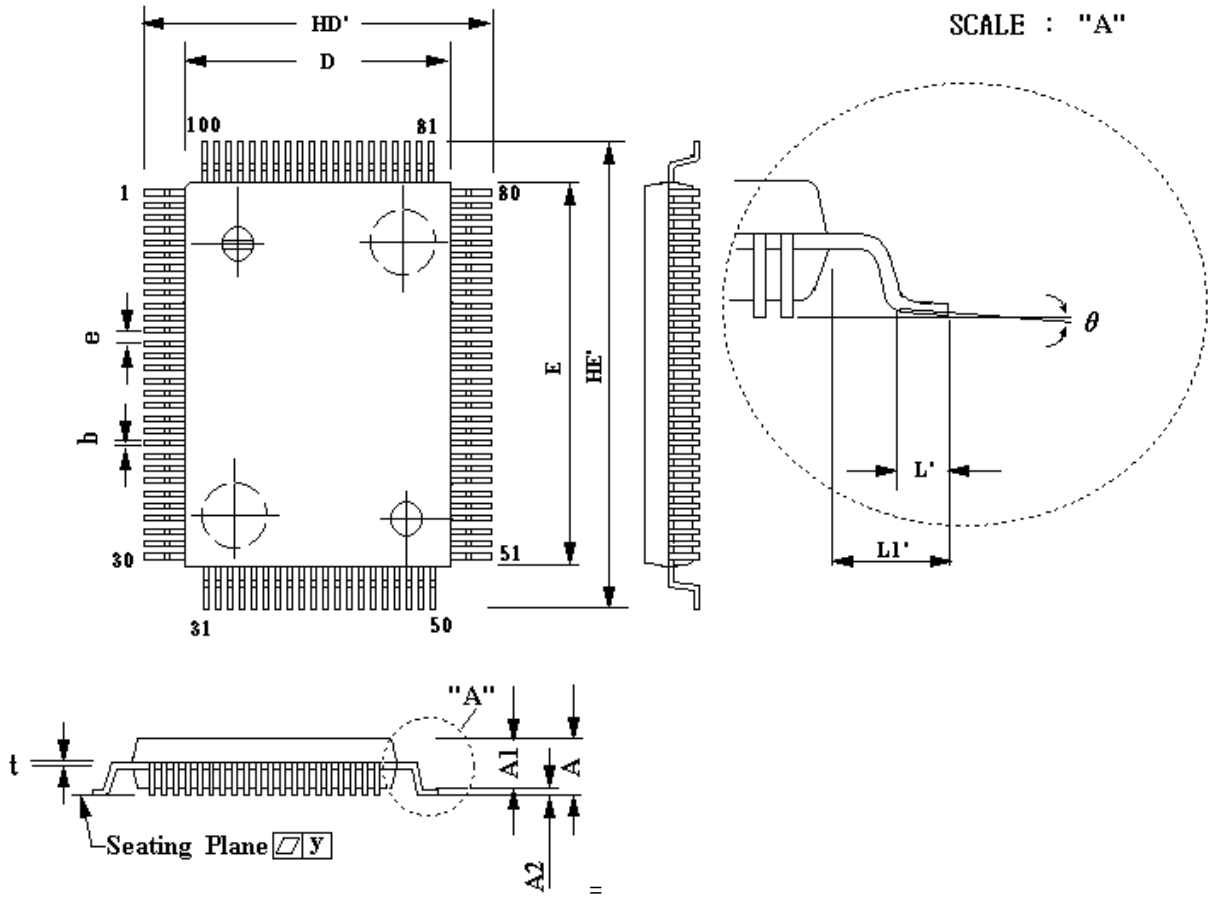
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. The data bus (Q) remains in High-Z following a WRITE cycle unless an $\overline{ADSP}$, $\overline{ADSC}$ or $\overline{ADV}$ cycle is performed.
4. $\overline{GW}$ is HIGH.
5. Back-to-back READs may be controlled by either $\overline{ADSP}$ or $\overline{ADSC}$.

PACKAGE DIMENSIONS
100-LEAD QFP SSRAM (14 x 20 mm)



SYMBOL	DIMENSIONS IN INCHES	DIMENTION IN MM
A	0.130(MAX)	3.302(MAX)
A1	0.112ßđ0.005	2.845ßđ0.127
A2	0.004(MIN)	0.102(MIN)
b	0.012+0.004-0.002	0.300+0.102-0.051
D	0.551ßđ0.005	14.000ßđ0.127
E	0.787ßđ0.005	20.000ßđ0.127
e	0.026ßđ0.006	0.650ßđ0.152
HD'	0.677ßđ0.008	17.200ßđ0.203
HE'	0.913ßđ0.008	23.200ßđ0.203
L'	0.032ßđ0.008	0.800ßđ0.203
L1'	0.063ßđ0.008	1.600ßđ0.203
t	0.006+0.004-0.002	0.150+0.102-0.051
y	0.004(MAX)	0.102(MAX)
á¡	$0^{ß`}$~$12^{ß`}$	$0^{ß`}$~$12^{ß`}$

PACKAGE DIMENSIONS
100-LEAD TQFP SSRAM (14 x 20 mm)



SYMBOL	DIMENSIONS IN INCHES	DIMENTION IN MM
A	0.063(MAX)	1.600(MAX)
A1	0.055ßđ0.005	1.400ßđ0.050
A2	0.002(MIN)	0.050(MIN)
b	0.013+0.002-0.004	0.320+0.060-0.100
D	0.551ßđ0.004	14.000ßđ0.100
E	0.787ßđ0.004	20.000ßđ0.100
e	0.026ßđ0.006	0.650ßđ0.152
HD'	0.630ßđ0.004	16.000ßđ0.100
HE'	0.866ßđ0.004	22.000ßđ0.100
L'	0.024ßđ0.006	0.600ßđ0.150
L1'	0.039ßđ0.006	1.000ßđ0.150
t	0.006ßđ0.002	0.150+0.050-0.060
y	0.003(MAX)	0.080(MAX)
á¡	0ß`~7ß`	0ß`~7ß`

PIN DESCRIPTIONS

PINS	SYM.	TYPE	DESCRIPTION
32-37, 44-48, 81, 82, 99, 100,	A0-A14	Input-Synchronous	Addresses: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. The burst counter generates internal addresses associated with A0 and A1, during burst cycle and wait cycle.
93-96	$\overline{BW1}$ $\overline{BW2}$ $\overline{BW3}$ $\overline{BW4}$	Input-Synchronous	Byte Writes: A byte write is LOW for a WRITE cyle and HIGH for a READ cycle. $\overline{BW1}$ controls DQ1-DQ8. $\overline{BW2}$ controls DQ9-DQ16. $\overline{BW3}$ controls DQ17-DQ24. $\overline{BW4}$ controls DQ25-DQ32. Data I/O are high impedance if either of these inputs are LOW , conditioned by $\overline{BWE}$ being LOW.
87	$\overline{BWE}$	Input-Synchronous	Write Enable: This active LOW input gates byte write operations and must meet the setup and hold times around the rising edge of CLK.
88	$\overline{GW}$	Input-Synchronous	Global Write: This active LOW input allows a full 32-bit WRITE to occur independent of the $\overline{BWE}$ and $\overline{BWn}$ lines and must meet the setup and hold times around the rising edge of CLK.
89	CLK	Input-Synchronous	Clock: This signal registers the addresses, data, chip enables, writecontrol and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	$\overline{CE}$	Input-Synchronous	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
92	$\overline{CE2}$	Input-Synchronous	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
97	CE2	Input-Synchronous	Synchronous Chip Enable: This active HIGH input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
86	$\overline{OE}$	Input	Output enable: This active LOW asynchronous input enables the data output drivers.
83	$\overline{ADV}$	Input-Synchronous	Address Advance: This active LOW input is used to control the internal burst counter. A HIGH on this pin generates wait cycle (no address advance).
84	$\overline{ADSP}$	Input-Synchronous	Address Status Processor: This active LOW input, along with $\overline{CE}$ being LOW, causes a new external address to be registered and a READ cycle is initiated using the new address.

PIN DESCRIPTIONS (continued)

QFP PINS	SYM.	TYPE	DESCRIPTION
85	$\overline{\text{ADSC}}$	Input-Synchronous	Address Status Controller:This active LOW input causes device to be deselected or selected along with new external address to be registered. A READ or WRITE cycle is initiated depending upon write control inputs.
14	$\overline{\text{FT}}$	Input-Static	A LOW on this pin selects in flow-through mode. A NC or HIGH on this pin selects in pipeline mode.
31	MODE	Input-Static	Mode: This input selects the burst sequence. A LOW on this pin selects LINEAR BURST. A NC or HIGH on this pin selects INTERLEAVED BURST. Do not alter input state while device is operating.
64	ZZ	Input	Snooze Enable: This active HIGH asynchronous input causes the device to enter a low-power standby mode in which all data in the memory arry is retained.
2, 3, 6-9, 12, 13, 18, 19, 22-25, 28, 29, 52, 53, 56-59, 62, 63, 68, 69, 72-75, 78, 79,	DQ1-DQ32	Input/ Output	Data Inputs/Outputs: First Byte is DQ1-DQ8. Second Byte is DQ9-DQ16. Third Byte is DQ17-DQ24. Fourth Byte is DQ25-DQ32. Input data must meet setup and hold times around the rising edge of CLK.
15,41,65,91	VCC	Supply	Power Supply: 3.3V +10%/-5%
17,40,67,90	VSS	Ground	Ground: GND
4,11,20,27,54, 61,70,77	VCCQ	I/O Supply	Output Buffer Supply: 3.3V +10%/-5%
5,10,21,26,55, 60,71,76	VSSQ	I/O Ground	Output Buffer Ground: GND
1,16,30,38, 39,42,43,49, 50, 51, 66,80	NC	-	No Connect: These signals are not internally conntected.

INTERLEAVED BURST ADDRESS TABLE (MODE = NC/VCC)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A00	A...A11	A...A10
A...A10	A...A11	A...A00	A...A01
A...A11	A...A10	A...A01	A...A00

LINEAR BURST ADDRESS TABLE (MODE = GND)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A10	A...A11	A...A00
A...A10	A...A11	A...A00	A...A01
A...A11	A...A00	A...A01	A...A10

PARTIAL TRUTH TABLE FOR READ/WRITE

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE one byte	H	L	L	H	H	H
WRITE all byte	H	L	L	L	L	L
WRITE all byte	L	X	X	X	X	X

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE}$	$\overline{CE2}$	CE2	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power Down	None	H	X	X	L	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	L	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	H	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	L	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	H	X	L	H	L	X	X	X	L-H	High-Z
Snooze Cycle, Power Down	None	X	X	X	H	X	X	X	X	X	X	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

Note: 1. X means "don't care." H means logic HIGH. L means logic LOW. $\overline{WRITE}$ = L means any one or more byte write enable signals ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ or $\overline{BW4}$) and $\overline{BWE}$ are LOW, or $\overline{GW}$ equals LOW. $\overline{WRITE}$ = H means all byte write signal are HIGH.

2. $\overline{BW1}$ = enables write to DQ1-DQ8. $\overline{BW2}$ = enables write to DQ9-DQ16. $\overline{BW3}$ = enables write to DQ17-DQ24. $\overline{BW4}$ =enables write to DQ25-DQ32.
3. All inputs except $\overline{OE}$ and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Suspending burst generates wait cycle.
5. For a write operation following a read operation. $\overline{OE}$ must be HIGH before the input data required setup time plus High-Z time for $\overline{OE}$ and staying HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be High-Z during power-up.
7. $\overline{ADSP}$ = LOW along with chip being selected always initiates an internal READ cycle at the L-H edge of CLK. A WRITE cycle can be performed by setting WRITE LOW for the CLK L-H edge of the subsequent wait cycle. Refer to WRITE timing diagram for clarification.

ABSOLUTE MAXIMUM RATINGS*

Voltage on VCC Supply Relative to VSS.
……-0.5V to +4.6V
I/O Supply Voltage VccQ ..... Vss -0.5V to Vcc
V_{IN}..... -0.5V to Vcc +0.5V
Storage Temperature (plastic)..... -55°C to +150°C
Junction Temperature .....…..... +150°C
Power Dissipation 1.0W
Short Circuit Output Current..... 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(0°C ≤ Ta ≤ 70°C; VCC = 3.3V +10%/-5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYM.	MIN	MAX	UNITS	NOTES
Input High (Logic) voltage		V_{IH}	2	VCCQ + 0.3	V	1, 2
Input Low (Logic) voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le VCC$	I_{LI}	-2	2	µA	14
Output Leakage Current	Output(s) disabled, $0V \le V_{OUT} \le VCC$	I_{LO}	-2	2	µA	
Output High Voltage	I_{OH} = -4.0 mA	V_{OH}	2.4		V	1, 11
Output Low Voltage	I_{OL} = 8.0 mA	V_{OL}		0.4	V	1, 11
Supply Voltage		Vcc	3.1	3.6	V	1

				MAX.				
DESCRIPTION	CONDITIONS	SYM.	TYP	-3.8	-4	-4.5	UNITS	NOTES
Power Supply Current : Operating	Device selected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; cycle time $\ge {}^{t}KC$ MIN; VCC = MAX; outputs open	I_{CC}	TBD	250	200	150	mA	3, 12, 13
Power Supply Current: Idle	Device selected; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$, $\overline{GW}$, $\overline{BWE} \ge V_{IH}$; all other inputs $\le V_{IL}$ or $\ge V_{IH}$; VCC = MAX; cycle time $\ge {}^{t}KC$ MIN: outputs open	I_{SB1}	TBD	60	60	60	mA	12, 13
CMOS Standby	Device deselected; VCC = MAX; all inputs ≤ VSS + 0.2 or ≥ VCC - 0.2; all inputs static; CLK frequency =0	I_{SB2}	TBD	10	10	10	mA	12, 13
TTL Standby	Device deselected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; all inputs static; VCC = MAX;CLK frequency = 0	I_{SB3}	TBD	25	25	25	mA	12, 13
Clock Running	Device deselected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; VCC =MAX; CLK cycle time $\ge {}^{t}KCMIN$	I_{SB4}	TBD	60	60	60	mA	12, 13

AC ELECTRICAL CHARACTERISTICS (Note 5) ($0°C \le T_A \le 70°C$; VCC=3.3V +0.3V/-0.165V)

DESCRIPTION		-3.8		-4		-4.5		UNITS	NOTES
	SYM.	MIN	MAX	MIN	MAX	MIN	MAX		
Clock(pipeline)									
Clock cycle time	t_{KC}	6.6		7.5		8.5		ns	
Clock to output valid	t_{KQ}		3.8		4		4.5		
Clock to output invalid	t_{KQX}	1.5		2		2		ns	
Clock to output in Low-Z	t_{KQLZ}	1.5		2		2		ns	
Clock(flow-through)									
Clock cycle time	t_{KC}	10.5		15		15		ns	
Clock to output valid	t_{KQ}		9.0		10		11		
Clock to output invalid	t_{KQX}	3		3		3		ns	
Clock to output in Low-Z	t_{KQLZ}	3		3		3		ns	
Output Times									
Clock HIGH time	t_{KH}	1.8		1.9		2.0		ns	
Clock LOW time	t_{KL}	1.8		1.9		2.0		ns	6, 7
Clock to output in High-Z	t_{KQHZ}		5		5		5	ns	6, 7
OE to output valid	t_{OEQ}		5		5		5	ns	9
OE to output in Low-Z	t_{OELZ}	0		0		0		ns	6, 7
OE to output in High-Z	t_{OEHZ}		5		5		5	ns	6, 7
Setup Times									
Address	t_{AS}	1.7		2.0		2.0		ns	8, 10
Address Status($\overline{ADSC}$, $\overline{ADSP}$)	t_{ADSS}	1.7		2.0		2.0		ns	8, 10
Address Advance ($\overline{ADV}$)	t_{AAS}	1.7		2.0		2.0		ns	8, 10
Byte Write Enables ($\overline{BW1}$ ~ $\overline{BW4}$, $\overline{BWE}$, $\overline{GW}$)	t_{WS}	1.7		2.0		2.0		ns	8, 10
Data-in	t_{DS}	1.7		2.0		2.0		ns	8, 10
Chip Enables($\overline{CE}$, $\overline{CE2}$,CE2)	t_{CES}	1.7		2.0		2.0		ns	8, 10
Hold Times									
Address	t_{AH}	0.5		0.5		0.5		ns	8, 10
Address Status($\overline{ADSC}$, $\overline{ADSP}$)	t_{ADSH}	0.5		0.5		0.5		ns	8, 10
Address Advance ($\overline{ADV}$)	t_{AAH}	0.5		0.5		0.5		ns	8, 10
Byte Write Enables ($\overline{BW1}$ ~ $\overline{BW4}$, $\overline{BWE}$, $\overline{GW}$)	t_{WH}	0.5		0.5		0.5		ns	8, 10
Data-in	t_{DH}	0.5		0.5		0.5		ns	8, 10
Chip Enables($\overline{CE}$, $\overline{CE2}$,CE2)	t_{CEH}	0.5		0.5		0.5		ns	8, 10

CAPACITANCE

DESCRIPTION	CONDITIONS	SYM.	TYP	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz VCC = 3.3V	C_I	3	4	pF	4
Input/ Output Capacitance(DQ)		C_O	6	7	pF	4

THERMAL CONSIDERATION

DESCRIPTION	CONDITIONS	SYM.	QFP TYP	UNITS	NOTES
Thermal Resistance - Junction to Ambient	Still air, soldered on 4.25x1.125 inch 4-layer PCB	Θ_{JA}	20	°C/W	
Thermal Resistance - Junction to Case		Θ_{JB}	1	°C/W	

AC TEST CONDITIONS

Input pulse levels	0V to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

Notes:

1. All voltages referenced to VSS (GND).
2. Overshoot: $V_{IH} \le +3.6$ V for $t \le {}^tKC/2$.
   Undershoot: $V_{IL} \le -1.0$ V for $t \le {}^tKC/2$.
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5 pF as in Fig. 2.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. A READ cycle is defined by byte write enables all HIGH or $\overline{ADSP}$ LOW along with chip enables being active for the required setup and hold times. A WRITE cycle is defined by at one byte or all byte WRITE per READ/WRITE TRUTH TABLE.
9. $\overline{OE}$ is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All synchronous inputs must meet specified setup and hold time, except for "don't care" as defined in the truth table.
11. AC I/O curves are available upon request.
12. "Device Deselected means the device is in POWER-DOWN mode as defined in the truth table. "Device Selected" means the device is active.
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
14. MODE pin has an internal pull-up and exhibits an input leakage current of ± 10μA.

OUTPUT LOADS

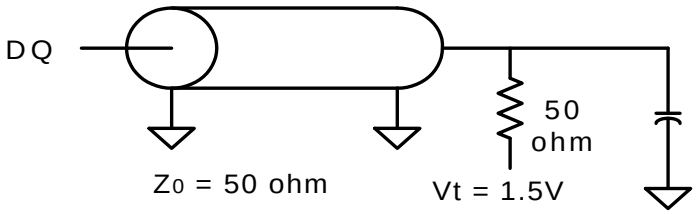


Fig. 1 output load equivalent

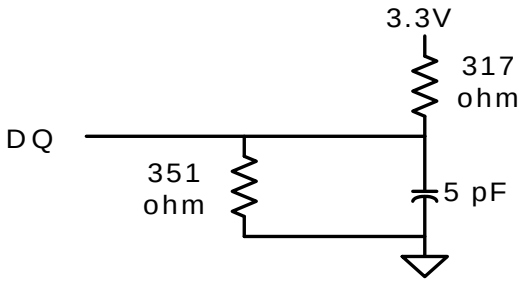


Fig. 2 output load equivalent

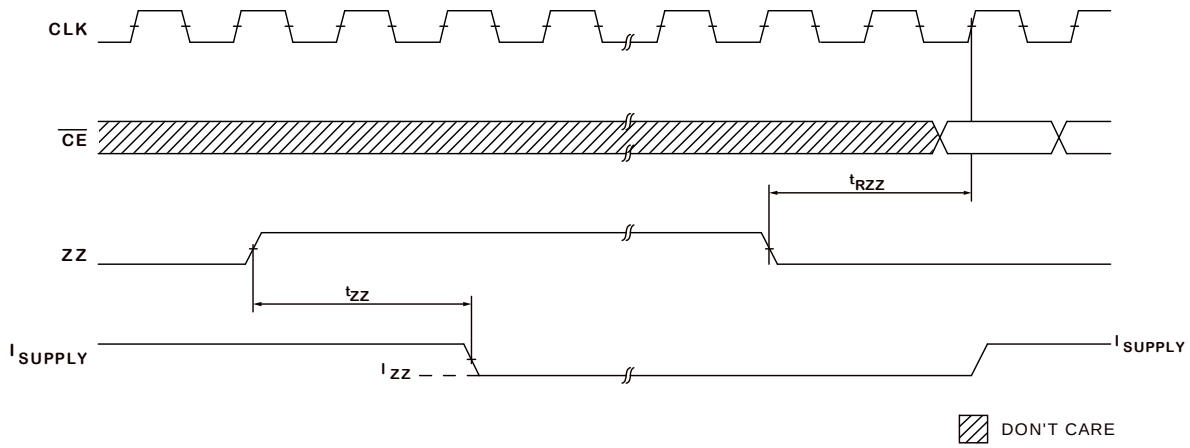
SNOOZE MODE

SNOOZE MODE is a low current, "power down" mode in which the device is deselected and current is reduced to I_{ZZ}. The duration of SNOOZE MODE is dictated by the length of time the ZZ pin is in a HIGH state. After entering SNOOZE MODE, the clock and all other inputs are ignored. The ZZ pin (pin 64) is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE. When the ZZ pin becomes a logic HIGH, I_{ZZ} is guaranteed after the setup time t_{ZZ} is met. Any access pending when entering SNOOZE MODE is not guaranteed to successfully complete. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.

SNOOZE MODE ELECTRICAL CHARACTERISTICS

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Current during SNOOZE MODE	$ZZ \geq V_{IH}$	I_{ZZ}		5	mA	
ZZ HIGH to SNOOZE MODE time		t_{ZZ}	$2(t_{KC})$		ns	4
SNOOZE MODE Operation Recovery Time		t_{RZZ}		$2(t_{KC})$	ns	4

SNOOZE MODE WAVEFORM



Note: 1. The $\overline{CE}$ signal shown above refers to a TRUE state on all chip selects for the device.

2. All other inputs held to static CMOS levels (VIN ≤ Vss + 0.2 V or ≥ Vcc -0.2 V).