SiI9233 HDMI Receiver with Repeater, Multi-channel Audio, and Deep Color Output

Data Sheet

SiI-DS-1032-A

March 2016

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1. General Description

The SiI9233 from Lattice Semiconductor is a 4-port receiver that is fully compliant with the HDMI 1.3 standard. AV receivers that output to DTVs displaying 10/12-bit color depth can now provide the highest quality protected digital audio/video over a single cable. The SiI9233 receiver can receive deep color video up to 12-bit, 1080p at 60 Hz. Efficient color space conversion receives RGB or YCbCr video data and outputs either standard-definition or high-definition RGB or YCbCr formats.

The SiI9233 receiver adds support for the extended gamut YCC or x.v.Color color space, which supports approximately 1.8 times the number of colors as the RGB color space. The x.v.Color color space also makes full use of the range on the standard 8-bit resolution per pixel.

1.1. Features

- 4-Port HDMI 1.3, HDCP 1.3, and DVI 1.0 compliant Receiver
- Integrated TMDS® core running at 25–225 MHz
- 36-bit digital video interface supports video processors:
  - x.v.Color to extended RGB
  - 36-bit RGB / YCbCr 4:4:4
  - 16/20/24-bit YCbCr 4:2:2
  - 8/10/12-bit YCbCr 4:2:2 (ITU BT.656)
  - Color Space Conversion for both RGB-to-YCbCr and YCbCr-to-RGB (both 601 and 709)
  - True 12-bit accurate output data using an internal14-bit wide processing path
  - Programmable drive strength from 2 mA to 14 mA.
  - Programmable output delay control to prevent simultaneous switching

1.2. Important Information

- See the Hot Plug Detect CTS Requirement sections for important information regarding HDMI compliance testing

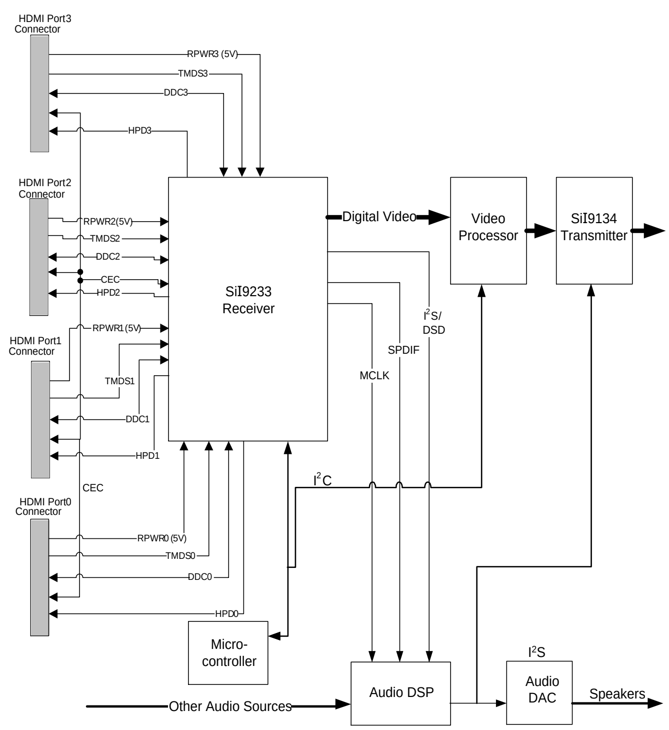


Figure 1.1. A/V Receiver Block Diagram

1.3. Overview

The SiI9233 HDMI Receiver can send and receive up to two channels of uncompressed digital audio at 192 kHz. Compressed streams are also supported through either the S/PDIF port or over I^2S for DTS-HD and Dolby TrueHD. An industry-standard I^2S port allows direct connection to low-cost audio DACs at up to 192 kHz. An S/PDIF port supports up to 192 kHz audio. Audio down-sampling allows the SiI9233 receiver to share the audio bus with a high-sample-rate audio DAC while down-sampling audio for an attached display that supports only lower rates.

The SiI9233 receiver provides additional integrated features to help lower system cost and provide enhanced features to the end consumer. The SiI9233 receiver integrates the Extended Display Identification Data (EDID) block, which is stored in embedded Non-Volatile Memory (NVM). This memory can be programmed at the time of manufacture using the local I^2C bus, similar to how existing EEPROMs are programmed today. On board RAM can also be loaded with EDID data from the system microcontroller during power up or initialization if the NVM is not used. The EDID is reflected on each of the four HDMI ports through the DDC bus. Flexibility is built in to allow mixing different EDID formats in an application. This feature can eliminate up to four EDID ROMs while also saving board space.

The SiI9233 receiver provides a complete, simple solution to enabling Consumer Electronics Control (CEC) in a DTV. CEC is a single-wire bus that transmits remote control commands throughout a home network. The SiI9233 receiver integrates both an HDMI-compliant I/O and Lattice Semiconductor's CEC API. The CEC I/O meets all HDMI compliance tests and eliminates the need for additional external components, again saving board space and reducing DTV BOM cost. The CEC API manages reception and transmission of all CEC signals according to the CEC protocol and makes the information available to the system microcontroller. This significantly lowers the system-level control by the system microcontroller, simplifying firmware overhead.

The SiI9233 receiver also incorporates a very robust standby power scheme. The standby power plane of the device is isolated from the rest of the device, and can be powered locally from an external +5 V standby power supply input to the device, or from the +5 V signal from one of the four HDMI connectors. This feature results in extremely low power consumption of the device when in standby mode, while both CEC and EDID are fully operational. Additionally, if using the NVM feature to store the EDID, only the +5 V power from the source device is needed to read the EDID, and the display can be completely unplugged from the AC power outlet.

The SiI9233 receiver also comes pre-programmed with HDCP keys. This set of keys simplifies the manufacturing process and lowers costs, while providing the highest level of HDCP key security.

Lattice Semiconductor's HDMI Receivers use the latest generation of TMDS core technology, supporting dynamic cable equalization that automatically detects the appropriate equalization required for the incoming signal, offering the best support for long cable connections. These TMDS cores pass all HDMI compliance tests.

1.4. Additional Features

- Digital audio interface supports high-end audio systems:
  - DTS-HD and DolbyTrueHD high bit rate audio support
  - I^2S output with 4 data signals for multi-channel formats
  - S/PDIF output supports PCM, Dolby Digital, DTS digital audio transmission (32-192 kHz Fs sample rate)
  - IEC60958 or IEC61937 compatible
  - Flexible, programmable I^2S channel mapping
  - 2:1 and 4:1 down-sampling to handle 96-kHz and 192-kHz audio streams.
- Intelligent audio mute capabilities avoids pops and noise with automatic soft mute and unmute.
- Integrated HDCP decryption engine for receiving protected audio and video content:
  - Pre-programmed HDCP keys provide highest level of key security and simplify manufacturing
  - Full support for HDCP repeaters (up to 16 attached downstream devices)
  - Built in HDCP self-test (BIST).
- HDCP Repeater support.
- Built-in Consumer Electronics Control (CEC)
  - HDMI-compliant CEC I/O simplifies design and lowers cost
  - Integrated CEC Programming Interface (CPI) lowers software overhead
  - Automatic Feature Abort response for unsupported commands
  - Automatic message retry on transmit.
- Integrated EDID in non-volatile memory with optional registers to override EDID for each port.

- Flexible power management
    - Separate Standby power pin
    - Standby power can be from HDMI +5V signal or locally
    - Extremely low standby power.
- 20 mm x 20 mm 144-pin TQFP package with ePad.

2. System Applications

The SiI9233 HDMI Receiver is designed for digital televisions that require support for HDMI v1.3 Deep Color. The SiI9233 receiver supports the HDMI v1.3 specification and allows receipt of 10/12-bit color depth up to 1080p resolutions. A single SiI9233 receiver provides four HDMI input ports. The video output interfaces to a video processor and the audio output can interface directly to an audio DAC or an audio DSP for further processing as shown in Figure 1.1.

2.1. Comparing SiI9233 with SiI9127, SiI9125 and SiI9135

Table 2.1 summarizes the functional differences among the SiI9127, SiI9125, the SiI9135, and the SiI9233.

Table 2.1. Summary of Features

Feature	SiI9125	SiI9127	SiI9135	SiI9223	SiI9233
HDMI Input Connections					
TMDS Input Ports	2	2	2	4	4
Color Depth	8/10/12-bit	8/10/12-bit	8/10/12-bit	8/10/12-bit	8/10/12-bit
DDC Input Ports	2	2	2	4	4
Maximum TMDS Input Clock	225 MHz	225 MHz	225 MHz	225 MHz	225 MHz
Video Output					
Digital Video Output Ports	1	1	1	1	1
Maximum Output Pixel Clock	165 MHz.	165 MHz.	165 MHz.	165 MHz.	165 MHz.
Maximum Output Bus Width	36	36	36	36	36
Audio Formats					
S/PDIF Output Ports	1	1	1	1	1
I2S Output	2 channel	2 channel	8 channel	2 channel	8 channel
DSD Output	2 channel	NA	6 channel	NA	8 channel
High Bit Rate Audio Support Compressed DTS-HD and Dolby True-HD	No	No	Yes	No	Yes
Maximum Audio Sample Rate (Fs)	192 kHz	192 kHz	192 kHz	192 kHz	192 kHz
Video Processing					
Color Space Converter	RGB to/from YCbCr	RGB to/from YCbCr x.v.Color to RGB	RGB to/from YCbCr	RGB to/from YCbCr x.v.Color to RGB	RGB to/from YCbCr x.v.Color to RGB
Pixel Clock Divider	÷ 4, ÷ 2	÷ 4, ÷ 2	÷ 4, ÷ 2	÷ 4, ÷ 2	÷ 4, ÷ 2
Digital Video Bus Mapping	swap Cb, Cr pins	swap Cb, Cr pins	swap Cb, Cr pins	swap Cb, Cr pins	swap Cb, Cr pins
Other Features					
Local fixed I2C Device Address	0x60/0x68 or 0x62/0x6A	0x60/0x68 or 0x62/0x6A	0x60/0x68 or 0x62/0x6A	0x60/0x68 or 0x62/0x6A	0x60/0x68 or 0x62/0x6A
Programmable I2C Device Address	NA	0x64, 0xC0, 0xE0, 0xE6, 0x90	NA	0x64, 0xC0, 0xE0, 0xE6, 0x90	0x64, 0xC0, 0xE0, 0xE6, 0x90
CEC	No	Yes	No	Yes	Yes
EDID	No	NVRAM	No	NVRAM	NVRAM
HDCP Repeater Support	No	No	Yes	No	Yes
Interlaced Format Detection Pin	Yes	Yes	Yes	Yes	Yes
Package	144-pin TQFP ePad	128-pin TQFP ePad	144-pin TQFP ePad	144-pin TQFP ePad	144-pin TQFP ePad

3. Functional Description

The SiI9233 receiver provides a complete solution for receiving HDMI-compliant digital audio and video. Specialized audio and video processing is available within the HDMI Receiver to add HDMI capability to consumer electronics such as DTVs. Figure 3.1 shows the functional blocks of the chip.

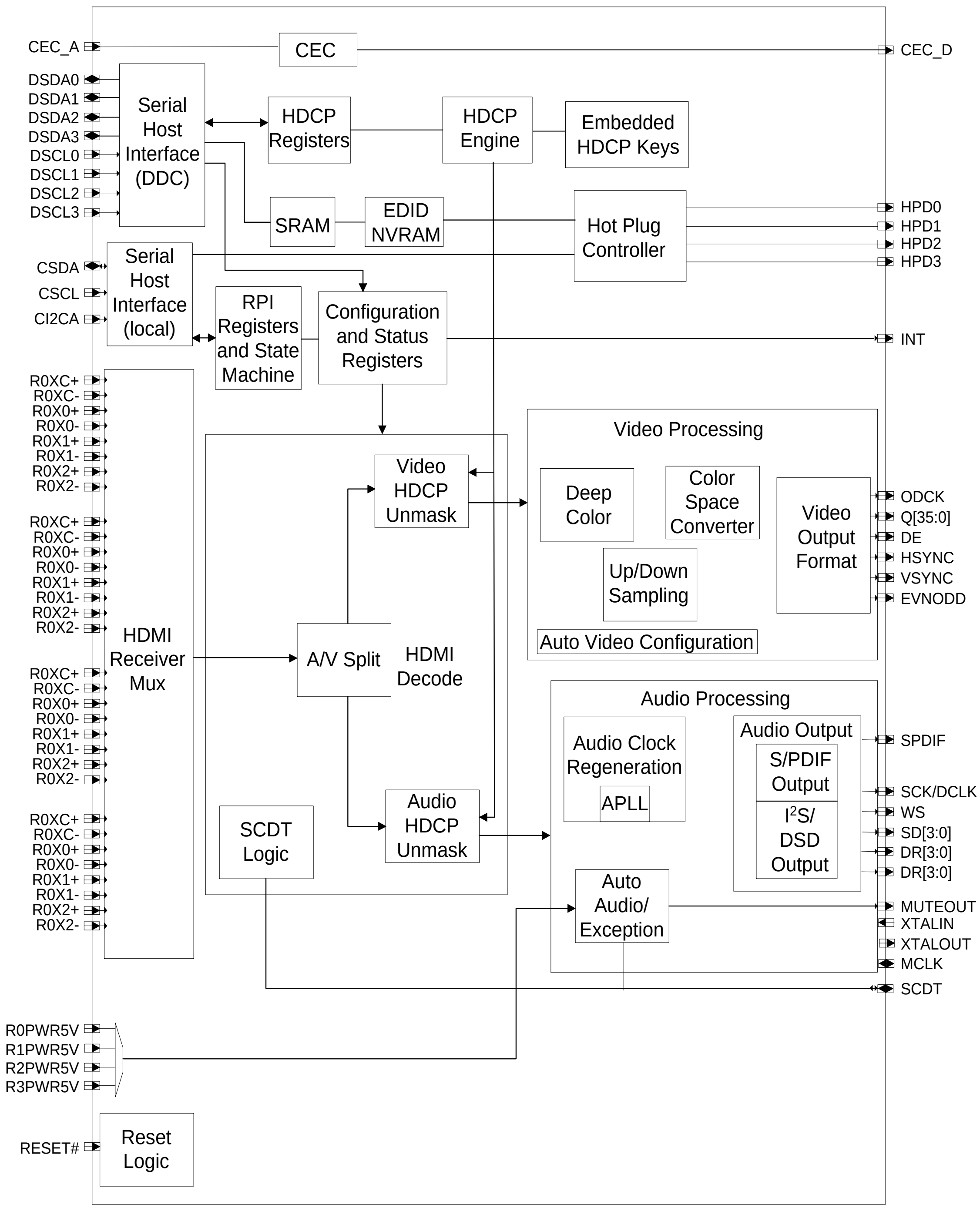


Figure 3.1. Functional Block Diagram

The SiI9233 receiver supports four HDMI input ports. Only one port can be active at any time.

3.1. TMDS Digital Cores

The TMDS Digital core is the latest generation core that supports HDMI v1.3 and the ability to carry 10/12-bit color depth. The core can receive TMDS data at up to 225 MHz. Each core performs 10-to-8-bit TMDS decoding on the video data and 10-to-4 bit TMDS decoding on the audio data received from the three TMDS differential data lines along with a TMDS differential clock. The TMDS core can sense a stopped clock or stopped video and software can put the HDMI receiver into power-down mode.

3.1.1. Active Port Detection and Selection

Only one port can be active at a time, under control of the HDMI Receiver's firmware. Active TMDS signaling can arrive at all ports, but only one has internal circuitry enabled. The firmware in the display controls these states using register settings.

Other control signals are associated with the TMDS signals on each HDMI port. The HDMI Receiver can monitor the +5V supply from each attached host. The firmware can poll registers to check on which ports are connected. The firmware also controls functional connection to one of the four E-DDC buses, enabling one while disabling the others. An attached host determines the active status of an attached HDMI device by polling the E-DDC bus to the HDMI Receiver.

Refer to the *SiI9223/9233/9127 HDMI Receivers Programmer's Reference* (SiI-PR-1019) for a complete description of port detection and selection.

3.2. HDCP Decryption Engine/XOR Mask

The HDCP decryption engine contains all the necessary logic to decrypt the incoming audio and video data. The decryption process is entirely controlled by the host side microcontroller/microprocessor through a set sequence of register reads and writes through the DDC channel. Pre-programmed HDCP keys and a Key Selection Vector (KSV) stored in the on-chip non-volatile memory are used in the decryption process. A resulting calculated value is applied to an XOR mask during each clock cycle to decrypt the audio/video data.

The SiI9233 also contains all the necessary logic to support full HDCP repeaters. The KSV values of downstream devices (up to 16 total) are written to the HDMI receiver through the local I^2C bus (CSDA/CSCL). As defined in the HDCP specification, Vi' is calculated and made available to the host on the DDC bus (DSDA/DSCL).

3.2.1. HDCP Embedded Keys

The SiI9233 HDMI Receiver comes pre-programmed with a set of production HDCP keys stored on-chip in non-volatile memory. System manufacturers do not need to purchase key sets from the Digital-Content LLC. All purchasing, programming, and security for the HDCP keys is handled by Lattice Semiconductor. The pre-programmed HDCP keys provide the highest level of security, as keys cannot be read out of the device after they are programmed. Before receiving samples of the SiI9233 receiver, customers must sign the HDCP license agreement (www.digital-cp.com) or a special NDA with Lattice Semiconductor.

3.3. Data Input and Conversion

3.3.1. Mode Control Logic

The mode control logic determines if the decrypted data is video, audio, or auxiliary information and directs it to the appropriate logic block.

3.3.2. Video Data Conversion and Video Output

The HDMI Receiver can output video in many different formats (see examples in Table 3.1) and can process the video data before it is sent, as shown in Figure 3.2. It is possible to bypass each of the processing blocks by setting the appropriate register bits.

Table 3.1. Digital Video Output Formats

Color Space	Video Format	Bus Width	HSYNC/ VSYNC	Output Clock (MHz)								Notes
				480i/576i[2, 3]	480p	XGA	720p	1080i	SXGA	1080p	UXGA	
RGB	4:4:4	36	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		30	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		24	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		12/15/18	Separate	27	27	65	74.25	74.25	—	—		4
YCbCr	4:4:4	36	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		30	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		24	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		12/15/18	Separate	27	27	65	74.25	74.25	—	—		4
	4:2:2	16/20/24	Separate	27	27	—	74.25	74.25	—	148.5	162	—
		16/20/24	Embedded	27	27	—	74.25	74.25	—	148.5	162	1
		8/10/12	Separate	27	54	—	148.5	148.5	—	—		—
		8/10/12	Embedded	27	54	—	148.5	148.5	—	—		1

Notes:

1. Embedded syncs use SAV/EAV coding.
2. 480i and 576i modes can output a 13.25 MHz clock using the internal clock divider.
3. Output clock frequency depends on programming of internal registers. Differential TMDS clock is always 25 MHz or faster.
4. Output clock supports 12/15/18-bit mode by using both edges.

3.3.2.1. **Color Range Scaling**

The color range depends on the video format, according to the CEA-861D specification. In some applications the 8-bit input range uses the entire span of 0x00 (0) to 0xFF (255) values. In other applications the range is scaled narrower. The HDMI Receiver cannot detect the incoming video data range and there is no required range specification in the HDMI AVI packet. The HDMI Receiver chooses scaling depending on the detected video format. 10 and 12-bit color range scaling are both handled the same way. Refer to the *SiI9223/9233/9127 HDMI Receivers Programmer's Reference* (SiI-PR-1019) for more details.

When the HDMI Receiver outputs embedded syncs (SAV/EAV codes), it also limits the YCbCr data output values to 1 to 254.

3.3.2.2. **Up Sample / Down Sample**

Additional logic can convert from 4:2:2 to 4:4:4 (8/10/12-bit) or from 4:4:4 (8/10/12-bit) to 4:2:2 YCbCr format. All processing is done with 14 bits of accuracy for true 12-bit data.

3.3.3. Deep Color Support

The HDMI v1.3 specification introduces color depth modes greater than 24 bits, known as Deep Color modes, to the HDMI system architecture. The Deep Color modes employ a new pixel packing scheme to enable the extra bits of higher color depth data to be carried over the existing TMDS data encoding scheme. Currently, three Deep Color modes are defined: 30-bit, 36-bit and 48-bit. The SiI9233 HDMI Receiver supports two of these three Deep Color modes: 30 and 36-bit modes. In addition, each Deep Color mode is supported to 1080p HD format.

For Deep Color modes, the TMDS clock is run faster than the pixel clock in order to create extra bandwidth for the additional bits of the higher color depth data. The increase in the TMDS clock is by the ratio of the pixel size to 24 bits, as follows:

30-bit mode: TMDS clock = 1.25x pixel clock (5:4)

36-bit mode: TMDS clock = 1.5x pixel clock (3:2)

Because the SiI9233 receiver supports 36-bit mode at 1080p, the highest TMDS clock rate it supports is 225 MHz. When in Deep Color mode, the transmitter periodically sends a General Control Packet with the current color depth and pixel packing phase information to the receiver. The SiI9233 receiver captures the color depth information in a register, which the firmware can then use to set the appropriate clock divider to recover the pixel clock and data.

3.3.4. x.v.Color Support

The SiI9233 receiver adds support for the extended gamut x.v.Color color space; this extended format has roughly 1.8 times more colors than the RGB color space. The use of the x.v.Color color space is made possible because of the availability of LED and laser-based light sources for the next generation displays. This format also makes use of the full range of values (1 to 254) in an 8-bit space instead of 16 to 235 in the RGB format. The use of x.v.Color along with Deep Color helps in reducing color banding and allows the display of a larger range of colors than is currently possible.

3.3.4.1. Color Space Conversion

Color space converter (CSC) blocks are provided to convert RGB data to Standard-Definition (ITU.601) or High-Definition (ITU.709) YCbCr formats, and vice-versa. To support the latest extended-gamut x.v.Color displays, the SiI9233 implements color space converter blocks to convert RGB data to extended-gamut Standard-Definition (ITU.601) or High-Definition (ITU.709) x.v.Color formats, and vice-versa.

RGB to YCbCr The RGB→YCbCr color space converter (CSC) can convert from video data RGB to standard definition (ITU.601) or to high definition (ITU.709) YCbCr formats. The HDMI AVI packet defines the color space of the incoming video.

YCbCr to RGB The YCbCr→RGB color space converter is available to interface to MPEG decoders with RGB-only inputs. The CSC can convert from YCbCr in standard-definition (ITU.601) or high-definition (ITU.709) to RGB.

3.3.4.2. Default Video Configuration

After hardware RESET, the HDMI Receiver chip is configured in its default mode. This mode is summarized in Table 3.2. For more details and for a complete register listing, refer to the *SiI9223/9233/9127 HDMI Receivers Programmer's Reference* (SiI-PR-1019).

Table 3.2. Default Video Processing

Video Control	Default after Hardware Reset	Note
HDCP Decryption	HDCP decryption is OFF	1
Color Space Conversion	No color space conversion	1
Color Space Selection	BT.601 selected	—
Color Range Scaling	No range scaling	1
Upsampling/Downsampling	No upsampling or downsampling	—
HSYNC & VSYNC Timing	No inversions of HSYNC or VSYNC	—
Data Bit Width	Uses 8-bit data	1
Pixel Clock Replication	No pixel clock replication	1
Power Down	Everything is powered down	—

Notes:

1. The HDMI Receiver assumes DVI mode after reset, which is RGB 24-bit 4:4:4 video with 0–255 range.

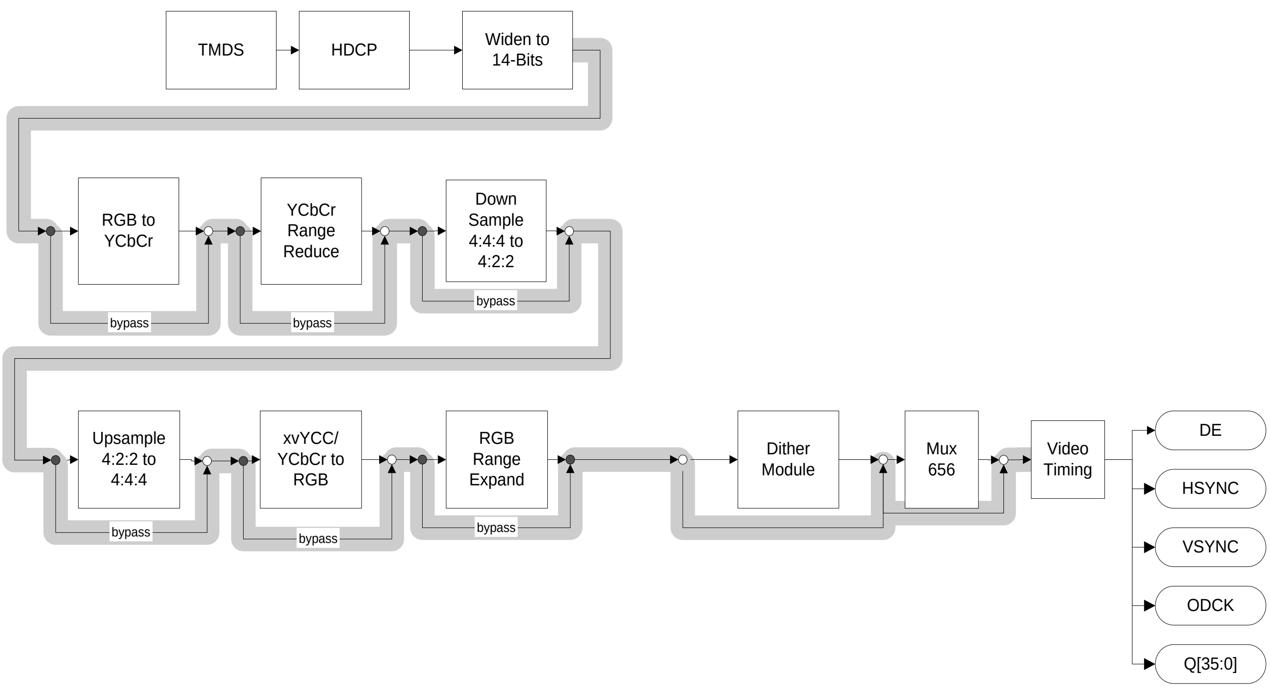


Figure 3.2. Default Video Processing Path

3.3.5. Automatic Video Configuration

The SiI9233 receiver adds automatic video configuration to simplify the firmware's task of updating the video path whenever the incoming video changes format. Bits in the HDMI Auxiliary Video Information (AVI) InfoFrame are used to reprogram the registers in the video path.

Table 3.3. AVI InfoFrame Video Path Details

AVI Byte 1 Bits [6:5]		AVI Byte 2 Bits [7:6]		AVI Byte 5 Bits [3:0]	
Y[1:0]	**Color Space**	**C[1:0]**	**Colorimetric**	**PR[3:0]**	**Pixel Repetition**
00	RGB 4:4:4	00	No Data	0000	No repetition
01	YCbCr 4:2:2	01	ITU 601	0001	Pixel sent 2 times
10	YCbCr 4:4:4	10	ITU 709	0010	Pixel sent 3 times
11	Future	11	Extended Colorimetry Information Valid	0011	Pixel sent 4 times
				0100	Pixel sent 5 times
				0101	Pixel sent 6 times
				0110	Pixel sent 7 times
				0111	Pixel sent 8 times
				1000	Pixel sent 9 times
				1001	Pixel sent 10 times

Notes on Table 3.3

1. The Auto Video Configuration assumes that the AVI information is accurate. If information is not available, then the SiI9233 receiver must choose the video path based on measurement of the incoming resolution.
2. Refer to EIA/CEA-861D Specification for details.
3. The SiI9233 receiver can support only pixel replication modes 0b0000, 0b0001, and 0b0011. Other modes are unsupported and can result in unpredictable behavior.

The format of the digital video output bus can be automatically configured to many different formats by programming the Auto Output Format Register. The available formats are listed in the table below. For detailed definitions of how to set this register, refer to the *SiI9223/9233/9127 HDMI Receivers Programmer's Reference* (SiI-PR-1019).

Table 3.4. Digital Output Formats Configurable through Auto Output Format Register

Digital Output Formats			
Color	**Width**	**MUX**	**Sync**
RGB	4:4:4	N	Sep.
YCbCr	4:4:4	N	Sep.
YCbCr	4:2:2	N	Sep.
YCbCr	4:2:2	Y	Sep.
YCbCr	4:2:2	Y	Emb.

3.4. Audio Data Capture Logic

The SiI9233 receiver can output digital audio over S/PDIF, four I²S outputs, or eight one-bit audio outputs.

3.4.1. S/PDIF

The S/PDIF stream can carry 2-channel uncompressed PCM data (IEC 60958) or a compressed bit stream for multi-channel (IEC 61937) formats. The audio data capture logic forms the audio data into packets according to the HDMI specification. The S/PDIF output supports audio sampling rates from 32 to 192 kHz. A separate master clock output (MCLK), coherent with the S/PDIF output, is provided for time-stamping purposes. *Coherent* means that the MCLK and S/PDIF must have been created from the same clock source. This is typically done by using the original MCLK to strobe out the S/PDIF from the sourcing chip. There is no setup or hold timing requirement on an output with respect to MCLK.

3.4.2. I²S

The I²S bus format is programmable through registers, to allow interfacing with I²S audio DACs or audio DSPs with I²S inputs. Refer to the Programmer's Reference for the different options on the I²S bus. Additionally, the MCLK (audio master clock) frequency is selectable to be an integer multiple of the audio sample rate F_S.

MCLK frequencies support various audio sample rates as shown in Table 3.5.

Table 3.5. Supported MCLK Frequencies

Multiple of Fs	Audio Sample Rate, Fs : I²S and S/PDIF Supported Rates						
	32 kHz	44.1 kHz	48 kHz	88.2 kHz	96 kHz	176.4 kHz	192 kHz
128	4.096 MHz	5.645 MHz	6.144 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz
192	6.144 MHz	8.467 MHz	9.216 MHz	16.934 MHz	18.432 MHz	33.868 MHz	36.864 MHz
256	8.192 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz
384	12.288 MHz	16.934 MHz	18.432 MHz	33.864 MHz	36.864 MHz		
512	16.384 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz		
768	24.576 MHz	33.869 MHz	36.864 MHz				
1024	32.768 MHz	45.158 MHz	49.152 MHz				
1152	36.864 MHz						

3.4.3. One-Bit Audio Input (DSD/SACD)

DSD (direct stream digital) is an audio data format defined for SACD (Super Audio CD) applications. It consists of four data outputs for the left channel, four data outputs for the right channel, and a clock for up to 8-channel support. One-bit Audio supports 64*Fs, with Fs being either 44.1 kHz or 88.2 kHz.

The one bit audio outputs are synchronous to the positive edge of the DSD Clock. For one bit audio, the sampling information is carried in the Audio InfoFrame, instead of the Channel Status bits.

3.4.4. High-Bitrate Audio on HDMI

The new high-bitrate compressed standards such as DTS-HD and Dolby TrueHD transmit data at bitrates as high as 18 to 24 Mbps. Because these bitrates are so high, DVD decoders and HDMI transmitters (as source devices), and DSP and HDMI receivers (as sink devices) must carry the data using four I²S lines rather than using a single very-high-speed S/PDIF or I²S bus (see Figure 3.3).

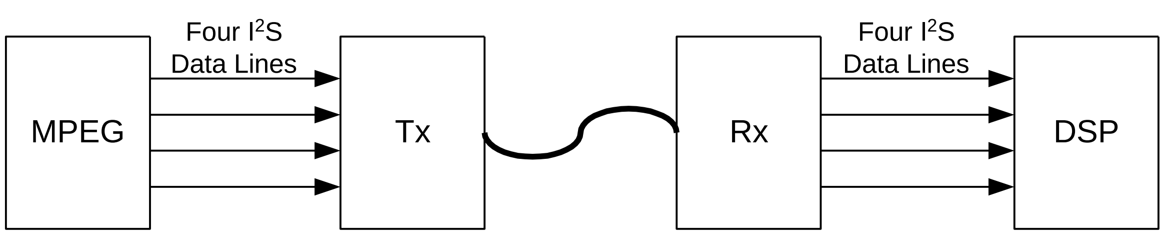


Figure 3.3: High Speed Data Transmission

The high-bitrate audio stream is originally encoded as a single stream. To send it over four I^2S lines, the DVD decoder needs to split this single stream into four streams. Because the single stream of data is being sent over four lines, the programmable ACR (Audio Clock Regeneration) rate is now four times the 96-kHz (384-kHz) or four times the 192-kHz (768-kHz) sample rate.

Figure 3.4 shows the high-bitrate stream before it has been split into four I^2S lines, and after it has been reassembled.

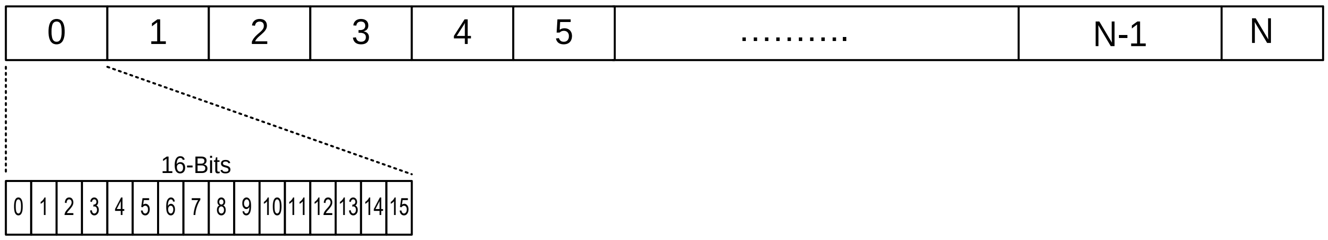


Figure 3.4: High-Bitrate Stream Before and After Reassembly and Splitting

Figure 3.5 shows the same high-bitrate audio stream after being split into four I^2S lines:

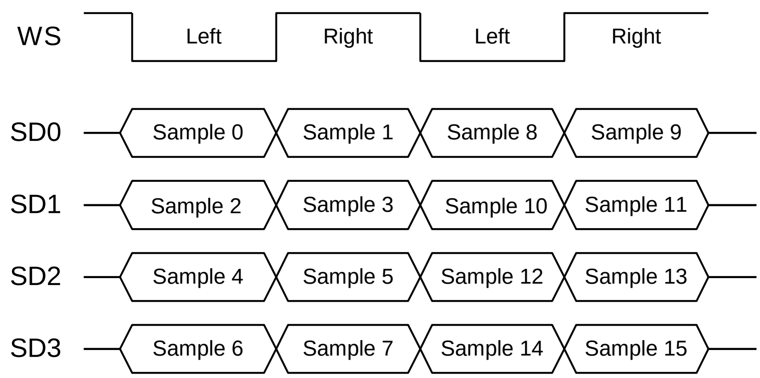


Figure 3.5. High-Bitrate Stream After Splitting

Table 3.6. Maximum Audio Sampling Frequency for All Video Format Timings

Description	Format Timing	Pixel Repetition	Vertical Freq. (Hz)	Max fs 8 ch (kHz)			Max fs 2 ch (kHz)
				4:2:2 and 4:4:4 24-bit	4:4:4 Deep Color (depth in bits)		
60 Hz Formats				**Standard**	**10**	**12**	
VGA	640x480p	none	59.94/60	48	48	48	192
480i	1440x480i	2	59.94/60	48	48	48	192
480i	2880x480i	4	59.94/60	192	192	192	192
240p	1440x240p	2	59.94/60	48	48	48	192
240p	2880x240p	4	59.94/60	192	192	192	192
480p	720x480p	none	59.94/60	48	48	48	192
480p	1440x480p	2	59.94/60	96	96	96	192
480p	2880x480p	4	59.94/60	192	192	192	192
720p	1280x720p	none	59.94/60	192	192	192	192
1080i	1920x1080i	none	59.94/60	192	192	192	192
1080p	1920x1080p	none	59.94/60	192	192	192	192
50 Hz Formats				**Standard**	**10**	**12**	
576i	1440x576i	2	50	48	48	48	192
576i	2880x576i	4	50	192	192	192	192
288p	1440x288p	2	50	48	48	48	192
288p	2880x288p	4	50	192	192	192	192
576p	720x576p	none	50	48	48	48	192
576p	1440x576p	2	50	96	96	96	192
576p	2880x576p	4	50	192	192	192	192
720p/50	1280x720p	none	50	192	192	192	192
1080i/50	1920x1080i	none	50	192	192	192	192
1080p/50	1920x1080p	none	50	192	192	192	192
1080p @ 24-30 Hz				**Standard**	**10**	**12**	
1080p	1920x1080p	none	24	192	192	192	192
1080p	1920x1080p	none	25	192	192	192	192
1080p	1920x1080p	none	29.97/30	192	192	192	192

3.4.5. Auto Audio Configuration

The SiI9233 receiver can control the audio output based on the current states of CablePlug, FIFO, Video, ECC, ACR, PLL, InfoFrame, and HDMI. Audio output is enabled only when all necessary conditions are met. If any critical condition is missing, then the audio output is disabled automatically.

3.4.6. Soft Mute

On command from a register bit or when automatically triggered with Automatic Audio Control (AAC), the SiI9233 receiver progressively reduces the audio data amplitude to mute the sound in a controlled manner. This feature is useful when there is an interruption to the HDMI audio stream (or an error) to prevent any audio pop from being sent to the I^2S or S/PDIF outputs.

3.5. Control and Configuration

3.5.1. Register/Configuration Logic

The register/configuration logic block incorporates all the registers required for configuring and managing the features of the SiI9233 HDMI Receiver. These registers are used to perform HDCP authentication, audio/video/auxiliary format processing, CEA-861B InfoFrame Packet format, and power-down control.

The registers are accessible from one of two serial ports. The first port is the DDC port, which is connected through the HDMI cable to the HDMI host. It is used to control the SiI9233 receiver from the host device for HDCP operation. The second port is the local I^{2}C port, which is used to control the SiI9233 receiver from the display device. This is shown in Figure 3.6. The Local Bus accesses the General Registers and the Common Registers. The DDC Bus accesses the HDCP Operation registers and the Common Registers.

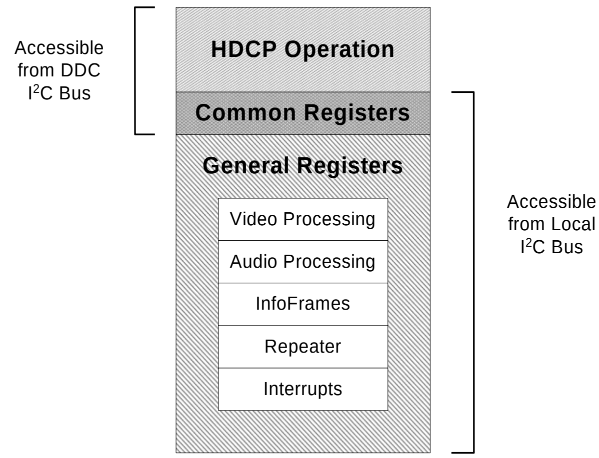


Figure 3.6. I^{2}C Register Domains

3.5.2. I^{2}C Serial Ports

The SiI9233 provides 5 I^{2}C serial interfaces: 4 DDC ports to communicate back to the HDMI or DVI hosts; one I^{2}C port for initialization and control by a local microcontroller in the display. Each interface is 5-V tolerant.

3.5.2.1. E-DDC Bus Interface to HDMI Host

The four DDC interfaces (DSDA0-3 and DSCL0-3) on the SiI9233 receiver are slave interfaces that can run up to 100 kHz. Each interface is connected to one E-DDC bus and is used for reading the integrated EDID in addition to HDCP authentication.

The SiISiI9233 receiver is accessible on the E-DDC bus at device addresses 0xA0 for the EDID, and 0x74 for HDCP control. This feature is compliant with the HDCP 1.1 Specification.

3.5.3. EDID FLASH and RAM Block

The EDID block consists of 1024 bytes of RAM. Each port has a block of 256 bytes of RAM for EDID data. This feature allows simultaneous reads of all ports from four different source devices that are connected to the SiI9233 receiver. In addition to the RAM, the EDID block contains 256 bytes of FLASH that is shared by all ports. As a result, the timing information must be identical among all the ports if the internal EDID is used. An additional area of FLASH contains unique CEC physical address and checksum values for each of the four ports. This feature allows simultaneous reads of all ports from four different source devices if they are connected and attempt an EDID read at the same time. If independent EDIDs are required on any of the ports, a CPU can externally load the 256 bytes of RAM for that port, by using the local I^{2}C bus.

The internal EDID can be selected on a per-port basis using registers on the local I^{2}C bus. For example, Port 0 and Port 1 can use the internal EDID, and Port 2 and Port 3 can use a discrete EEPROM for the EDID.

3.5.4. CEC Interface

The Consumer Electronics Control (CEC) Interface block provides CEC electrically compliant signals between CEC devices and a CEC master. It allows products to meet the electrical specifications of CEC signaling by translating the LVTTL signals of an external microcontroller (CEC host-side or Tx-side) to CEC signaling levels for CEC devices at the Rx-side, and vice versa.

Additionally, a CEC controller compatible with the Lattice Semiconductor CEC Programming Interface (CPI) is included on-chip. This CEC controller has a high-level register interface accessible through the I^{2}C interface which can be used to send and receive CEC commands. This controller makes CEC control very easy and straightforward, and removes the burden of having a host CPU perform these low-level transactions on the CEC bus.

3.5.4.1. **I^2C Interface to Display Controller**

The Controller I^2C interface (CSDA, CSCL) on the SiI9233 receiver is a slave interface capable of running up to 400 kHz. This bus is used to configure the SiI9233 by reading/writing to the appropriate registers. The SiI9233 receiver is accessible on the local I^2C bus at two device addresses. Refer to the *SiI9223/9233/9127 HDMI Receivers Programmer's Reference* (SiI-PR-1019) for more information.

3.5.5. Standby and HDMI Port Power Supplies

The SiI9233 receiver incorporates a 5-volt standby power supply pin (SBVCC5) that can be used to supply power to the EDID and CEC portions of the device when all other power supplies are turned off. This results in an extremely low power mode, but allows the EDID to be readable, and the CEC controller to be functional in this low power standby mode. No damage will occur to the device when in this mode.

If all power is off for the device, such as the TV being unplugged from the AC electrical outlet, the EDID can still be read from the source by using power from the HDMI connector +5V signal. In this case, an internal power MUX will automatically switch to the HDMI connector power to use for powering the EDID logic. In this mode, only the EDID block is functional, with all other functions of the device in power off mode. No damage will occur to the device in this mode.

4. Electrical Specifications

4.1. Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
IOVCC33	I/O Pin Supply Voltage	–0.3	—	4.0	V	1, 2, 3
AVCC12	TMDS Analog Supply Voltage	–0.3	—	1.9	V	1, 2
AVCC33	TMDS Analog Supply Voltage	–0.3	—	4.0	V	1, 2
APVCC12	Audio PLL Supply Voltage	–0.3	—	1.9	V	1, 2
CVCC12	Digital Core Supply Voltage	–0.3	—	1.9	V	1, 2
XTALVCC33	ACR PLL Crystal Oscillator Supply Voltage	–0.3	—	4.0	V	1, 2
SBVCC5	Standby Supply Voltage	–0.3	—	5.7	V	1,2
V_I	Input Voltage	–0.3	—	IOVCC33 + 0.3	V	1, 2
$V_{5V\text{-}Tolerant}$	Input Voltage on 5-V tolerant Pins	–0.3	—	5.5	V	5
T_J	Junction Temperature	—	—	125	°C	—
T_{STG}	Storage Temperature	–65	—	150	°C	—

Notes:

1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions.
3. Voltage undershoot or overshoot cannot exceed absolute maximum conditions.
4. Refer to the SiI9233 Qualification Report for information on ESD performance.
5. All VCCs must be powered to the device. If the device is unpowered and 5V is applied to these inputs, damage can occur.

4.2. Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
IOVCC33	I/O Pin Supply Voltage	3.13	3.3	3.47	V	1, 4
AVCC12	TMDS Analog Supply Voltage	1.14	1.2	1.26	V	1, 6
AVCC33	TMDS Analog Supply Voltage	3.13	3.3	3.47	V	3
APVCC12	Audio PLL Supply Voltage	1.14	1.2	1.26	—	—
CVCC12	Digital Core Supply Voltage	1.14	1.2	1.26	V	2
XTALVCC33	ACR PLL Crystal Oscillator Supply Voltage	3.13	3.3	3.47	V	4
SBVCC5	Standby Supply Voltage	4.75	5.0	5.25	V	—
RxPWR5V	DDC I^2C I/O Reference Voltage	4.75	5.00	5.25	V	—
DIFF33	Difference between two 3.3-V Power Pins	—	—	1.0	V	4
DIFF12	Difference between two 1.2-V Power Pins	—	—	1.0	V	4
DIFF3312	Difference between any 3.3-V and 1.2-V Pin	–1.0		2.6	V	4, 5
V_{CCN}	Supply Voltage Noise	—	—	100	mV_{P-P}	7
T_A	Ambient Temperature (with power applied)	0	25	70	°C	—
Θ_{ja}	Ambient Thermal Resistance (Theta JA)	—	—	27	°C/W	—

Notes:

1. IOVCC33 and AVCC33 pins should be controlled from one power source.
2. CVCC12 should be controlled from one power source.
3. AVCC12 pin should be regulated.
4. Power supply sequencing must guarantee that power pins stay within these limits of each other. See Figure 4.4.
5. No 1.2 V pin can be more than DIFF3312[min] higher than any 3.3 V pin. No 3.3 V pin can be more than DIFF3312[max] higher than any 1.2 V pin.
6. The HDMI 1.0 Specification requires termination voltage (AVCC33) to be controlled to 3.3 V ±5%. The SiI9233 tolerates a wider range of ±300 mV.
7. The supply voltage noise is measured at test point VCCTP in Figure 5.2 on page 42. The ferrite bead provides filtering of power supply noise. The figure is representative and applies to other VCC pins as well.
8. Airflow at 0 m/s.
9. The schematics on page 70 show decoupling and power supply regulation.

4.3. DC Specifications

4.3.1. Digital I/O Specifications

Symbol	Parameter	Pin Type[3]	Conditions[2]	Min	Typ	Max	Units	Note
V_{IH}	High-level Input Voltage	LVTTL	—	2.0	—	—	V	—
V_{IL}	Low-level Input Voltage	LVTTL	—		—	0.8	V	—
V_{TH+}	Low to HIGH Threshold RESET # Pin	Schmitt	—	1.46	—	—	V	5
V_{TH-}	HIGH to Low Threshold RESET# Pin	Schmitt	—	—	—	0.96	V	5
DDC V_{TH+}	Low to HIGH Threshold DSDA0, DSDA1, DSCL0 and DSCL1 pins.	Schmitt	—	3.0	—		V	—
DDC V_{TH-}	HIGH to Low Threshold DSDA0, DSDA1, DSCL0 and DSCL1 pins.	Schmitt	—	—	—	1.5	V	—
Local I^2C V_{TH+}	Low to HIGH Threshold CSCL and CSDA pins	Schmitt	—	2.1	—	—	V	11, 13
Local I^2C V_{TH-}	HIGH to Low Threshold CSCL and CSDA pins	Schmitt	—	—	—	0.86	V	11, 13
V_{OH}	High-level Output Voltage	LVTTL	—	2.4	—		V	10
V_{OL}	Low-level Output Voltage	LVTTL	—	—	—	0.4	V	10
I_{OL}	Output Leakage Current	—	High Impedance	–10	—	10	μA	—
V_{ID}	Differential Input Voltage	—	—	75	250	780	mV	4
I_{OD4}	4mA Digital Output Drive	Output	V_{OUT} = 2.4 V	4	—	—	mA	1, 6, 7
			V_{OUT} = 0.4 V	4	—	—	mA	1, 6, 7
I_{OD8}	8mA Digital Output Drive	Output	V_{OUT} = 2.4 V	8	—	—	mA	1, 6, 8
			V_{OUT} = 0.4 V	8	—	—	mA	1, 6, 8
I_{OD12}	12mA Digital Output Drive	Output	V_{OUT} = 2.4 V	12	—	—	mA	1, 6, 9
			V_{OUT} = 0.4 V	12	—	—	mA	1, 6, 9
R_{PD}	Internal Pull Down Resistor	Outputs	IOVCC33=3.3 V	25	50	110	kΩ	1, 12
I_{OPD}	Output Pull Down Current	Outputs	IOVCC33=3.6 V	—	60	90	μA	1, 12
I_{IPD}	Input Pull Down Current	Input	IOVCC33=3.6 V	—	60	90	μA	1

Notes:

1. These limits are guaranteed by design.
2. Under normal operating conditions unless otherwise specified, including output pin loading C_L = 10 pF.
3. Refer to *Pin Descriptions* (beginning on page 21) for pin type designations for all package pins.
4. Differential input voltage is a single-ended measurement, according to DVI Specification.
5. Schmitt trigger input pin thresholds V_{TH+} and V_{TH-} correspond to V_{IH} and V_{IL}, respectively.
6. Minimum output drive specified at ambient = 70 °C and IOVCC33 = 3.0 V. Typical output drive specified at ambient = 25 °C and IOVCC33 = 3.3 V. Maximum output drive specified at ambient = 0 °C and IOVCC33 = 3.6 V.
7. I_{OD4} Output applies to pins SPDIF, SCK, WS, SD[3:0], DCLK, INT, and CSDA.
8. I_{OD8} Output applies to pins DE, HSYNC, VSYNC, Q[35:0].and MCLK.
9. I_{OD12} Output applies to pin ODCK.
10. Note that the SPDIF output drives LVTTL levels, not the low-swing levels defined by IEC958.
11. The SCL and SDA pins are not true open-drain buffers. When no VCC is applied to the chip, these pins can continue to draw a small current, and prevent the master IC from communicating with other devices on the I^2C bus. Therefore, do not power-down the SiI9233 (remove VCC) unless the attached I^2C bus is completely idle.
12. The chip includes an internal pull-down resistor on many of the output pins. When tri-stated, these pins draw a pull down current according to this specification when the signal is driven HIGH by another source device.
13. With –10% IOVCC33 supply, the HIGH-to-LOW threshold on DDC and I^2C bus is marginal. A –5% tolerance on the IOVCC33 power supply is recommended.

4.3.2. DC Power Supply Pin Specifications

4.3.2.1. Total Power versus Power-Down Modes

				Typ[3]			Max[4]				
Symbol	**Parameter**	**Mode**	**Frequency**	**3.3V**	**1.2V**	**SBVCC5**	**3.3V**	**1.2V**	**SBVCC5**	**Units**	**Notes**
I_{PDQ3}	Complete Power-Down Current	A	X				4	0	—	mA	1, 6
I_{PDS}	Sleep Power-down Current	B	27 MHz				5	4	5	mA	2, 7
			74.25 MHz				6	4	5	mA	
			150 MHz				4	4	5	mA	
			225 MHz				7	5	5	mA	
I_{STBY}	Standby Current	C	27 MHz				0	0	5	mA	2, 8
			74.25 MHz				0	0	5	mA	
			150 MHz				0	0	5	mA	
			225 MHz				0	0	5	mA	
I_{UNS}	Unselected Current	D	27 MHz	15	25	5	19	33	5	mA	2, 8
			74.25 MHz	17	27	5	21	34	5	mA	
			150 MHz	16	28	5	18	36	5	mA	
			225 MHz	18	30	5	23	39	5	mA	
I_{CCTD}	Full Power Digital Out Current	E	27 MHz	81	76	5	105	88	5	mA	2, 10
			74.25 MHz	100	160	5	165	181	5	mA	
			150 MHz	123	279	5	247	337	5	mA	
			225 MHz	139	394	5	316	472	5	mA	

Notes:

1. Power is not related to input TMDS clock (RxC) frequency because the selected TMDS port is powered down.
2. Power is related to input TMDS clock (RxC) frequency at the selected TMDS port. Only one port can be selected.
3. Typical power specifications measured with supplies at typical normal operating conditions; and a video pattern that combines gray scale, checkerboard and text.
4. Maximum power limits measured with supplies at maximum normal operating conditions, minimum normal operating ambient temperature, and a video pattern with single-pixel vertical lines.
5. Registers are always accessible on local I^2C (CSDA/CSCL) without active link clock.
6. Power Down Mode A: Minimum power. Everything is powered off. Host sees no termination of TMDS signals on any of the four TMDS ports. I^2C access is still available.
7. Power Down Mode B: Powers down as in Mode C, but also powers down SCDT logic. CKDT state can be polled in register, but interrupts and the INT output pin are inactive. Host device can sense TMDS termination.
8. Power Down Mode C: Power off to 3.3 V and 1.2 V supplies. Power on to SBVCC5 standby supply.
9. Power Down Mode D: Monitor SCDT on selected TMDS port with outputs tri-stated. HDCP continues in the selected port, but the output of the HDMI Receiver can be connected to a shared bus.
10. Digital Functional Mode E: Full Operation on one port with digital outputs

4.3.2.2. Power-Down Mode Definitions

Mode		3.3V supply	1.2v supply	SBVCC5	Description
A	Power Down	ON	ON	ON	Minimum power. Everything is powered off. Host sees no termination of TMDS signals on any of the four TMDS ports. I^2C access is still available.
B	Sleep Mode Power	ON	ON	ON	Powers down as in Mode C, but also powers down SCDT logic. CKDT state can be polled in register, but interrupts and the INT output pin are inactive. Host device can sense TMDS termination.
C	Standby Power	OFF	OFF	ON	Power off to 3.3 V and 1.2 V supplies. Power on to SBVCC5 standby supply.
D	Unselected Power	ON	ON	ON	Monitor SCDT on selected TMDS port with outputs tri-stated. HDCP continues in the selected port, but the output of the HDMI Receiver can be connected to a shared bus.
E	Digital	ON	ON	ON	Full operation on one port with digital outputs.

Notes:

1. PD Clks include PD_MCLK#, PD_XTAL#, PD_APLL# and PD_PCLK# all set to zero.
2. PD Outs include PD_AO#, and PD_VO# all set to zero.

4.4. AC Specifications

4.4.1. TMDS Input Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{DPS}	Intra-Pair Differential Input Skew	—	—	—	T_{BIT}	ps		2, 4
T_{CCS}	Channel to Channel Differential Input Skew	—	—	—	T_{CIP}	ns	Figure 4.3	2, 3
F_{RXC}	Differential Input Clock Frequency	—	25	—	225	MHz	—	—
T_{RXC}	Differential Input Clock Period	—	4.44	—	40	ns	—	—
T_{IJIT}	Differential Input Clock Jitter tolerance (0.3Tbit)	74.25 MHz	—	—	400	ps	—	2, 5, 6

Notes:

1. Under normal operating conditions unless otherwise specified, including output pin loading of C_L = 10 pF.
2. Guaranteed by design.
3. IDCK Period (refer to the applicable Lattice Semiconductor HDMI Transmitter Data Sheet).
4. 1/10 of IDCK Period (refer to the applicable Lattice Semiconductor HDMI Transmitter Data Sheet).
5. Jitter defined per HDMI Specification.
6. Jitter measured with Clock Recovery Unit per HDMI Specification. Actual jitter tolerance can be higher depending on the frequency of the jitter.

Refer to the *SiI9223/9233/9127 HDMI Receivers Programmer's Reference* (SiI-PR-1019) for more details on controlling timing modes.

4.4.2. Video Output Timings

4.4.2.1. 12/15/18-Bit Data Output Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
D_{LHT}	Low-to-High Rise Time Transition	C_L = 10 pF	—	—	3	ns	Figure 4.6	2
D_{HLT}	High-to-Low Fall Time Transition	C_L = 10 pF	—	—	3	ns	Figure 4.6	2
R_{CIP}	ODCK Cycle Time	C_L = 10 pF	13	—	40	ns	Figure 4.7	8
F_{CIP}	ODCK Frequency	C_L = 10 pF	25	—	82.5	MHz	—	5
T_{DUTY}	ODCK Duty Cycle	C_L = 10 pF	40%	—	60%	R_{CIP}	Figure 4.7	3
T_{CK2OUT}	Clock-to-Output Delay	C_L = 10 pF	0.8	—	3.8	ns	Figure 4.7	—

4.4.2.2. 16/20/24/30/36-Bit Data Output Timings

Symbol	Parameter		Conditions	Min	Typ	Max	Units	Figure	Notes
D_{LHT}	Low-to-High Rise Time Transition		C_L = 10 pF	—	—	3	ns	Figure 4.6	2
D_{HLT}	High-to-Low Fall Time Transition		C_L = 10 pF	—	—	3	ns	Figure 4.6	2
T_{DUTY}	ODCK Duty Cycle		C_L = 10 pF	40%	—	60%	R_{CIP}	Figure 4.7	3
T_{CK2OUT}	ODCK-to-Output Delay		C_L = 10 pF	0.92	—	2.9	ns	Figure 4.7	—
R_{CIP}	Output Clock Cycle Time	SiI9233CTU	C_L = 10 pF	6.06	—	40	ns	Figure 4.7	5, 8
F_{CIP}	Output Clock Frequency	SiI9233CTU	C_L = 10 pF	25	—	165	MHz	Figure 4.7	5

Notes:

1. Under normal operating conditions unless otherwise specified, including output pin loading of C_L=10 pF.
2. Rise time and fall time specifications apply to HSYNC, VSYNC, DE, ODCK, EVNODD and Q[35:0].
3. Output clock duty cycle is independent of the differential input clock duty cycle. Duty cycle is a component of output setup and hold times.
4. See Table 4.2 on page 34 for calculation of worst case output setup and hold times.
5. All output timings are defined at the maximum operating ODCK frequency, F_{CIP}, unless otherwise specified.
6. F_{CIP} can be the same as F_{RXC} or one-half of F_{RXC}, depending on OCLKDIV setting. F_{CIP} can also be F_{RXC} /1.25 or F_{RXC} /1.5 if deep color mode is being transmitted.
7. R_{CIP} is the inverse of F_{CIP} and is not a controlling specification.
8. Output skew specified when ODCK is programmed to divide-by-two mode.

4.4.3. Audio Output Timings

4.4.3.1. I^{2}S Output Port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{tr}	SCK Clock Period (TX)	C_L = 10 pF	1.00	—	—	T_{tr}	Figure 4.8	1
T_{HC}	SCK Clock HIGH Time	C_L = 10 pF	0.35	—	—	T_{tr}		1
T_{LC}	SCK Clock LOW Time	C_L = 10 pF	0.35	—	—	T_{tr}		1
T_{SU}	Setup Time, SCK to SD/WS	C_L = 10 pF	$0.4T_{TR} – 5$	—	—	ns		1
T_{HD}	Hold Time, SCK to SD/WS	C_L = 10 pF	$0.4T_{TR} – 5$	—	—	ns		1
$T_{SCKDUTY}$	SCK Duty Cycle	C_L = 10 pF	40%	—	60%	T_{tr}		1
T_{SCK2SD}	SCK to SD or WS Delay	C_L = 10 pF	–5	—	+5	ns		2
T_{AUDDLY}	Audio Pipeline Delay	—	—	40	80	µs	—	—

Notes:

1. Refer to Figure 4.8. Meets timings in Philips I^{2}S Specification.
2. Applies also to SDC-to-WS delay.

4.4.3.2. S/PDIF Output Port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{SPCYC}	SPDIF Cycle Time	C_L = 10 pF	—	1.0	—	UI	Figure 4.9	1, 2
F_{SPDIF}	SPDIF Frequency	—	4	—	24	MHz		3
T_{SPDUTY}	SPDIF Duty Cycle	C_L = 10 pF	90%	—	110%	UI		2, 5
$T_{MCLKCYC}$	MCLK Cycle Time	C_L = 10 pF	20	—	250	ns	Figure 4.10	1, 2, 4
F_{MCLK}	MCLK Frequency	C_L = 10 pF	4	—	50	MHz		1, 2, 4
$T_{MCLKDUTY}$	MCLK Duty Cycle	C_L = 10 pF	40%	—	60%	$T_{MCLKCYC}$		2, 4
T_{AUDDLY}	Audio Pipeline Delay	—	—	40	80	µs	—	—

Notes:

1. Guaranteed by design.
2. Proportional to unit time (UI), according to sample rate.
3. SPDIF is not a true clock, but is generated from the internal 128Fs clock, for Fs from 128 to 512 kHz.
4. MCLK refers to MCLKOUT.
5. Intrinsic jitter on S/PDIF output can limit its use as an S/PDIF transmitter. The S/PDIF intrinsic jitter is approximately 0.1UI.

4.4.3.3. Audio Crystal Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
F_{XTAL}	External Crystal Freq.	—	—	27	—	MHz	Figure 4.1	1, 2

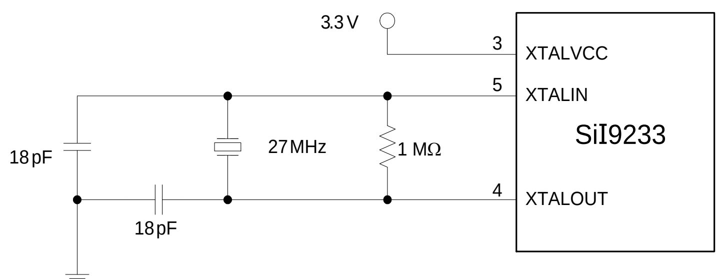


Figure 4.1. Audio Crystal Schematic for the SiI9233 Receiver

Notes:

1. The HDMI Receiver has been fully characterized for optimum audio quality and CEC timing calibration using 27.000 MHz. Use Citizen part number CSA309-27.000MABJ crystal or equivalent. A less expensive, but not fully characterized circuit, can use a TTL level clock source.
2. The XTALIN/XTALOUT pin pair must be driven with a clock in all applications.

4.4.4. Miscellaneous Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{I2CDVD}	SDA Data Valid delay from SCL falling edge	C_L = 400 pF	—	—	700	ns	—	—
F_{DDC}	Speed on TMDS DDC Ports	C_L = 400 pF	—	—	100	kHz	—	2
F_{I^2C}	Speed on Local I^2C Port	C_L = 400 pF	—	—	400	kHz	—	3
T_{RESET}	RESET# Signal Low Time for valid reset	—	50	—	—	µs	Figure 4.5	—
$T_{STARTUP}$	Startup time from power supplies valid	—	—	—	100	ms	—	5
$T_{BKSVINIT}$	HDCP BKSV Load Time	—	—	—	2.2	ms	—	4

Notes:

1. Under normal operating conditions unless otherwise specified, including output pin loading of C_L = 10 pF.
2. DDC ports are limited to 100 kHz by the HDMI Specification, and meet I^2C standard mode timings.
3. Local I^2C port (CSCL/CSDA) meets standard mode I^2C timing requirements to 400 kHz.
4. The time required to load the KSV values internal to the HDMI Receiver after a RESET# and the start of an active TMDS clock. An attached HDCP host device should not attempt to read the HDMI receiver BKSV values until after this time. The $T_{BKSVINIT}$ Min and Max values are based on the maximum and minimum allowable XCLK frequencies. The loading of the BKSV values requires a valid XCLK and TMDS clock.
5. $T_{STARTUP}$ is the startup time required for the device to be operational once power is stable. This startup time is due to the on board voltage regulator for the EDID and CEC and a power on reset circuit.

4.4.5. Interrupt Timings

4.4.5.1. Interrupt Output Pin Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{FSC}	Link disabled (DE inactive) to SCDT LOW	—	—	0.15	40	ms	Figure 4.2	1, 2, 3, 8
T_{HSC}	Link enabled (DE active) to SCDT HIGH	—	—	—	4	DE	Figure 4.2	1, 2, 4, 8
T_{CICD}	RXC inactive to CKDT LOW	—	—	—	100	µs	Figure 4.2	1, 2, 8
T_{CACD}	RXC active to CKDT HIGH	—	—	—	10	µs	Figure 4.2	1, 2, 8
T_{INT}	Response Time for INT from Input Change	—	—	—	100	µs	—	1, 5, 8
T_{CIOD}	RXC inactive to ODCK inactive	—	—	—	100	ns	—	1, 8
T_{CAOD}	RXC active to ODCK active and stable	—	—	—	10	ms	—	1, 6, 8
T_{SRRF}	Delay from SCDT rising edge to Software Reset falling edge	—	—	—	100	ms	Figure 4.5	7

Notes:

1. Guaranteed by design.
2. SCDT and CKDT are register bits in this device.
3. SCDT changes to LOW after DE is HIGH for approximately 4096 pixel clock cycles, or after DE is LOW for approximately 1,000,000 clock cycles. At 27 MHz pixel clock, this delay for DE HIGH is approximately 150 µs, and the delay for DE LOW is approximately 40 ms.
4. SCDT changes to HIGH when clock is active (T_{CACD}) and at least 4 DE edges have been recognized. At 720p, the DE period is 22 µs, so SCDT responds approximately 50 µs after T_{CACD}.
5. The INT pin changes state after a change in input condition when the corresponding interrupt is enabled.
6. Output clock (ODCK) becomes active before it becomes stable. Use the SCDT signal as the indicator of stable video output timings, as this depends on decoding of DE signals with active RXC (see T_{FSC}).
7. Software Reset must be asserted and then de-asserted within the specified maximum time after rising edge of Sync Detect (SCDT). Access to both SWRST and SCDT can be limited by the speed of the I^2C connection.
8. SCDT is HIGH only when CKDT is also HIGH. When the HDMI Receiver is in a powered-down mode, the INT output pin indicates the current state of SCDT. Thus, a power-down HDMI Receiver signals a micro connected to the INT pin whenever SCDT changes from LOW to HIGH or HIGH to LOW.

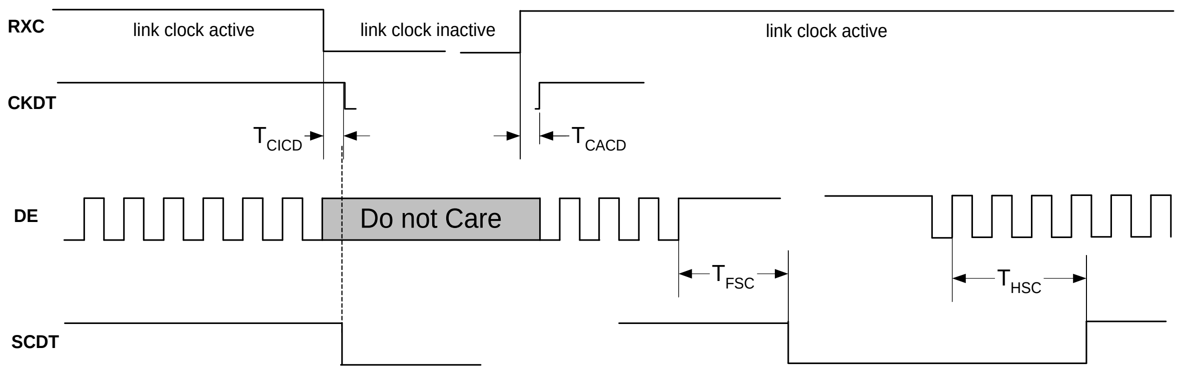


Figure 4.2. SCDT and CKDT Timing from DE or RXC Inactive/Active

Notes:

1. The SCDT shown in Figure 4.2 is a register bit. SCDT remains HIGH if DE is stuck in LOW while RXC remains active, but SCDT changes to LOW if DE is stuck HIGH while RXC remains active.
2. The CKDT shown in Figure 4.2 is a register bit. CKDT changes to LOW whenever RXC stops, and changes to HIGH when RXC starts. SCDT changes to LOW when CKDT changes to LOW.
3. SCDT changes to LOW when CKDT changes to LOW. SCDT changes to HIGH at T_{HSC} after CKDT changes to HIGH.
4. The INT output pin changes state after the SCDT or CKDT register bit is set or cleared if those interrupts are enabled.

Refer to the *SiI9223/9233/9127 HDMI Receivers Programmer's Reference* (SiI-PR-1019) for more details on controlling timing modes.

4.5. Timing Diagrams

4.5.1. TMDS Input Timing Diagrams

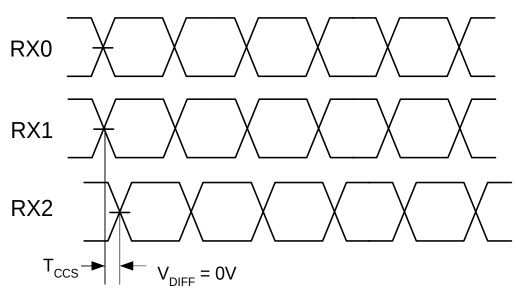


Figure 4.3. TMDS Channel-to-Channel Skew Timing

4.5.2. Power Supply Control Timings

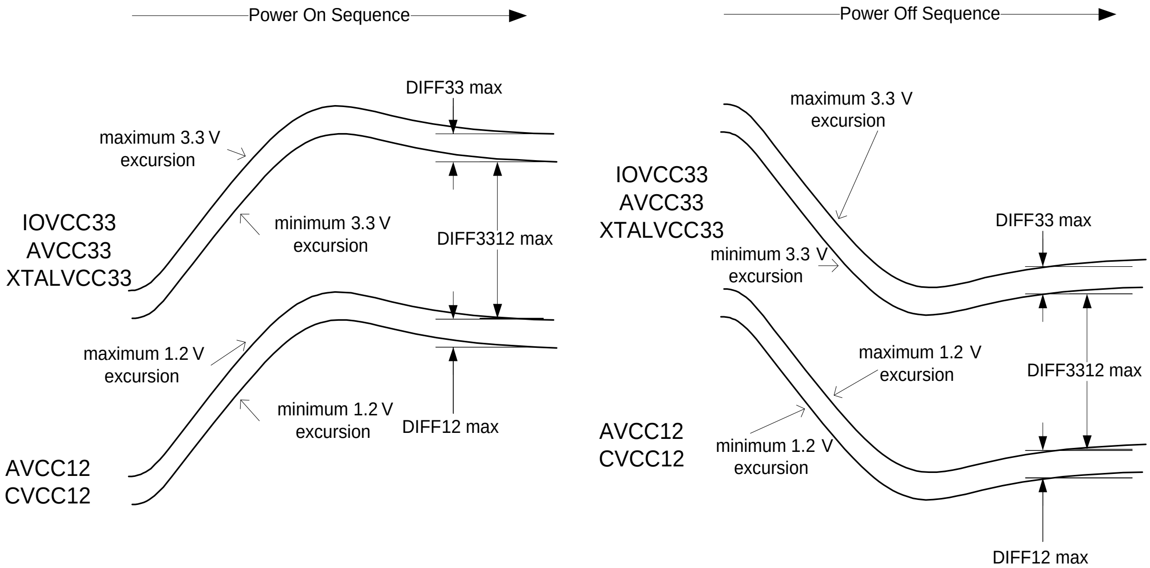
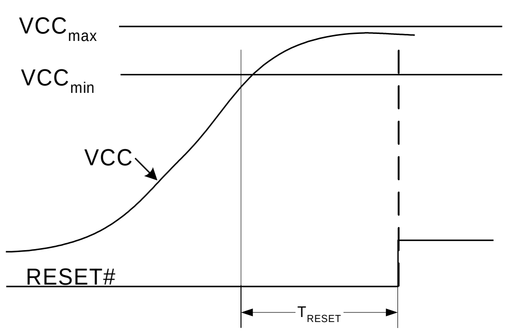
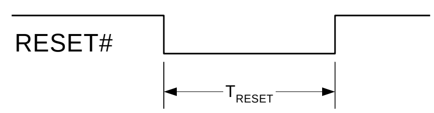


Figure 4.4. Power Supply Sequencing

4.5.3. Reset Timings



Note that VCC must be stable between its limits for Normal Operating Conditions for T_{RESET} before RESET# is HIGH.



RESET# must be pulled LOW for T_{RESET} before accessing registers. This can be done by holding RESET# LOW until T_{RESET} after stable power (at left); OR by pulling RESET# LOW from a HIGH state (at right) for at least T_{RESET}.

Figure 4.5. RESET# Minimum Timings

4.5.4. Digital Video Output Timing Diagrams

4.5.4.1. Output Transition Times

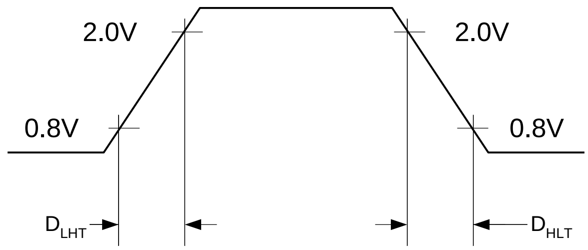


Figure 4.6. Video Digital Output Transition Times

4.5.4.2. Output Clock to Output Data Delay

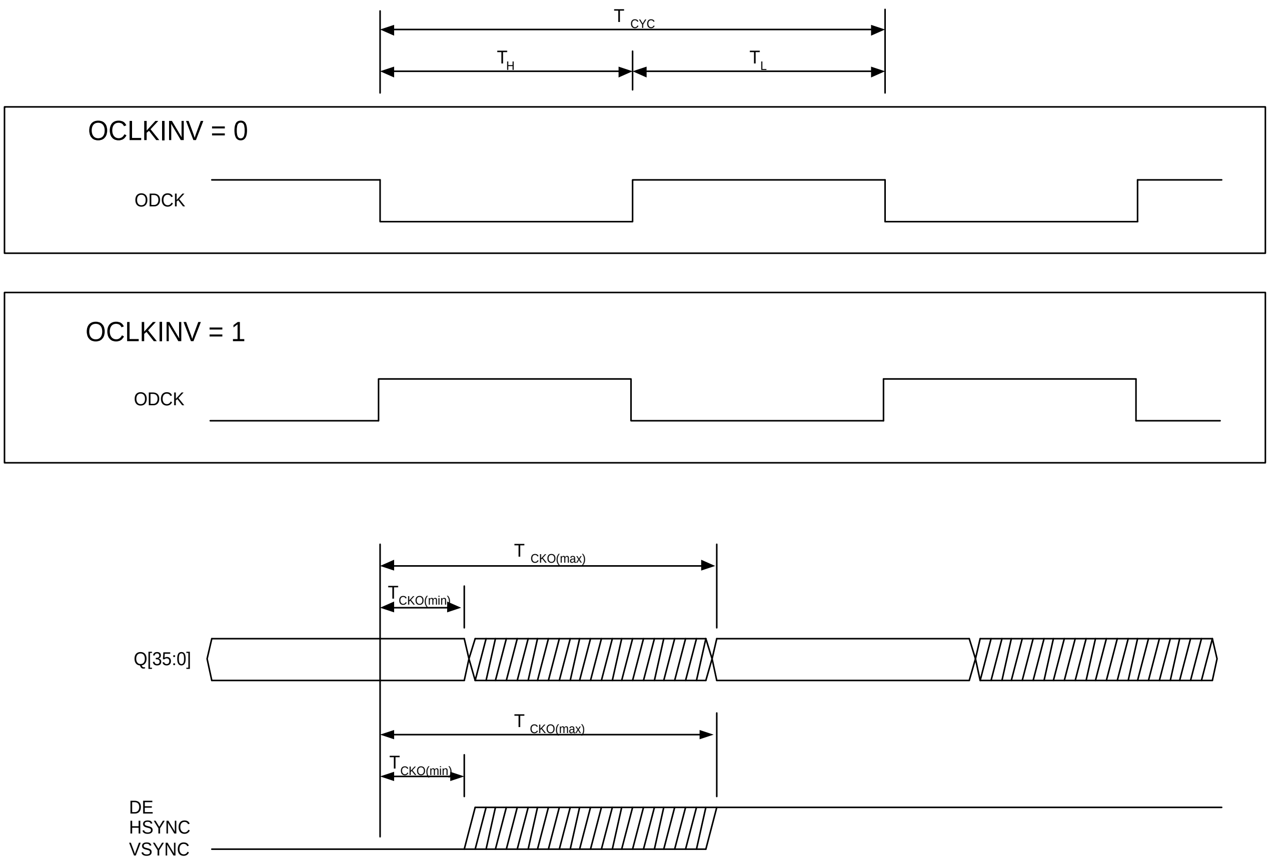


Figure 4.7. Receiver Clock-to-Output Delay and Duty Cycle Limits

4.5.5. Digital Audio Output Timings

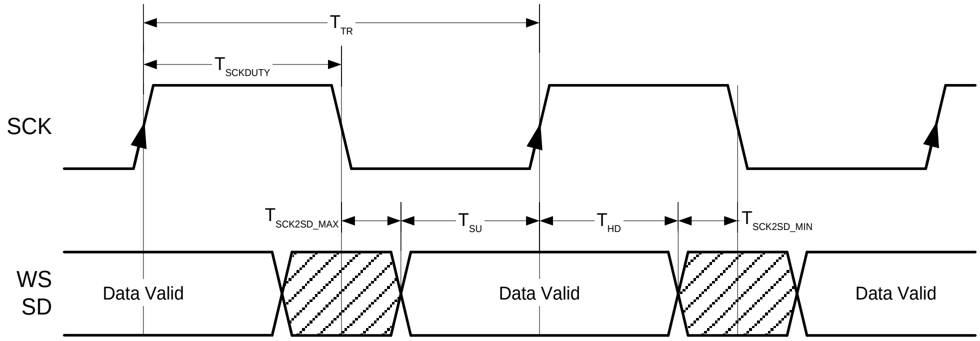


Figure 4.8. I²S Output Timings

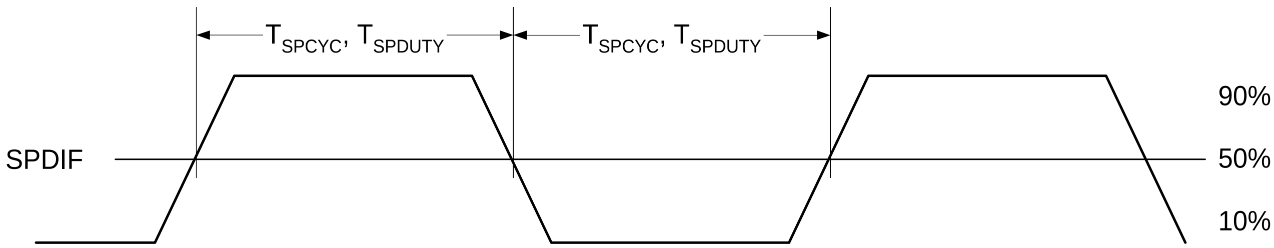


Figure 4.9. S/PDIF Output Timings

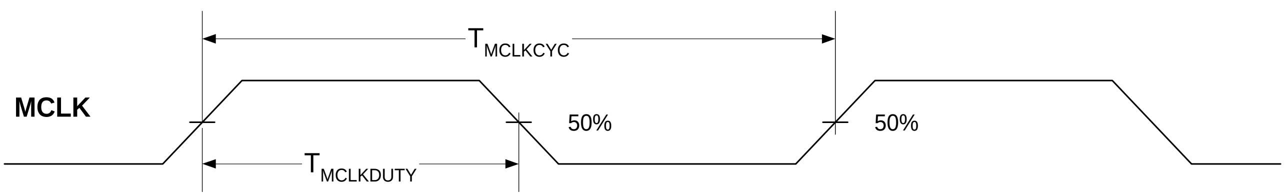


Figure 4.10. MCLK Timings

4.6. Calculating Setup and Hold Times for Video Bus

4.6.1. 24/30/36-Bit Mode

Output data is clocked out on one rising (or falling) edge of ODCK, and is then captured downstream using the same polarity ODCK edge one clock period later. The setup time of data to ODCK and hold time of ODCK to data are therefore a function of the worst case ODCK to output delay, as shown in Figure 4.11. The active rising ODCK edge is shown with an arrowhead. For OCK_INV=1, reverse the logic.

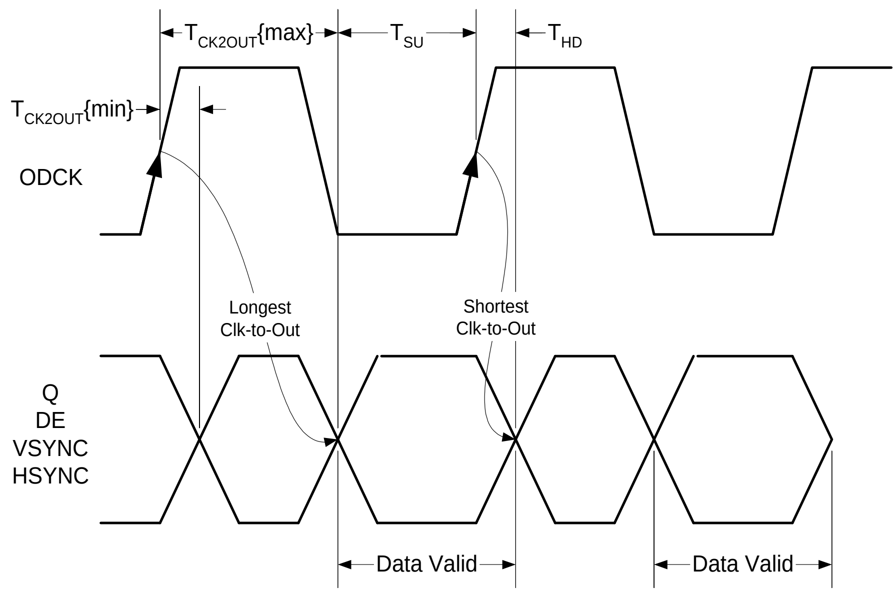


Figure 4.11. 24/30/36-Bit Mode Receiver Output Setup and Hold Times

Table 4.1 shows minimum calculated setup and hold times for commonly used ODCK frequencies. The setup and hold times apply to DE, VSYNC, HSYNC and Data output pins, with output load of 10pF. These are approximations. Hold time is not related to ODCK frequency.

Table 4.1. Calculation of 24/30/36-Bit Output Setup and Hold Times

	Symbol	Parameter	T_{ODCK}		Min
24/30/36-Bit Mode	T_{SU}	Setup Time to ODCK = T_{ODCK}-T_{CK2OUT}{max}	27 MHz	37.0 ns	33.2 ns
			74.25 MHz	13.5 ns	9.7 ns
	T_{HD}	Hold Time from ODCK = T_{CK2OUT}{min}	27 MHz	37.0 ns	0.8 ns

4.6.2. 12/15/18-Bit Dual-Edge Mode

Output data is clocked out on each edge of ODCK (both rising and falling), and is then captured downstream using the opposite ODCK edge. The setup time of data to ODCK is a function of the shortest duty cycle and the longest ODCK to output delay. The hold time does not depend on duty cycle (since every edge is used), and is a function only of the shortest ODCK to output delay.

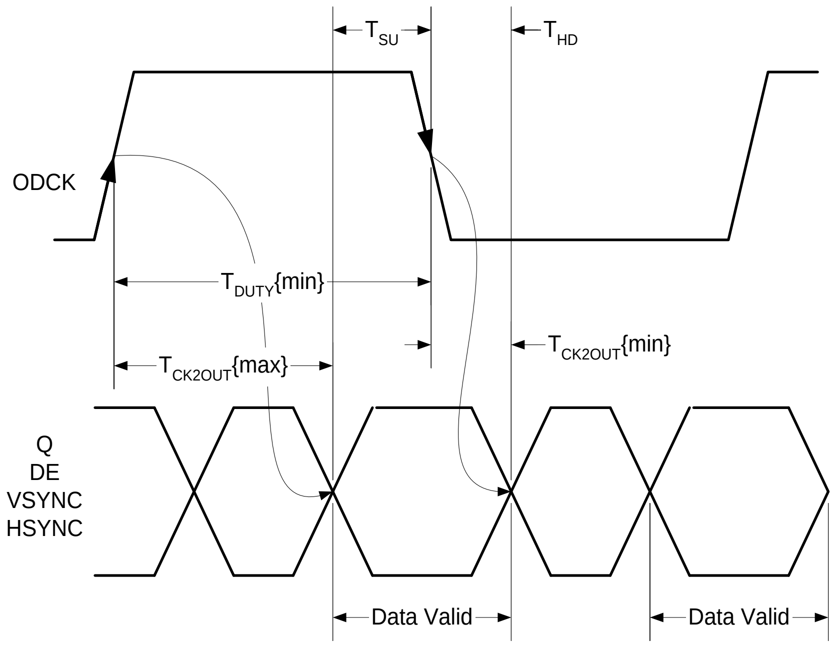


Figure 4.12. 12/15/18-Bit Mode Receiver Output Setup and Hold Times

Table 4.2 shows minimum calculated setup and hold times for commonly used ODCK frequencies, up to the maximum allowed for 12/15/18-bit mode. The setup and hold times apply to DE, VSYNC, HSYNC and Data output pins, with output load of 10 pF. These are approximations. Hold time is not related to ODCK frequency.

Table 4.2. Calculation of 12/15/18-Bit Output Setup and Hold Times

	Symbol	Parameter	T_{ODCK}		Min
12/15/18-Bit Mode	T_{SU}	Setup Time to ODCK $=T_{ODCK}\bullet T_{DUTY}\{min\}-T_{CK2OUT}\{max\}$	27 MHz	37.0 ns	34.1 ns
			74.25 MHz	13.5 ns	10.6 ns
	T_{HD}	Hold Time from ODCK = $T_{CK2OUT}\{min\}$	27 MHz	37.0 ns	0.8ns

4.7. Calculating Setup and Hold Times for I²S Audio Bus

Valid serial data is available at T_{sck2sd} after the falling edge of the first SCK cycle, and then captured downstream using the active rising edge of SCK one clock period later. The setup time of data to SCK (T_{SU}) and hold time of SCK to data (T_{HD}) are therefore a function of the worst case SCK-to-output data delay (Tsck2sd). Figure 4.8 illustrates this timing relationship. Note that the active SCK edge (rising edge) is shown with an arrowhead. For a falling edge sampling clock, the logic is reversed.

Table 4.3 shows the setup and hold time calculation examples for various audio sample frequencies. The formula used in these examples also applies when calculating the setup and hold times for other audio sampling frequencies.

Table 4.3. I²S Setup and Hold Time Calculations

Symbol	Parameter	FWS (kHz)	FSCLK (MHz)	Ttr	Min
T_{SU}	Setup Time, SCK to SD/WS $= T_{TR} – (T_{SCKDUTY\_WORST} + T_{SCK2SD\_MAX})$ $= T_{TR} – (0.6T_{TR} + 5ns)$ $= 0.4T_{TR} – 5ns$	32 kHz	2.048	488 ns	190 ns
		44.1 kHz	2.822	354 ns	136 ns
		48 kHz	3.072	326 ns	125 ns
		96 kHz	6.144	163 ns	60 ns
		192 kHz	12.288	81 ns	27 ns
T_{HD}	Hold Time, SCK to SD/WS $= (T_{SCKDUTY\_WORST} - T_{SCK2SD\_MIN})$ $= 0.4T_{TR} – 5ns$	32 kHz	2.048	488 ns	190 ns
		44.1 kHz	2.822	354 ns	136 ns
		48 kHz	3.072	326 ns	125 ns
		96 kHz	6.144	163 ns	60 ns
		192 kHz	12.288	81 ns	27 ns

Note: The sample calculations shown are based on WS=64 SCLK rising edges.

5. Pin Diagram and Descriptions

Figure 5.1 shows the pin connections for the SiI9233 in the 144-pin TQFP package. Individual pin functions are described beginning on page 36.

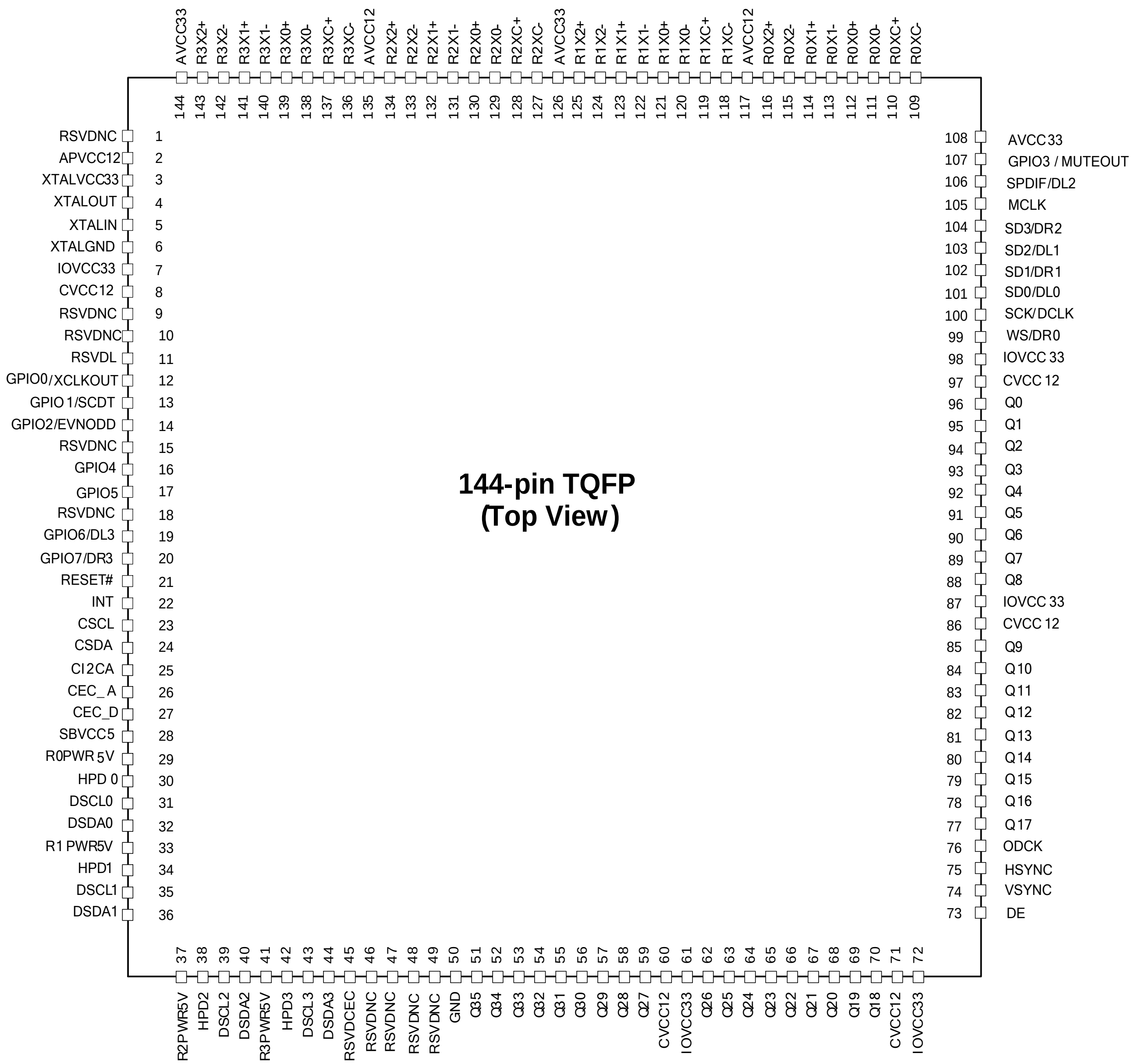


Figure 5.1. Pin Diagram

5.1. Pin Descriptions

5.1.1. Digital Video Output Pins

Pin Name	Pin #	Strength	Type	Dir	Description
Q0	96	Programmable	LVTTL	Output	36-Bit Output Pixel Data Bus. The Q[35:0] bus is highly configurable using the various video configuration registers. It supports a wide array of output formats, including multiple RGB and YCbCr bus formats. Using the appropriate bits in the PD_SYS2 register, the output drivers can be put into a high impedance (tri-state) mode. A weak, internal pull-down device brings each output to ground.
Q1	95				
Q2	94				
Q3	93				
Q4	92				
Q5	91				
Q6	90				
Q7	89				
Q8	88				
Q9	85				
Q10	84				
Q11	83				
Q12	82				
Q13	81				
Q14	80				
Q15	79				
Q16	78				
Q17	77				
Q18	70				
Q19	69				
Q20	68				
Q21	67				
Q22	66				
Q23	65				
Q24	64				
Q25	63				
Q26	62				
Q27	59				
Q28	58				
Q29	57				
Q30	56				
Q31	55				
Q32	54				
Q33	53				
Q34	52				
Q35	51				
DE	73	Programmable	LVTTL	Output	Data Enable.
HSYNC	75	Programmable	LVTTL	Output	Horizontal Sync Output
VSYNC	74	Programmable	LVTTL	Output	Vertical Sync Output
GPIO2 / EVNODD	14	8 mA	LVTTL	Bi-Di	Programmable GPIO2 or Indicates Even or Odd Field for Interlaced Formats.
ODCK	76	Programmable	LVTTL	Output	Output Data Clock.

Notes:

1. HSYNC and VSYNC outputs carry sync signals for both embedded and separate sync configurations.

2. When transporting video data that uses fewer than 36 bits, the unused bits on the Q[] bus can still carry switching pixel data signals. Unused Q[35:0] bus pins should be unconnected, masked or ignored by downstream devices. For example, carrying YCbCr 4:2:2 data with 16-bit width (see page 51), the bits Q[0] through Q[7] output switching signals.
3. The output data bus, Q0 to Q35, can be wire-ORed to another device such that one device is always tri-stated. However, the Q0-Q35 pins do not have bus hold internal pull-up or pull-down resistors, and so cannot pull the bus HIGH or LOW when all connected devices are tri-stated.
4. The drive strength of these pins can be programmed in 2-mA steps between 2 mA and 14 mA: Q[0:35], DE, HSYNC, VSYNC, and ODCK.

5.1.2. Digital Audio Output Pins

Pin Name	Pin #	Strength	Type	Dir	Description
XTALIN	5	—	5-V tolerant LVTTL	In	Crystal Clock Input. Also allows LVTTL input. Frequency required: 26-28.5 MHz
XTALOUT	4	4 mA	LVTTL	Out	Crystal Clock Output
GPIO0 / XCLKOUT	12	4 mA	LVTTL	Bi-Di	Programmable GPIO0 or additional Clock Output from crystal oscillator circuit
MCLK	105	8 mA	LVTTL	Bi-Di	Audio Master Clock Output.
SCK/DCLK	100	4 mA	LVTTL	Out	I^2S Serial Clock Output.
SD3/DR2 SD2/DL1 SD1/DR1 SD0/DL0	104 103 102 101	4 mA	LVTTL	Out	I^2S Serial Data Output / DSD Audio Output Configurable to be shared with DSD. SD0 = DSD Serial Left Ch0 Data Output SD1 = DSD Serial Right Ch1 Data Output SD2 = DSD Serial Left Ch1 Data Output SD3 = DSD Serial Right Ch2 Data Output
WS/DR0	99	4 mA	LVTTL	Out	I^2S Word Select Output. DSD Serial Right Ch0 Data Output.
SPDIF/DL2	106	4 mA	LVTTL	Out	S/PDIF Audio Output. DSD Serial Left Channel 2 data output.
GPIO6/DL3	19	4 mA	LVTTL	Bi-Di	Programmable GPIO6. DSD Serial Left Channel 3 data output.
GPIO7/DR3	20	4 mA	LVTTL	Bi-Di	Programmable GPIO7. DSD Serial Right Channel 3 data output.
GPIO3/ MUTEOUT	107	4 mA	LVTTL	Bi-Di	Programmable GPIO3 or Mute Audio Output. Signal to the external downstream audio device, audio DAC, etc. to mute audio output.

Note: The XTALIN pin can either be driven at LVTTL levels by a clock (leaving XTALOUT unconnected), or connected through a crystal to XTALOUT. Refer to the schematic on page 73.

5.1.3. Configuration/Programming Pins

Pin Name	Pin #	Strength	Type	Dir	Description
INT	22	4 mA	LVTTL	Out	Interrupt Output. Configurable polarity and push-pull output. Multiple sources of interrupt can be enabled through the INT_EN register. See Note 1.
RESET#	21	—	Schmitt	In	Reset Pin. Active LOW. 5-V tolerant
CSCL	23	—	Schmitt	In	Configuration/Status I^2C Clock. 5-V tolerant. Chip configuration/status, CEA-861 support and downstream HDCP repeater-specific registers are accessed via this I^2C port. True open drain, so does not pull to GND if power is not applied.
CSDA	24	3 mA	Schmitt	Bi-Di	Configuration/Status I^2C Data. 5-V tolerant. Chip configuration/status, CEA-861 support and downstream HDCP repeater-specific registers are accessed via this I^2C port. True open drain, so does not pull to GND if power is not applied.
CI2CA	25	—	LVTTL	In	Local I^2C Address Select. 5-V tolerant Low = Addresses 0x60/0x68 High = Addresses 0x62/0x6A
GPIO1/SCDT	13	4 mA	LVTTL	Out	Programmable GPIO1 or SCDT. Indicates Active Video at HDMI Input Port. Sync detection indicator.
GPIO4	16	4 mA	LVTTL	Bi-Di	Programmable GPIO4
GPIO5	17	4 mA	LVTTL	Bi-Di	Programmable GPIO5
RSVDNC	1, 9, 10, 15, 18, 46–49	—	—	—	Reserved, must be left unconnected
RSVDL	11	—	—	In	Reserved, must be tied to ground

Note: The INT pin can be programmed to be either a push-pull LVTTL output or an open-drain output.

5.1.4. HDMI Control Signal Pins

Pin Name	Pin #	Strength	Type	Dir	Description
DSCL0 DSCL1 DSCL2 DSCL3	31 35 39 43	—	SchmittOD	In	DDC I2C Clock for respective port. 5-V tolerant. HDCP KSV, An and Ri values are exchanged over an I2C port during authentication. True open drain, so does not pull to GND if power is not applied.
DSDA0 DSDA1 DSDA2 DSDA3	32 36 40 44	3 mA	SchmittOD	Bi-Di	DDC I2C Data for respective port. 5-V tolerant. HDCP KSV, An and Ri values are exchanged over an I2C during authentication. True open drain, so does not pull to GND if power is not applied.
HPD0 HPD1 HPD2 HPD3	30 34 38 42	4 mA	LVTTL	Out	Hotplug output signal to HDMI connector for respective port. Indicates EDID is readable. See the Hot Plug Detect CTS Requirement section for important information.
R0PWR5V R1PWR5V R2PWR5V R3PWR5V	29 33 37 41	—	LVTTL	In	5V power and port detection input for respective port. 5-V tolerant. Used to power internal EDID when device is not powered. See Note 1,2
CEC_A	26	—	CEC compliant 5-V tolerant	Bi-Di	HDMI compliant CEC I/O used to interface to CEC devices. This pin connects to the CEC signal of all HDMI connectors in the system. This pin has an internal pull-up resistor.
CEC_D	27	—	LVTTL Schmitt	Bi-Di	CEC interface to local system. True open-drain. An external pull-up is required. This pin typically connects to the local CPU.
RSVDCEC	45	—	—	—	Reserved

Note:

1. There is no power sequence requirement on RxPWR5V pins.
2. The operation condition of the RxPWR5V pins is 5 V ±5%.

5.1.5. Differential Signal Data Pins

Pin Name	Pin #	Type	Description	
R0XC+	110	Analog	TMDS Input Clock Pair.	HDMI Port 0
R0XC-	109			
R0X0+	112	Analog	TMDS Input Data Pairs.	
R0X0-	111			
R0X1+	114			
R0X1-	113			
R0X2+	116			
R0X2-	115			
R1XC+	119	Analog	TMDS Input Clock Pair.	HDMI Port 1
R1XC-	118			
R1X0+	121	Analog	TMDS Input Data Pairs.	
R1X0-	120			
R1X1+	123			
R1X1-	122			
R1X2+	125			
R1X2-	124			
R2XC+	128	Analog	TMDS Input Clock Pair.	HDMI Port 2
R2XC-	127			
R2X0+	130	Analog	TMDS Input Data Pairs.	
R2X0-	129			
R2X1+	132			
R2X1-	131			
R2X2+	134			
R2X2-	133			
R3XC+	137	Analog	TMDS Input Clock Pair.	HDMI Port 3
R3XC-	136			
R3X0+	139	Analog	TMDS Input Data Pairs.	
R3X0-	138			
R3X1+	141			
R3X1-	140			
R3X2+	143			
R3X2-	142			

5.1.6. Power and Ground Pins

Pin Name	Pin #	Type	Description	Supply
CVCC12	8, 60, 71, 86, 97	Power	Digital Logic VCC	1.2 V
IOVCC33	7, 61, 72, 87, 98	Power	Input/Output Pin VCC	3.3 V
AVCC33	108, 126, 144	Power	TMDS Analog VCC 3.3V	3.3 V
AVCC12	117, 135	Power	TMDS Analog VCC 1.2V	1.2 V
APVCC12	2	Power	Audio Clock Regeneration PLL Analog VCC. Must be connected to 1.2V	1.2 V
XTALVCC33	3	Power	Audio Clock Regeneration PLL Crystal Oscillator Power. Must be connected to 3.3V	3.3 V
XTALGND	6	Ground	Audio Clock Regeneration ground	Ground
SBVCC5	28	Power	Standby power supply. All other supplies can be off with SBVCC5 on	5 V
GND	50, ePad (bottom of package)	Ground	ePad must be soldered to ground	Ground

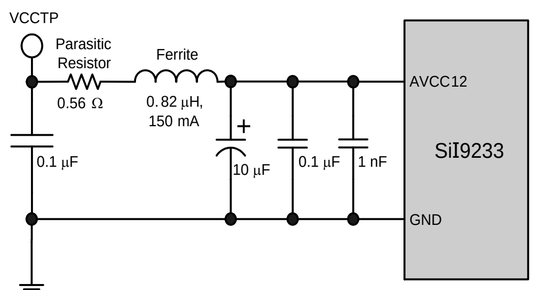


Figure 5.2. Test Point VCCTP for VCC Noise Tolerance Spec

Notes:

1. The Ferrite (0.82 µH, 150 mA) attenuates the PLL power supply noise at 10’s of KHz and above.

The optional parasitic resistor minimizes the peaking. The typical value used here is 0.56 Ω. 1 Ω is the maximum

6. Video Path

The SiI9233 receiver accepts all valid HDMI input formats and can transform that video in a variety of ways to produce the proper video output format. The following pages describe how to control the video path formatting and how to assign output pins for each video output format.

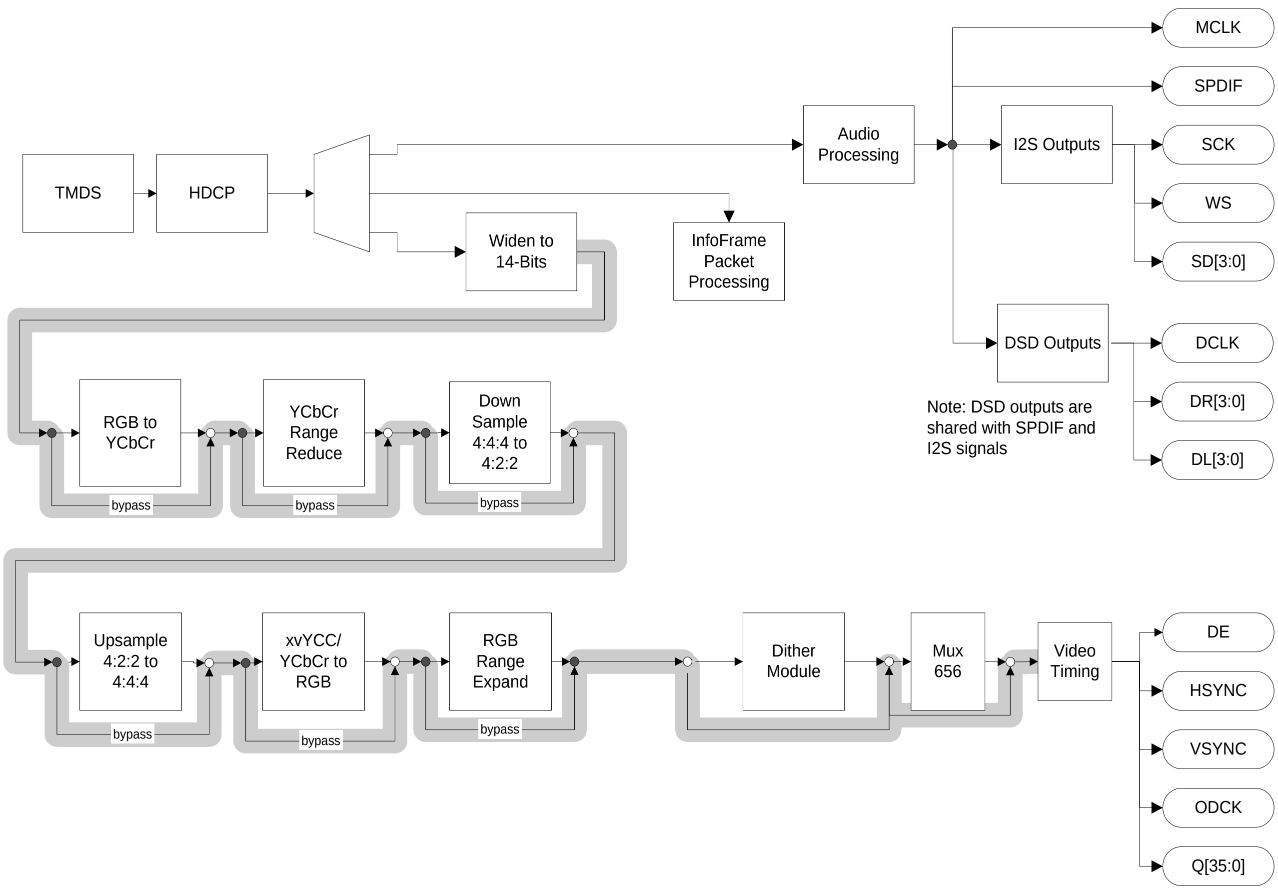


Figure 6.1. Receiver Video and Audio Data Processing Paths

The processing blocks in the figure above correspond to those shown in Figure 6.2 through Figure 6.4.

6.1. HDMI Input Modes to SiI9233 Receiver Output Modes

The HDMI link supports transport of video in any of three modes: RGB 4:4:4, YCbCr 4:4:4 or YCbCr 4:2:2. The flexible video path in the SiI9233 allows reformatting of video data to a set of output modes. Table 6.1 lists the supported transformations and points to the figure for each. In every case, the HDMI link itself carries separate syncs.

Table 6.1. Translating HDMI Formats to Output Formats

		Output Format						
		Digital						
		RGB 4:4:4	**YCbCr 4:4:4**	**YCbCr 4:2:2**	**YCbCr 4:2:2**	**YC Mux**	**YC Mux**	
	Output Syncs	**Separate**	**Separate**	**Separate**	**Embedded**	**Separate**	**Embedded**	**Note**
HDMI Input Mode	RGB 4:4:4	Figure 6.2A	Figure 6.2B	Figure 6.2C	Figure 6.2D	Figure 6.2E	Figure 6.2F	
	YCbCr 4:4:4	Figure 6.3A	Figure 6.3B	Figure 6.3C	Figure 6.3D	Figure 6.3E	Figure 6.3F	
	YCbCr 4:2:2	Figure 6.4A	Figure 6.4B	Figure 6.4C	Figure 6.4D	Figure 6.4E	Figure 6.4F	

6.1.1. HDMI RGB 4:4:4 Input Processing

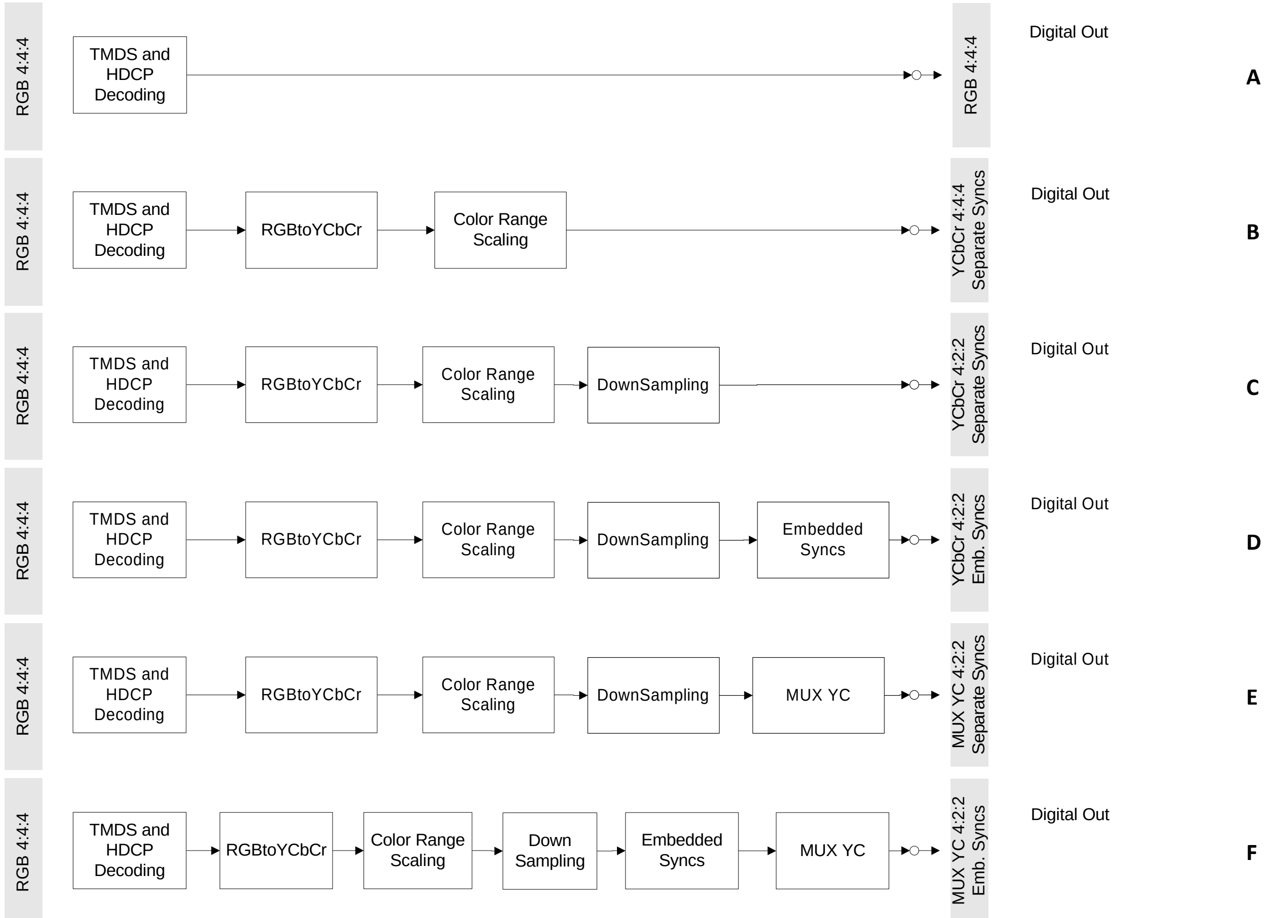


Figure 6.2. HDMI RGB 4:4:4 Input to Video Output Transformations

6.1.2. HDMI YCbCr 4:4:4 Input Processing

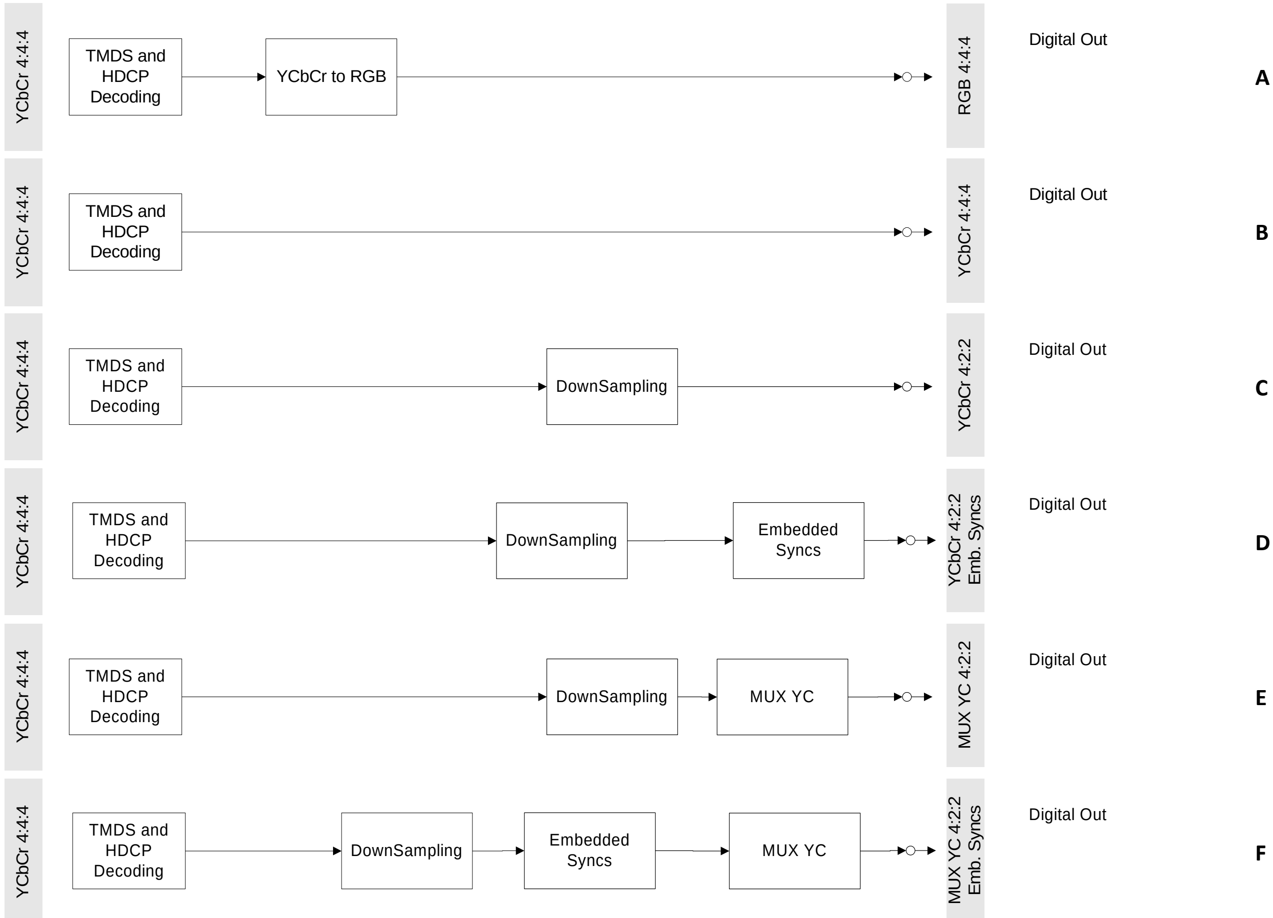


Figure 6.3. HDMI YCbCr 4:4:4 Input to Video Output Transformations

6.1.3. HDMI YCbCr 4:2:2 Input Processing

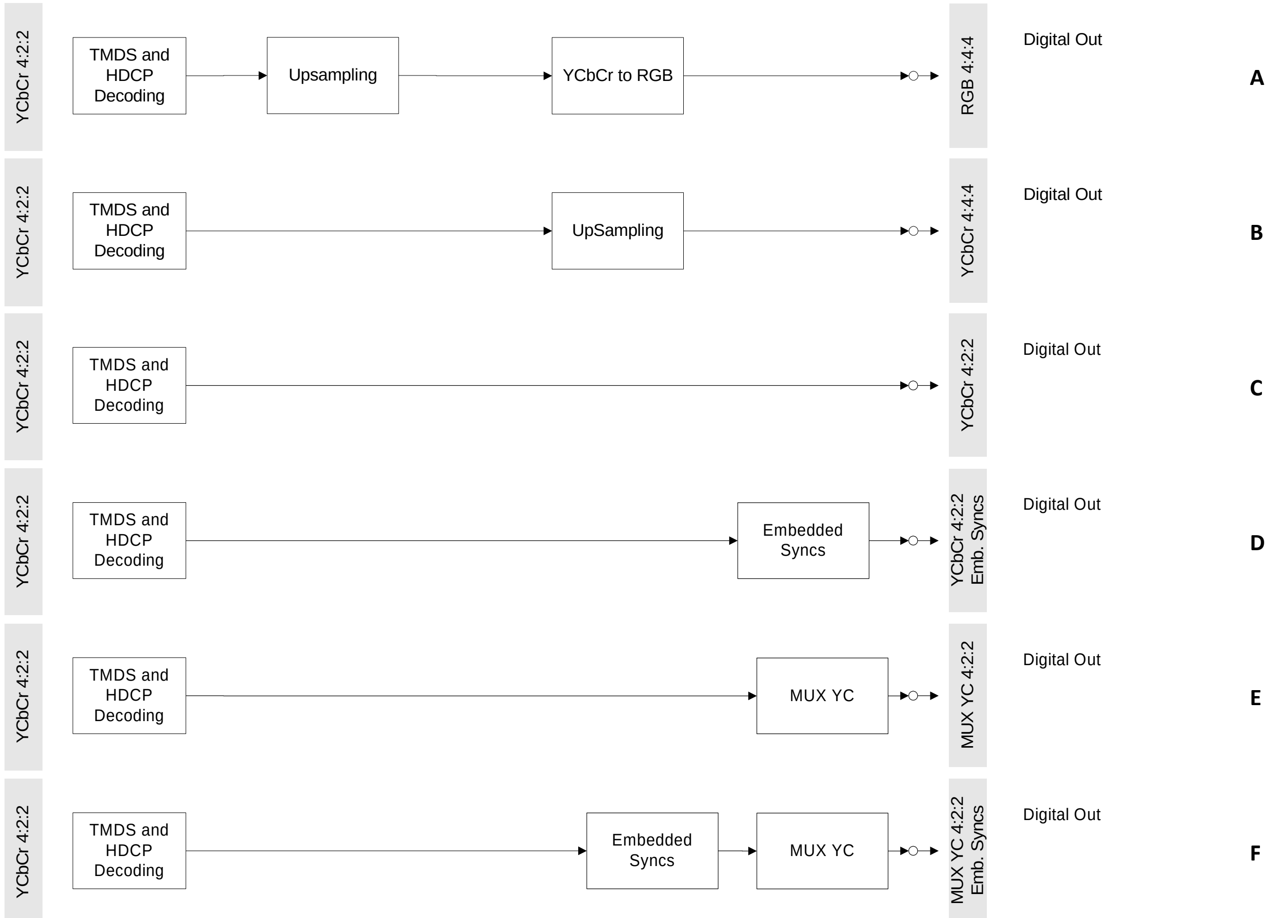


Figure 6.4. HDMI YCbCr 4:2:2 Input to Video Output Transformations

6.2. SiI9233 Receiver Output Mode Configuration

The SiI9233 receiver supports multiple output data mappings. Some have separate control signals while some have embedded control signals. The selection of data mapping mode should be consistent at the pins and in the corresponding register settings. Refer to the *SiI9223/9233/9127 HDMI Receivers Programmer's Reference* (SiI-PR-1019) for more details.

Table 6.2. Output Video Formats

Output Mode	Data Widths	Pixel Replication	Syncs	Page	Notes
RGB 4:4:4	24, 30, 36	1x	Separate	49	3, 7
YCbCr 4:4:4	24, 30, 36	1x	Separate	49	1. 3. 7
YC 4:2:2 Sep. Syncs	16, 20, 24	1x	Separate	51	2, 3
YC 4:2:2 Sep. Syncs	16, 20, 24	2x	Separate	51	2, 3, 8
YC 4:2:2 Emb. Syncs	16, 20, 24	1x	Embedded	54	2, 5
YC MUX 4:2:2	8, 10, 12	2x	Separate	57	2, 4, 8
YC MUX 4:2:2 Emb. Syncs	8, 10, 12	2x	Embedded	59	2, 5, 6, 8, 9

Notes:

1. YC 4:4:4 data contains one Cr, one Cb and one Y value for every pixel.
2. YC 4:2:2 data contains one Cr and one Cb value for every two pixels; and one Y value for every pixel.
3. These formats can be carried across the HDMI link. Refer to the *HDMI Specification*, Section 6.2.3. The link clock must be within the specified range of the SiI9233 receiver.
4. In YC MUX mode data is sent to one or two 8/10/12-bit channels.
5. YC MUX with embedded SAV/EAV signal.
6. Syncs are embedded using SAV/EAV codes.
7. A 2x clock can also be sent with 4:4:4 data.
8. When sending a 2x clock the HDMI source must also send AVI InfoFrames with an accurate pixel replication field. Refer to *HDMI Spec 1.0*, Section 6.4.
9. 2x clocking does not support YC 4:2:2 embedded Sync timings for 720p or 1080i, as the output clock frequency would exceed the range allowed for the SiI9233 receiver.

The SiI9233 receiver can output video in various formats on its parallel digital output bus. Some transformation of the data received over HDMI is necessary in some modes. Digital output is used with either 4:4:4 or 4:2:2 data.

The diagrams do not include separation of the audio and InfoFrame packets from the HDMI stream, which occurs immediately after the TMDS and (optional) HDCP decoding. The HDMI link always carries separate HSYNC and VSYNC and DE. Therefore the SAV/EAV sync encoder must be used whenever the output mode includes embedded sync.

The timing diagrams in Figure 6.5 through Figure 6.9 show only a representation of the DE, HSYNC and VSYNC timings. These timings are specific to the video resolution, as defined by EIA/CEA-861B and other specs. The number of pixels shown per DE HIGH time is representative, to show the data formatting.

6.2.1. RGB and YCbCr 4:4:4 Formats with Separate Syncs

The pixel clock runs at the pixel rate and a complete definition of each pixel is output on each clock. Figure 6.5 shows RGB data. The same timing format is used for YCbCr 4:4:4 as listed in Table 6.3. Figure 6.5 shows timings with OCLKDIV = 0 and OCKINV = 1.

Table 6.3. 4:4:4 Mappings

Pin	36-bit	36-bit	30-bit	30-bit	24-bit	24-bit
Name	RGB	YCbCr	RGB	YCbCr	RGB	YCbCr
Q0	B0	Cb0	NC	NC	NC	NC
Q1	B1	Cb1	NC	NC	NC	NC
Q2	B2	Cb2	B0	Cb0	NC	NC
Q3	B3	Cb3	B1	Cb1	NC	NC
Q4	B4	Cb4	B2	Cb2	B0	Cb0
Q5	B5	Cb5	B3	Cb3	B1	Cb1
Q6	B6	Cb6	B4	Cb4	B2	Cb2
Q7	B7	Cb7	B5	Cb5	B3	Cb3
Q8	B8	Cb8	B6	Cb6	B4	Cb4
Q9	B9	Cb9	B7	Cb7	B5	Cb5
Q10	B10	Cb10	B8	Cb8	B6	Cb6
Q11	B11	Cb11	B9	Cb9	B7	Cb7
Q12	G0	Y0	NC	NC	NC	NC
Q13	G1	Y1	NC	NC	NC	NC
Q14	G2	Y2	G0	Y0	NC	NC
Q15	G3	Y3	G1	Y1	NC	NC
Q16	G4	Y4	G2	Y2	G0	Y0
Q17	G5	Y5	G3	Y3	G1	Y1
Q18	G6	Y6	G4	Y4	G2	Y2
Q19	G7	Y7	G5	Y5	G3	Y3
Q20	G8	Y8	G6	Y6	G4	Y4
Q21	G9	Y9	G7	Y7	G5	Y5
Q22	G10	Y10	G8	Y8	G6	Y6
Q23	G11	Y11	G9	Y9	G7	Y7
Q24	R0	Cr0	NC	NC	NC	NC
Q25	R1	Cr1	NC	NC	NC	NC
Q26	R2	Cr2	R0	Cr0	NC	NC
Q27	R3	Cr3	R1	Cr1	NC	NC
Q28	R4	Cr4	R2	Cr2	R0	Cr0
Q29	R5	Cr5	R3	Cr3	R1	Cr1
Q30	R6	Cr6	R4	Cr4	R2	Cr2
Q31	R7	Cr7	R5	Cr5	R3	Cr3
Q32	R8	Cr8	R6	Cr6	R4	Cr4
Q33	R9	Cr9	R7	Cr7	R5	Cr5
Q34	R10	Cr10	R8	Cr8	R6	Cr6
Q35	R11	Cr11	R9	Cr9	R7	Cr7
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

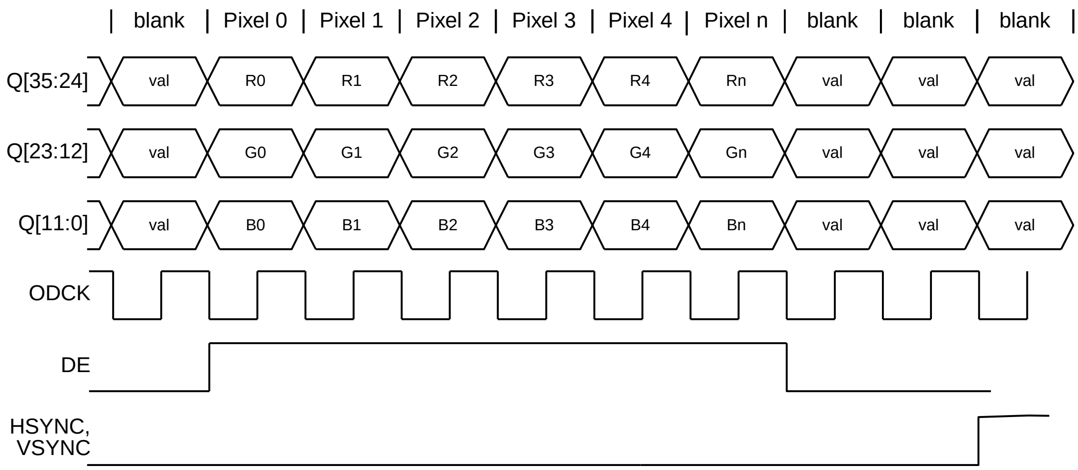


Figure 6.5. 4:4:4 Timing Diagram

Note: The *val* data is defined in various specifications to specific values. These values are controlled by setting the appropriate SiI9233 registers, because no pixel data is carried on HDMI during blanking.

6.2.2. YC 4:2:2 Formats with Separate Syncs

The YC 4:2:2 formats output one pixel for every pixel clock period. A luminance (Y) value is sent for every pixel, but the chrominance values (Cb and Cr) are sent over two pixels. Pixel data can be 24-bit, 20-bit or 16-bit. HSYNC and VSYNC are output separately on their own pins. The DE HIGH time must contain an even number of pixel clocks. Figure 6.6 shows timings with OCLKDIV = 0 and OCKINV = 1.

Table 6.4. YC 4:2:2 Separate Sync Pin Mappings

Pin	16-bit YC		20-bit YC		24-bit YC	
Name	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
Q0	NC	NC	NC	NC	NC	NC
Q1	NC	NC	NC	NC	NC	NC
Q2	NC	NC	NC	NC	NC	NC
Q3	NC	NC	NC	NC	NC	NC
Q4	NC	NC	NC	NC	NC	NC
Q5	NC	NC	NC	NC	NC	NC
Q6	NC	NC	NC	NC	NC	NC
Q7	NC	NC	NC	NC	NC	NC
Q8	NC	NC	NC	NC	NC	NC
Q9	NC	NC	NC	NC	NC	NC
Q10	NC	NC	NC	NC	NC	NC
Q11	NC	NC	NC	NC	NC	NC
Q12	NC	NC	NC	NC	Y0	Y0
Q13	NC	NC	NC	NC	Y1	Y1
Q14	NC	NC	Y0	Y0	Y2	Y2
Q15	NC	NC	Y1	Y1	Y3	Y3
Q16	Y0	Y0	Y2	Y2	Y4	Y4
Q17	Y1	Y1	Y3	Y3	Y5	Y5
Q18	Y2	Y2	Y4	Y4	Y6	Y6
Q19	Y3	Y3	Y5	Y5	Y7	Y7
Q20	Y4	Y4	Y6	Y6	Y8	Y8
Q21	Y5	Y5	Y7	Y7	Y9	Y9
Q22	Y6	Y6	Y8	Y8	Y10	Y10
Q23	Y7	Y7	Y9	Y9	Y11	Y11
Q24	NC	NC	NC	NC	Cb0	Cr0
Q25	NC	NC	NC	NC	Cb1	Cr1
Q26	NC	NC	Cb0	Cr0	Cb2	Cr2
Q27	NC	NC	Cb1	Cr1	Cb3	Cr3
Q28	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
Q29	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
Q30	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
Q31	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
Q32	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
Q33	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
Q34	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
Q35	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

Table 6.5. YC 4:2:2 (Pass Through Only) Separate Sync Pin Mapping

Pin	16-bit YC		20-bit YC		24-bit YC	
Name	**Pixel #0**	**Pixel #1**	**Pixel #0**	**Pixel #1**	**Pixel #0**	**Pixel #1**
Q0	NC	NC	NC	NC	NC	NC
Q1	NC	NC	NC	NC	NC	NC
Q2	NC	NC	NC	NC	NC	NC
Q3	NC	NC	NC	NC	NC	NC
Q4	NC	NC	NC	NC	Y0	Y0
Q5	NC	NC	NC	NC	Y1	Y1
Q6	NC	NC	Y0	Y0	Y2	Y2
Q7	NC	NC	Y1	Y1	Y3	Y3
Q8	NC	NC	NC	NC	Cb0	Cr0
Q9	NC	NC	NC	NC	Cb1	Cr1
Q10	NC	NC	Cb0	Cr0	Cb2	Cr2
Q11	NC	NC	Cb1	Cr1	Cb3	Cr3
Q12	NC	NC	NC	NC	NC	NC
Q13	NC	NC	NC	NC	NC	NC
Q14	NC	NC	NC	NC	NC	NC
Q15	NC	NC	NC	NC	NC	NC
Q16	Y0	Y0	Y2	Y2	Y4	Y4
Q17	Y1	Y1	Y3	Y3	Y5	Y5
Q18	Y2	Y2	Y4	Y4	Y6	Y6
Q19	Y3	Y3	Y5	Y5	Y7	Y7
Q20	Y4	Y4	Y6	Y6	Y8	Y8
Q21	Y5	Y5	Y7	Y7	Y9	Y9
Q22	Y6	Y6	Y8	Y8	Y10	Y10
Q23	Y7	Y7	Y9	Y9	Y11	Y11
Q24	NC	NC	NC	NC	NC	NC
Q25	NC	NC	NC	NC	NC	NC
Q26	NC	NC	NC	NC	NC	NC
Q27	NC	NC	NC	NC	NC	NC
Q28	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
Q29	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
Q30	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
Q31	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
Q32	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
Q33	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
Q34	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
Q35	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

Note: This pin mapping is only valid when the input video format is YC 4:2:2 and the output video format is YC 4:2:2 also. No video processing block should be enabled when this pin mapping is used.

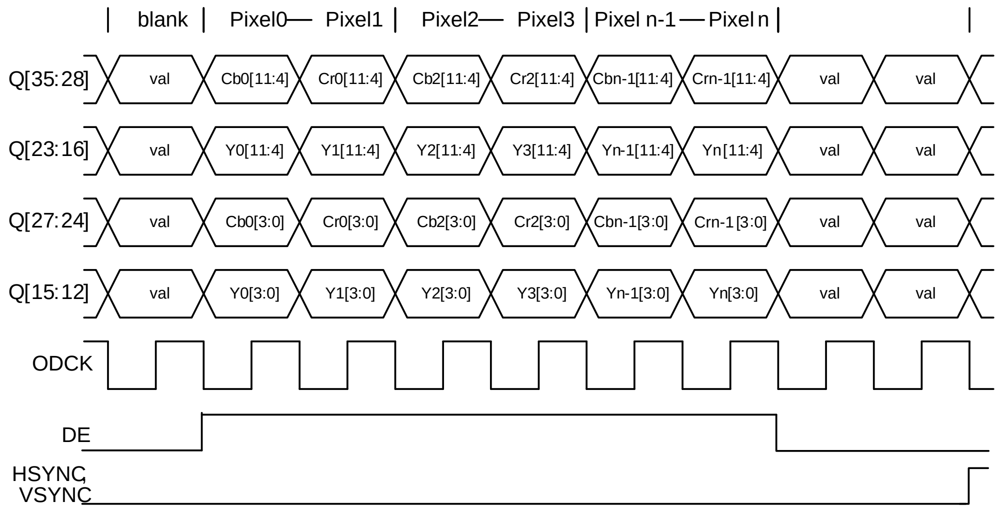


Figure 6.6. YC Timing Diagram

Note: The *val* data is defined in various specifications to specific values. These values are controlled by setting the appropriate SiI9233 registers, because no pixel data is carried on HDMI during blanking.

6.2.3. YC 4:2:2 Formats with Embedded Syncs

The YC 4:2:2 embedded sync format is identical to the previous format (YC 4:2:2), except that the syncs are embedded and not separate. Pixel data can be 24-bit, 20-bit or 16-bit. DE is always output. Figure 6.7 shows the Start of Active Video (SAV) preamble, the End of Active Video" (EAV) suffix, and shows timings with OCLKDIV = 0 and OCKINV = 1.

Table 6.6. YC 4:2:2 Embedded Sync Pin Mappings

Pin	16-bit YC		20-bit YC		24-bit YC	
Name	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
Q0	NC	NC	NC	NC	NC	NC
Q1	NC	NC	NC	NC	NC	NC
Q2	NC	NC	NC	NC	NC	NC
Q3	NC	NC	NC	NC	NC	NC
Q4	NC	NC	NC	NC	NC	NC
Q5	NC	NC	NC	NC	NC	NC
Q6	NC	NC	NC	NC	NC	NC
Q7	NC	NC	NC	NC	NC	NC
Q8	NC	NC	NC	NC	NC	NC
Q9	NC	NC	NC	NC	NC	NC
Q10	NC	NC	NC	NC	NC	NC
Q11	NC	NC	NC	NC	NC	NC
Q12	NC	NC	NC	NC	Y0	Y0
Q13	NC	NC	NC	NC	Y1	Y1
Q14	NC	NC	Y0	Y0	Y2	Y2
Q15	NC	NC	Y1	Y1	Y3	Y3
Q16	Y0	Y0	Y2	Y2	Y4	Y4
Q17	Y1	Y1	Y3	Y3	Y5	Y5
Q18	Y2	Y2	Y4	Y4	Y6	Y6
Q19	Y3	Y3	Y5	Y5	Y7	Y7
Q20	Y4	Y4	Y6	Y6	Y8	Y8
Q21	Y5	Y5	Y7	Y7	Y9	Y9
Q22	Y6	Y6	Y8	Y8	Y10	Y10
Q23	Y7	Y7	Y9	Y9	Y11	Y11
Q24	NC	NC	NC	NC	Cb0	Cr0
Q25	NC	NC	NC	NC	Cb1	Cr1
Q26	NC	NC	Cb0	Cr0	Cb2	Cr2
Q27	NC	NC	Cb1	Cr1	Cb3	Cr3
Q28	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
Q29	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
Q30	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
Q31	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
Q32	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
Q33	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
Q34	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
Q35	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded
VSYNC	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded
DE	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded

Table 6.7. YC 4:2:2 (Pass Through Only) Embedded Sync Pin Mapping

Pin	16-bit YC		20-bit YC		24-bit YC	
Name	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
Q0	NC	NC	NC	NC	NC	NC
Q1	NC	NC	NC	NC	NC	NC
Q2	NC	NC	NC	NC	NC	NC
Q3	NC	NC	NC	NC	NC	NC
Q4	NC	NC	NC	NC	Y0	Y0
Q5	NC	NC	NC	NC	Y1	Y1
Q6	NC	NC	Y0	Y0	Y2	Y2
Q7	NC	NC	Y1	Y1	Y3	Y3
Q8	NC	NC	NC	NC	Cb0	Cr0
Q9	NC	NC	NC	NC	Cb1	Cr1
Q10	NC	NC	Cb0	Cr0	Cb2	Cr2
Q11	NC	NC	Cb1	Cr1	Cb3	Cr3
Q12	NC	NC	NC	NC	NC	NC
Q13	NC	NC	NC	NC	NC	NC
Q14	NC	NC	NC	NC	NC	NC
Q15	NC	NC	NC	NC	NC	NC
Q16	Y0	Y0	Y2	Y2	Y4	Y4
Q17	Y1	Y1	Y3	Y3	Y5	Y5
Q18	Y2	Y2	Y4	Y4	Y6	Y6
Q19	Y3	Y3	Y5	Y5	Y7	Y7
Q20	Y4	Y4	Y6	Y6	Y8	Y8
Q21	Y5	Y5	Y7	Y7	Y9	Y9
Q22	Y6	Y6	Y8	Y8	Y10	Y10
Q23	Y7	Y7	Y9	Y9	Y11	Y11
Q24	NC	NC	NC	NC	NC	NC
Q25	NC	NC	NC	NC	NC	NC
Q26	NC	NC	NC	NC	NC	NC
Q27	NC	NC	NC	NC	NC	NC
Q28	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
Q29	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
Q30	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
Q31	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
Q32	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
Q33	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
Q34	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
Q35	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded
VSYNC	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded
DE	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded

Note: This pin mapping is only valid when the input video format is YC 4:2:2 and the output video format is YC 4:2:2 also. No video processing block should be enabled when this pin mapping is used.

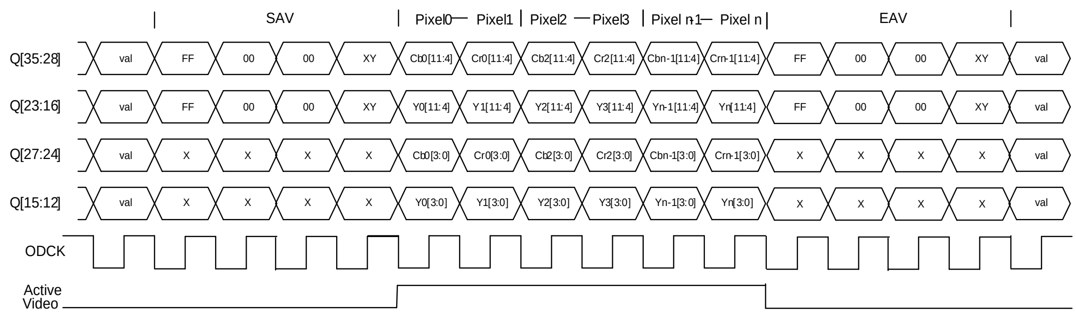


Figure 6.7. YC 4:2:2 Embedded Sync Timing Diagram

Note: The val data is defined in various specifications to specific values. These values are controlled by setting the appropriate SiI9233 registers, because no pixel data is carried on HDMI during blanking. SAV/EAV codes appear as an 8-bit field on both Q[35:28] (per SMPTE) and Q[23:16].

6.2.4. YC Mux (4:2:2) Formats with Separate Syncs

The video data is multiplexed onto fewer pins than the mapping in Table 6.8, but complete luminance (Y) and chrominance (Cb and Cr) data is still provided for each pixel because the output pixel clock runs at twice the pixel rate. Figure 6.8 shows the 24-bit mode. The 16- and 20-bit mappings use fewer output pins for the pixel data. Note the separate syncs. Figure 6.8 shows OCLKDIV = 0 and OCKINV = 1.

Table 6.8. YC Mux 4:2:2 Mappings

Pin	8-bit	10-bit	12-bit
Name	YCbCr	YCbCr	YCbCr
Q0	NC	NC	NC
Q1	NC	NC	NC
Q2	NC	NC	NC
Q3	NC	NC	NC
Q4	NC	NC	NC
Q5	NC	NC	NC
Q6	NC	NC	NC
Q7	NC	NC	NC
Q8	NC	NC	NC
Q9	NC	NC	NC
Q10	NC	NC	NC
Q11	NC	NC	NC
Q12	NC	NC	D0
Q13	NC	NC	D1
Q14	NC	D0	D2
Q15	NC	D1	D3
Q16	D0	D2	D4
Q17	D1	D3	D5
Q18	D2	D4	D6
Q19	D3	D5	D7
Q20	D4	D6	D8
Q21	D5	D7	D9
Q22	D6	D8	D10
Q23	D7	D9	D11
Q24	NC	NC	NC
Q25	NC	NC	NC
Q26	NC	NC	NC
Q27	NC	NC	NC
Q28	NC	NC	NC
Q29	NC	NC	NC
Q30	NC	NC	NC
Q31	NC	NC	NC
Q32	NC	NC	NC
Q33	NC	NC	NC
Q34	NC	NC	NC
Q35	NC	NC	NC
HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE

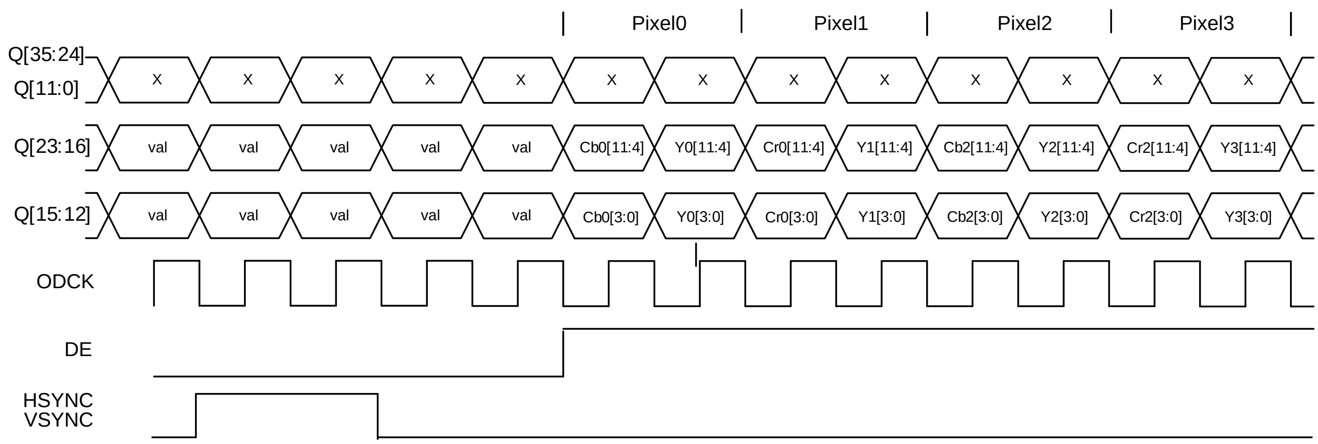


Figure 6.8. YC Mux 4:2:2 Timing Diagram

Note: The *val* data is defined in various specifications to specific values. These values are controlled by setting the appropriate SiI9233 registers, because no pixel data is carried on HDMI during blanking.

6.2.5. YC Mux 4:2:2 Formats with Embedded Syncs

This mode is similar to that on page 57, but with embedded syncs. It is similar to YC 4:2:2 with embedded syncs, but also multiplexes the luminance (Y) and chrominance (Cb and Cr) onto the same pins on alternating pixel clock cycles. Normally this mode is used only for 480i, 480p, 576i and 576p modes. Output clock rate is half the pixel clock rate on the link. SAV code is shown before rise of DE. EAV follows the falling edge of DE. See the ITU-R BT.656 Specification. 480p, 54-MHz output can be achieved if the input differential clock is 54 MHz. Figure 6.9 shows OCLKDIV = 0 and OCKINV = 1.

Table 6.9. YC Mux 4:2:2 Embedded Sync Pin Mapping

Pin	8-bit	10-bit	12-bit
Name	YCbCr	YCbCr	YCbCr
Q0	NC	NC	NC
Q1	NC	NC	NC
Q2	NC	NC	NC
Q3	NC	NC	NC
Q4	NC	NC	NC
Q5	NC	NC	NC
Q6	NC	NC	NC
Q7	NC	NC	NC
Q8	NC	NC	NC
Q9	NC	NC	NC
Q10	NC	NC	NC
Q11	NC	NC	NC
Q12	NC	NC	D0
Q13	NC	NC	D1
Q14	NC	D0	D2
Q15	NC	D1	D3
Q16	D0	D2	D4
Q17	D1	D3	D5
Q18	D2	D4	D6
Q19	D3	D5	D7
Q20	D4	D6	D8
Q21	D5	D7	D9
Q22	D6	D8	D10
Q23	D7	D9	D11
Q24	NC	NC	NC
Q25	NC	NC	NC
Q26	NC	NC	NC
Q27	NC	NC	NC
Q28	NC	NC	NC
Q29	NC	NC	NC
Q30	NC	NC	NC
Q31	NC	NC	NC
Q32	NC	NC	NC
Q33	NC	NC	NC
Q34	NC	NC	NC
Q35	NC	NC	NC
HSYNC	Embedded	Embedded	Embedded
VSYNC	Embedded	Embedded	Embedded
DE	Embedded	Embedded	Embedded

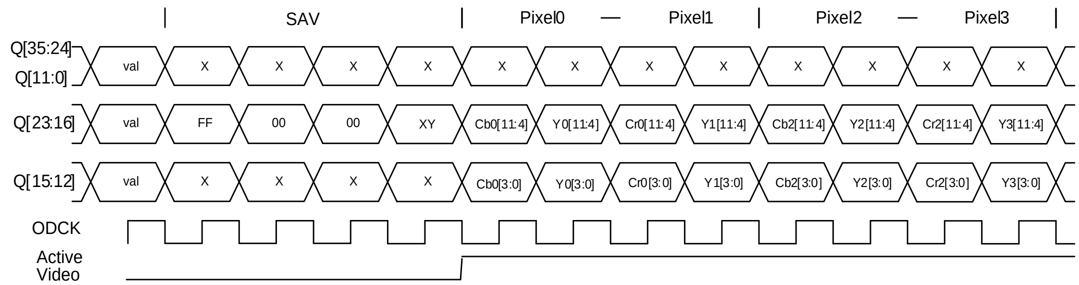


Figure 6.9. YC Mux 4:2:2 Embedded Sync Encoding Timing Diagram

Note: The *val* data is defined in various specifications to specific values. These values are controlled by setting the appropriate SiI9233 registers, because no pixel data is carried on HDMI during blanking. Refer to the *SiI9223/9233/9127 HDMI Receivers Programmer's Reference* (SiI-PR-1019) for details.

6.2.6. 12/15/18-Bit RGB and YCbCr 4:4:4 Formats with Separate Syncs

The output clock runs at the pixel rate and a complete definition of each pixel is output on each clock. One clock edge drives out half the pixel data on 12/15/18 pins. The opposite clock edge drives out the remaining half of the pixel data on the same 12/15/18 pins. Figure 6.10 shows RGB data. The same timing format is used for YCbCr 4:4:4 as listed in the columns of Table 6.10. Control signals (DE, HSYNC and VSYNC) change state with respect to the first edge of ODCK.

Table 6.10. 12/15/18-Bit Output 4:4:4 Mappings

	24-bit				30-bit				36-bit			
Pin	RGB		YCbCr		RGB		YCbCr		RGB		YCbCr	
Name	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge
Q0	NC	NC	NC	NC	NC	NC	NC	NC	B0	G6	Cb0	Y6
Q1	NC	NC	NC	NC	NC	NC	NC	NC	B1	G7	Cb1	Y7
Q2	NC	NC	NC	NC	NC	NC	NC	NC	B2	G8	Cb2	Y8
Q3	NC	NC	NC	NC	B0	G5	Cb0	Y5	B3	G9	Cb3	Y9
Q4	NC	NC	NC	NC	B1	G6	Cb1	Y6	B4	G10	Cb4	Y10
Q5	NC	NC	NC	NC	B2	G7	Cb2	Y7	B5	G11	Cb5	Y11
Q6	B0	G4	Cb0	Y4	B3	G8	Cb3	Y8	B6	R0	Cb6	Cr0
Q7	B1	G5	Cb1	Y5	B4	G9	Cb4	Y9	B7	R1	Cb7	Cr1
Q8	B2	G6	Cb2	Y6	B5	R0	Cb5	Cr0	B8	R2	Cb8	Cr2
Q9	B3	G7	Cb3	Y7	B6	R1	Cb6	Cr1	B9	R3	Cb9	Cr3
Q10	B4	R0	Cb4	Cr0	B7	R2	Cb7	Cr2	B10	R4	Cb10	Cr4
Q11	B5	R1	Cb5	Cr1	B8	R3	Cb8	Cr3	B11	R5	Cb11	Cr5
Q12	B6	R2	Cb6	Cr2	B9	R4	Cb9	Cr4	G0	R6	Y0	Cr6
Q13	B7	R3	Cb7	Cr3	G0	R5	Y0	Cr5	G1	R7	Y1	Cr7
Q14	G0	R4	Y0	Cr4	G1	R6	Y1	Cr6	G2	R8	Y2	Cr8
Q15	G1	R5	Y1	Cr5	G2	R7	Y2	Cr7	G3	R9	Y3	Cr9
Q16	G2	R6	Y2	Cr6	G3	R8	Y3	Cr8	G4	R10	Y4	Cr10
Q17	G3	R7	Y3	Cr7	G4	R9	Y4	Cr9	G5	R11	Y5	Cr11
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE

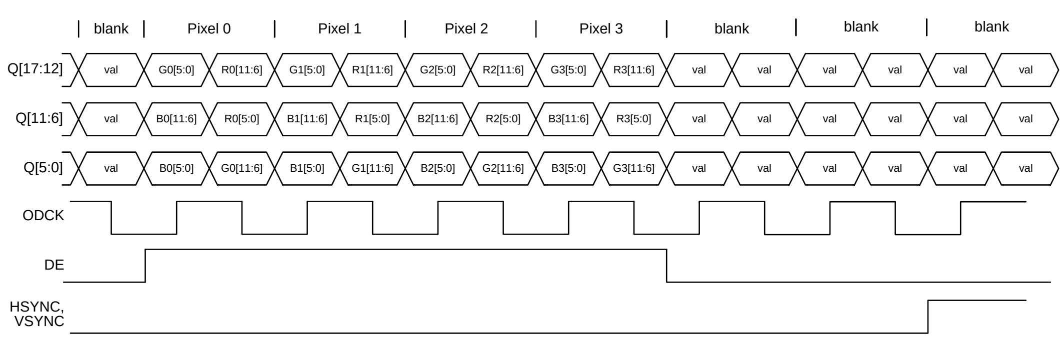


Figure 6.10. 18-Bit Output 4:4:4 Timing Diagram

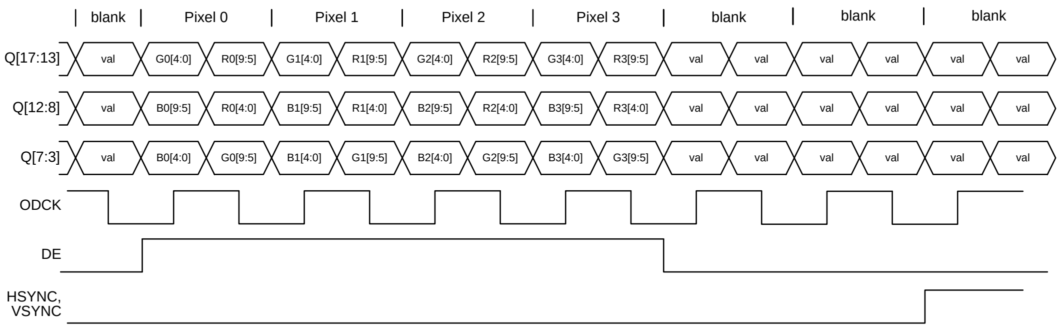


Figure 6.11. 15-Bit Output 4:4:4 Timing Diagram

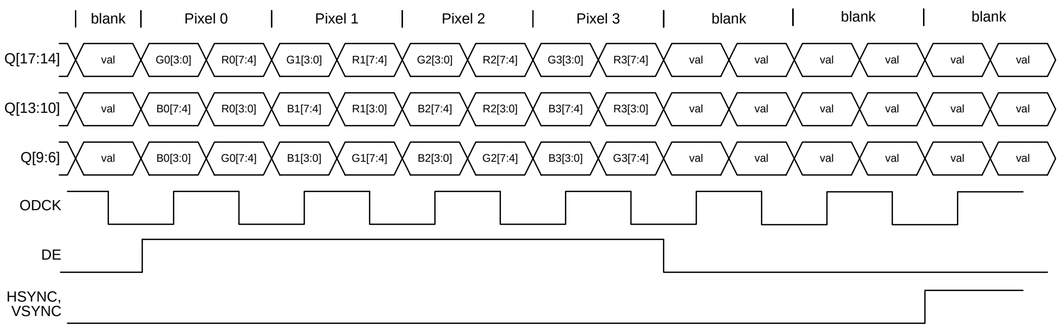


Figure 6.12. 12-Bit Output 4:4:4 Timing Diagram

7. I^{2}C Interfaces

7.1. HDCP E-DDC / I^{2}C Interface

The HDCP protocol requires values to be exchanged between the video transmitter and video receiver. These values are exchanged over the DDC channel of the DVI interface. The E-DDC channel follows the I^{2}C serial protocol. In a system design using an SiI9233 receiver, the SiI9233 device is the video Receiver and has a connection to the E-DDC bus with a slave address of 0x74 The I^{2}C read operation is shown in Figure 7.1, and the write operation in Figure 7.2.

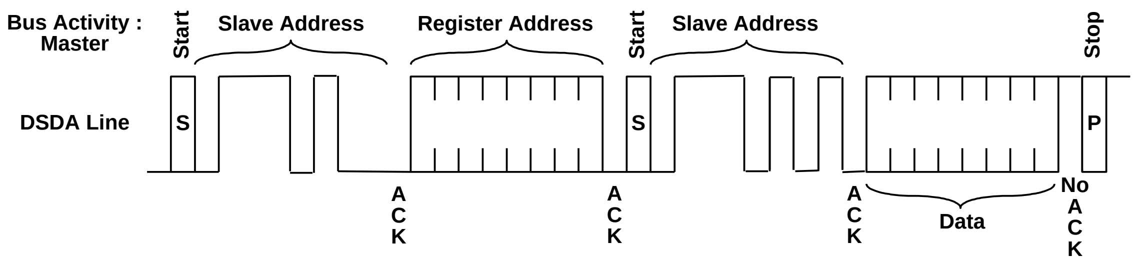


Figure 7.1. I^{2}C Byte Read

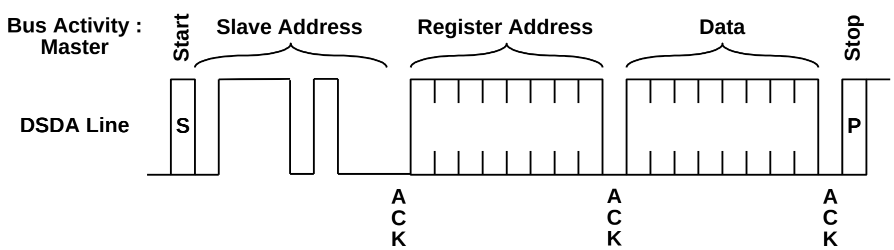


Figure 7.2. I^{2}C Byte Write

Multiple bytes can be transferred in each transaction, regardless of whether they are reads or writes. The operations are similar to those in Figure 7.1 and Figure 7.2 except that there is more than one data phase. An ACK follow each byte except the last byte in a read operation. Byte addresses increment, with the least significant byte transferred first, and the most significant byte last. See the I^{2}C specification for more information.

There is also a "Short Read" format, designed to improve the efficiency of Ri register reads (which must be done every two seconds while encryption is enabled). This transaction is shown in Figure 7.3. Note that there is no register address phase (only the slave address phase), because the register address is reset to 0x08 (Ri) after a hardware or software reset, and after the STOP condition on any preceding I^{2}C transaction.

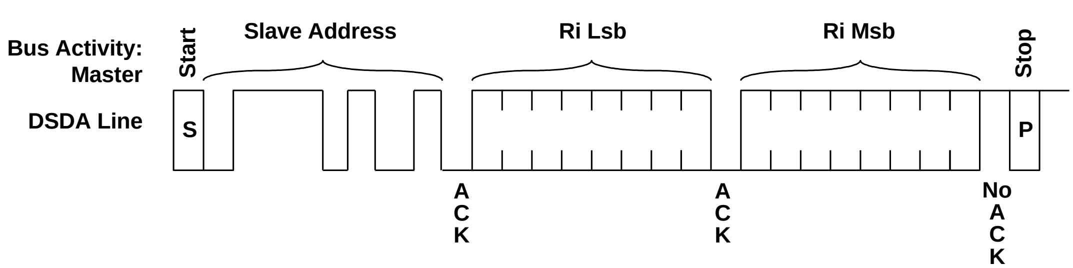


Figure 7.3. Short Read Sequence

7.2. Local I²C Interface

The SiI9233 HDMI Receiver has a second I²C port accessible only to the controller in the display device. It is separate from the E-DDC bus. The HDMI Receiver is a slave device that responds to six binary I²C device addresses of seven bits each. This I²C interface only supports the read operation in Figure 7.1, and the write operation in Figure 7.2. It does not support the short read operation shown in Figure 7.3. Note that the I²C data pin for the local I²C bus is CSDA, instead of the DSDA pin shown in these figures.

The local I²C interface on the SiI9233 receiver (pins CSCL and CSDA) is a slave interface that can run up to 400 kHz. This bus is used to configure and control the SiI9233 receiver by reading/writing to necessary registers.

The local I²C interface of the SiI9233 receiver consists of 6 separate I²C slave addresses. The SiI223 receiver will therefore appear as 6 separate devices on the I²C local bus. The first two of these addresses, used for HDMI Control and general low level register control, are fixed, and can only be set to one of two values by using the CI2CA pin. The other 3 addresses (used for CEC, EDID, and x.v.Color) have an I²C register programmable address mapped into the HDMI Control register space, so the default value can be changed if there is a bus conflict with another device.

Table 7.1. Control of the Default I²C Addresses with the CI2CA Pin

	CI2CA=LOW	Ci2CA=HIGH
HDMI Control and low level registers (fixed)	0x60 & 0x68	0x62 & 0x6A
X.V.Color Registers (programmable)	0x64	
EDID Registers (programmable)	0xE0	0xE4
CEC Registers (programmable)	0xC0	0xC4

The HDMI Control and low level registers are fixed after reset based on CI2CA pin and cannot be changed. The I²C slave address for the x.v.Color registers, EDID Control registers, and the CEC Control registers each have a register associated with them that allows the address to be changed. See the *SiI9223/9233/9127 HDMI Receivers Programmer's Reference* (SiI-PR-1019) for more information.

7.3. Video Requirement for I²C Access

The SiI9233 receiver does not require an active video clock to access its registers from either the E-DDC port or the local I²C port. Read-Write registers can be written and then read back. Read-only registers that provide values for an active video or audio stream return indeterminate values if there is no video clock and no active syncs.

Use the SCDT and CKDT register bits to determine when active video is being received by the chip.

7.4. I²C Registers

The register values that are exchanged over the HDMI DDC I²C serial interface with the SiI9233 for HDCP are described in the HDCP 1.0 Specification (February 2000) in *Section 2.6 – HDCP Port*. Refer to the *SiI9223/9233/9127 HDMI Receivers Programmer's Reference* (SiI-PR-1019) for details on these and all other SiI9233 registers.

8. Hot Plug Detect CTS Requirement

To comply with with HDMI Compliance Test Specification Test ID 8-11*, HPD Output Resistance*, the circuit shown in Figure 8.1 must be added to each SiISiI9233 input port that is used in the design.

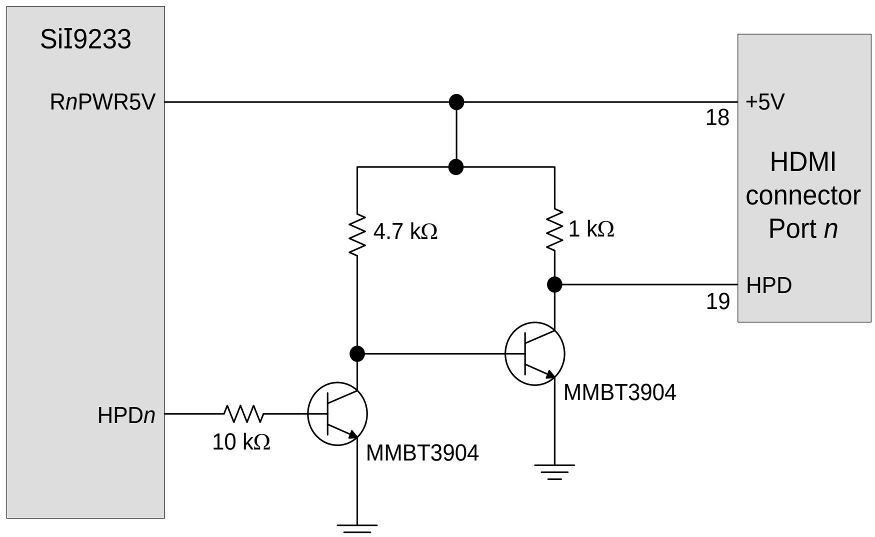


Figure 8.1: HPD CTS Compliance Requirement Schematic

9. Design Recommendations

The following information is provided as recommendations that are based on the experience of Lattice Semiconductor engineers and customers. If you choose to deviate from these recommendations for a particular application, Lattice Semiconductor strongly suggests that you contact one of its technical representatives for an evaluation of the change.

9.1. Power Control

The low-power standby state feature of the SiI9233 receiver provides a design option of leaving the chip always powered, as opposed to powering it on and off. Leaving the chip powered and using the PD# register bit to put it in a lower power state can result in faster system response time, depending on the system Vcc supply ramp-up delay.

9.1.1. Power Pin Current Demands

The limits shown in Table 9.1 indicate the current demanded by each group of power pins on the SiI9233 device. These limits were characterized at maximum VCC, 0 °C ambient temperature and for fast-fast silicon. Actual application current demands can be lower than these figures, and varies with video resolution and audio clock frequency.

Table 9.1. Maximum Power Domain Currents versus Video Mode

Mode	ODCK (MHz)	3.3V Power Domain Currents (mA)		
		IOVCC33	AVCC33	XTALVCC33
480p	27.0	39	51	7
1080i	74.25	100	51	7
1080p	148.5	182	51	7
1080p@12-bit[1]	225	252	51	7

Mode	ODCK (MHz)	1.2V Power Domain Currents (mA)		
		AVCC12	CVCC12	APVCC12
480p	27.0	36	52	5
1080i	74.25	54	127	5
1080p	148.5	84	253	5
1080p@12-bit[1]	225	129	343	5

Notes:

1. Measured with 12-bits/pixel video data.
2. Measured with 192 kHz, 8-channel audio, except for 480p mode which used 48 kHz, 8-channel audio.
3. Measured with RGB input, vertical black-white/1-pixel stripe (Moire2) pattern, converting to YCbCr output (digital for IOVCC33).
4. Only one core can be selected at a time. The TMDSxSEL register bit turns off the unselected core, except for the termination to AVCC33.

AVCC33 current includes 40 mA for the unselected TMDS core. Only 5 mA of this current is dissipated as power in the HDMI Receiver; the remainder is dissipated in the HDMI transmitter. The AVCC33 current on the unselected core can be reduced to 5 mA by asserting the corresponding PD_TERMx# register bit.

9.2. HDMI Receiver DDC Bus Protection

The I^2C pins on the VESA DDC Specification (available at www.vesa.org) defines the DDC interconnect bus to be a 5-V signaling path. The I^2C pins on the HDMI Receiver chip are 5-V tolerant. And these pins are true open-drain I/O. The pull-up resistors on the DDC bus should be pulled up using the 5-V supply from the HDMI connector. Refer to Figure 9.9 on page 74.

9.3. Decoupling Capacitors

Designers should include decoupling and bypass capacitors at each power pin in the layout. These are shown schematically in Figure 9.4 on page 71. Place these components as closely as possible to the SiI9233 pins and avoid routing through vias. Figure 9.1 shows the various types of power pins on the HDMI Receiver.

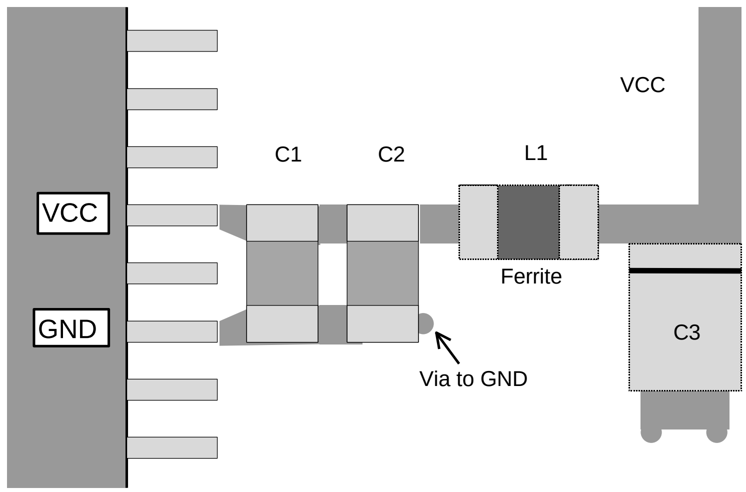


Figure 9.1. Decoupling and Bypass Capacitor Placement

9.4. ESD Protection

The HDMI Receiver chip is designed to withstand electrostatic discharge to 2 kV. In applications where higher protection levels are required, ESD limiting components can be placed on the differential lines coming into the chip. These components typically have a capacitive effect, reducing the signal quality at higher clock frequencies on the link. Use of the lowest capacitance devices is suggested; in no case should the capacitance value exceed 5 pF.

Series resistors can be included on the TMDS lines (see Figure 9.9 on page 74) to counteract the impedance effects of ESD protection diodes. The diodes typically lower the impedance because of their capacitance. The resistors raise the impedance to stay within the HDMI specification centered on a 100-Ω differential.

9.5. HDMI Receiver Layout

The HDMI Receiver chip should be placed as closely as possible to the input connectors that carry the TMDS signals. For a system using industry-standard HDMI connectors (see www.hdmi.org), the differential lines should be routed as directly as possible from connector to HDMI Receiver. Lattice Semiconductor HDMI receivers are tolerant of skews between differential pairs, so spiral skew compensation for path length differences is not required. Each differential pair should be routed together, minimizing the number of vias through which the signal lines are routed. The distance separating the two traces of the differential pair should be kept to a minimum.

In order to achieve the optimal input TMDS signal quality, please follow the layout guidelines below:

1. Lay out all differential pairs with controlled impedance of 100 Ω differential.
2. Cut out all copper planes (ground and power) that are less than 45 mils underneath the TMDS traces near the HDMI receiver with dimensions as shown below.

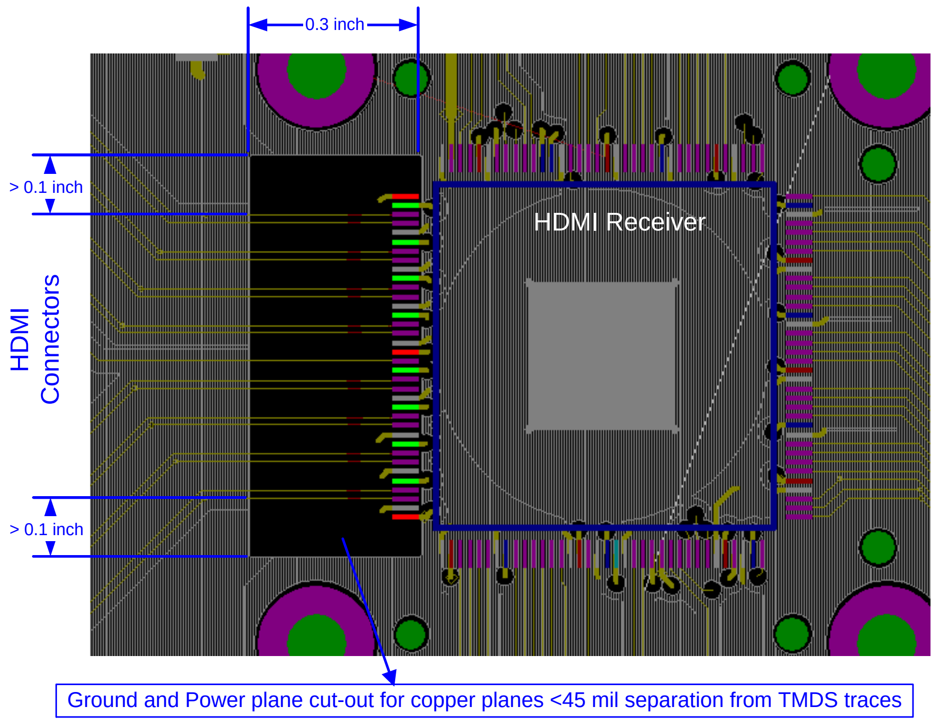


Figure 9.2. Cut-out Reference Plane Dimensions

3. If ESD suppression devices or common mode chokes are used, place them near the HDMI connector, away from the HDMI Receiver IC. Do not place them over the ground and power plane cutout near the HDMI receiver.

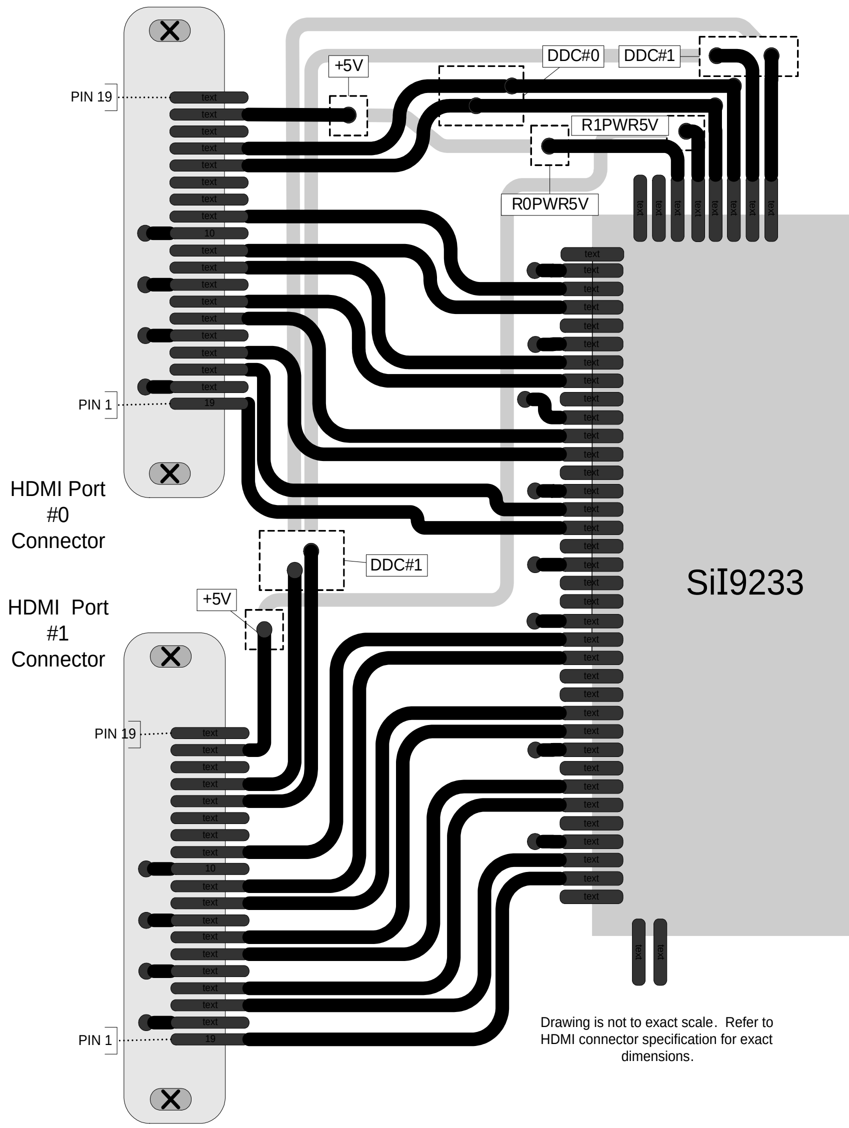


Figure 9.3. HDMI to Receiver Routing – Top View

Note the sixteen TMDS traces connected directly from the HDMI connectors (left) to the pins on the SiI9233 receiver (right). Trace impedance should be 100 Ω differential in each pair and 50 Ω single-ended if possible. Trace width and pitch depends on the PCB construction. Not all connections are shown — the drawing demonstrates routing of TMDS lines without crossovers, vias, or ESD protection. Refer also to Figure 9.9.

9.6. EMI Considerations

Electromagnetic interference is a function of board layout, shielding, HDMI Receiver component operating voltage, and frequency of operation, among other factors. When attempting to control emissions, do not place any passive components on the differential signal lines (aside from any essential ESD protection as described earlier). The differential signaling used in HDMI is inherently low in EMI as long as the routing recommendations noted in the Receiver Layout section are followed.

The PCB ground plane should extend unbroken under as much of the HDMI Receiver chip and associated circuitry as possible, with all ground pins of the chip using a common ground.

9.7. XTALIN Clock Required in All Designs

9.7.1. Description

The SiI9233 receiver uses the clock at the XTALIN/XTALOUT pin pair to control the internal audio pipeline. This clock is also used to control the interrupt processing, the internal reading of HDCP keys and internal CEC timing calibration.

The XTALIN/XTALOUT pin pair must be driven with a clock in all applications, even when the design does not support audio processing. The clock frequency must be 27.000 MHz.

9.7.2. Recommendation

For designs that do not support audio, the XTALIN pin can be connected to an ordinary 27-MHz LVTTL clock source, which is commonly available on HDMI sink designs. There is no requirement that this clock source be low jitter. The XTALOUT pin can be left unconnected when XTALIN is driven with a LVTTL clock.

9.8. Typical Circuit

Representative circuits for application of the SiI9233 HDMI Receiver chip are shown in Figure 9.4 through Figure 9.8. For a detailed review of your intended circuit implementation, contact your Lattice Semiconductor representative.

9.8.1. Power Supply Decoupling

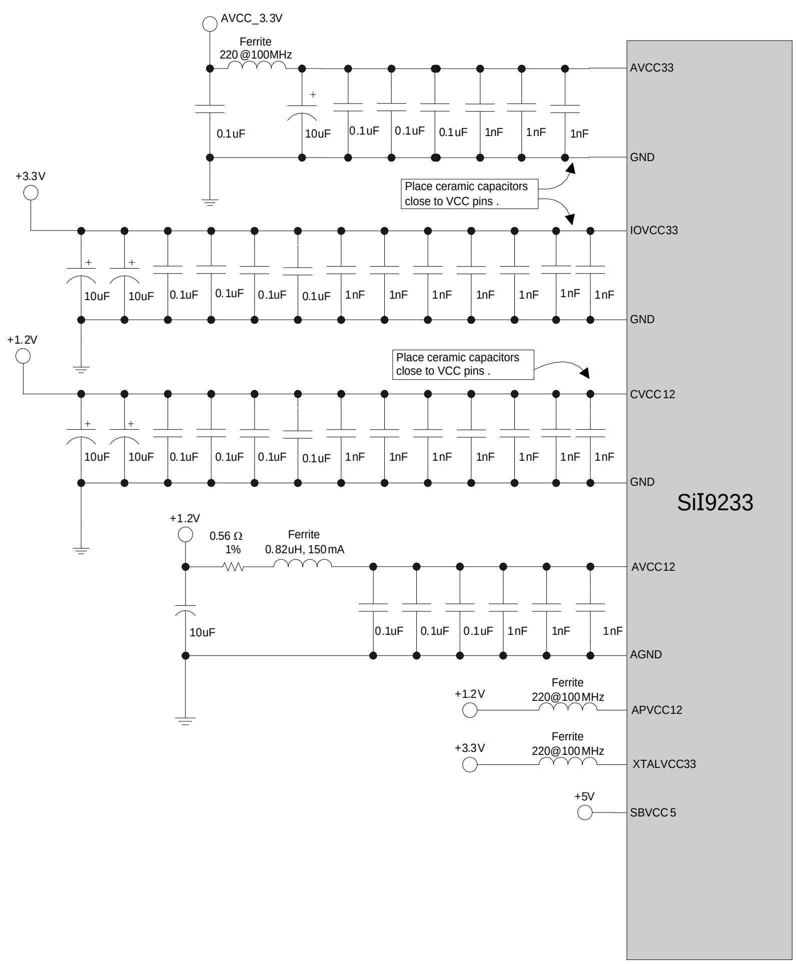


Figure 9.4. Power Supply Decoupling and PLL Filtering Schematic

The ferrite on AVCC33 attenuates noise above 10 kHz. A parasitic resistor helps to minimize the peaking. An example device (surface mount, 0805 package) is part number MLF2012DR82 from TDK. A data sheet is available at www.tdk.co.jp

9.8.2. HDMI Port Connections

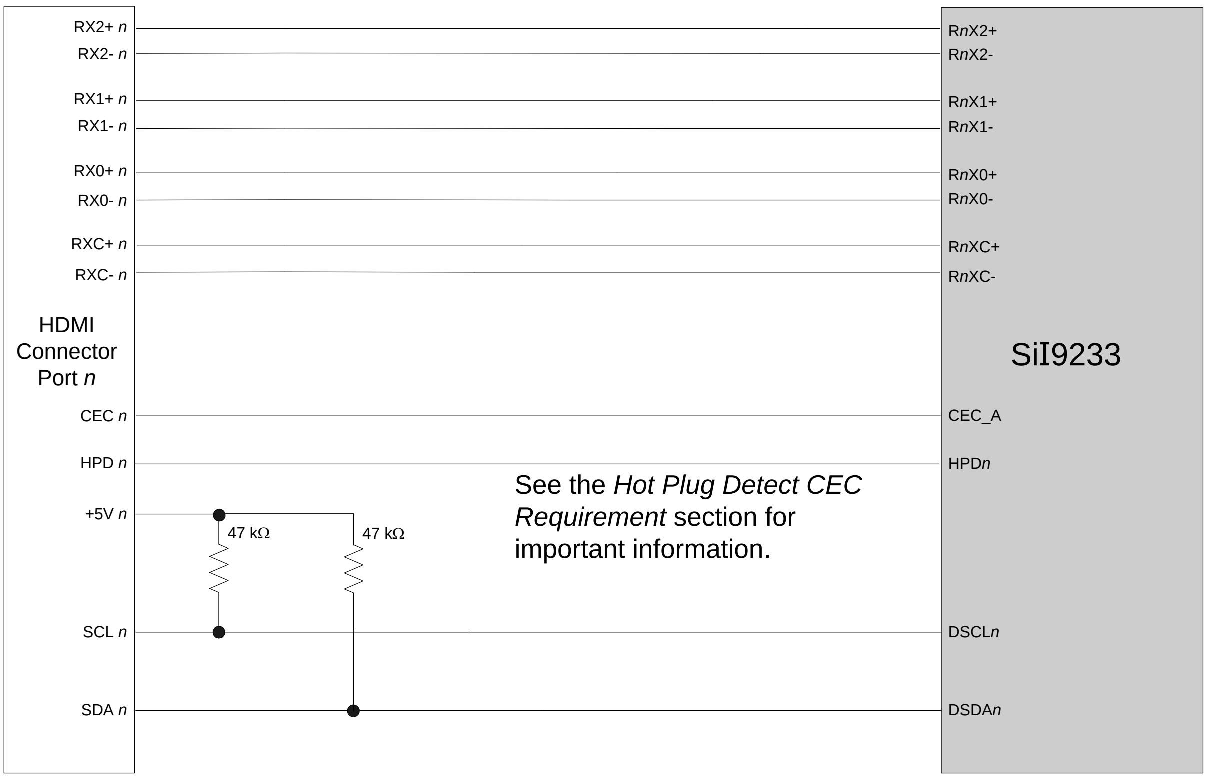


Figure 9.5. HDMI Port Connections Schematic

Note: Repeat the schematic for each HDMI input port on the SiI9233 receiver.

9.8.3. Digital Video Output Connections

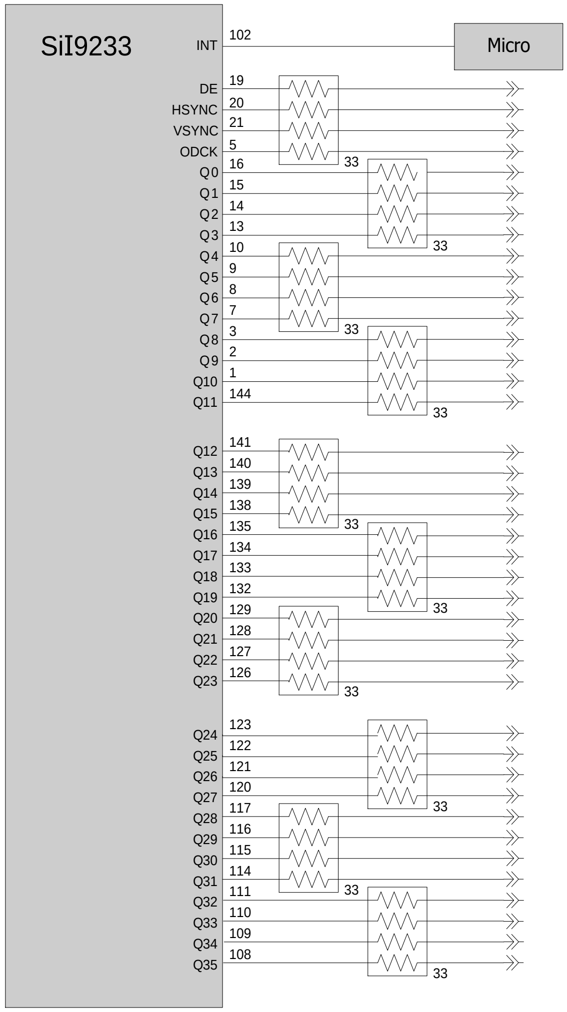


Figure 9.6. Digital Display Schematic

The 3.3V to the level-shifters and pull-up resistors should be powered-down whenever the 3.3 V is powered-down on the HDMI Receiver itself.

The HDMI Receiver's INT output can be connected as an interrupt to the microcontroller, or the microcontroller can poll register 0x70 (INTR_STATE) to determine if any of the enabled interrupts have occurred. Refer to the *SiI9223/9233/9127 HDMI Receivers Programmer's Reference* (SiI-PR-1019) for details. The HDMI Receiver's VSYNC output can be connected to the micro if it is necessary to monitor the vertical refresh rate of the incoming video.

9.8.4. Digital Audio Output Connections

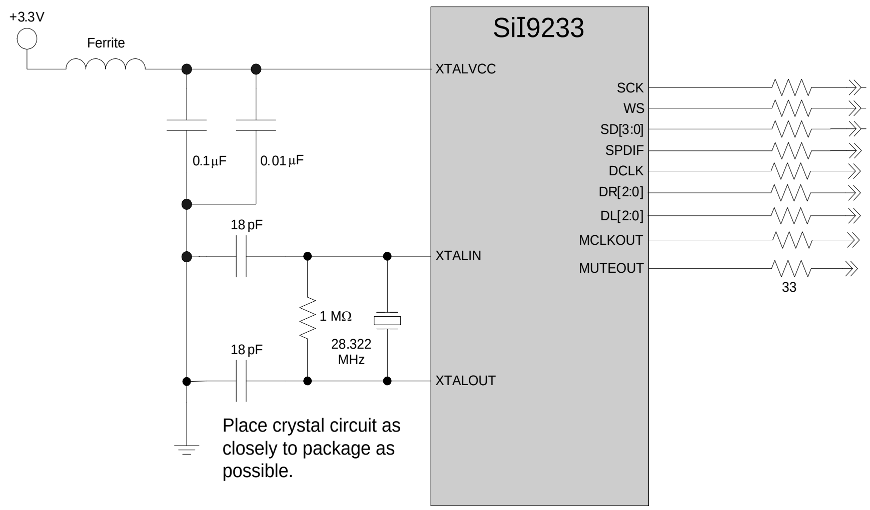


Figure 9.7. Audio Output Schematic

9.8.5. Control Signal Connections

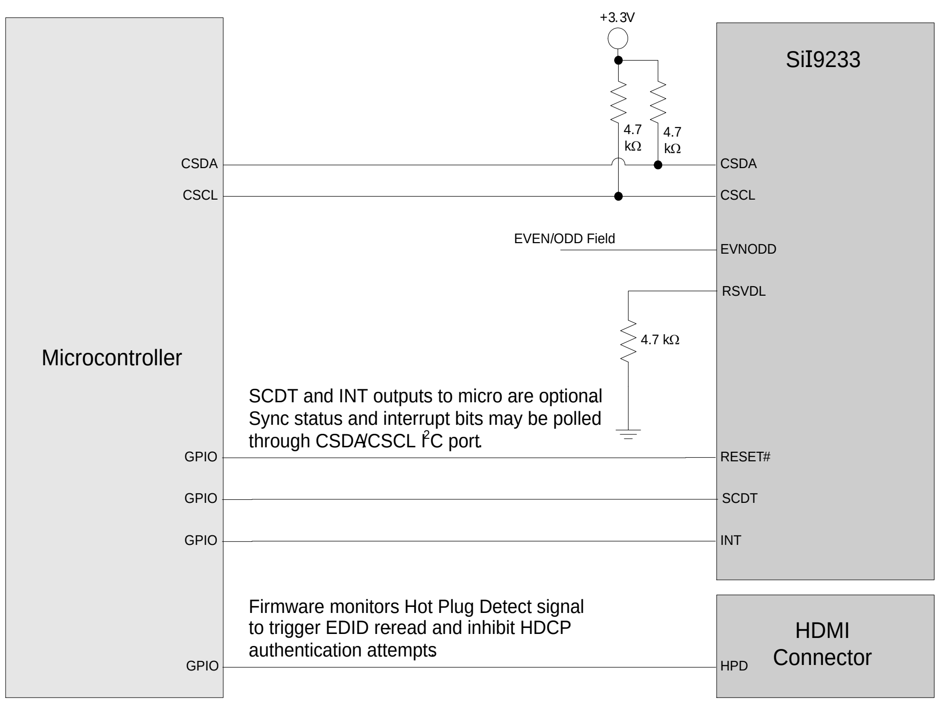


Figure 9.8. Controller Connections Schematic

9.9. Layout

Figure 9.9 shows an example of routing TMDS lines between the SiI9233 and the HDMI connector.

9.9.1. TMDS Input Port Connections

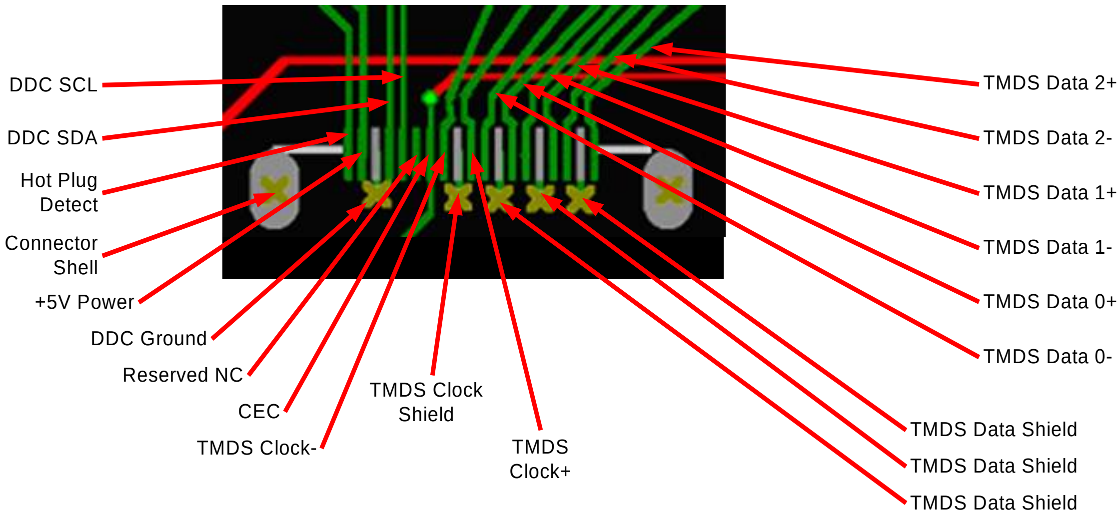
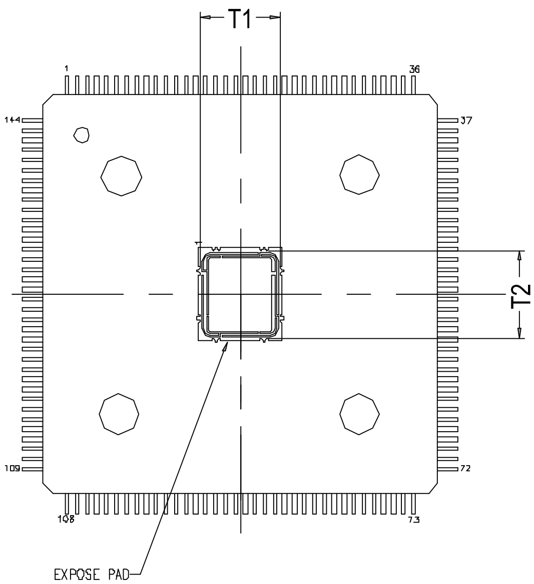


Figure 9.9. TMDS Input Signal Assignments

10. Packaging

10.1. ePad Enhancement

The SiI9233 receiver is packaged in a TQFP package with ePad that must be soldered to ground. The ePad dimensions are shown in Figure 10.1.



ePad Dimensions

		typ	max
T1	ePad Height	4.064	4.214
T2	ePad Width	4.445	4.595
ΔT	ePad tolerance		±.15

All dimensions are in millimeters.

Center the ePad on the package center lines with the tolerance shown.

A clearance of at least 0.25mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid any electrical shorts.

Tabs may have smaller dimensions than the maximums shown above, and may not appear at all, because minimum width and height are 0.0 mm.

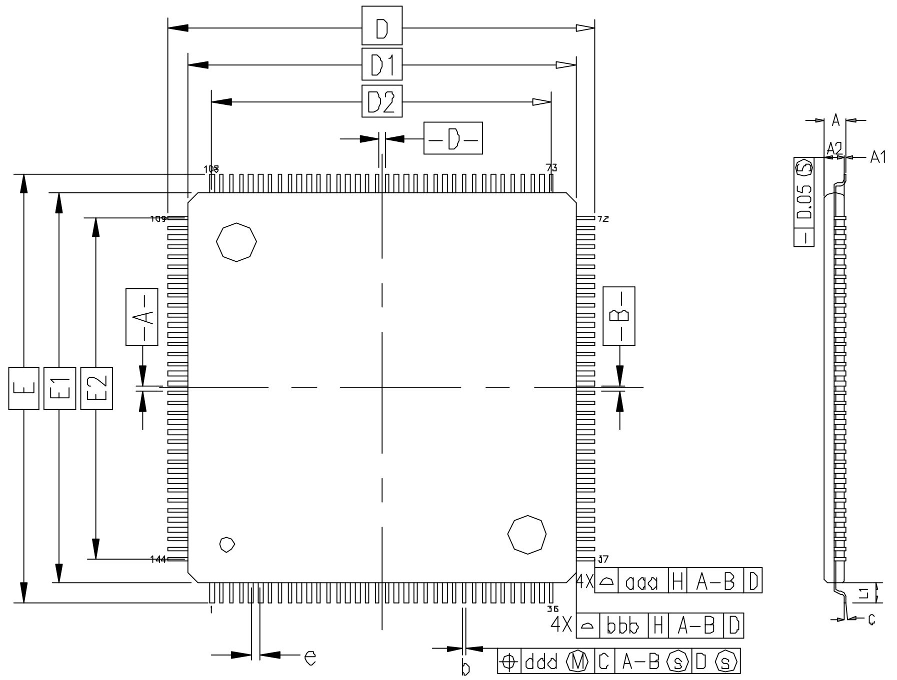
Lattice Semiconductor requires that the ePad be soldered to the PCB and electrically grounded on the PCB. The ePad must not be electrically connected to any other voltage level except ground (GND).

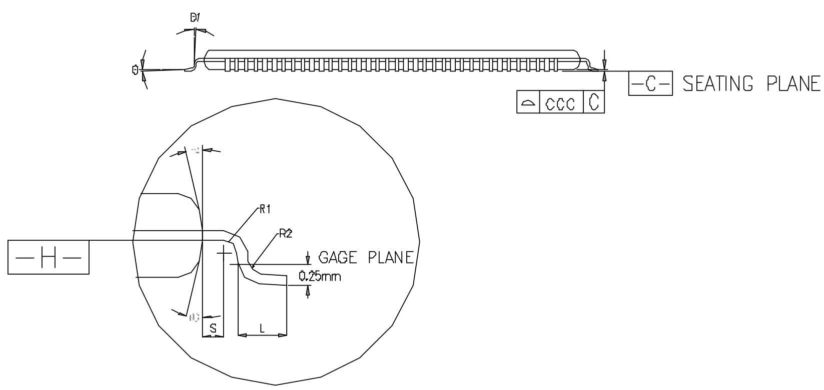
Figure 10.1. ePad Diagram

10.2. PCB Layout Guidelines

Refer to Lattice Semiconductor document *PCB Layout Guidelines: Designing with Exposed Pads* (SiI-AN-0129) for basic PCB design guidelines when designing with thermally enhanced packages using the exposed pad. This application note is intended for use by PCB layout designers.

10.3. 144-pin TQFP Package Dimensions





JEDEC Package Code MS-026-AFB

		typ	max
A	Thickness	1.10	1.20
A1	Stand-off	0.10	0.15
A2	Body Thickness	1.00	1.05
D1	Body Size	20.00	20.00
E1	Body Size	20.00	20.00
D	Footprint	22.00	22.00
E	Footprint	22.00	22.00
D2	Lead Row Width	17.50	17.50
E2	Lead Row Width	17.50	17.50
	Lead Count	144	
L1	Lead Length	1.00	
L	Lead Foot	0.60	0.75
b	Lead Width	0.20	0.27
c	Lead Thickness		0.20
e	Lead Pitch	0.50	0.50
aaa	Form Tolerance	0.20	0.20
bbb	Form Tolerance	0.20	0.20
ccc	Position Tolerance	0.08	0.08
ddd	Position Tolerance	0.08	0.08

Dimensions in millimeters.

Overall thickness A=A1+A2.

Figure 10.2. 144-Pin TQFP Package Diagram

10.4. Marking Specification

Drawing is not to scale and pin count shown is representative. Refer to specifics in Figure 10.2 on page 76.

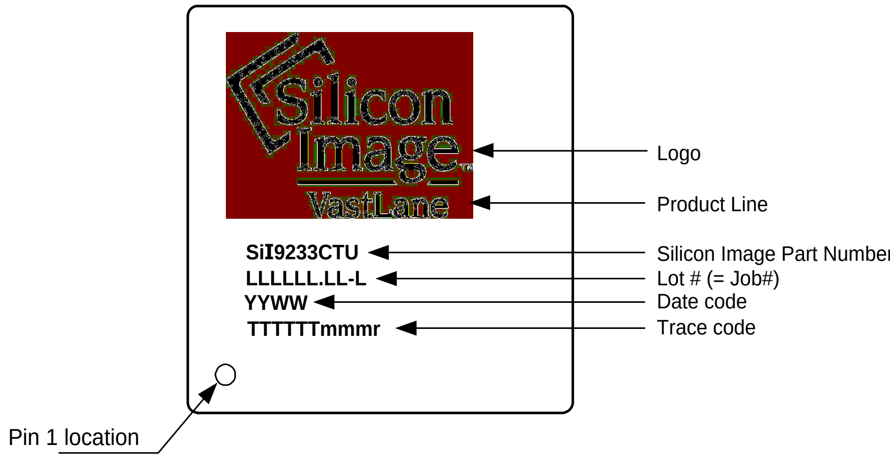


Figure 10.3. Marking Diagram

10.5. Ordering Information

Production Part Numbers:

SiI9233

TMDS Input Clock Range	Part Number
25–225 MHz	SiI9233CTU

The universal package may be used in lead-free and ordinary process lines.

Revision History

Revision A, March 2016

Updated to latest template.

Revision A, August 2008

First production release.

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