

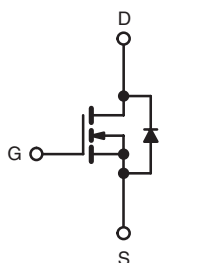
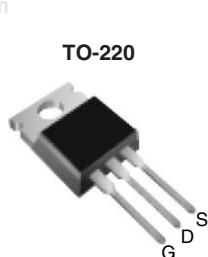


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	600 V	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V	1.2
Q_g (Max.) (nC)	39	
Q_{gs} (nC)	10	
Q_{gd} (nC)	19	
Configuration	Single	

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N-Channel MOSFET

FEATURES

- Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30 V, V_{GS} Rating
- Reduced C_{iss} , C_{oss} , C_{rss}
- Extremely High Frequency Operation
- Repetitive Avalanche Rated
- Lead (Pb)-free Available

RoHS*
COMPLIANT

DESCRIPTION

This new series of low charge Power MOSFETs achieve significantly lower gate charge over conventional Power MOSFETs. Utilizing the new LCDMOS technology, the device improvements are achieved without added product cost, allowing for reduced gate drive requirements and total system savings. In addition reduced switching losses and improved efficiency are achievable in a variety of high frequency applications. Frequencies of a few MHz at high current are possible using the new low charge Power MOSFETs.

These device improvements combined with the proven ruggedness and reliability that are characteristic of Power MOSFETs offer the designer a new standard in power transistors for switching applications.

ORDERING INFORMATION

Package	TO-220
Lead (Pb)-free	IRFBC40LCPbF
	SiHFBC40LC-E3
SnPb	IRFBC40LC
	SiHFBC40LC

ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$, unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Gate-Source Voltage			V _{GS}	± 30	V
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	I _D	6.2	A
		T _C = 100 °C		3.9	
Pulsed Drain Current ^a			I _{DM}	25	
Linear Derating Factor				1.0	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	530	mJ
Repetitive Avalanche Current ^a			I _{AR}	6.2	A
Repetitive Avalanche Energy ^a			E _{AR}	13	mJ
Maximum Power Dissipation	T _C = 25 °C		P _D	125	W
Peak Diode Recovery dV/dt ^c			dV/dt	3.0	V/ns
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300 ^d	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50$ V, starting $T_J = 25^\circ\text{C}$, $L = 25$ mH, $R_G = 25\ \Omega$, $I_{AS} = 6.2$ A (see fig. 12).
- $I_{SD} \leq 6.2$ A, $dI/dt \leq 80$ A/ μs , $V_{DD} \leq V_{DS}$, $T_J \leq 150^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

SPECIFICATIONS $T_J = 25\text{ °C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		600	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.70	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 600 V, V _{GS} = 0 V		-	-	100	μA
		V _{DS} = 480 V, V _{GS} = 0 V, T _J = 125 °C		-	-	500	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 3.7 A ^b	-	-	1.2	Ω
Forward Transconductance	g _{fs}	V _{DS} = 100 V, I _D = 3.7 A ^b		3.7	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V V _{DS} = 25 V f = 1.0 MHz, see fig. 5		-	1100	-	pF
Output Capacitance	C _{oss}			-	140	-	
Reverse Transfer Capacitance	C _{rss}			-	15	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 6.2 A, V _{DS} = 360 V, see fig. 6 and 13 ^b	-	-	39	nC
Gate-Source Charge	Q _{gs}			-	-	10	
Gate-Drain Charge	Q _{gd}			-	-	19	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 300 V, I _D = 6.2 A R _G = 9.1 Ω, R _D = 47 Ω, see fig. 10 ^b		-	12	-	ns
Rise Time	t _r			-	20	-	
Turn-Off Delay Time	t _{d(off)}			-	27	-	
Fall Time	t _f			-	17	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	6.2	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	25	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 6.2 A, V _{GS} = 0 V ^b		-	-	1.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 6.2 A, dI/dt = 100 A/μs ^b		-	440	680	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	2.1	3.2	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

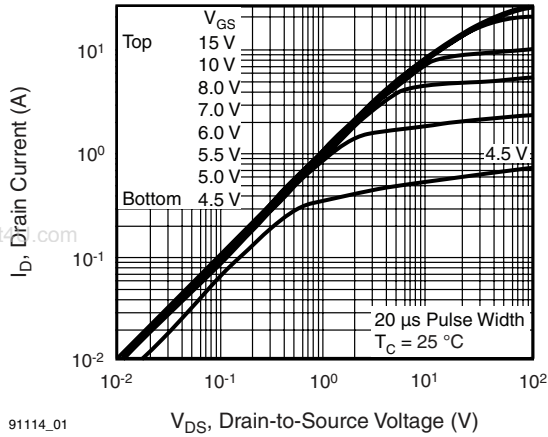


Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

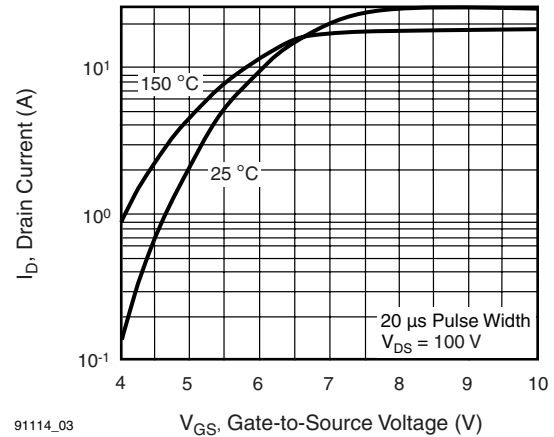


Fig. 3 - Typical Transfer Characteristics

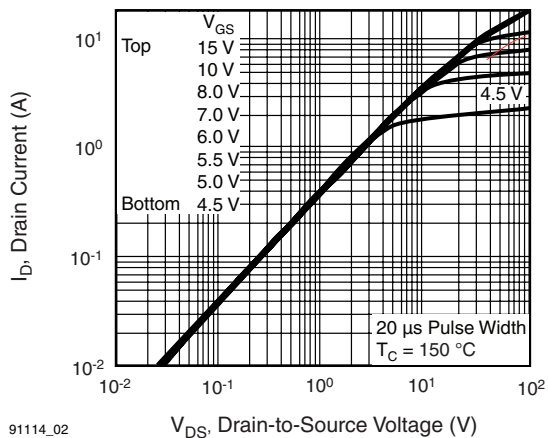


Fig. 2 - Typical Output Characteristics, $T_C = 150^\circ\text{C}$

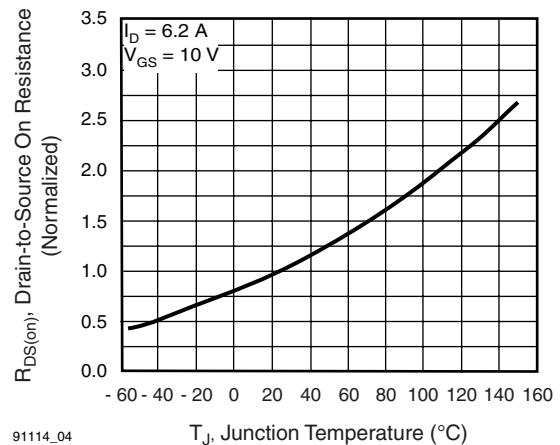
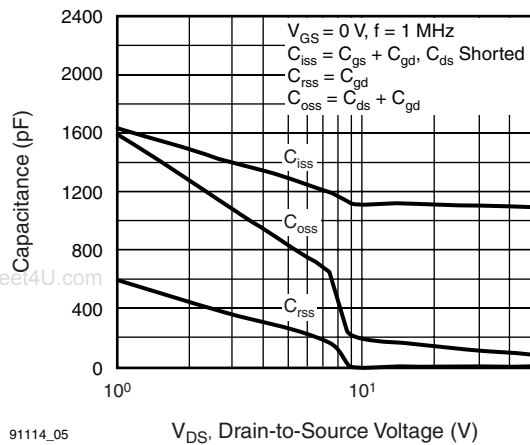
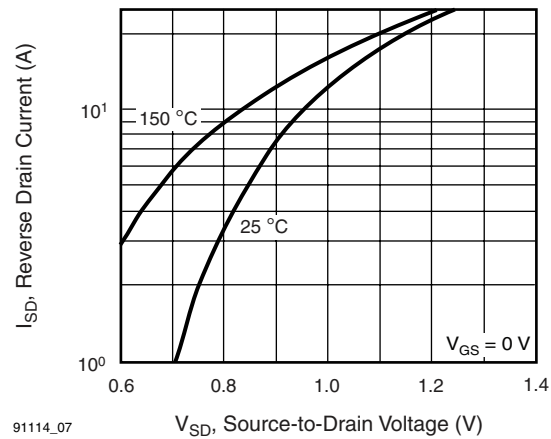


Fig. 4 - Normalized On-Resistance vs. Temperature



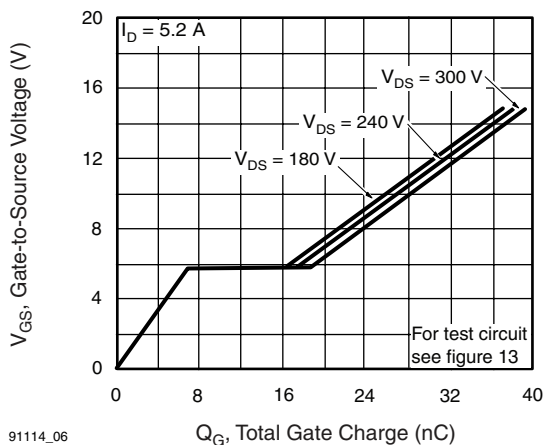
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Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



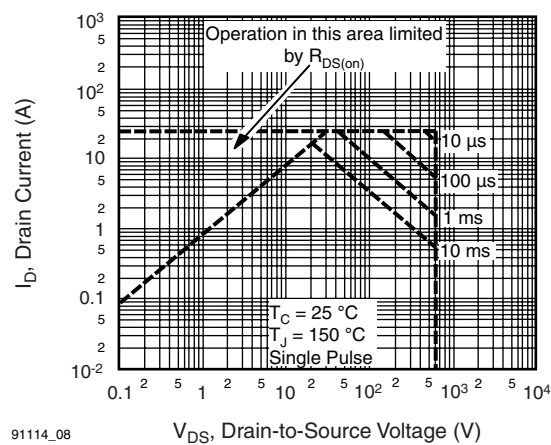
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Fig. 7 - Typical Source-Drain Diode Forward Voltage



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Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



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Fig. 8 - Maximum Safe Operating Area

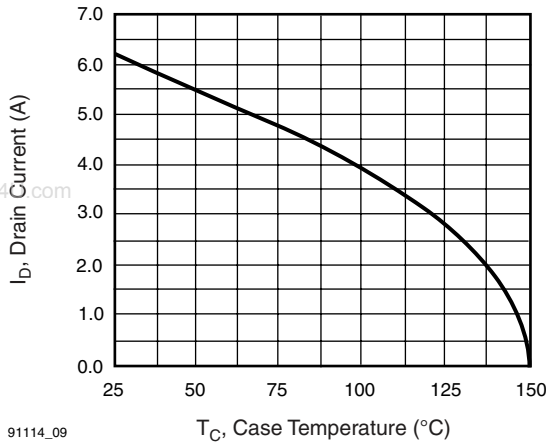


Fig. 9 - Maximum Drain Current vs. Case Temperature

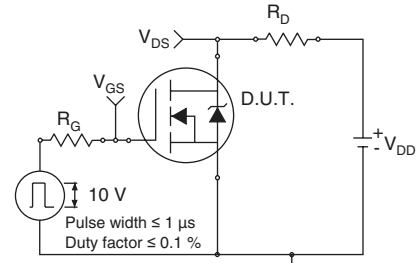


Fig. 10a - Switching Time Test Circuit

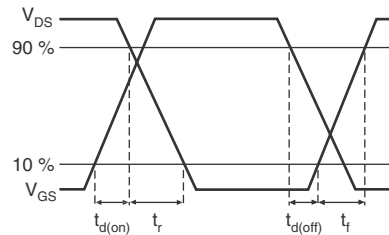


Fig. 10b - Switching Time Waveforms

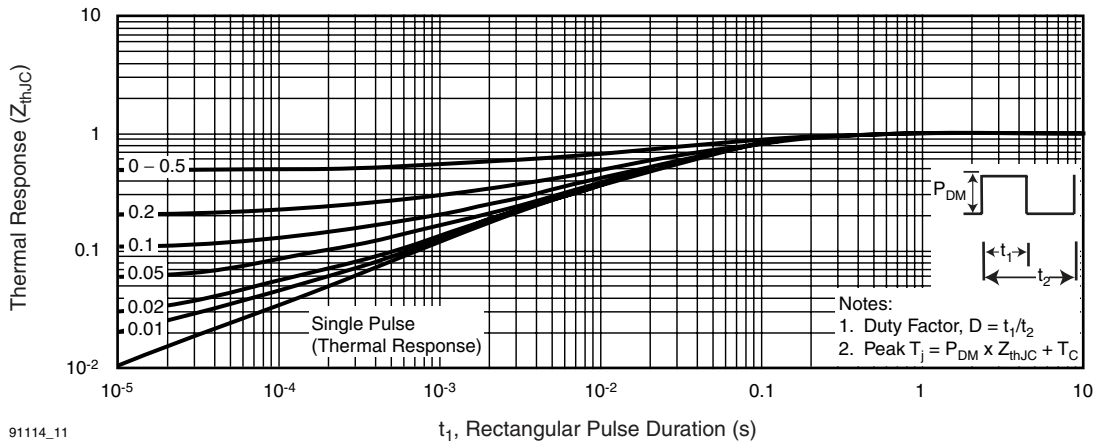


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

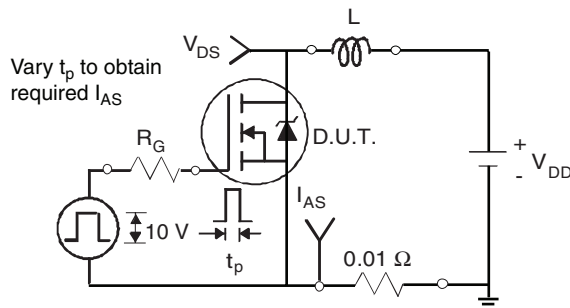


Fig. 12a - Unclamped Inductive Test Circuit

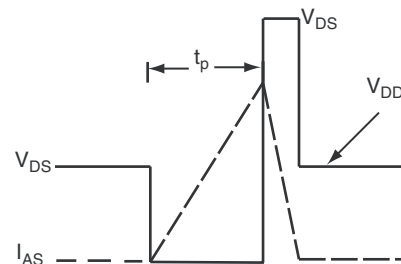


Fig. 12b - Unclamped Inductive Waveforms

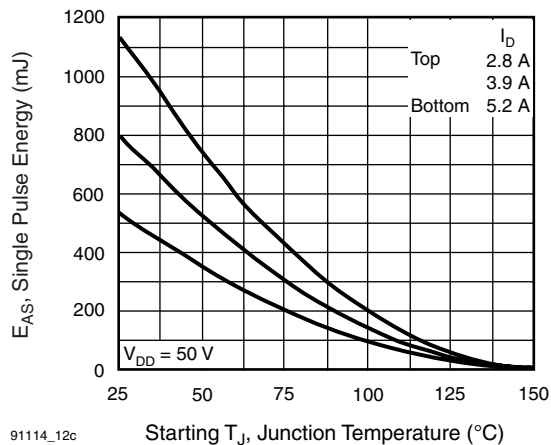


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

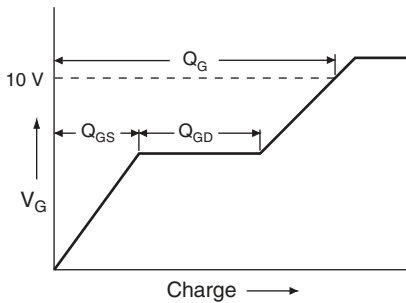


Fig. 13a - Basic Gate Charge Waveform

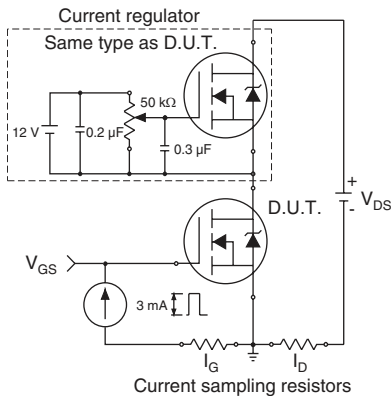


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

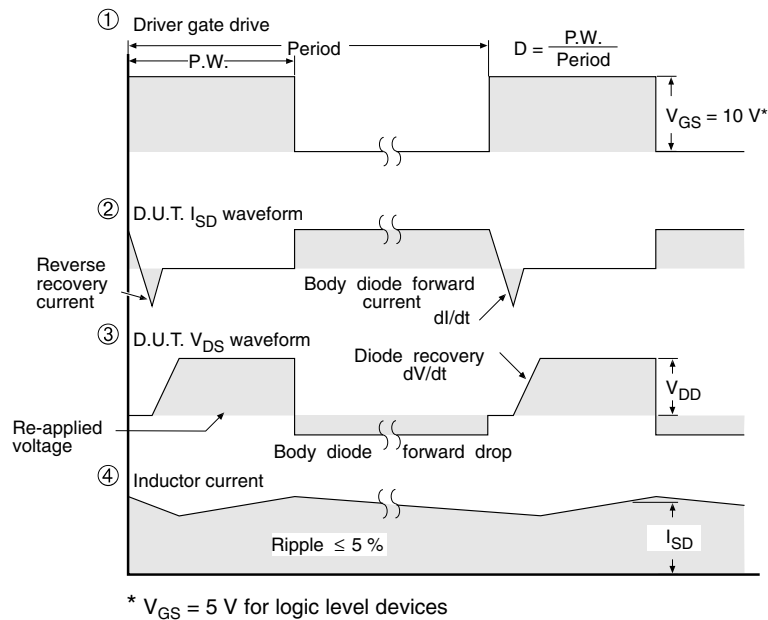
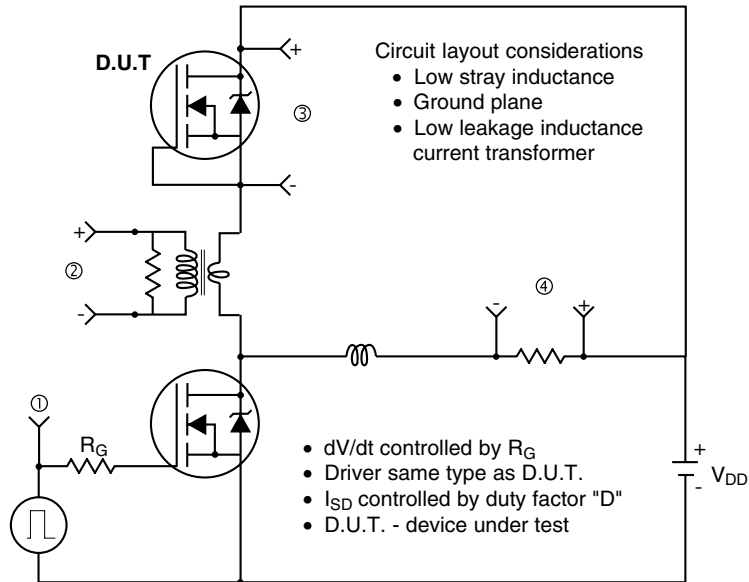


Fig. 14 -For N-Channel

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