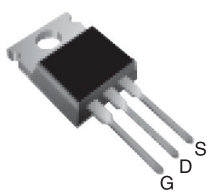
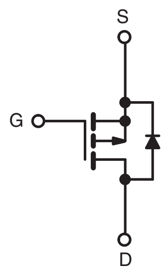
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	- 50	
$R_{DS(on)}$ (Ω)	V_{GS} = - 10 V	0.33
Q_g (Max.) (nC)	26	
Q_{gs} (nC)	6.2	
Q_{gd} (nC)	8.6	
Configuration	Single	

TO-220





P-Channel MOSFET

FEATURES

- P-Channel Versatility
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- Excellent Temperature Stability
- Lead (Pb)-free Available

Pb Available
RoHS*
COMPLIANT

DESCRIPTION

The Power MOSFET technology is the key to Vishay's advanced line of Power MOSFET transistors. The efficient geometry and unique processing of the Power MOSFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P-Channel Power MOSFET's are designed for application which require the convenience of reverse polarity operation. They retain all of the features of the more common N-Channel Power MOSFET's such as voltage control, very fast switching, ease of paralleling, and excellent temperature stability.

P-Channel Power MOSFETs are intended for use in power stages where complementary symmetry with N-Channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.

ORDERING INFORMATION	
Package	TO-220
Lead (Pb)-free	IRF9Z22PbF
	SiHF9Z22-E3
SnPb	IRF9Z22
	SiHF9Z22

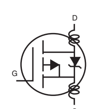
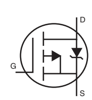
ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	- 50	V
Gate-Source Voltage			V_{GS}	± 20	
Drain-Gate Voltage (R_{GS} = 20 KΩ)			V_{GDR}	- 50	
Continuous Drain Current	V_{GS} at - 10 V	T_C = 25 °C	I_D	- 8.9	A
		T_C = 100 °C		- 5.6	
Pulsed Drain Current[a]			I_{DM}	- 36	
Linear Derating Factor				0.32	W/°C
Inductive Current, Clamped	L = 100 µH		I_{LM}	- 36	A
Unclamped Inductive Current (Avalanche Current)			I_L	- 2.2	A
Maximum Power Dissipation	T_C = 25 °C		P_D	40	W
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = - 25 V, starting T_J = 25 °C, L =100 µH, R_G = 25 Ω
c. $I_{SD} \leq$ - 6.7 A, dI/dt ≤ 90 A/µs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 175 °C.
d. 0.063" (1.6 mm) from case.
* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	80	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	1.0	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.1	

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 50	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 2.0	-	- 4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = max. rating, V_{GS} = 0 V	-	-	- 250	µA
		V_{DS} = max. rating x 0,8, V_{GS} = 0 V, T_J =125°C	-	-	- 1000	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = - 10 V, I_D = - 5.6 A[b]	-	0.28	0.33	Ω
Forward Transconductance	g_{fs}	V_{DS} = 2 x V_{GS}, I_{DS} = - 5.6 A[b]	2.3	3.5	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = - 25 V, f = 1.0 MHz, see fig. 9	-	480	-	pF
Output Capacitance	C_{oss}		-	320	-	
Reverse Transfer Capacitance	C_{rss}		-	58	-	
Total Gate Charge	Q_g	V_{GS} = - 10 V, I_D = - 9.7 A, V_{DS} = - 0.8 max. rating. see fig. 17	-	17	26	nC
Gate-Source Charge	Q_{gs}		-	4.1	6.2	
Gate-Drain Charge	Q_{gd}		-	5.7	8.6	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 25 V, I_D = - 9.7 A, R_G = 18 Ω, R_D = 2.4 Ω, see fig. 16 (MOSFET switching times are essentially independent of operating temperature)	-	8.2	12	ns
Rise Time	t_r		-	57	86	
Turn-Off Delay Time	$t_{d(off)}$		-	12	18	
Fall Time	t_f		-	25	38	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	- 9.7	A
Pulsed Diode Forward Current[a]	I_{SM}		-	-	- 39	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = - 9.7 A, V_{GS} = 0 V[b]	-	-	- 6.3	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = - 9.7 A, dI/dt = 100 A/µs[b]	56	110	280	ns
Body Diode Reverse Recovery Charge	Q_{rr}		0.17	0.34	0.85	µC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

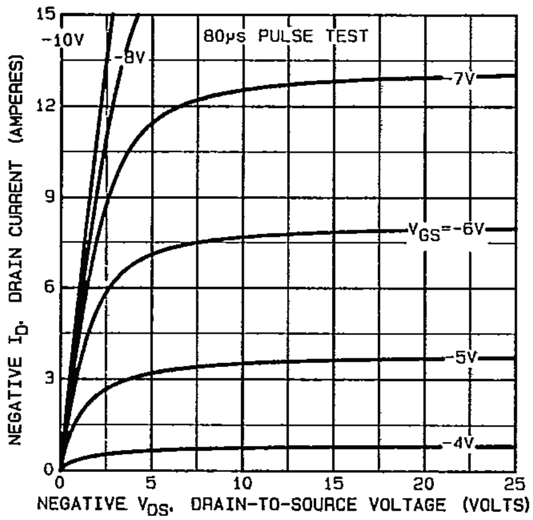


Fig. 1 - Typical Output Characteristics

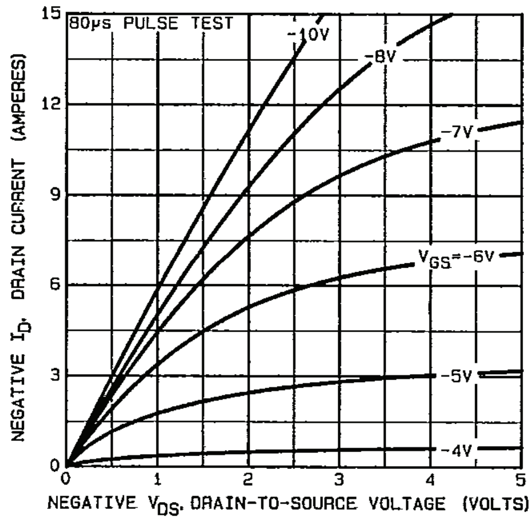


Fig. 3 - Typical Saturation Characteristics

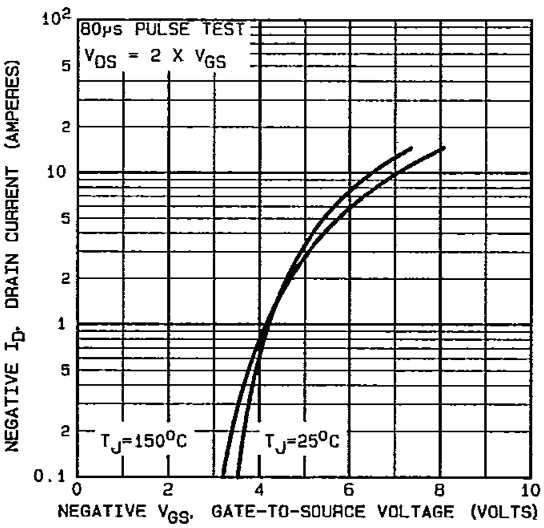


Fig. 2 - Typical Transfer Characteristics

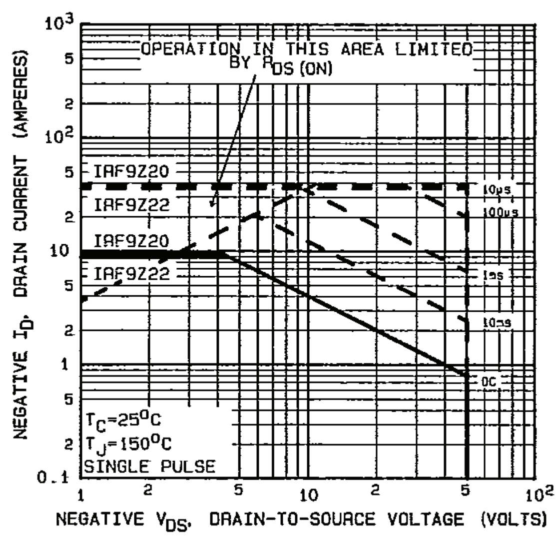


Fig. 4 - Maximum Safe Operating Area

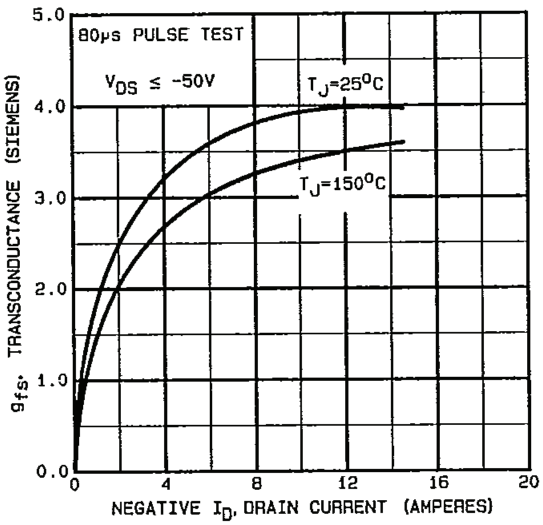


Fig. 5 - Typical Transconductance vs. Drain Current

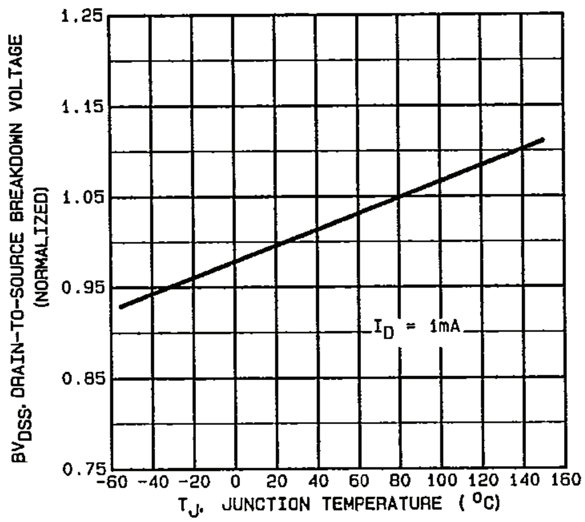


Fig. 7 - Typical Source-Drain Diode Forward Voltage

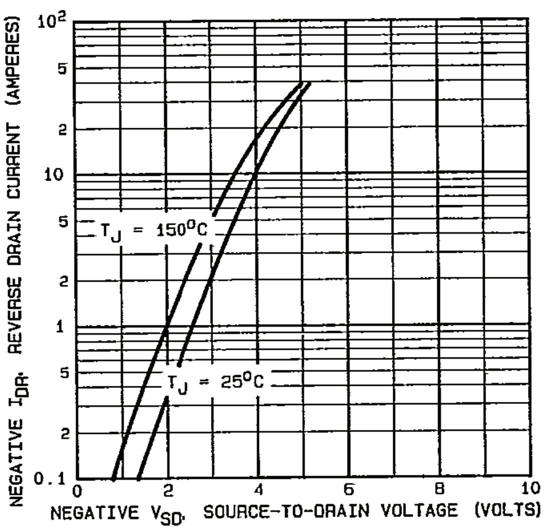


Fig. 6 - Breakdown Voltage vs. Temperature

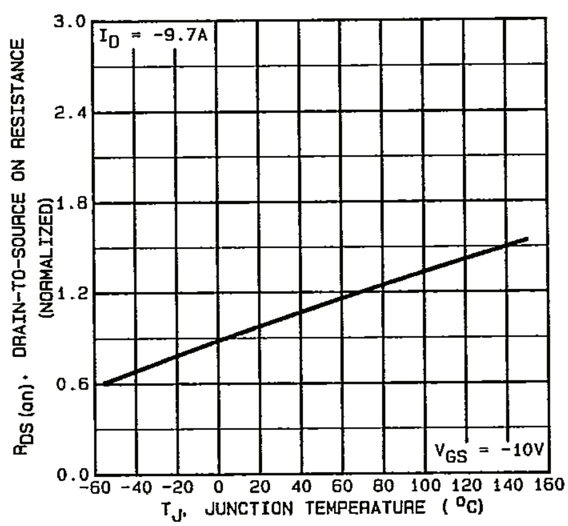


Fig. 8 - Normalized On-Resistance vs. Temperature

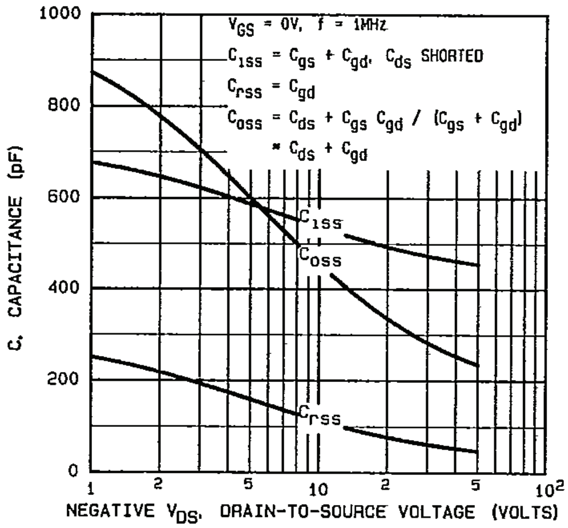


Fig. 9 - Typical Capacitance vs. Drain-to-Source Voltage

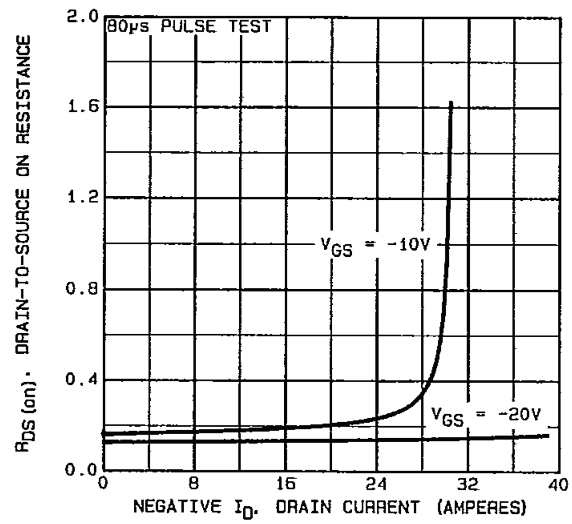


Fig. 11 - Typical Gate Charge vs. Gate-to-Source Voltage

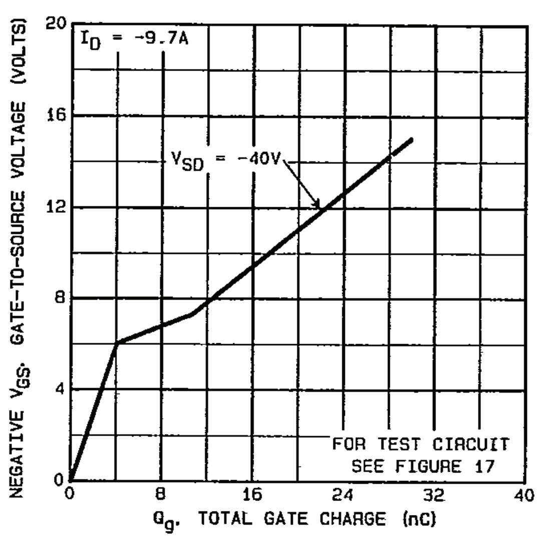


Fig. 10 - Typical Gate Charge vs. Gate-to-Source Voltage

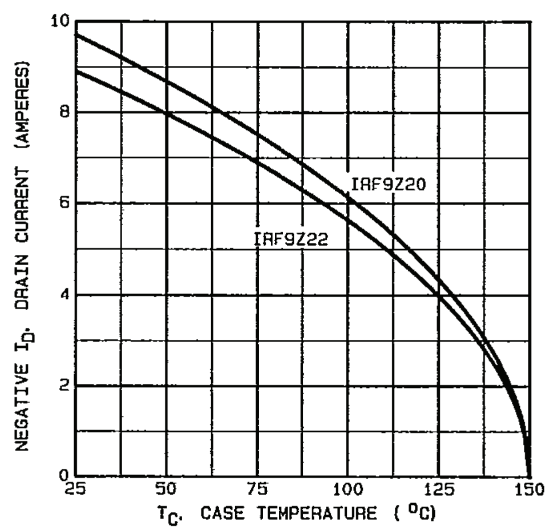


Fig. 12 - Maximum Drain Current vs. Case Temperature

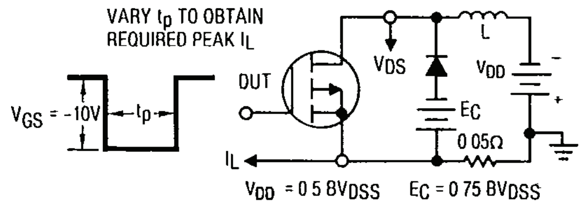


Fig. 13a - Clamped Inductive Test Circuit

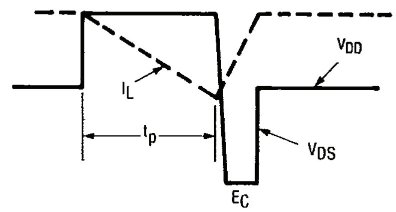


Fig. 13b - Clamped Inductive Waveforms

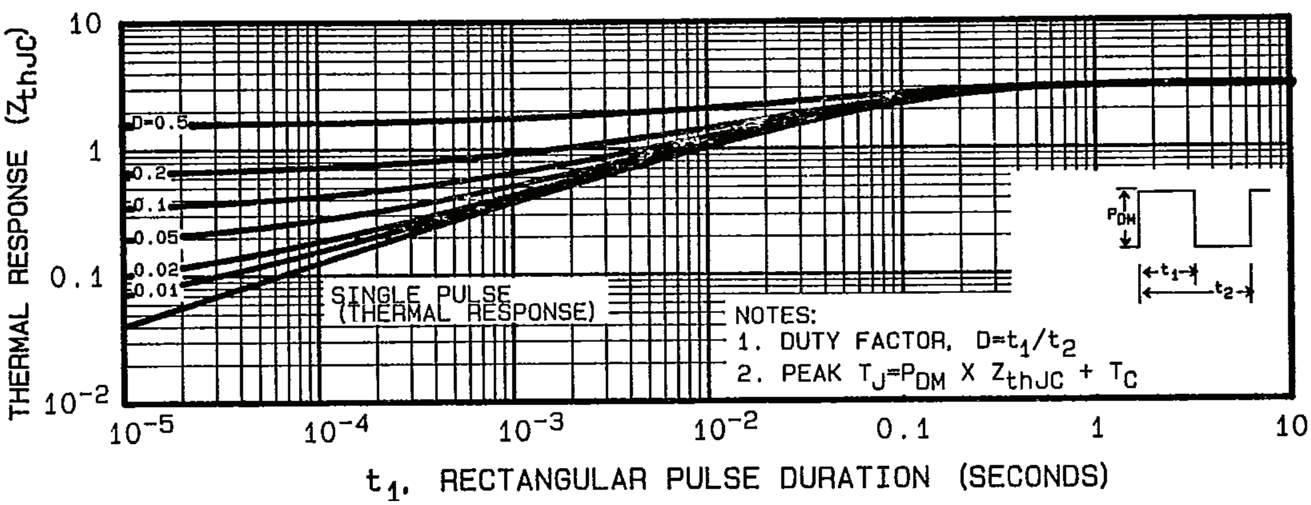


Fig. 14 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration

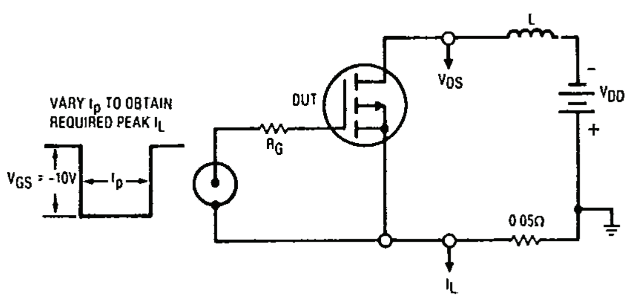


Fig. 15a - Unclamped Inductive Test Circuit

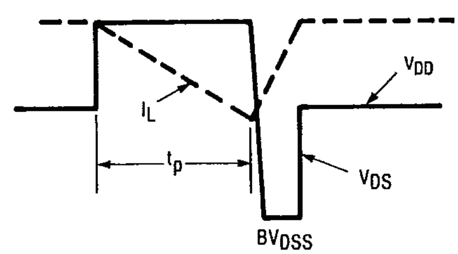


Fig. 15b - Unclamped Inductive Load Test Waveforms

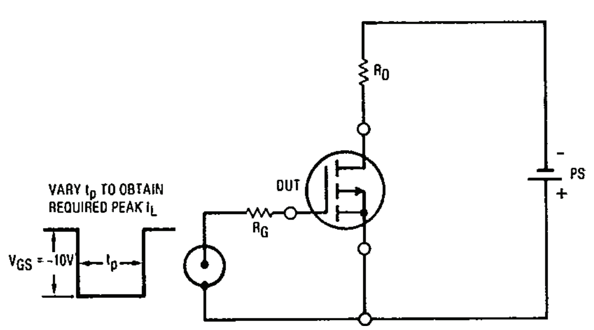


Fig. 16 - Switching Time Test Circuit

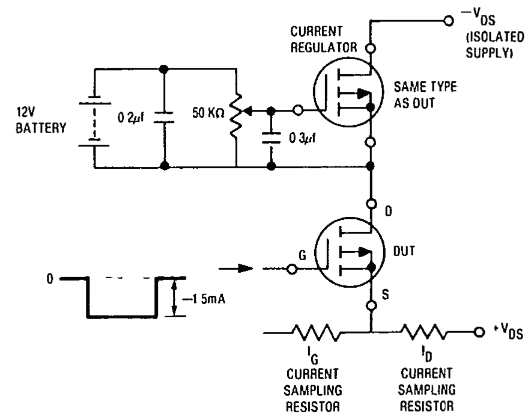


Fig. 17 - Gate Charge Test Circuit

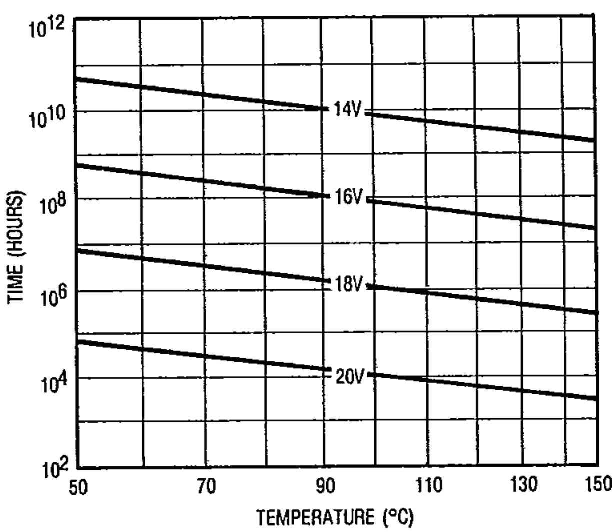


Fig. 18 - Typical Time to Accumulated 1 % Gate Failure

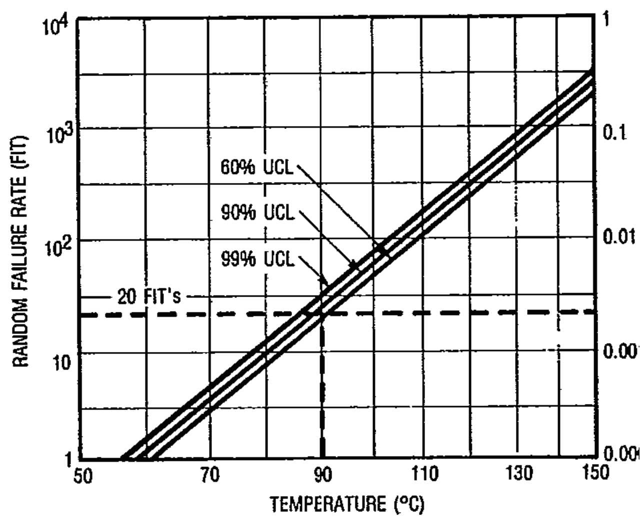
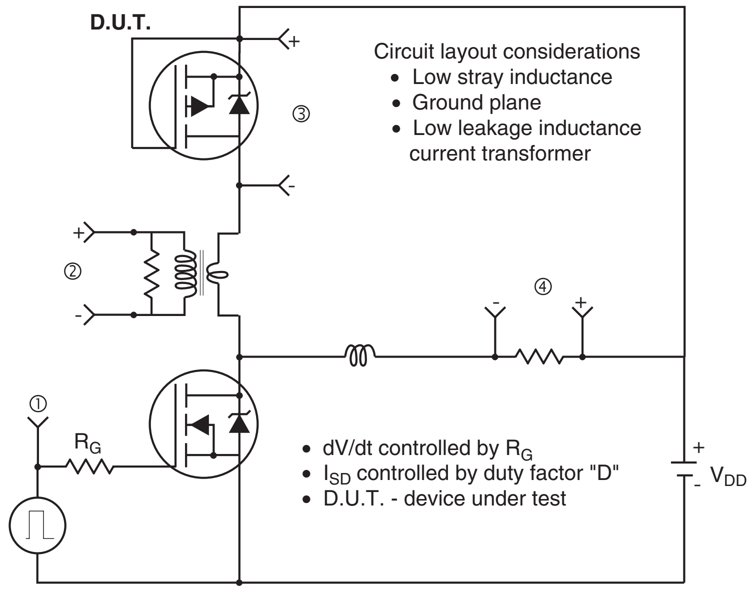
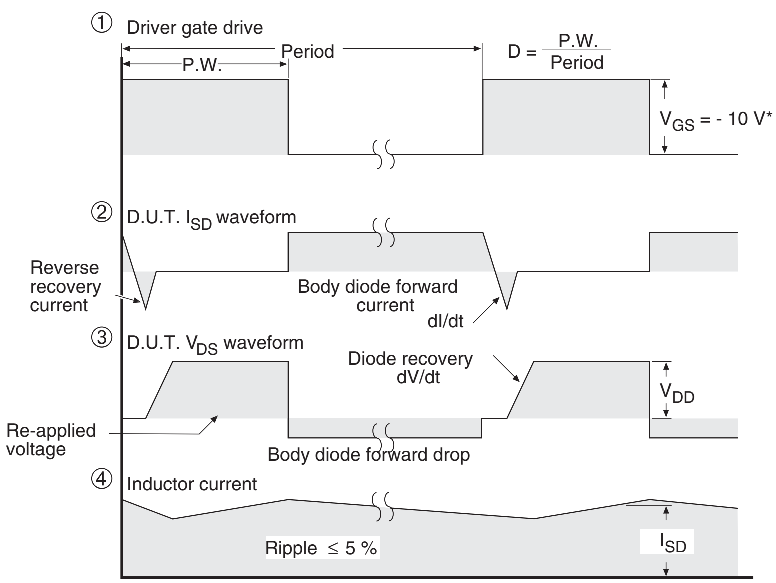


Fig. 19 - Typical High Temperature Reverse Bias (HTRB) Failure Rate

Peak Diode Recovery dV/dt Test Circuit



• Compliment N-Channel of D.U.T. for driver



* V_{GS} = - 5 V for logic level and - 3 V drive devices

Fig. 20 - For P-Channel

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