



P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY									
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)	Q _g (Typ.)						
- 20	0.025 at V _{GS} = - 4.5 V	- 12 ^a							
	0.031 at V _{GS} = - 2.5 V	- 12 ^a	24 nC						
	0.041 at V _{GS} = - 1.8 V		24 110						
	0.070 at V _{GS} = - 1.5 V	- 4							

FEATURES

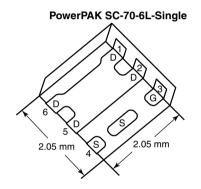
- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® SC-70 Package
 - Small Footprint Area
 - Low On-Resistance
- 100 % R_q Tested
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

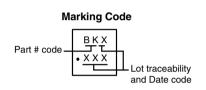
COMPLIANT HALOGEN

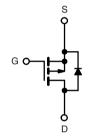
FREE

APPLICATIONS

Load Switch, PA Switch and Battery Switch for Portable







Ordering Information:

SiA431DJ-T4-GE3 (Lead (Pb)-free and Halogen-free) SiA431DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

P-Channel MOSFET

ABSOLUTE MAXIMUM RATING	S T _A = 25 °C, unles	ss otherwise not	ed	
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	- 20	V
Gate-Source Voltage		V _{GS}	± 8	v
Continuous Drain Current (T _J = 150 °C)	$T_{C} = 25 ^{\circ}\text{C}$ $T_{C} = 70 ^{\circ}\text{C}$ $T_{A} = 25 ^{\circ}\text{C}$ $T_{A} = 70 ^{\circ}\text{C}$	I _D	- 12 ^a - 12 ^a - 12 ^a - 9.6 ^{b, c} - 7.7 ^{b, c}	A
Pulsed Drain Current	*	I _{DM} - 30		
Continuous Source-Drain Diode Current	$T_{C} = 25 ^{\circ}\text{C}$ $T_{A} = 25 ^{\circ}\text{C}$	I _S	- 12 ^a - 2.9 ^{b, c}	
Maximum Power Dissipation	$T_{C} = 25 ^{\circ}\text{C}$ $T_{C} = 70 ^{\circ}\text{C}$ $T_{A} = 25 ^{\circ}\text{C}$ $T_{A} = 70 ^{\circ}\text{C}$	P _D	19 12 3.5 ^{b, c} 2.2 ^{b, c}	w
Operating Junction and Storage Temperature R	T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperatur	e) ^{d, e}	J	260	

THERMAL RESISTANCE RATINGS									
Parameter	Symbol	Typical	Maximum	Unit					
Maximum Junction-to-Ambient ^{b, f}	t ≤ 5 s	R _{thJA}	28	36	°C/W				
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	5.3	6.5	O/ VV				

Notes:

- a. Package limited.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 5 s.
- d. See Solder Profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under Steady State conditions is 80 °C/W.

Document Number: 65267 S12-1141-Rev. B, 21-May-12

SiA431DJ

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SPECIFICATIONS T _J = 25 °C, unless otherwise noted									
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit			
Static	W	V _{GS} = 0 V, I _D = - 250 μA	00			\ \/			
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 20	44.5		V			
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 14.5		mV/°C			
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			2.7					
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 0.4		- 0.85	V			
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V			± 100	nA			
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 20 V, V _{GS} = 0 V			- 1	μΑ			
	500	$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			- 10				
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	- 20			Α			
		$V_{GS} = -4.5 \text{ V}, I_D = -6.5 \text{ A}$		0.020	0.025				
Drain Course On State Projectones	R _{DS(on)}	$V_{GS} = -2.5 \text{ V}, I_D = -5.8 \text{ A}$		0.025	0.031	Ω			
Drain-Source On-State Resistance ^a	1 (DS(on)	$V_{GS} = -1.8 \text{ V}, I_D = -2.5 \text{ A}$		0.034	0.041				
		V _{GS} = - 1.5 V, I _D = - 1.5 A		0.045	0.070				
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 10 V, I _D = - 6.5 A		31		S			
Dynamic ^b				•	l	l			
Input Capacitance	C _{iss}			1700		pF			
Output Capacitance	C _{oss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		230					
Reverse Transfer Capacitance	C _{rss}			205					
Total Cata Chausa	0	V _{DS} = - 10 V, V _{GS} = - 8 V, I _D = - 9.6 A		40	60	nC			
Total Gate Charge	Qg			24	36				
Gate-Source Charge	Q _{gs}	V _{DS} = - 10 V, V _{GS} = - 4.5 V, I _D = - 9.6 A		2.4					
Gate-Drain Charge	Q_{gd}			6.5					
Gate Resistance	R_{g}	f = 1 MHz	1.3	6.3	13	Ω			
Turn-On Delay Time	t _{d(on)}			22	35				
Rise Time	t _r	$V_{DD} = -10 \text{ V}, R_{L} = 1.3 \Omega$		25	40				
Turn-Off Delay Time	t _{d(off)}	$I_D \cong -7.7 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$		65	100				
Fall Time	t _f			25	40				
Turn-On Delay Time	t _{d(on)}			10	15	ns			
Rise Time	t _r	$V_{DD} = -10 \text{ V, R}_{L} = 1.3 \Omega$		10	15				
Turn-Off Delay Time	t _{d(off)}	$I_D \cong -7.7 \text{ A}, V_{GEN} = -8 \text{ V}, R_g = 1 \Omega$		65	100	•			
Fall Time	t _f	<u> </u>		20	30	1			
Drain-Source Body Diode Characterist									
Continuous Source-Drain Diode Current	Is	T _C = 25 °C			- 12				
Pulse Diode Forward Current	I _{SM}	-			- 30	Α			
Body Diode Voltage	V _{SD}	I _S = - 7.7 A, V _{GS} = 0 V		- 0.8	- 1.2	V			
Body Diode Reverse Recovery Time	t _{rr}	, do		35	60	ns			
Body Diode Reverse Recovery Charge	Q _{rr}	1		21	35	nC			
Reverse Recovery Fall Time	t _a	I _F = - 7.7 A, dI/dt = 100 A/μs, T _J = 25 °C		20	30				
Reverse Recovery Rise Time	t _b	1		15		ns			
Tieverse Hecovery Hise Time	ър.			10	1				

Notes:

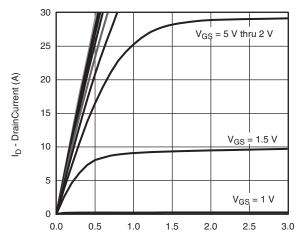
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

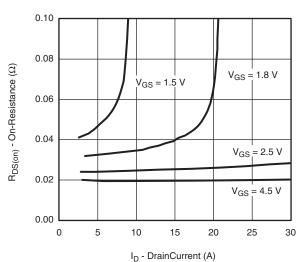


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

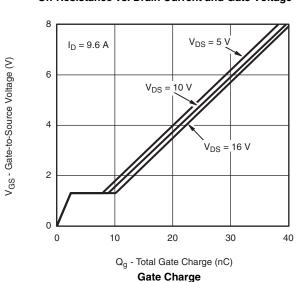


V_{DS} - Drain-to-Source Voltage (V)



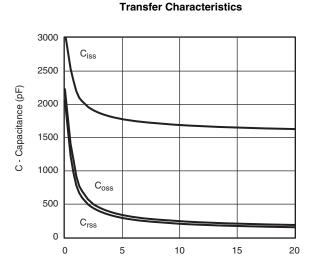


On-Resistance vs. Drain Current and Gate Voltage



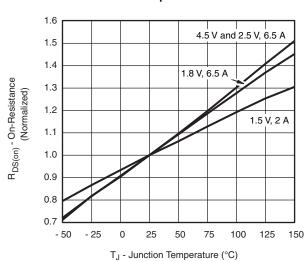
 $T_{C} = -55 \, ^{\circ}C$ $T_{C} = 125 \, ^{\circ}C$ $T_{C} = 25 \, ^{\circ}C$ $T_{C} = 25 \, ^{\circ}C$ $T_{C} = 25 \, ^{\circ}C$ $T_{C} = 125 \, ^{\circ}C$

V_{GS} - Gate-to-Source Voltage (V)



V_{DS} - Drain-to-Source Voltage (V)

Capacitance



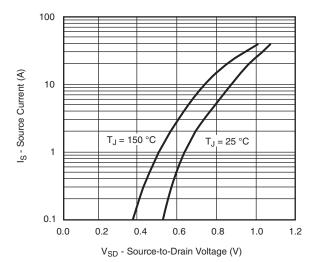
On-Resistance vs. Junction Temperature

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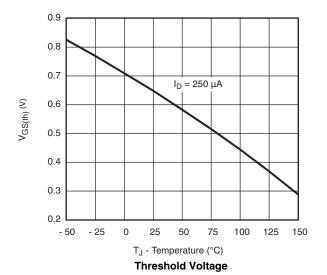
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

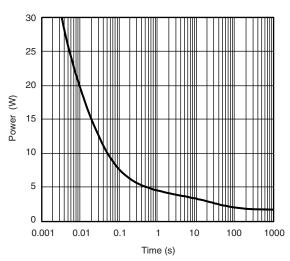


Soure-Drain Diode Forward Voltage

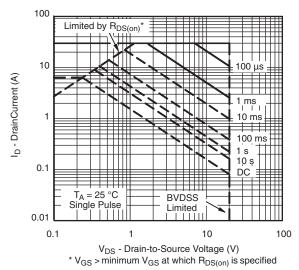


V_{GS} - Gate-to-Source Voltage (V)

On-Resistance vs. Gate-to-Source Voltage



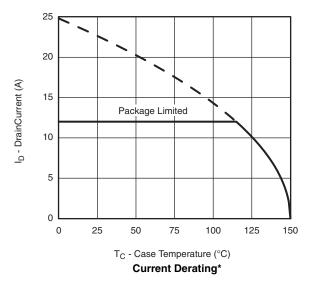
Single Pulse Power, Junction-to-Ambient

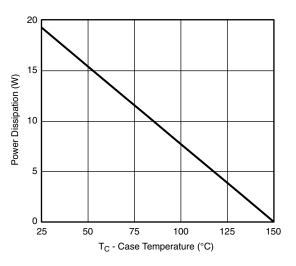


Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





Power Derating

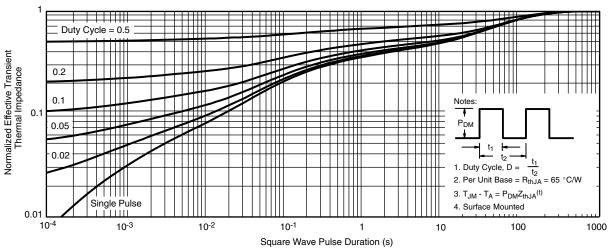
^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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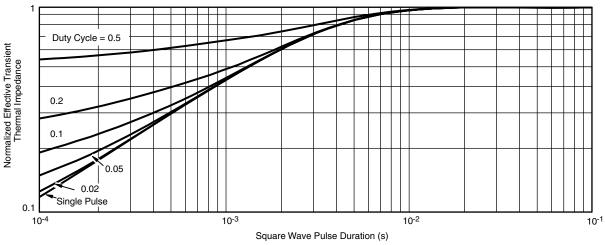
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65267.





PowerPAK® SC70-6L





BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



- All dimensions are in millimeters
 Package outline exclusive of mold flash and metal burr
 Package outline inclusive of plating

			SINGL	NGLE PAD DUAL PAD								
DIM	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
Α	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
С	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
е		0.65 BSC			0.026 BSC		0.65 BSC			0.026 BSC		
K		0.275 TYP			0.011 TYP		0.275 TYP		0.011 TYP			
K1		0.400 TYP		0.016 TYP		0.320 TYP			0.013 TYP			
K2		0.240 TYP		0.009 TYP		0.252 TYP		0.010 TYP				
К3		0.225 TYP		0.009 TYP					•	•		
K4		0.355 TYP		0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006

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DWG: 5934

06-Aug-07



RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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ATTLICATION NOT



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