COMPLIANT

HALOGEN

FREE





Dual P-Channel 20 V (D-S) MOSFET

PRODU	ICT SUMMARY		
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)	Q _g (Typ.)
- 20	$0.059 \text{ at V}_{GS} = -4.5 \text{ V}$	- 6 ^a	6.9 nC
- 20	0.096 at V _{GS} = - 2.5 V	- 6 ^a	0.5110

FEATURES

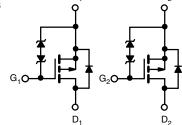
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- New Thermally Enhanced PowerPAK[®] ChipFET[®] Package
 - Small Footprint Area
 - Low On-Resistance
 - Thin 0.8 mm Profile
- Typical ESD Performance 1500 V in HBM
- Compliant to RoHS Directive 2002/95/EC

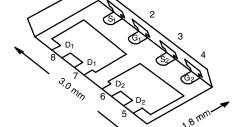
APPLICATIONS

 Load Switch and Charger Switch for Portable Devices

DC/DC Converters

Lot Traceability and Date Code





PowerPAK ChipFET Dual

Bottom View

Ordering Information: Si5999EDU-T1-GE3 (Lead (Pb)-free and Halogen-free)

P-Channel MOSFET P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	S (T _A = 25 °C, unle	ess otherwise	noted)		
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage		V_{DS}	- 20	V	
Gate-Source Voltage		V_{GS}	± 12	ľ	
	T _C = 25 °C		- 6 ^a		
Continuous Drain Current (T _{.1} = 150 °C)	T _C = 70 °C	l _D	- 6 ^a		
Continuous Diain Gunent (1) = 100 C)	T _A = 25 °C		- 5 ^{b, c}		
	T _A = 70 °C		- 4 ^{b, c}	Α	
Pulsed Drain Current (t = 300 μs)		I _{DM}	- 20		
Continuous Source-Drain Diode Current	T _C = 25 °C	I _S	- 6 ^a		
Continuous Source-Diam Diode Current	T _A = 25 °C	'9	- 1.9 ^{b, c}		
	$T_C = 25 ^{\circ}C$		10.4		
Maximum Power Dissipation	$T_C = 70 ^{\circ}C$	P _D	6.7	w	
Maximum i ower bissipation	T _A = 25 °C		2.3 ^{b, c}] "	
	T _A = 70 °C		1.5 ^{b, c}		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{d, e}		_	260]	

Marking Code
OA XXX

Part # Code

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	t ≤ 5 s	R_{thJA}	43	55	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	9.5	12	0/ **

Notes:

- a. Package limited.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 5 s.
- d. See solder profile (www.vishay.com/ppg?73257). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under steady state conditions is 105 °C/W.

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Parameter Symbol Test Conditions Min. Typ. Max. Unit Static Static Unit Static	SPECIFICATIONS ($T_J = 25 ^{\circ}C_1$	unless oth	erwise noted)					
Drain-Source Breakdown Voltage Vos	•	1		Min.	Тур.	Max.	Unit	
Vos Temperature Coefficient ΔV _{OS} (T _J) I _D = -250 μA - 16 MoV/C Gate-Source Threshold Voltage V _{OS(H)} V _{DS} = V _{OS} I _D = -250 μA - 0.6 - 1.5 V Gate-Source Leakage I _{GSS} V _{OS} = V _{OS} I _D = -250 μA - 0.6 - 1.5 V Gate-Source Leakage I _{GSS} V _{OS} = OV, V _{OS} = ±4.5 V - ± 10 ± 10 ± 10 Zero Gate Voltage Drain Current I _{DSS} V _{OS} = OV, V _{OS} = OV, T _{OS} = OV - 1 ± 10 ± 1 On-State Drain Current ^a I _{D(III)} V _{OS} = -5.5 V, V _{OS} = -4.5 V - 20 A A Drain-Source On-State Resistance ^a I _{D(III)} V _{OS} = -4.5 V, I _D = -3.5 A 0.047 0.059 Ω </td <td>Static</td> <td></td> <td></td> <td></td> <td>1</td> <td>•</td> <td></td>	Static				1	•		
VGS(th) Temperature Coefficient AVGS(th) VGS(th) VGS = -260 μA -0.6 -1.5 V	Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	- 20			V	
Vasining Temperature Coefficient ΔV _{GS(III)} / V _{GS(III)} V Dis = V _{GS} , Ip = -250 μA - 0.6 - 1.5 V Gate-Source Leakage I _{GSS} V _{DS} = 0, V _{GS} = ± 12 V ± 10 ± 10 μμΑ Zero Gate Voltage Drain Current I _{GSS} V _{DS} = 0, V _{GS} = ± 4.5 V ± 10 ± 1 μμΑ On-State Drain Current ^a I _{D(III)} V _{DS} = -20 V, V _{GS} = 0 V ± 1 1 A On-State Drain Current ^a I _{D(III)} V _{DS} = -20 V, V _{GS} = 0 V ± 0 ± 1 A On-State Drain Current ^a I _{D(III)} V _{DS} = -20 V, V _{GS} = 0 V ± 0 1 A On-State Pasistance R _{DS(III)} V _{DS} = -50 V, V _{GS} = -4.5 V, I _D = -3.5 A 0.0.047 0.059 D Pormard Transconductance ^a 9tb V _{DS} = -10 V, I _D = -3.5 A 11 S S Dynamic ^b V _{DS} = -10 V, I _D = -3.5 A 11 4.96 D P P P P P P P P P P P P P P P P	V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	L = 250 uA		- 16		\//9C	
Gate-Source Leakage I_GSS	V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = - 250 μA		3		mv/°C	
Sass Vos Vo	Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 0.6		- 1.5	V	
Vos = 0 V, Vos = 4 · 5 · V 1	Oata Oassaa Laaka sa		$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 10	μΑ	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Gate-Source Leakage	IGSS	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 4.5 \text{ V}$			± 1		
On-State Drain Current ^a I _{D(on)} V _{DS} = -20 V, V _{GS} = 0 V, I _J = 5° C -10 A On-State Drain Current ^a I _{D(on)} V _{DS} ≤ -5 V, V _{GS} = -4.5 V -20 — A Drain-Source On-State Resistance ^a R _{DS} (on) V _{DS} ≤ -5 V, V _{DS} = -3.5 A 0.047 0.059 Forward Transconductance ^a 9 _{Is} V _{DS} = -10 V, V _{DS} = -3.5 A 111 S Dynamic ^b Input Capacitance C _{ISS} V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz 496 — Output Capacitance C _{ISS} V _{DS} = -10 V, V _{GS} = -10 V, I _D = -5 A 13.2 20 Output Capacitance C _{ISS} V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -5 A 13.2 20 Output Capacitance C _{ISS} V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -5 A 13.2 20 Output Capacitance C _{ISS} V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -5 A 13.2 20 Other Capacitance C _{IS} V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -5 A 13.2 20 Gate-Source Charge Q _g I = 1 MHz 2 8 16 Ω	Zone Oate Wellere Brain Oursel		V _{DS} = - 20 V, V _{GS} = 0 V			- 1		
Drain-Source On-State Resistance ^a R _{DS(on)} V _{GS} = -4.5 V, I _D = -3.5 A (0.047 0.059) Ω Forward Transconductance ^a 9Is V _{DS} = -10 V, I _D = -3.5 A (0.077 0.096) 11 S Dynamic ^b Input Capacitance C _{Iss} V _{DS} = -10 V, I _D = -3.5 A (0.047 0.096) 11 S Output Capacitance C _{Iss} V _{DS} = -10 V, I _D = -3.5 A (0.047 0.096) 11 S Reverse Transfer Capacitance C _{Iss} V _{DS} = -10 V, I _D = -3.5 A (0.047 0.096) 1486 (0.047 0.096) PF Reverse Transfer Capacitance C _{Iss} V _{DS} = -10 V, V _{DS} = -0 V, I _D = -3.5 A (0.047 0.096) 1411 (0.047 0.096) PF Reverse Transfer Capacitance C _{Iss} V _{DS} = -10 V, V _{DS} = 0 V, I _D = -5 A (0.047 0.096) 13.2 (0.047 0.096) 20 12.1 (0.047 0.096) PF Gate Position Charge Q _g V _{DS} = -10 V, V _{QS} = -4.5 V, I _D = -5 A (0.047 0.096) 1.6 (0.047 0.096) 1.6 (0.047 0.096) 1.6 (0.047 0.096) 1.6 (0.047 0.096) 1.6 (0.047 0.096) 1.6 (0.047 0.096) 1.0 (0.047 0.096) 1.0 (0.047 0.096) 1.0 (0.047 0.096) 1.0 (0.047 0.096) 1.0 (0.047 0.096) 1.0 (0.047 0.096)	Zero Gate Voltage Drain Current	IDSS	$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			- 10		
Drain-Source On-State Resistance ^a Pos(on) V _{GS} = -2.5 V, l _D = -1.5 A 0.077 0.096 Ω Forward Transconductance ^a 9fs V _{DS} = -10 V, l _D = -3.5 A 11 S S Dynamic ^b Untput Capacitance C _{ISS} V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz 141	On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	- 20			Α	
Promard Transconductance ⁸ 9s V _{DS} = -10 V, I _D = -3.5 A 11 S S		_	$V_{GS} = -4.5 \text{ V}, I_D = -3.5 \text{ A}$		0.047	0.059		
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Drain-Source On-State Resistance ^a	H _{DS(on)}	V _{GS} = - 2.5 V, I _D = - 1.5 A		0.077	0.096	Ω	
$ \begin{array}{ c c c c c } \hline \text{Input Capacitance} & C_{\text{iss}} \\ \hline \text{Output Capacitance} & C_{\text{css}} \\ \hline \text{Output Capacitance} & C_{\text{css}} \\ \hline \text{Reverse Transfer Capacitance} & C_{\text{rss}} \\ \hline \hline \text{Total Gate Charge} & Q_g \\ \hline \text{Gate-Source Charge} & Q_{gs} \\ \hline \text{Gate-Drain Charge} & Q_{gs} \\ \hline \text{Gate-In Incharge} & Q_{gs} \\ \hline \text{Gate-In Incharge} & Q_{gs} \\ \hline \text{Gate-Drain Charge} & Q_{gs} \\ \hline \text{Gate-Incharge} & Q_{gs} \\ \hline \text{Gate-Drain Charge} & Q_{gs} \\ \hline \text{Gate-Incharge} & Q_{gs} \\ \hline \text{Gate-Drain Charge} & Q_{gs} \\ \hline \text{Gate-Incharge} & Q_{gs} \\ \hline \text{Gate-Incharge} & Q_{gs} \\ \hline \text{Gate-Drain Charge} & Q_{gs} \\ \hline \text{Incharge} & Q_{gs} \\ $	Forward Transconductance ^a	9 _{fs}	V _{DS} = - 10 V, I _D = - 3.5 A		11		S	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Dynamic ^b					l .		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Input Capacitance	C _{iss}			496			
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Output Capacitance	C _{oss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		141		pF	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Reverse Transfer Capacitance				121			
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	T. 10 . 0		V _{DS} = - 10 V, V _{GS} = - 10 V, I _D = - 5 A		13.2	20		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Total Gate Charge				6.9	10.5		
$ \begin{array}{ c c c c c c c c } \hline \text{Gate-Drain Charge} & Q_{gd} \\ \hline \text{Gate Resistance} & R_g & f = 1 \text{MHz} & 2 & 8 & 16 & \Omega \\ \hline \text{Turn-On Delay Time} & t_{d(on)} \\ \hline \text{Rise Time} & t_r \\ \hline \text{Turn-Off Delay Time} & t_{d(off)} \\ \hline \text{Fall Time} & t_f \\ \hline \text{Turn-On Delay Time} & t_{d(on)} \\ \hline \text{Fall Time} & t_f \\ \hline \text{Turn-On Delay Time} & t_{d(on)} \\ \hline \text{Rise Time} & t_r \\ \hline \text{Turn-Off Delay Time} & t_{d(on)} \\ \hline \text{Rise Time} & t_r \\ \hline \text{Turn-Off Delay Time} & t_{d(off)} \\ \hline \text{Fall Time} & t_f \\ \hline \hline \text{Turn-Off Delay Time} & t_{d(off)} \\ \hline \text{Fall Time} & t_f \\ \hline \hline \\ \hline \hline \textbf{Drain-Source Body Diode Characteristics} \\ \hline \hline \textbf{Continuous Source-Drain Diode Current} & I_S \\ \hline \text{Body Diode Forward Current} & I_{SM} \\ \hline \text{Body Diode Reverse Recovery Time} & t_{rr} \\ \hline \text{Body Diode Reverse Recovery Charge} & Q_{rr} \\ \hline \text{Reverse Recovery Fall Time} & t_a \\ \hline \end{array} \begin{array}{c} 1.8 \\ 17 \\ 20 \\ 17 \\ 20 \\ 20 \\ 20 \\ 20 \\ 20 \\ 20 \\ 20 \\ 2$	Gate-Source Charge	Q _{gs}	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -5 \text{ A}$		1.6		nC	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Gate-Drain Charge	Q_{gd}			1.8		1	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Gate Resistance	R_g	f = 1 MHz	2	8	16	Ω	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Turn-On Delay Time	t _{d(on)}			17	26		
	Rise Time	t _r	V_{DD} = - 10 V, R_L = 2.5 Ω		21	32	1	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Turn-Off Delay Time		$I_D\cong$ - 4 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		26	40		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Fall Time	t _f			13	20		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Turn-On Delay Time	t _{d(on)}			6	12	ns	
Fall Time t_f	Rise Time	t _r	V_{DD} = - 10 V, R_L = 2.5 Ω		11	22	1	
	Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ - 4 A, V_{GEN} = - 10 V, R_g = 1 Ω		23	35	1	
	Fall Time	1			11	22		
Pulse Diode Forward Current I_{SM} -20 Body Diode Voltage V_{SD} $I_{S} = -4 \text{ A}, V_{GS} = 0 \text{ V}$ -0.85 -1.2 V Body Diode Reverse Recovery Time t_{rr} Body Diode Reverse Recovery Charge Q_{rr} Reverse Recovery Fall Time t_a $I_{F} = -4 \text{ A}, \text{ dl/dt} = 100 \text{ A/µs}, T_{J} = 25 ^{\circ}\text{C}$ $I_{F} = -4 \text{ A}, \text{ dl/dt} = 100 \text{ A/µs}, T_{J} = 25 ^{\circ}\text{C}$	Drain-Source Body Diode Characteristic	cs						
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 6		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Pulse Diode Forward Current	ode Forward Current		- 20	1 A			
Body Diode Reverse Recovery Time t_{rr} Body Diode Reverse Recovery Charge Q_{rr} Reverse Recovery Fall Time t_a $I_F = -4 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$ $I_F = -4 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$	Body Diode Voltage		I _S = -4 A, V _{GS} = 0 V		- 0.85	- 1.2	V	
Body Diode Reverse Recovery Charge Q_{rr} Reverse Recovery Fall Time t_a $I_F = -4 \text{ A, dI/dt} = 100 \text{ A/µs, T}_J = 25 \text{ °C}$ $10 20 \text{ nC}$ 14					24	48	ns	
Reverse Recovery Fall Time t_a $I_F = -4 \text{ A}$, $dI/dt = 100 \text{ A/µs}$, $I_J = 25 \text{ °C}$ 14					10	20	nC	
ns		t	$I_F = -4 \text{ A}$, dl/dt = 100 A/ μ s, $T_J = 25 ^{\circ}\text{C}$					
	Reverse Recovery Rise Time	t _b						

Notes:

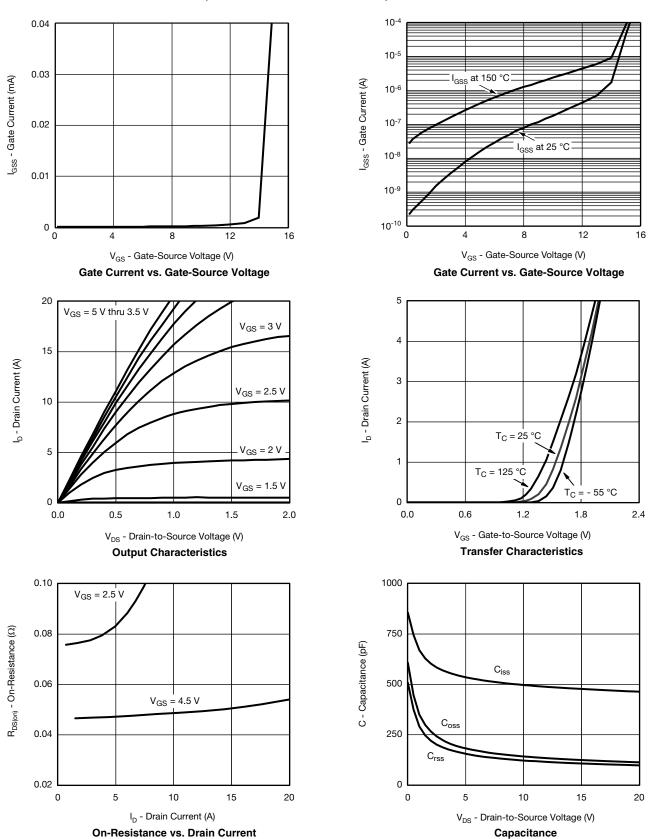
- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.





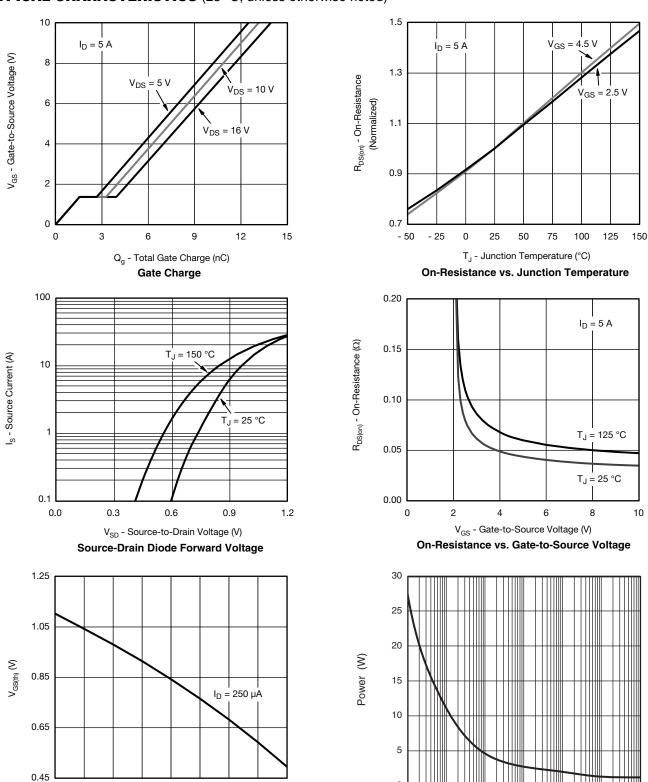
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



0.01

0.001

- 50

- 25

0

25

50

T_J - Temperature (°C)

Threshold Voltage

75

100

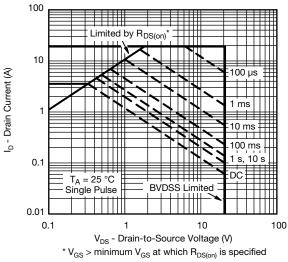
125

100

1000

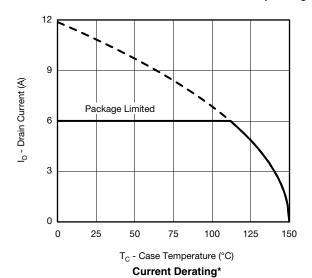


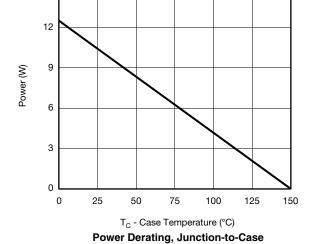
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

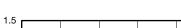


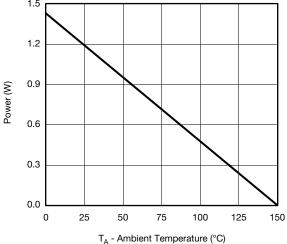
Safe Operating Area, Junction-to-Ambient

15









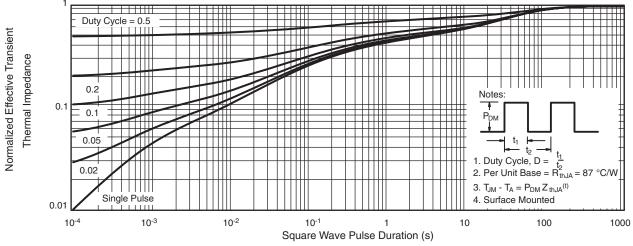
Power Derating, Junction-to-Ambient

^{*} The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

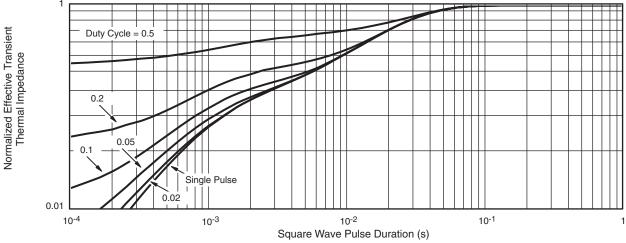
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

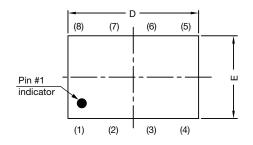


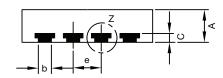
Normalized Thermal Transient Impedance, Junction-to-Case

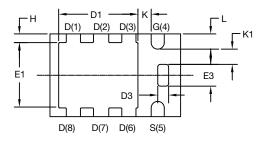
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67019.



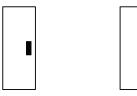
PowerPAK® ChipFET® Case Outline







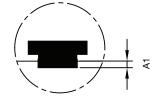
Backside view of single pad



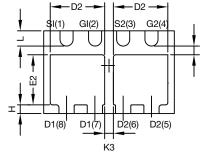
Side view of single



Side view of dual



Detail Z



Backside view of dual pad

	MILLIMETERS			INCHES			
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Α	0.70	0.75	0.85	0.028	0.030	0.033	
A1	0	-	0.05	0	-	0.002	
b	0.25	0.30	0.35	0.010	0.012	0.014	
С	0.15	0.20	0.25	0.006	0.008	0.010	
D	2.92	3.00	3.08	0.115	0.118	0.121	
D1	1.75	1.87	2.00	0.069	0.074	0.079	
D2	1.07	1.20	1.32	0.042	0.047	0.052	
D3	0.20	0.25	0.30	0.008	0.010	0.012	
E	1.82	1.90	1.98	0.072	0.075	0.078	
E1	1.38	1.50	1.63	0.054	0.059	0.064	
E2	0.92	1.05	1.17	0.036	0.041	0.046	
E3	0.45	0.50	0.55	0.018	0.020	0.022	
е		0.65 BSC		0.026 BSC			
Н	0.15	0.20	0.25	0.006	0.008	0.010	
K	0.25	-	-	0.010	-	ı	
K1	0.30	-	-	0.012	-	ı	
K2	0.20	-	-	0.008	-	ı	
K3	0.20	-	-	0.008	-	ı	
L	0.30	0.35	0.40	0.012	0.014	0.016	

C14-0630-Rev. E, 21-Jul-14

Note

DWG: 5940

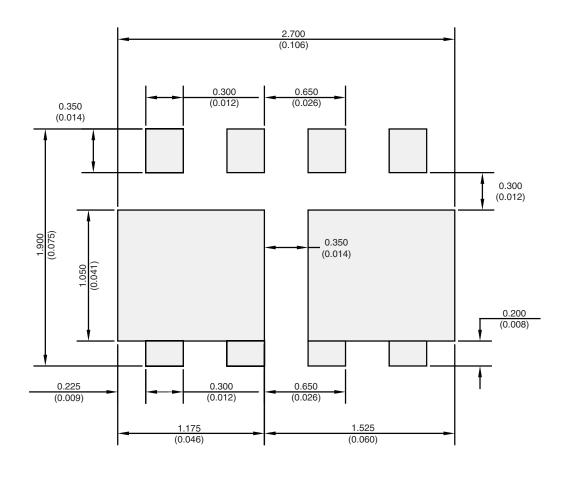
Revision: 21-Jul-14

• Millimeters will govern

Z



RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Dual



Recommended Minimum Pads Dimensions in mm/(Inches)

Note: This is Flipped Mirror Image Pin #1 Location is Top Left Corner

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