



Vishay Siliconix

# **Dual N-Channel 1.5-V (G-S) MOSFET**

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	$r_{DS(on)}\left(\Omega\right)$	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ)	
8	$0.032 \text{ at V}_{GS} = 4.5 \text{ V}$	4 <sup>a</sup>		
	0.036 at V <sub>GS</sub> = 2.5 V	4 <sup>a</sup>	7.3 nC	
	0.045 at V <sub>GS</sub> = 1.8 V	4 <sup>a</sup>	7.3110	
	0.054 at V <sub>GS</sub> = 1.5 V	4 <sup>a</sup>		

#### **FEATURES**

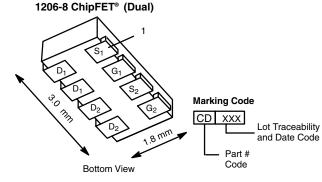
- TrenchFET® Power MOSFET: 1.5 V Rated
- Ultra -low on-resistance in compact, thermally enhanced ChipFET® package



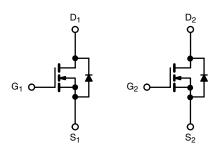
COMPLIANT

#### **APPLICATIONS**

- Load switch for portable applications
  - Guaranteed operation at V<sub>GS</sub> = 1.5 V critical for opti mized design and space savings



Ordering Information: Si5920DC-T1-E3 (Lead (Pb)-free)



N-Channel MOSFET

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	$\Gamma_A = 25  ^{\circ}\text{C}, \text{ unlet}$	ess otherwise i	noted		
Parameter	Parameter		Limit	Unit	
Drain-Source Voltage	Drain-Source Voltage		8	V	
Gate-Source Voltage	Gate-Source Voltage		± 5	V	
	T <sub>C</sub> = 25 °C	I <sub>D</sub>	4 <sup>a</sup>		
Continuous Drain Current (T <sub>.I</sub> = 150 °C)	T <sub>C</sub> = 70 °C		4 <sup>a</sup>		
Continuous Brain Current (1) = 130 O)	T <sub>A</sub> = 25 °C		4 <sup>a</sup>		
Data Charatal Laure	T <sub>A</sub> = 70 °C		4 <sup>a</sup>	Α	
W.Data Pulsed Drain Current	Pulsed Drain Current		25		
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C	Is	2.6		
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	'S	1.7 <sup>c</sup>	$\neg$	
	T <sub>C</sub> = 25 °C		3.12		
Maximum Power Dissipation	T <sub>C</sub> = 70 °C	P <sub>D</sub>	2.0	w	
Maximum rower Dissipation	T <sub>A</sub> = 25 °C		2.04 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C		1.3 <sup>b, c</sup>	1	
Operating Junction and Storage Temperature Range	Operating Junction and Storage Temperature Range		- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) <sup>d, o</sup>	Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 5 sec	$R_{thJA}$	50	60	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State	$R_{thJF}$	30	40		

#### Notes:

- a. Package limited.
  b. Surface Mounted on 1" x 1" FR4 Board.
- c. t = 5 sec. d. See Solder Profile (http://www.vishay.com/ppg?73257). The 1206-8 ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under Steady State conditions is 90 °C/W.

# **Si5920DC**

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Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static	<u> </u>	,					
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	8			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = 250 μA		8.2		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_{J}$	ι <sub>D</sub> = 250 μΑ		- 2.6			
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	0.3		1	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 5 \text{ V}$			± 100	ns	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 8 V, V <sub>GS</sub> = 0 V			1		
		$V_{DS} = 8 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			10	μA	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \le 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	25			Α	
	, ,	$V_{GS} = 4.5 \text{ V}, I_D = 6.8 \text{ A}$		0.025	0.032	Ω	
Durin Course On Otal During	r	$V_{GS} = 2.5 \text{ V}, I_D = 6.3 \text{ A}$		0.0285	0.036		
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 1.8 V, I <sub>D</sub> = 2.5 A		0.036	0.045		
		V <sub>GS</sub> = 1.5 V, I <sub>D</sub> = 1.8 A		0.041	0.054		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	$V_{DS} = 4 \text{ V}, I_{D} = 6.8 \text{ A}$		18		S	
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>			680		pF	
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 4 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		230			
Reverse Transfer Capacitance	C <sub>rss</sub>			140			
Total Cata Charga		$V_{DS} = 4 \text{ V}, V_{GS} = 5 \text{ V}, I_D = 6.8 \text{ A}$		8	12	nC	
Total Gate Charge	Q <sub>g</sub>			7.3	11		
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 4 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 6.8 \text{ A}$		0.84			
Gate-Drain Charge	$Q_{gd}$			1.26			
Gate Resistance	$R_g$	f = 1 MHz		1.8	2.7	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			8	12		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 4 V, $R_L$ = 0.73 $\Omega$		11	17	- ns	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 5.5 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		18	27		
Fall Time	t <sub>f</sub>			7	11		
<b>Drain-Source Body Diode Characteristic</b>	s						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			2.6	А	
Pulse Diode Forward Current	I <sub>SM</sub>				25		
Body Diode Voltage	$V_{SD}$	$I_S = 2.6 \text{ A}, V_{GS} = 0 \text{ V}$		8.0	1.2	V	
Body Diode Reverse Recovery Time t <sub>rr</sub>				12	18	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> = 2.6 A, di/dt = 100 A/μs, T <sub>.I</sub> = 25 °C		3	5	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	1 2.0 Λ, αι/αι - 100 Α/μ5, 1 J = 25 C		7		ns	
Reverse Recovery Rise Time	t <sub>b</sub>			5			

www

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

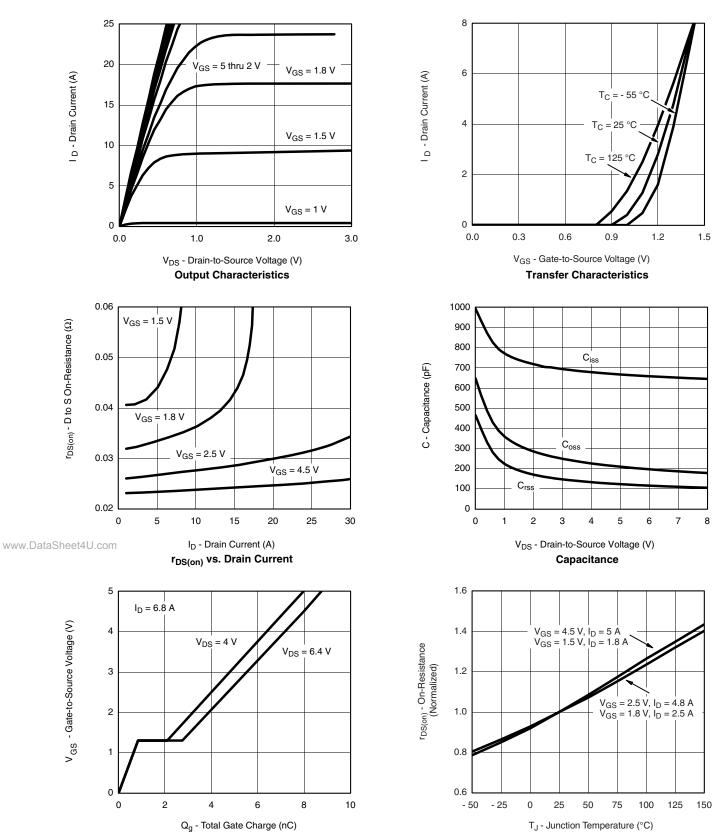
Notes: a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %. b. Guaranteed by design, not subject to production testing.





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#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



**Gate Charge** 

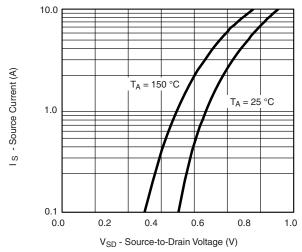
On-Resistance vs. Junction Temperature

## **Si5920DC**

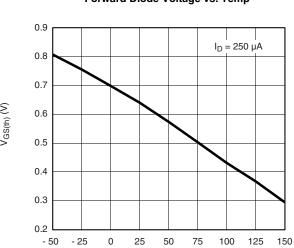
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# www.DataSheet4U.com **VISHAY**<sub>®</sub>

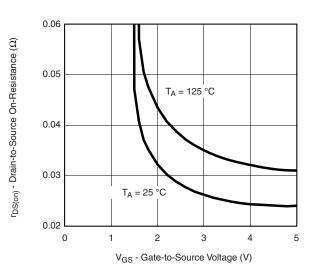
#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



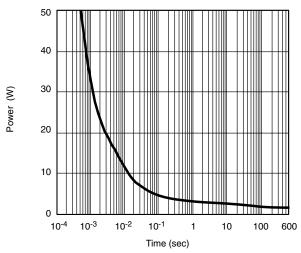
#### Forward Diode Voltage vs. Temp



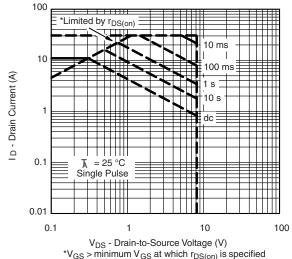
T<sub>J</sub> - Temperature (°C) www.DataSheet4U.com **Threshold Voltage** 



r<sub>DS(on)</sub> vs. V<sub>GS</sub> vs. Temperature



**Single Pulse Power** 



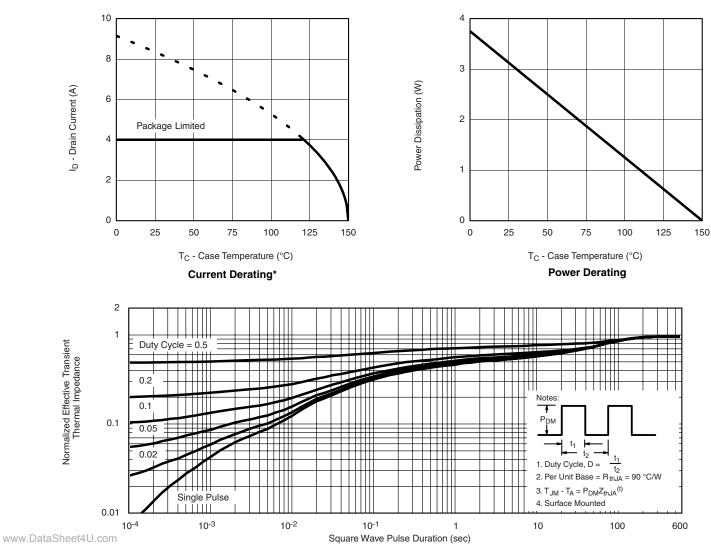
 $^*V_{GS}$  > minimum  $V_{GS}$  at which  $r_{DS(on)}$  is specified

Safe Operating Area, Junction-to-Case



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#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient

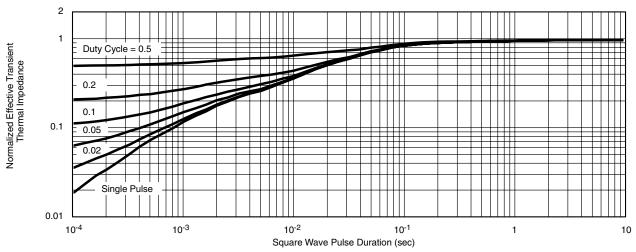
\*The power dissipation  $P_D$  is based on  $T_{J(max)}$  = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

# **Si5920DC**

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### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Foot

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Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="http://www.vishay.com/ppg?73490">http://www.vishay.com/ppg?73490</a>.



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