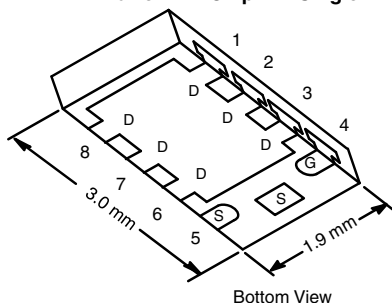


P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY

| V _{DS} (V) | R _{DS(on)} (Ω) (Max.) | I _D (A) ^a | Q _g (Typ.) |
|---------------------|-------------------------------------|---------------------------------|-----------------------|
| - 20 | 0.0096 at V _{GS} = - 4.5 V | - 25 | 43 nC |
| | 0.0132 at V _{GS} = - 2.5 V | - 25 | |
| | 0.0220 at V _{GS} = - 1.8 V | - 7 | |

PowerPAK ChipFET Single



Bottom View

Ordering Information:

Si5415AEDU-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

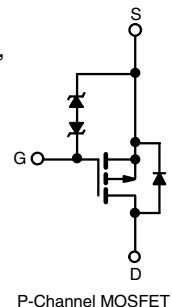
- TrenchFET® Power MOSFET
- Thermally Enhanced PowerPAK® ChipFET Package
 - Small Footprint Area
 - Low On-Resistance
- 100 % R_g and UIS Tested
- Typical ESD Protection: 5500 V (HBM)
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



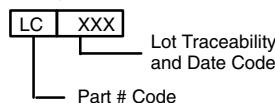
RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Portable Devices such as Smart Phones, Tablet PCs and Mobile Computing
 - Battery Switch
 - Load Switch
 - Power Management



Marking Code



ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

| Parameter | Symbol | Limit | Unit |
|--|-----------------------------------|------------------------|------|
| Drain-Source Voltage | V _{DS} | - 20 | V |
| Gate-Source Voltage | V _{GS} | ± 8 | |
| Continuous Drain Current (T _J = 150 °C) | I _D | T _C = 25 °C | A |
| | | T _C = 70 °C | |
| | | T _A = 25 °C | |
| | | T _A = 70 °C | |
| Pulsed Drain Current (t = 100 μs) | I _{DM} | - 70 | A |
| Continuous Source-Drain Diode Current | I _S | T _C = 25 °C | |
| | | T _A = 25 °C | |
| Single Avalanche Current | I _{AS} | - 15 | mJ |
| Single Avalanche Energy | E _{AS} | 11 | |
| Maximum Power Dissipation | P _D | T _C = 25 °C | W |
| | | T _C = 70 °C | |
| | | T _A = 25 °C | |
| | | T _A = 70 °C | |
| Operating Junction and Storage Temperature Range | T _J , T _{stg} | - 50 to 150 | °C |
| Soldering Recommendations (Peak Temperature) ^{d, e} | | 260 | |

THERMAL RESISTANCE RATINGS

| Parameter | Symbol | Typical | Maximum | Unit |
|---|-------------------|---------|---------|------|
| Maximum Junction-to-Ambient ^{b, f} | R _{thJA} | 34 | 40 | °C/W |
| Maximum Junction-to-Case (Drain) | R _{thJC} | 3 | 4 | |

Notes

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 90 °C/W.

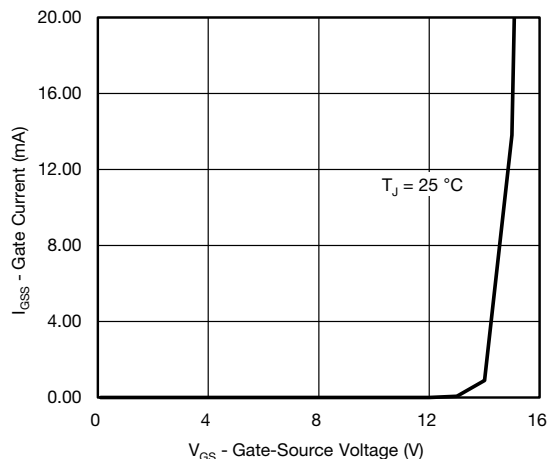
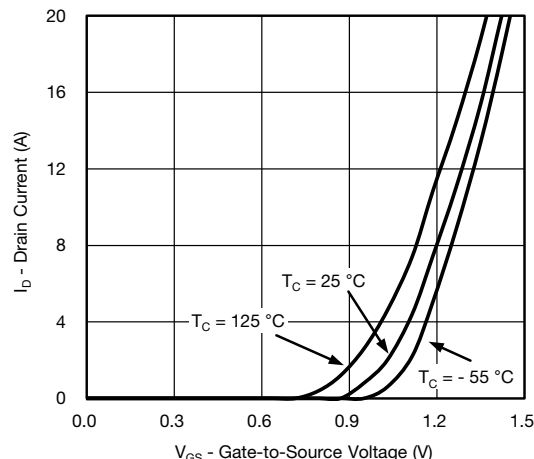
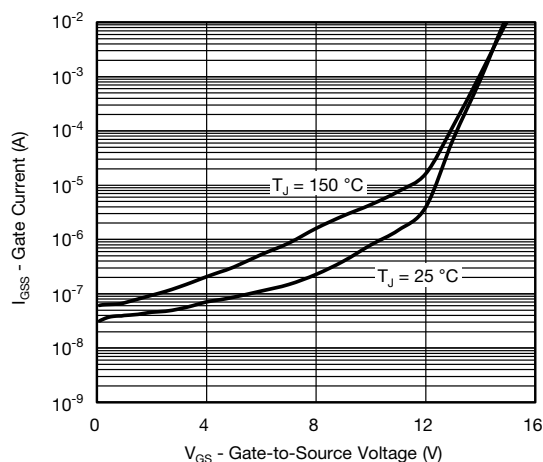
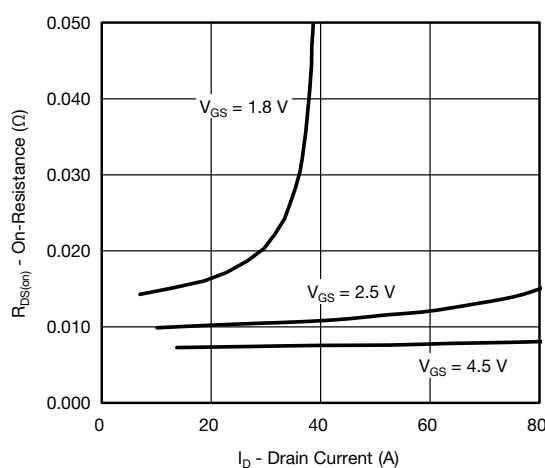
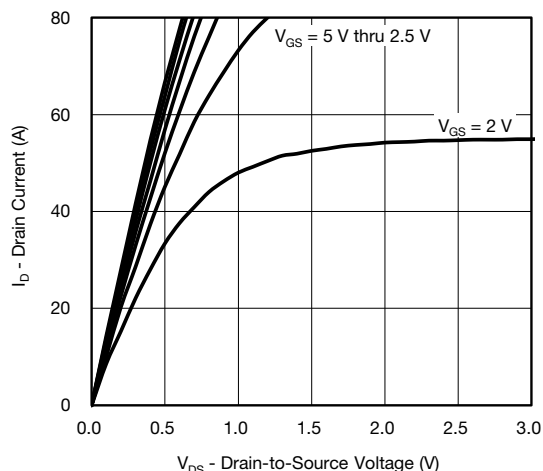
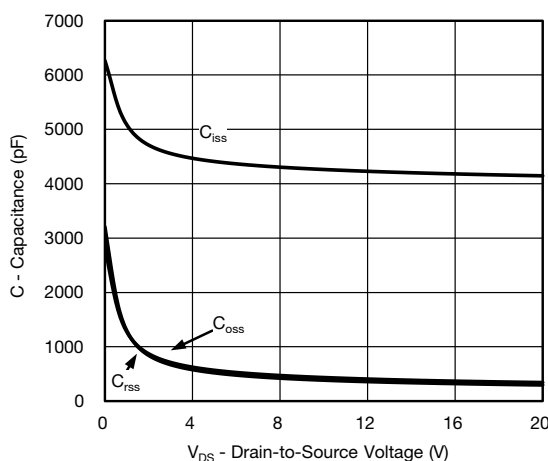


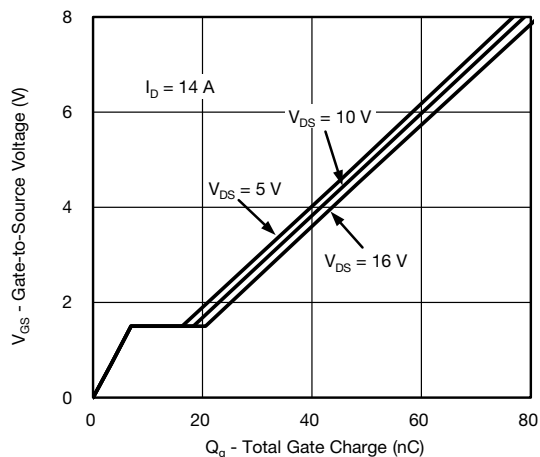
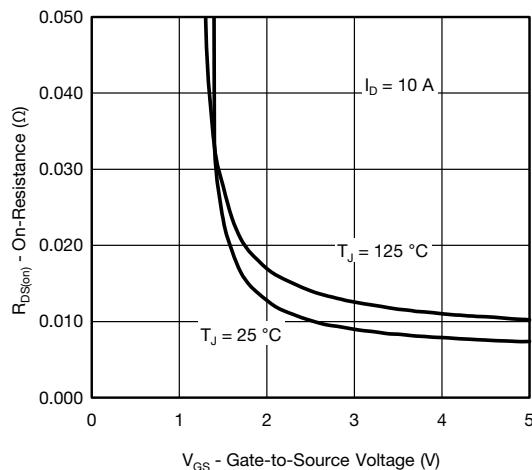
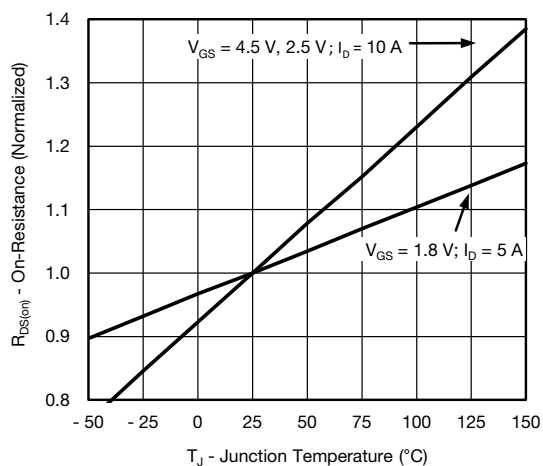
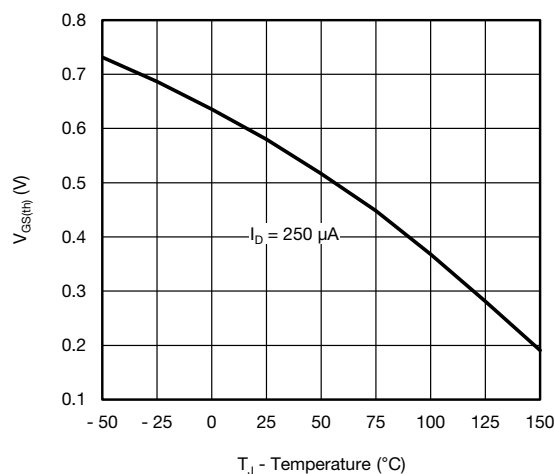
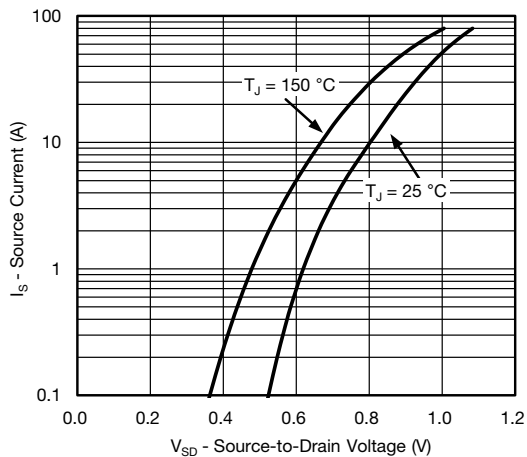
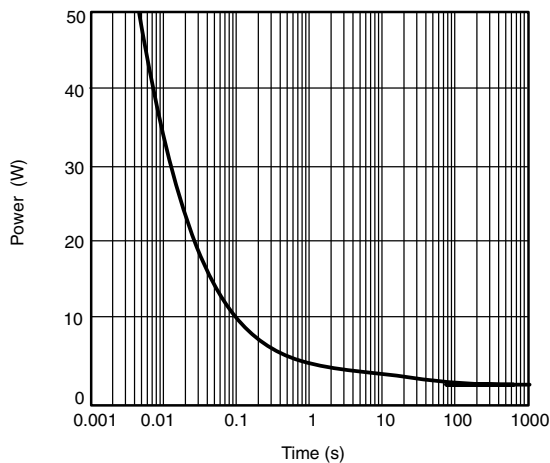
| SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) | | | | | | | |
|---|--------------------------------------|---|-------|--------|--------|-------|--|
| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit | |
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V _{DS} | V _{GS} = 0 V, I _D = - 250 μA | - 20 | | | V | |
| V _{DS} Temperature Coefficient | ΔV _{DS} /T _J | I _D = - 250 μA | | - 11 | | mV/°C | |
| V _{GS(th)} Temperature Coefficient | ΔV _{GS(th)} /T _J | | | 2.8 | | | |
| Gate-Source Threshold Voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D = - 250 μA | - 0.4 | | - 1 | V | |
| Gate-Source Leakage | I _{GSS} | V _{DS} = 0 V, V _{GS} = ± 8 V | | | ± 2 | μA | |
| | | V _{DS} = 0 V, V _{GS} = ± 4.5 V | | | ± 0.2 | | |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} = - 20 V, V _{GS} = 0 V | | | - 1 | | |
| | | V _{DS} = - 20 V, V _{GS} = 0 V, T _J = 55 °C | | | - 10 | | |
| On-State Drain Current ^a | I _{D(on)} | V _{DS} ≤ - 5 V, V _{GS} = - 4.5 V | - 10 | | | A | |
| Drain-Source On-State Resistance ^a | R _{DS(on)} | V _{GS} = - 4.5 V, I _D = - 10 A | | 0.0081 | 0.0096 | Ω | |
| | | V _{GS} = - 2.5 V, I _D = - 5 A | | 0.0110 | 0.0132 | | |
| | | V _{GS} = - 1.8 V, I _D = - 2 A | | 0.0170 | 0.0220 | | |
| Forward Transconductance ^a | g _{fs} | V _{GS} = - 10 V, I _D = - 10 A | | 47 | | S | |
| Dynamic ^b | | | | | | | |
| Input Capacitance | C _{iss} | V _{DS} = - 10 V, V _{GS} = 0 V, f = 1 MHz | | 4300 | | pF | |
| Output Capacitance | C _{oss} | | | 445 | | | |
| Reverse Transfer Capacitance | C _{rss} | | | 400 | | | |
| Total Gate Charge | Q _g | V _{DS} = - 10 V, V _{GS} = - 8 V, I _D = - 14 A | | 80 | 120 | nC | |
| | | V _{DS} = - 10 V, V _{GS} = - 4.5 V, I _D = - 14 A | | 43 | 65 | | |
| Gate-Source Charge | Q _{gs} | | | 7 | | | |
| Gate-Drain Charge | Q _{gd} | | | 11.4 | | | |
| Gate Resistance | R _g | f = 1 MHz | 0.6 | 3.3 | 6.6 | Ω | |
| Turn-On Delay Time | t _{d(on)} | V _{DD} = - 10 V, R _L = 1 Ω I _D ≅ - 10 A, V _{GEN} = - 4.5 V, R _g = 1 Ω | | 30 | 60 | ns | |
| Rise Time | t _r | | | 45 | 90 | | |
| Turn-Off Delay Time | t _{d(off)} | | | 75 | 150 | | |
| Fall Time | t _f | | | 25 | 50 | | |
| Turn-On Delay Time | t _{d(on)} | V _{DD} = - 10 V, R _L = 1 Ω I _D ≅ - 10 A, V _{GEN} = - 8 V, R _g = 1 Ω | | 12 | 25 | | |
| Rise Time | t _r | | | 5 | 10 | | |
| Turn-Off Delay Time | t _{d(off)} | | | 80 | 160 | | |
| Fall Time | t _f | | | 20 | 40 | | |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I _S | T _C = 25 °C | | | - 25 | A | |
| Pulse Diode Forward Current (t = 100 μs) | I _{SM} | | | | - 70 | | |
| Body Diode Voltage | V _{SD} | I _S = - 10 A, V _{GS} = 0 V | | - 0.8 | - 1.2 | V | |
| Body Diode Reverse Recovery Time | t _{rr} | I _F = - 10 A, di/dt = 100 A/μs, T _J = 25 °C | | 35 | 70 | ns | |
| Body Diode Reverse Recovery Charge | Q _{rr} | | | 21 | 40 | nC | |
| Reverse Recovery Fall Time | t _a | | | 20 | | ns | |
| Reverse Recovery Rise Time | t _b | | | 15 | | | |

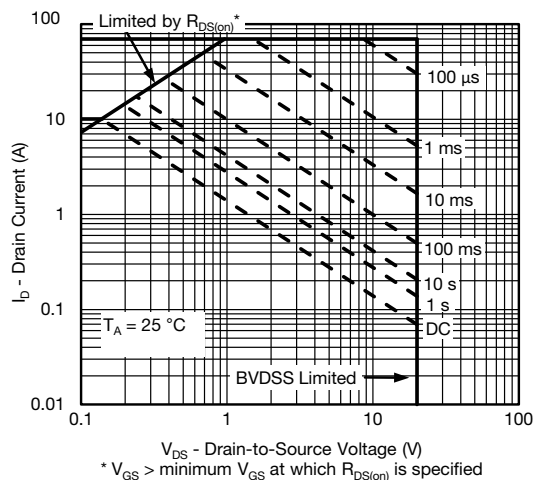
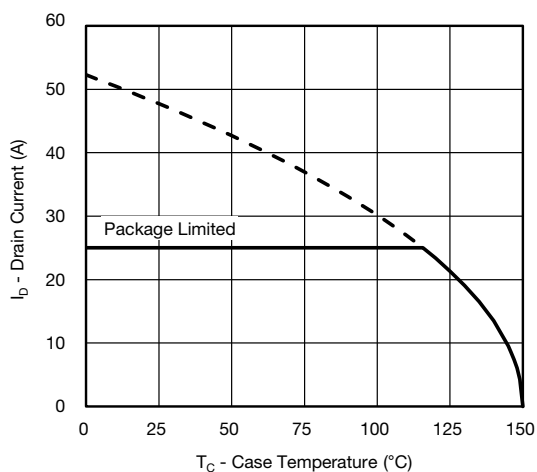
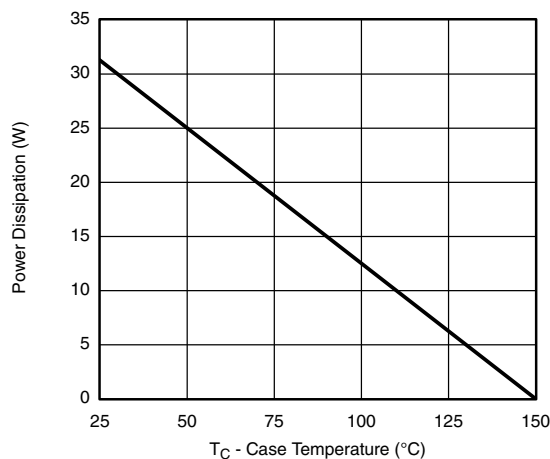
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Gate Current vs. Gate-Source Voltage

Transfer Characteristics

Gate Current vs. Gate-Source Voltage

On-Resistance vs. Drain Current and Gate Voltage

Output Characteristics

Capacitance

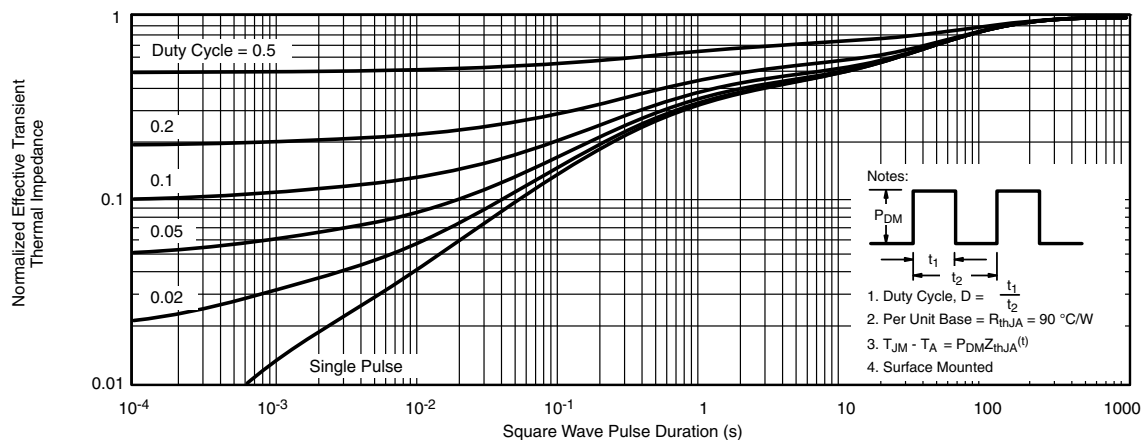
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Gate Charge

On-Resistance vs. Gate-to-Source Voltage

On-Resistance vs. Junction Temperature

Threshold Voltage

Source-Drain Diode Forward Voltage

Single Pulse Power, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Safe Operating Area, Junction-to-Ambient

Current Derating*

Power Derating

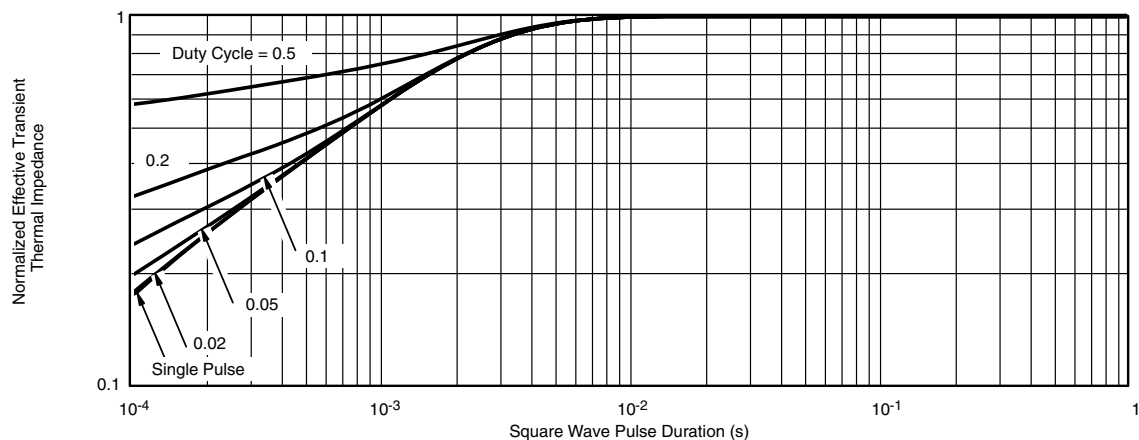
* The power dissipation P_D is based on $T_{J(max.)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

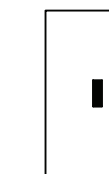
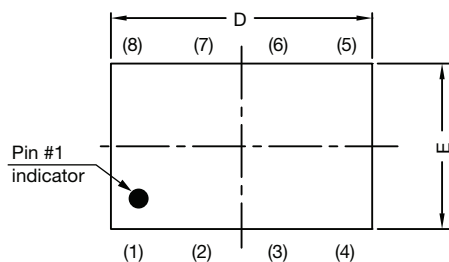


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62837.



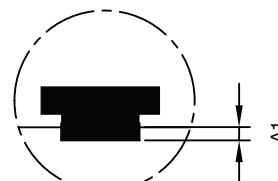
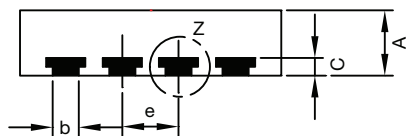
PowerPAK® ChipFET® Case Outline



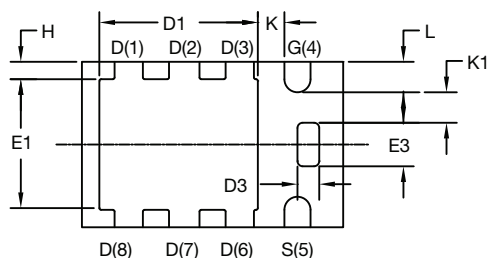
Side view of single



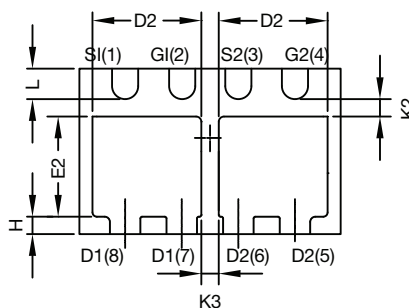
Side view of dual



Detail Z



Backside view of single pad



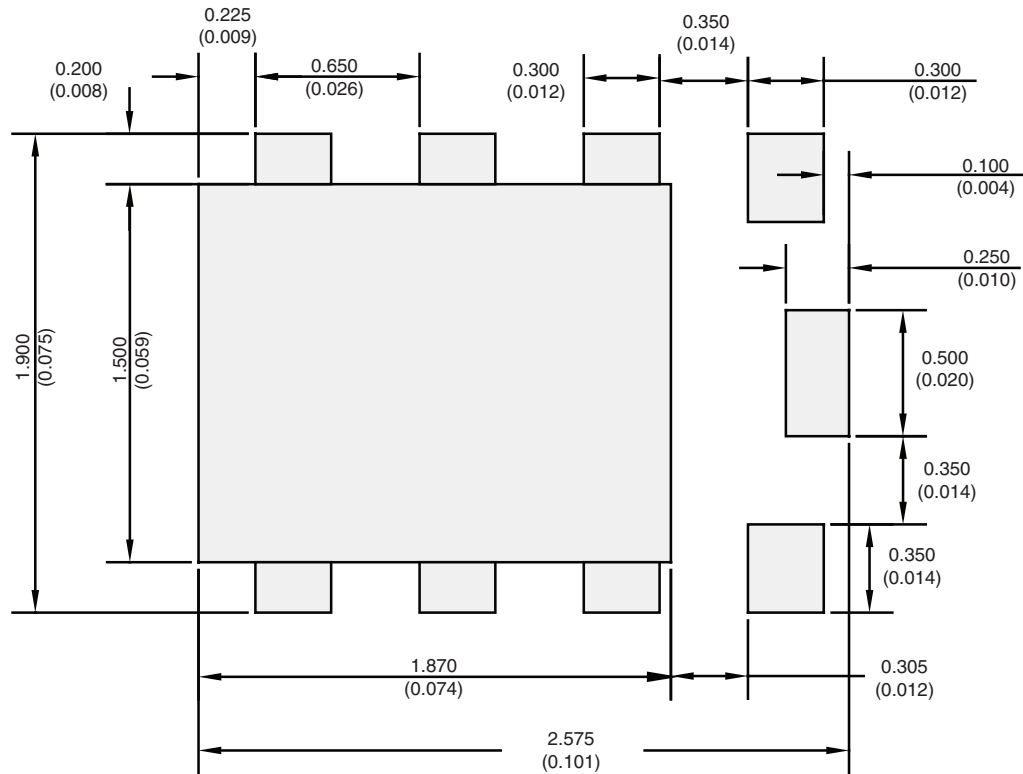
Backside view of dual pad

| DIM. | MILLIMETERS | | | INCHES | | |
|----------------------------|-------------|------|------|-----------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.85 | 0.028 | 0.030 | 0.033 |
| A1 | 0 | - | 0.05 | 0 | - | 0.002 |
| b | 0.25 | 0.30 | 0.35 | 0.010 | 0.012 | 0.014 |
| C | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D | 2.92 | 3.00 | 3.08 | 0.115 | 0.118 | 0.121 |
| D1 | 1.75 | 1.87 | 2.00 | 0.069 | 0.074 | 0.079 |
| D2 | 1.07 | 1.20 | 1.32 | 0.042 | 0.047 | 0.052 |
| D3 | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| E | 1.82 | 1.90 | 1.98 | 0.072 | 0.075 | 0.078 |
| E1 | 1.38 | 1.50 | 1.63 | 0.054 | 0.059 | 0.064 |
| E2 | 0.92 | 1.05 | 1.17 | 0.036 | 0.041 | 0.046 |
| E3 | 0.45 | 0.50 | 0.55 | 0.018 | 0.020 | 0.022 |
| e | 0.65 BSC | | | 0.026 BSC | | |
| H | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| K | 0.25 | - | - | 0.010 | - | - |
| K1 | 0.30 | - | - | 0.012 | - | - |
| K2 | 0.20 | - | - | 0.008 | - | - |
| K3 | 0.20 | - | - | 0.008 | - | - |
| L | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |
| C14-0630-Rev. E, 21-Jul-14 | | | | | | |
| DWG: 5940 | | | | | | |

Note

- Millimeters will govern

RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Single



Recommended Minimum Pads
Dimensions in mm/(Inches)

[Return to Index](#)



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