Si5366

PRECISION CLOCK MULTIPLIER/JITTER ATTENUATOR

Features

- Selectable output frequencies ranging from 8 kHz to 1050 MHz
- Ultra-low jitter clock outputs w/jitter generation as low as 0.3 ps rms (12 kHz–20 MHz)
- Integrated loop filter with selectable loop bandwidth (60 Hz to 8.4 kHz)
- Meets OC-192 GR-253-CORE jitter specifications
- Four clock inputs w/manual or automatically controlled hitless switching
- Five clock outputs with selectable signal format (LVPECL, LVDS, CML, CMOS)
- SONET frame sync switching and regeneration
- Support for ITU G.709 FEC ratios (255/238, 255/237, 255/236)
- LOL, LOS, FOS alarm outputs
- Pin-controlled output phase adjust
- Pin-programmable settings
- On-chip voltage regulator for 1.8 ±5%, 2.5 V ±10%, or 3.3 V ±10% operation
- Small size: 14 x 14 mm 100-pin TQFP
- Pb-free, RoHS-compliant

Ordering Information:

See page 25.

Applications

- SONET/SDH OC-48/STM-16 and OC-192/STM-64 line cards
- GbE/10GbE, 1/2/4/8/10G Fibre Channel line cards
- ITU G.709 line cards
- Optical modules
- Test and measurement
- Synchronous Ethernet

Description

The Si5366 is a jitter-attenuating precision clock multiplier for high-speed communication systems, including SONET OC-48/OC-192, Ethernet, and Fibre Channel. The Si5366 accepts four clock inputs ranging from 8 kHz to 707 MHz and generates five frequency-multiplied clock outputs ranging from 8 kHz to 1050 MHz. The input clock frequency and clock multiplication ratio are selectable from a table of popular SONET, Ethernet, and Fibre Channel frequencies. The Si5366 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. Operating from a single 1.8, 2.5, or 3.3 V supply, the Si5366 is ideal for providing clock multiplication and jitter attenuation in high performance timing applications.

Functional Block Diagram

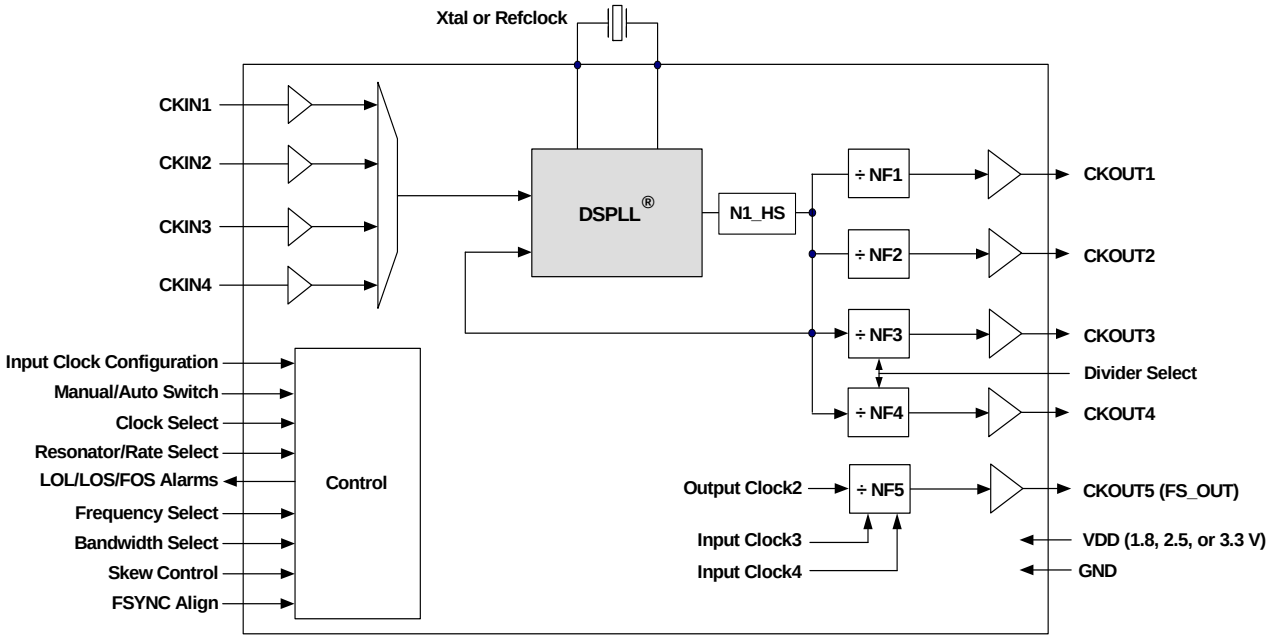

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Table 1. Recommended Operating Conditions[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–40	25	85	C
Supply Voltage during Normal Operation	V_{DD}	3.3 V Nominal[2]	2.97	3.3	3.63	V
		2.5 V Nominal	2.25	2.5	2.75	V
		1.8 V Nominal	1.71	1.8	1.89	V

Notes:
1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 ºC unless otherwise stated.
2. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.

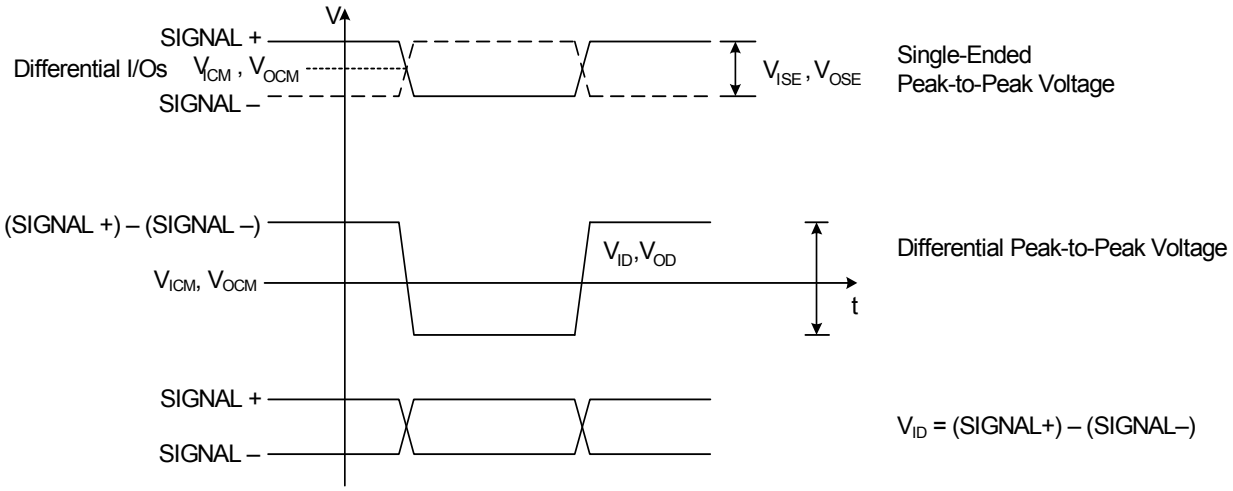


Figure 1. Differential Voltage Characteristics

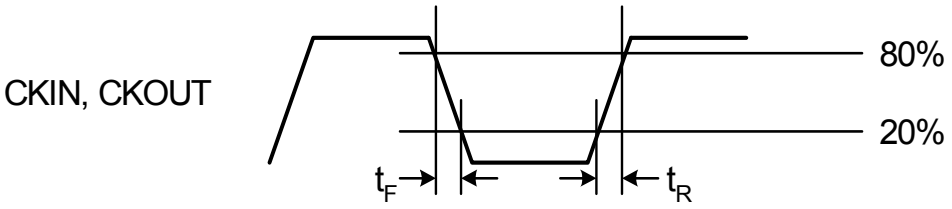


Figure 2. Rise/Fall Time Characteristics

Table 2. DC Characteristics

(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current[1,6]	I_{DD}	LVPECL Format 622.08 MHz Out All CKOUTs Enabled	—	394	435	mA
		LVPECL Format 622.08 MHz Out 1 CKOUT Enabled	—	253	284	mA
		CMOS Format 19.44 MHz Out All CKOUTs Enabled	—	278	400	mA
		CMOS Format 19.44 MHz Out 1 CKOUT Enabled	—	229	261	mA
		Disable Mode	—	165	—	mA
CKINn Input Pins[2]						
Input Common Mode Voltage (Input Threshold Voltage)	V_{ICM}	1.8 V ± 5%	0.9	—	1.4	V
		2.5 V ± 10%	1	—	1.7	V
		3.3 V ± 10%	1.1	—	1.95	V
Input Resistance	CKN_{RIN}	Single-ended	20	40	60	kΩ
Single-Ended Input Voltage Swing (See Absolute Specs)	V_{ISE}	f_{CKIN} < 212.5 MHz See Figure 1.	0.2	—	—	V_{PP}
		f_{CKIN} > 212.5 MHz See Figure 1.	0.25	—	—	V_{PP}
Differential Input Voltage Swing (See Absolute Specs)	V_{ID}	f_{CKIN} < 212.5 MHz See Figure 1.	0.2	—	—	V_{PP}
		f_{CKIN} > 212.5 MHz See Figure 1.	0.25	—	—	V_{PP}

Notes:

1. Current draw is independent of supply voltage
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal VDD ≥ 2.5 V.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.
6. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Clocks (CKOUTn)[3,5,6]						
Common Mode	CKO_{VCM}	LVPECL 100 Ω load line-to-line	V_{DD} –1.42	—	V_{DD} –1.25	V
Differential Output Swing	CKO_{VD}	LVPECL 100 Ω load line-to-line	1.1	—	1.9	V_{PP}
Single Ended Output Swing	CKO_{VSE}	LVPECL 100 Ω load line-to-line	0.5	—	0.93	V_{PP}
Differential Output Voltage	CKO_{VD}	CML 100 Ω load line-to-line	350	425	500	mV_{PP}
Common Mode Output Voltage	CKO_{VCM}	CML 100 Ω load line-to-line	—	V_{DD}-0.36	—	V
Differential Output Voltage	CKO_{VD}	LVDS 100 Ω load line-to-line	500	700	900	mV_{PP}
		Low Swing LVDS 100 Ω load line-to-line	350	425	500	mV_{PP}
Common Mode Output Voltage	CKO_{VCM}	LVDS 100 Ω load line-to-line	1.125	1.2	1.275	V
Differential Output Resistance	CKO_{RD}	CML, LVPECL, LVDS	—	200	—	Ω
Output Voltage Low	CKO_{VOLLH}	CMOS	—	—	0.4	V
Output Voltage High	CKO_{VOHLH}	V_{DD} = 1.71 V CMOS	0.8 x V_{DD}	—	—	V
Output Drive Current (CMOS driving into CKO_{VOL} for output low or CKO_{VOH} for output high. CKOUT+ and CKOUT– shorted externally)	CKO_{IO}	V_{DD} = 1.8 V	—	7.5	—	mA
		V_{DD} = 3.3 V	—	32	—	mA

Notes:
1. Current draw is independent of supply voltage
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal VDD ≥ 2.5 V.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.
6. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
2-Level LVCMOS Input Pins						
Input Voltage Low	V_{IL}	V_{DD} = 1.71 V	—	—	0.5	V
		V_{DD} = 2.25 V	—	—	0.7	V
		V_{DD} = 2.97 V	—	—	0.8	V
Input Voltage High	V_{IH}	V_{DD} = 1.89 V	1.4	—	—	V
		V_{DD} = 2.25 V	1.8	—	—	V
		V_{DD} = 3.63 V	2.5	—	—	V

Notes:
1. Current draw is independent of supply voltage
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal VDD ≥ 2.5 V.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.
6. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
3-Level Input Pins[4]						
Input Voltage Low	V_{ILL}		—	—	0.15 x V_{DD}	V
Input Voltage Mid	V_{IMM}		0.45 x V_{DD}	—	0.55 x V_{DD}	V
Input Voltage High	V_{IHH}		0.85 x V_{DD}	—	—	V
Input Low Current	I_{ILL}	See Note 4	–20	—	—	µA
Input Mid Current	I_{IMM}	See Note 4	–2	—	+2	µA
Input High Current	I_{IHH}	See Note 4	—	—	20	µA
LVCMOS Output Pins						
Output Voltage Low	V_{OL}	IO = 2 mA V_{DD} = 1.71 V	—	—	0.4	V
Output Voltage Low		IO = 2 mA V_{DD} = 2.97 V	—	—	0.4	V
Output Voltage High	V_{OH}	IO = –2 mA V_{DD} = 1.71 V	V_{DD} –0.4	—	—	V
Output Voltage High		IO = –2 mA V_{DD} = 2.97 V	V_{DD} –0.4	—	—	V

Notes:
1. Current draw is independent of supply voltage
2. No under- or overshoot is allowed.
3. LVPECL outputs require nominal VDD ≥ 2.5 V.
4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.
5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.
6. The LVPECL and CMOS output formats draw more current than either LVDS or CML; however, there are restrictions in the allowed output format pin settings so that the maximum power dissipation for the TQFP devices is limited when they are operated at 3.3 V. When there are four enabled LVPECL or CMOS outputs, the fifth output must be disabled. When there are five enabled outputs, there can be no more than three outputs that are either LVPECL or CMOS.

Table 3. AC Characteristics

(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single-Ended Reference Clock Input Pin XA (XB with cap to GND)						
Input Resistance	XA_{RIN}	RATE[1:0] = LM, MH, ac-coupled	—	12	—	kΩ
Input Voltage Swing	XA_{VPP}	RATE[1:0] = LM, MH, ac-coupled	0.5	—	1.2	V_{PP}
Differential Reference Clock Input Pins (XA/XB)						
Input Voltage Swing	XA/XB_{VPP}	RATE[1:0] = LM, MH	0.5	—	2.4	V_{PP}
CKINn Input Pins						
Input Frequency	CKN_F		.008	—	707.35	MHz
CKIN3 and CKIN4 used as FSYNC pins	CKN_F		—	8	—	kHz
Input Duty Cycle (Minimum Pulse Width)	CKN_{DC}	Whichever is smaller (i.e., the 40% / 60% limitation applies only to high frequency clocks)	40	—	60	%
			2	—	—	ns
Input Capacitance	CKN_{CIN}		—	—	3	pF
Input Rise/Fall Time	CKN_{TRF}	20–80% See Figure 2	—	—	11	ns
CKOUTn Output Pins (See ordering section for speed grade vs frequency limits)						
Output Frequency (Output not configured for CMOS or Disabled)	CKO_F		0.008	—	1050	MHz
Maximum Output Frequency in CMOS Format	CKO_F		—	—	212.5	MHz
Output Rise/Fall (20–80 %) @ 622.08 MHz output	CKO_{TRF}	Output not configured for CMOS or Disabled See Figure 2	—	230	350	ps
Output Rise/Fall (20–80%) @ 212.5 MHz output	CKO_{TRF}	CMOS Output V_{DD} = 1.71 C_{LOAD} = 5 pF	—	—	8	ns
***Note:** Input to output phase skew after an ICAL is not controlled and can assume any value.						

Table 3. AC Characteristics

(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Rise/Fall (20–80%) @ 212.5 MHz output	CKO_{TRF}	CMOS Output V_{DD} = 2.97 C_{LOAD} = 5 pF	—	—	2	ns
Output Duty Cycle Uncertainty @ 622.08 MHz	CKO_{DC}	100 Ω Load Line-to-Line Measured at 50% Point (Not for CMOS)	—	—	±40	ps
LVCMOS Input Pins						
Minimum Reset Pulse Width	t_{RSTMN}		1	—	—	µs
Input Capacitance	C_{in}		—	—	3	pF
LVCMOS Output Pins						
Rise/Fall Times	t_{RF}	C_{LOAD} = 20 pF See Figure 2	—	25	—	ns
LOSn Trigger Window	LOS_{TRIG}	From last CKINn ↑ to ↓ Internal detection of LOSn	—	—	4.5 x N3	T_{CKIN}
Time to Clear LOL after LOS Cleared	t_{CLRLOL}	↓LOS to ↓LOL Fold = Fnew Stable XA/XB reference	—	10	—	ms
Device Skew						
Output Clock Skew	t_{SKEW}	↑ of CKOUTn to ↑ of CKOUT_m, CKOUTn and CKOUT_m at same frequency	—	—	100	ps
Phase Change due to Temperature Variation*	t_{TEMP}	Max phase changes from –40 to +85 °C	—	300	500	ps
***Note:** Input to output phase skew after an ICAL is not controlled and can assume any value.						

Table 3. AC Characteristics

(V_{DD} = 1.8 ± 5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PLL Performance (fin = fout = 622.08 MHz; BW = 120 Hz; LVPECL)						
Lock Time	t_{LOCKMP}	Start of ICAL to ↓ of LOL	—	35	1200	ms
Output Clock Phase Change	t_{P_STEP}	After clock switch f3 ≥ 128 kHz	—	200	—	ps
Closed Loop Jitter Peaking	J_{PK}		—	0.05	0.1	dB
Jitter Tolerance	J_{TOL}	Jitter Frequency ≥ Loop Bandwidth	5000/BW	—	—	ns pk-pk
Phase Noise fout = 622.08 MHz	CKO_{PN}	1 kHz Offset	—	–106	—	dBc/Hz
		10 kHz Offset	—	–121	—	dBc/Hz
		100 kHz Offset	—	–132	—	dBc/Hz
		1 MHz Offset	—	–131	—	dBc/Hz
Spurious Noise	SP_{SPUR}	Max spur @ n x F3 (n ≥ 1, n x F3 < 100 MHz)	—	–93	–70	dBc

***Note:** Input to output phase skew after an ICAL is not controlled and can assume any value.

Table 4. Jitter Generation

Parameter	Symbol	Test Condition*		Min	Typ	Max	GR-253-Specification	Unit
		Measurement Filter	DSPLL BW[2]					
Jitter Gen OC-192	JGEN	0.02–80 MHz	120 Hz	—	4.2	6.2	30	ps_{PP}
				—	.27	.42	N/A	ps_{rms}
		4–80 MHz	120 Hz	—	3.7	6.4	10	ps_{PP}
				—	.14	.31	N/A	ps_{rms}
		0.05–80 MHz	120 Hz	—	4.4	6.9	10	ps_{PP}
				—	.26	.41	1.0	ps $_{rms}$
Jitter Gen OC-48	JGEN	0.12–20 MHz	120 Hz	—	3.5	5.4	40.2	ps_{PP}
				—	.27	.41	4.02	ps $_{rms}$

***Note:** Test conditions:
1. fIN = fOUT = 622.08 MHz.
2. Clock input: LVPECL .
3. Clock output: LVPECL.
4. PLL bandwidth: 120 Hz.
5. 114.285 MHz 3rd OT crystal used as XA/XB input.
6. V_{DD} = 2.5 V.
7. T_A = 85 °C.
8. Jitter integration bands include low-pass (–20 dB/Dec) and high-pass (–60 dB/Dec) roll-offs per Telecordia GR-253-CORE.

Table 5. Thermal Characteristics

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	31	C°/W

Table 6. Absolute Maximum Ratings*

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}		–0.5	—	3.8	V
LVCMOS Input Voltage	V_{DIG}		–0.3		V_{DD}+0.3	V
CKINn Voltage Level Limits	CKN_{VIN}		0	—	V_{DD}	V
XA/XB Voltage Level Limits	XA_{VIN}		0	—	1.2	V
Operating Junction Temperature	T_{JCT}		–55	—	150	ºC
Storage Temperature Range	T_{STG}		–55	—	150	ºC
ESD HBM Tolerance (100 pF, 1.5 kΩ); All pins except CKIN+/CKIN–			2	—	—	kV
ESD MM Tolerance; All pins except CKIN+/CKIN–			150	—	—	V
ESD HBM Tolerance (100 pF, 1.5 kΩ); CKIN+/CKIN–			700	—	—	V
ESD MM Tolerance; CKIN+/CKIN–			100	—	—	V
Latch-up Tolerance			JESD78 Compliant			

***Note:** Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

1. Typical Phase Noise Performance

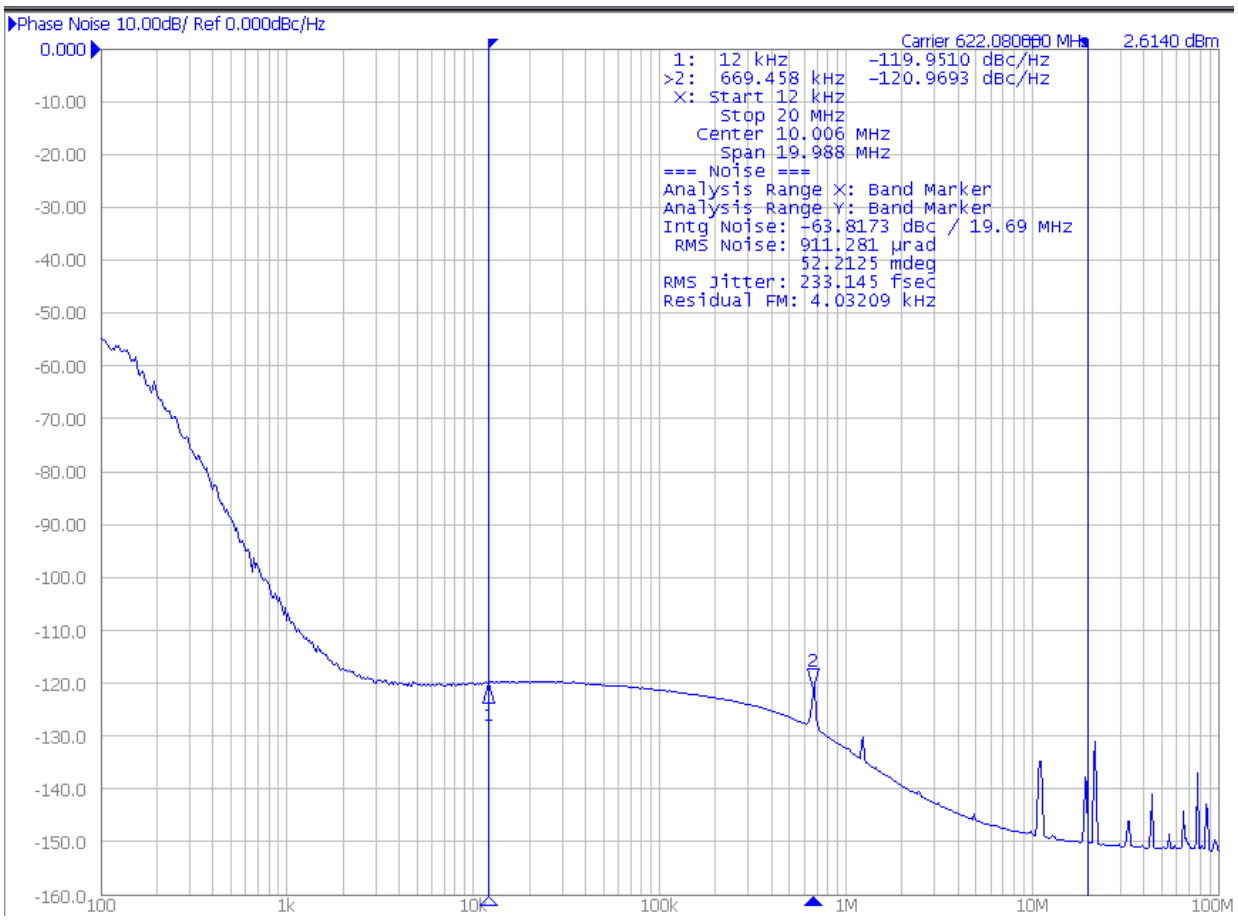
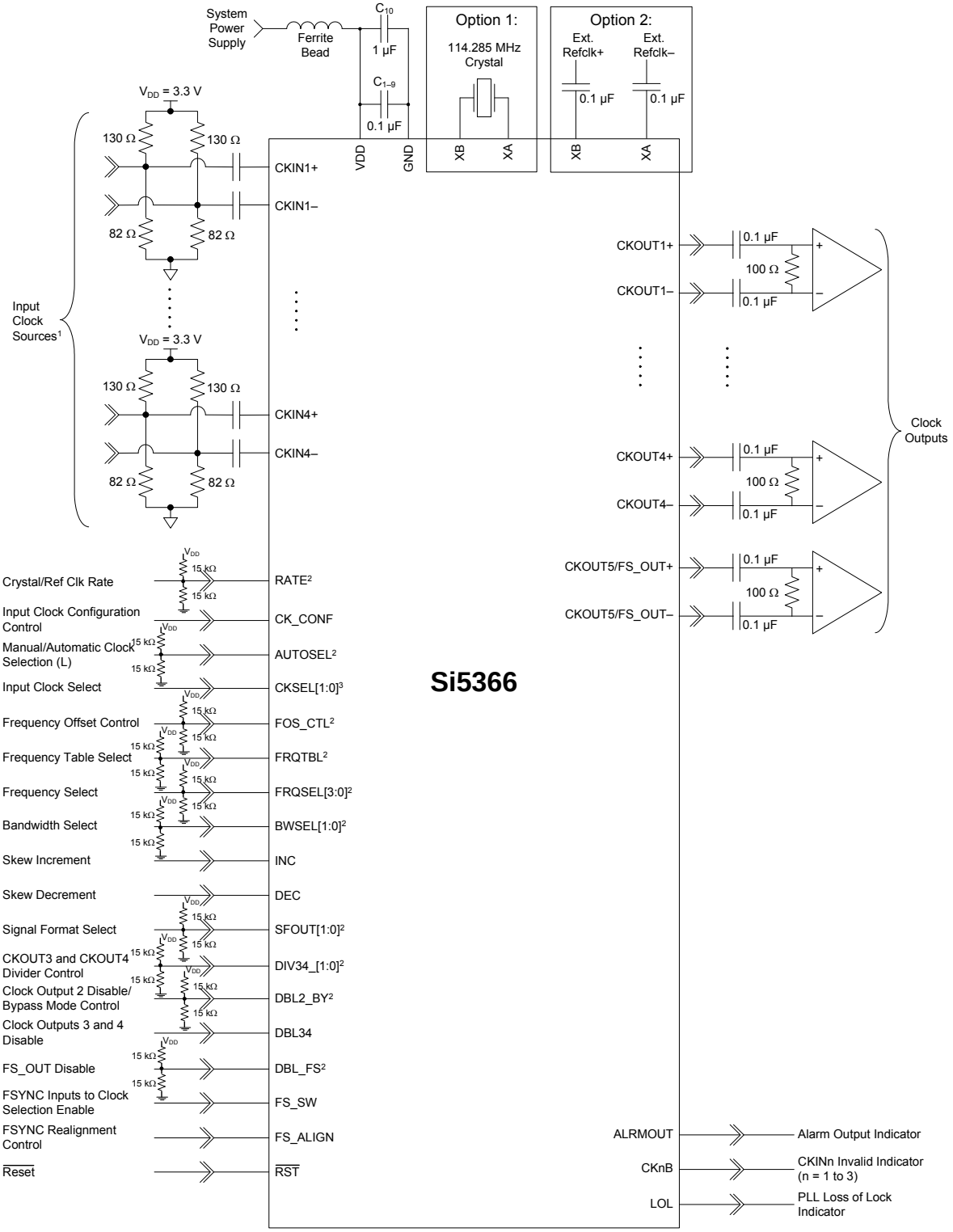


Figure 3. Typical Phase Noise Plot

Table 7. RMS Jitter by Band

Jitter Band	RMS Jitter
SONET_OC48, 12 kHz to 20 MHz	249 fs
SONET_OC192_A, 20 kHz to 80 MHz	274 fs
SONET_OC192_B, 4 MHz to 80 MHz	166 fs
SONET_OC192_C, 50 kHz to 80 MHz	267 fs
Brick Wall_800 Hz to 80 MHz	274 fs
***Note:** Jitter integration bands include low-pass (–20 dB/Dec) and hi-pass (–60 dB/Dec) roll-offs per Telcordia GR-253-CORE.	

2. Typical Application Schematic



Notes: 1. Assumes differential LVPECL termination (3.3 V) on clock inputs.
2. Denotes tri-level input pins with states designated as L (ground), M (VDD/2), and H (VDD).
3. Assumes manual input clock selection.

Figure 4. Si5366 Typical Application Circuit

3. Functional Description

The Si5366 is a jitter-attenuating precision clock multiplier for high-speed communication systems, including SONET OC-48/OC-192, Ethernet, and Fibre Channel. The Si5366 accepts four clock inputs ranging from 8 kHz to 707 MHz and generates five frequency-multiplied clock outputs ranging from 8 kHz to 1050 MHz. By default the four clock inputs are at the same frequency and the five clock outputs are at the same frequency. Two of the output clocks can be divided down further to generate an integer sub-multiple frequency. Optionally, the fifth clock output can be configured as a 8 kHz SONET/SDH frame synchronization output that is phase aligned with one of the high-speed output clocks. The input clock frequency and clock multiplication ratio are selectable from a table of popular SONET, Ethernet, and Fibre Channel frequencies. In addition to providing clock multiplication in SONET and datacom applications, the Si5366 supports SONET-to-datacom frequency translations. Silicon Laboratories offers a PC-based software utility, DSPLL*sim*, that can be used to look up valid Si5366 frequency translations. This utility can be downloaded from http://www.silabs.com/timing (click on Documentation).

The Si5366 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The Si5366 PLL loop bandwidth is selectable via the BWSEL[1:0] pins and supports a range from 60 Hz to 8.4 kHz. The DSPLL*sim* software utility can be used to calculate valid loop bandwidth settings for a given input clock frequency/clock multiplication ratio.

The Si5366 supports hitless switching between input clocks in compliance with GR-253-CORE and GR-1244-CORE that greatly minimizes the propagation of phase transients to the clock outputs during an input clock transition (<200 ps typ). Manual and automatic revertive and non-revertive input clock switching options are available via the AUTOSEL input pin. The Si5366 monitors the four input clocks for loss-of-signal and provides a LOS alarm when it detects missing pulses on any of the four input clocks. The device monitors the lock status of the PLL. The lock detect algorithm works by continuously monitoring the phase of the input clock in relation to the phase of the feedback clock. If a potential phase cycle slip is detected, the LOL output is set high. The Si5366 monitors the frequency of CKIN1, CKIN3, and CKIN4 with respect to a reference frequency applied to CKIN2, and generates a frequency offset alarm (FOS) if the threshold is exceeded.

This FOS feature is available for SONET applications in which both the monitored frequency on CKIN1, CKIN3, and CKIN4 and the reference frequency are integer multiples of 19.44 MHz. Both Stratum 3/3E and SONET Minimum Clock (SMC) FOS thresholds are supported.

The Si5366 provides a digital hold capability that allows the device to continue generation of a stable output clock when the selected input reference is lost. During digital hold, the DSPLL is locked to an input frequency that existed a fixed amount of time before the error event occurred, eliminating the effects of phase and frequency transients that may occur immediately preceding digital hold.

The Si5366 has five differential clock outputs. The signal format of the clock outputs is selectable to support LVPECL, LVDS, CML, or CMOS loads. If not required, unused clock outputs can be powered down to minimize power consumption. The phase difference between the selected input clock and the output clocks is adjustable in 200 ps increments for system skew control. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 1.8, 2.5, or 3.3 V supply.

3.1. External Reference

An external, high quality clock or a low-cost 114.285 MHz 3rd overtone crystal is used as part of a fixed-frequency oscillator within the DSPLL. This external reference is required for the device to perform jitter attenuation. Silicon Laboratories recommends using a high-quality crystal. Specific recommendations may be found in the Family Reference Manual.

In digital hold, the DSPLL remains locked to this external reference. Any changes in the frequency of this reference when the DSPLL is in digital hold, will be tracked by the output of the device. Note that crystals can have temperature sensitivities.

3.2. Further Documentation

Consult the Silicon Laboratories Any-Frequency Precision Clock Family Reference Manual (FRM) for detailed information about the Si5366. Additional design support is available from Silicon Laboratories through your distributor.

Silicon Laboratories has developed a PC-based software utility called DSPLL*sim* to simplify device configuration, including frequency planning and loop bandwidth selection. The FRM and this utility can be downloaded from http://www.silabs.com/timing; click on Documentation.

4. Pin Descriptions: Si5366 (Top View)

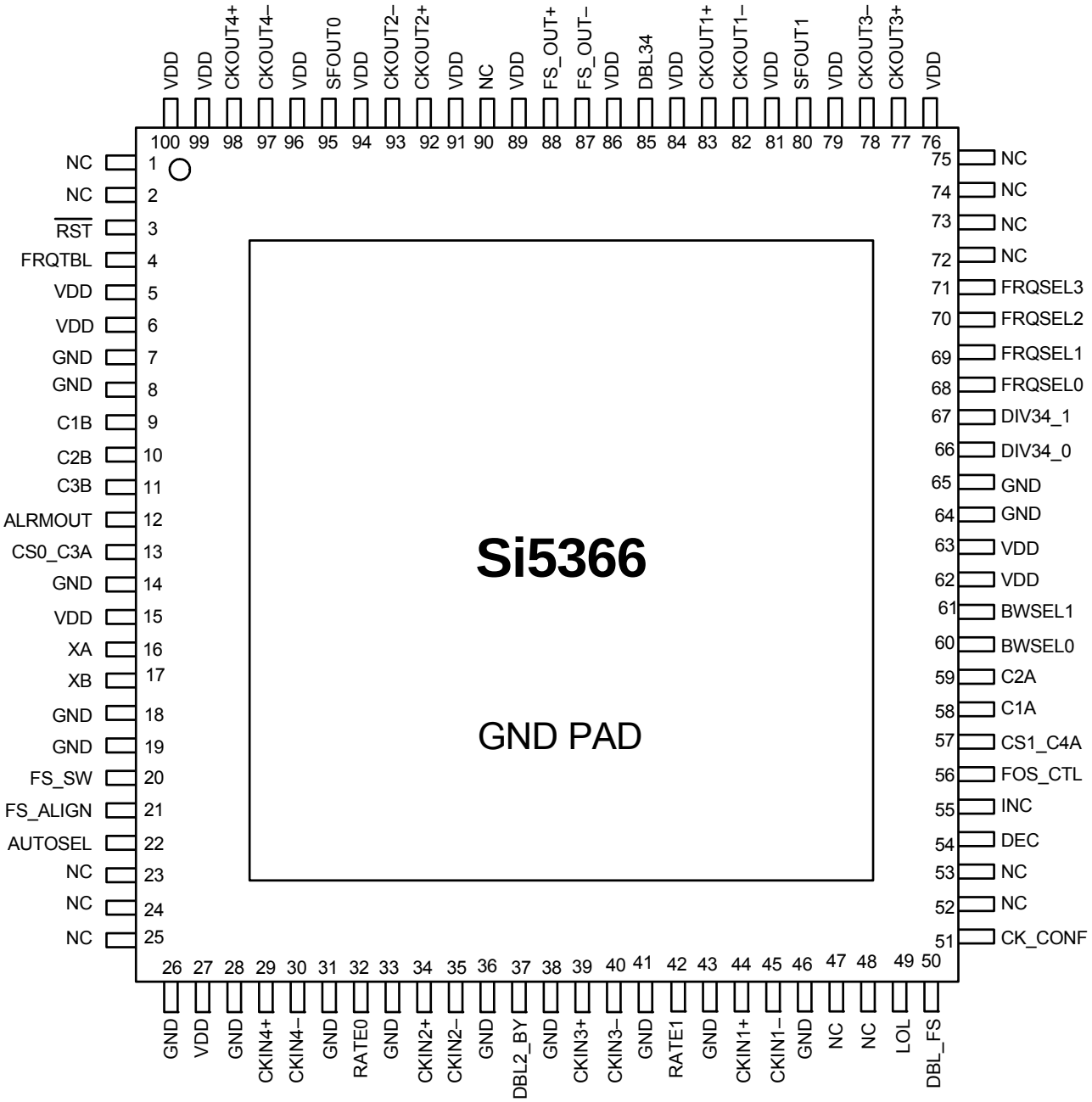


Table 8. Si5366 Pin Descriptions

Pin #	Pin Name	I/O	Signal Level	Description
1, 2, 23, 24, 25, 47, 48, 52, 53, 72, 73, 74, 75, 90	NC			**No Connect.** These pins must be left unconnected for normal operation.
3	$\overline{\text{RST}}$	I	LVCMOS	**External Reset.** Active low input that performs external hardware reset of device. Resets all internal logic to a known state and forces the device registers to their default value. Clock outputs are disabled during reset. After rising edge of $\overline{\text{RST}}$ signal, the device will perform an internal self-calibration when a valid input signal is present. This pin has a weak pull-up.
4	FRQTBL	I	3-Level	**Frequency Table Select.** This pin selects SONET/SDH, datacom, or SONET/SDH to datacom frequency translation table. L = SONET/SDH. M = Datacom. H = SONET/SDH to Datacom. This pin has both weak pull-ups and weak pull-downs and defaults to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
5, 6, 15, 27, 62, 63, 76, 79, 81, 84, 86, 89, 91, 94, 96, 99, 100	V_{DD}	V_{DD}	Supply	**V_{DD}.** The device operates from a 1.8 or 2.5 V supply. Bypass capacitors should be associated with the following V_{DD} pins: Pins — Bypass Cap 5, 6 — 0.1 µF 15 — 0.1 µF 27 — 0.1 µF 62, 63 — 0.1 µF 76, 79 — 1.0 µF 81, 84 — 0.1 µF 86, 89 — 0.1 µF 91, 94 — 0.1 µF 96, 99, 100 — 0.1 µF
7, 8, 14, 18, 19, 26, 28, 31, 33, 36, 38, 41, 43, 46, 64, 65	GND	GND	Supply	**Ground.** This pin must be connected to system ground. Minimize the ground path impedance for optimal performance.
9	C1B	O	LVCMOS	**CKIN1 Invalid Indicator.** This pin is an active high alarm output associated with CKIN1. Once triggered, the alarm will remain high until CKIN1 is validated. 0 = No alarm on CKIN1. 1 = Alarm on CKIN1.

Table 8. Si5366 Pin Descriptions (Continued)

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>I/O</th><th>Signal Level</th><th>Description</th></tr>
<tr><td>10</td><td>C2B</td><td>O</td><td>LVCMOS</td><td>CKIN2 Invalid Indicator.
This pin is an active high alarm output associated with CKIN2. Once triggered, the alarm will remain high until CKIN2 is validated.
0 = No alarm on CKIN2.
1 = Alarm on CKIN2.</td></tr>
<tr><td>11</td><td>C3B</td><td>O</td><td>LVCMOS</td><td>CKIN3 Invalid Indicator.
This pin is an active high alarm output associated with CKIN3.
0 = No alarm on CKIN3.
1 = Alarm on CKIN3.</td></tr>
<tr><td>12</td><td>ALRMOUT</td><td>O</td><td>LVCMOS</td><td>Alarm Output Indicator.
This pin is an active high alarm output associated with CKIN4 or the frame sync alignment alarm.
0 = ALRMOUT not active.
1 = ALRMOUT active.</td></tr>
<tr><td>13
57</td><td>CS0_C3A
CS1_C4A</td><td>I/O</td><td>LVCMO</td><td>Input Clock Select/CKINn Active Clock Indicator.
Input: If manual clock selection mode is chosen (AUTOSEL = L), the CS[1:0] pins function as the manual input clock selector control.
<table>
<tr><th>CS[1:0]</th><th>Active Input Clock</th></tr>
<tr><td>00</td><td>CKIN1</td></tr>
<tr><td>01</td><td>CKIN2</td></tr>
<tr><td>10</td><td>CKIN3</td></tr>
<tr><td>11</td><td>CKIN4</td></tr>
</table>
These inputs are internally deglitched to prevent inadvertent clock switching during changes in the CSn input state. If configured as input, these pins must not float.
Output: If automatic clock detection is chosen (AUTOSEL = M or H), these pins function as the CKINn active clock indicator output.
0 = CKINn is not the active input clock.
1 = CKINn is currently the active input clock to the PLL.</td></tr>
<tr><td>16
17</td><td>XA
XB</td><td>I</td><td>ANALOG</td><td>External Crystal or Reference Clock.
An external crystal or an external clock should be connected to these pins. Frequency of crystal or external clock is set by the RATE pins. The quality of the selected crystal or external clock affects the quality of the part's output; refer to the Family Reference Manual for external reference selection and interfacing.</td></tr>
<tr><td>20</td><td>FS_SW</td><td>I</td><td>LVCMOS</td><td>FSYNC Inputs to Clock Selection Enable.
If CK_CONF = 1, this pin enables the use of the CKIN3 and CKIN4 loss-of-signal indicators as inputs to the clock selection state machine.
0 = Do not use CKIN3 and CKIN4 LOS indicators as inputs to the clock selection state machine.
1 = Use CKIN3 and CKIN4 LOS indicators as inputs to the clock selection state machine.
This pin has a weak pull-down.</td></tr>
</table>

Table 8. Si5366 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
21	FS_ALIGN	I	LVCMOS	**FSYNC Alignment Control.** If CK_CONF = 1, a logic high on this pin causes the FS_OUT phase to be realigned to the rising edge of the currently active input sync (CKIN3 or CKIN4). 0 = No realignment. 1 = Realignment. This pin has a weak pull-down.
22	AUTOSEL	I	3-Level	**Manual/Automatic Clock Selection.** Three level input that selects the method of input clock selection to be used. L = Manual. M = Automatic non-revertive. H = Automatic revertive. This pin has both weak pull-ups and weak pull-downs and defaults to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
29 30	CKIN4+ CKIN4–	I	MULTI	**Clock Input 4.** Differential clock input. This input can also be driven with a single-ended signal. CKIN4 serves as the frame sync input associated with the CKIN2 clock when CK_CONF = 1.
32 42	RATE0 RATE1	I	3-Level	**External Crystal or Reference Clock Rate.** Three-level inputs that select the type and rate of external crystal or reference clock to be applied to the XA/XB port. Refer to the Family Reference Manual for settings. These pins have both a weak pull-up and a weak pull-down and default to M. Some designs may require an external resistor voltage divider when driven by an active device.
34 35	CKIN2+ CKIN2–	I	MULTI	**Clock Input 2.** Differential input clock. This input can also be driven with a single-ended signal.
37	DBL2_BY	I	3-Level	**CKOUT2 Disable/PLL Bypass Mode Control.** Controls enable of CKOUT2 divider/output buffer path and PLL bypass mode. L = CKOUT2 Enabled. M = CKOUT2 Disabled. H = BYPASS Mode with CKOUT2 enabled. Bypass mode does not support CMOS outputs. This pin has both weak pull-ups and weak pull-downs and defaults to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
39 40	CKIN3+ CKIN3–	I	MULTI	**Clock Input 3.** Differential clock input. This input can also be driven with a single-ended signal. CKIN3 serves as the frame sync input associated with the CKIN1 clock when CK_CONF = 1.
44 45	CKIN1+ CKIN1–	I	MULTI	**Clock Input 1.** Differential clock input. This input can also be driven with a single-ended signal.

Table 8. Si5366 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
49	LOL	O	LVCMOS	**PLL Loss of Lock Indicator.** This pin functions as the active high PLL loss of lock indicator. 0 = PLL locked. 1 = PLL unlocked.
50	DBL_FS	I	3-Level	**FS_OUT Disable.** This pin performs the following functions: L = Normal operation. Output path is active and signal format is determined by SFOUT inputs. M = CMOS signal format. Overrides SFOUT signal format to allow FS_OUT to operate in CMOS format while the clock outputs operate in a differential output format. H = Powerdown. Entire FS_OUT divider and output buffer path is powered down. This pin has both weak pull-ups and weak pull-downs and defaults to M.Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
51	CK_CONF	I	LVCMOS	**Input Clock Configuration Control.** This pin controls the input clock configuration. 0 = CKIN1, 2, 3, 4 inputs, no FS_OUT alignment. 1 = CKIN1, 3 and CKIN2, 4 clock/FSYNC pairs. This pin has a weak pull-down.
54	DEC	I	LVCMOS	**Coarse Skew Decrement.** A pulse on this pin decreases the input to output device skew by $1/f_{OSC}$ (approximately 200 ps). Detailed operations and timing characteristics for this pin may be found in the Any-Frequency Precision Clock Family Reference Manual. There is no limit on the range of skew adjustment by this method. If both INC and DEC are tied high, phase buildout is disabled and the device maintains a fixed-phase relationship between the selected input clock and the output clock during an input clock switch. Detailed operations and timing characteristics for this pin may be found in the Any-Frequency Precision Clock Family Reference Manual. This pin has a weak pull-down.
55	INC	I	LVCMOS	**Coarse Skew Increment.** A pulse on this pin increases the input to output skew by $1/f_{OSC}$ (approximately 200 ps). Detailed operations and timing characteristics for this pin may be found in the Any-Frequency Precision Clock Family Reference Manual. There is no limit on the range of skew adjustment by this method. If both INC and DEC are tied high, phase buildout is disabled and the device maintains a fixed-phase relationship between the selected input clock and the output clock during an input clock switch. Detailed operations and timing characteristics for this pin may be found in the Any-Frequency Precision Clock Family Reference Manual. **Note:** INC does not increase skew if NI_HS = 4. This pin has a weak pull-down.

Table 8. Si5366 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
56	FOS_CTL	I	3-Level	**Frequency Offset Control.** This pin enables or disables use of the CKIN2 FOS reference as an input to the clock selection state machine. L = FOS Disabled. M = Stratum 3/3E FOS Threshold. H = SONET Minimum Clock FOS Threshold. This pin has both weak pull-ups and weak pull-downs and defaults to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
58	C1A	O	LVCMOS	**CKIN1 Active Clock Indicator.** This pin serves as the CKIN1 active clock indicator. 0 = CKIN1 is not the active input clock. 1 = CKIN1 is currently the active input clock to the PLL.
59	C2A	O	LVCMOS	**CKIN2 Active Clock Indicator.** This pin serves as the CKIN2 active clock indicator. 0 = CKIN2 is not the active input clock. 1 = CKIN2 is currently the active input clock to the PLL.
60 61	BWSEL0 BWSEL1	I	3-Level	**Bandwidth Select.** These pins are three level inputs that select the DSPLL closed loop bandwidth. Detailed operations and timing characteristics for these pins may be found in the Any-Frequency Precision Clock Family Reference Manual. These pins have both weak pull-ups and weak pull-downs and default to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
66 67	DIV34_0 DIV34_1	I	3-Level	**CKOUT3 and CKOUT4 Divider Control.** These pins control the division of CKOUT3 and CKOUT4 relative to the CKOUT2 output frequency. Detailed operations and timing characteristics for these pins may be found in the Any-Frequency Precision Clock Family Reference Manual. These pins have both weak pull-ups and weak pull-downs and default to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
68 69 70 71	FRQSEL0 FRQSEL1 FRQSEL2 FRQSEL3	I	3-Level	**Multiplier Select.** These pins are three level inputs that select the input clock and clock multiplication setting according to the Any-Frequency Precision Clock Family Reference Manual, depending on the FRQTBL setting. These pins have both weak pull-ups and weak pull-downs and default to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
77 78	CKOUT3+ CKOUT3–	O	MULTI	**Clock Output 3.** Differential output clock with a frequency specified by FRQSEL and FRQTBL settings. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.

Table 8. Si5366 Pin Descriptions (Continued)

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>I/O</th><th>Signal Level</th><th>Description</th></tr>
<tr><td>80
95</td><td>SFOUT1
SFOUT0</td><td>I</td><td>3-Level</td><td>Signal Format Select.
Three level inputs that select the output signal format (common mode voltage and differential swing) for all of the clock outputs except FS_OUT. See DBL_FS pin descripition.
<table>
<tr><th>SFOUT[1:0]</th><th>Signal Format</th></tr>
<tr><td>HH</td><td>Reserved</td></tr>
<tr><td>HM</td><td>LVDS</td></tr>
<tr><td>HL</td><td>CML</td></tr>
<tr><td>MH</td><td>LVPECL</td></tr>
<tr><td>MM</td><td>Reserved</td></tr>
<tr><td>ML</td><td>LVDS—Low Swing</td></tr>
<tr><td>LH</td><td>CMOS</td></tr>
<tr><td>LM</td><td>Disabled</td></tr>
<tr><td>LL</td><td>Reserved</td></tr>
</table>
Bypass mode is not supported with CMOS outputs. These pins have both weak pull-ups and weak pull-downs and default to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.</td></tr>
<tr><td>82
83</td><td>CKOUT1–
CKOUT1+</td><td>O</td><td>MULTI</td><td>Clock Output 1.
Differential output clock with a frequency specified by FRQSEL and FRQTBL. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.</td></tr>
<tr><td>85</td><td>DBL34</td><td>I</td><td>LVCMOS</td><td>Output 3 and 4 Disable.
Active high input. When active, entire CKOUT3 and CKOUT4 divider and output buffer path is powered down. CKOUT3 and CKOUT4 outputs will be in tristate mode during powerdown. This pin has a weak pull-up.</td></tr>
<tr><td>87
88</td><td>FS_OUT–
FS_OUT+</td><td>O</td><td>MULTI</td><td>Frame Sync Output.
Differential 8 kHz frame sync output or fifth high-speed clock output with a frequency specified by FRQSEL and FRQTBL. Output signal format is selected by SFOUT pins. Detailed operations and timing characteristics for this pin may be found in the Any-Frequency Precision Clock Family Reference Manual. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.</td></tr>
<tr><td>92
93</td><td>CKOUT2+
CKOUT2–</td><td>O</td><td>MULTI</td><td>Clock Output 2.
Differential output clock with a frequency specified by FRQSEL and FRQTBL. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.</td></tr>
</table>

Table 8. Si5366 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
97 98	CKOUT4– CKOUT4+	O	MULTI	**Clock Output 4.** Differential output clock with a frequency specified by FRQSEL and FRQTBL settings. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
GND PAD	GND PAD	GND	Supply	**Ground Pad**. The ground pad must provide a low thermal and electrical impedance to a ground plane.

5. Ordering Guide

Ordering Part Number	Package	ROHS6, Pb-Free	Temperature Range
Si5366-C-GQ	100-Pin 14 x 14 mm TQFP	Yes	–40 to 85 °C

6. Package Outline: 100-Pin TQFP

Figure 5 illustrates the package details for the Si5366. Table 9 lists the values for the dimensions shown in the illustration.

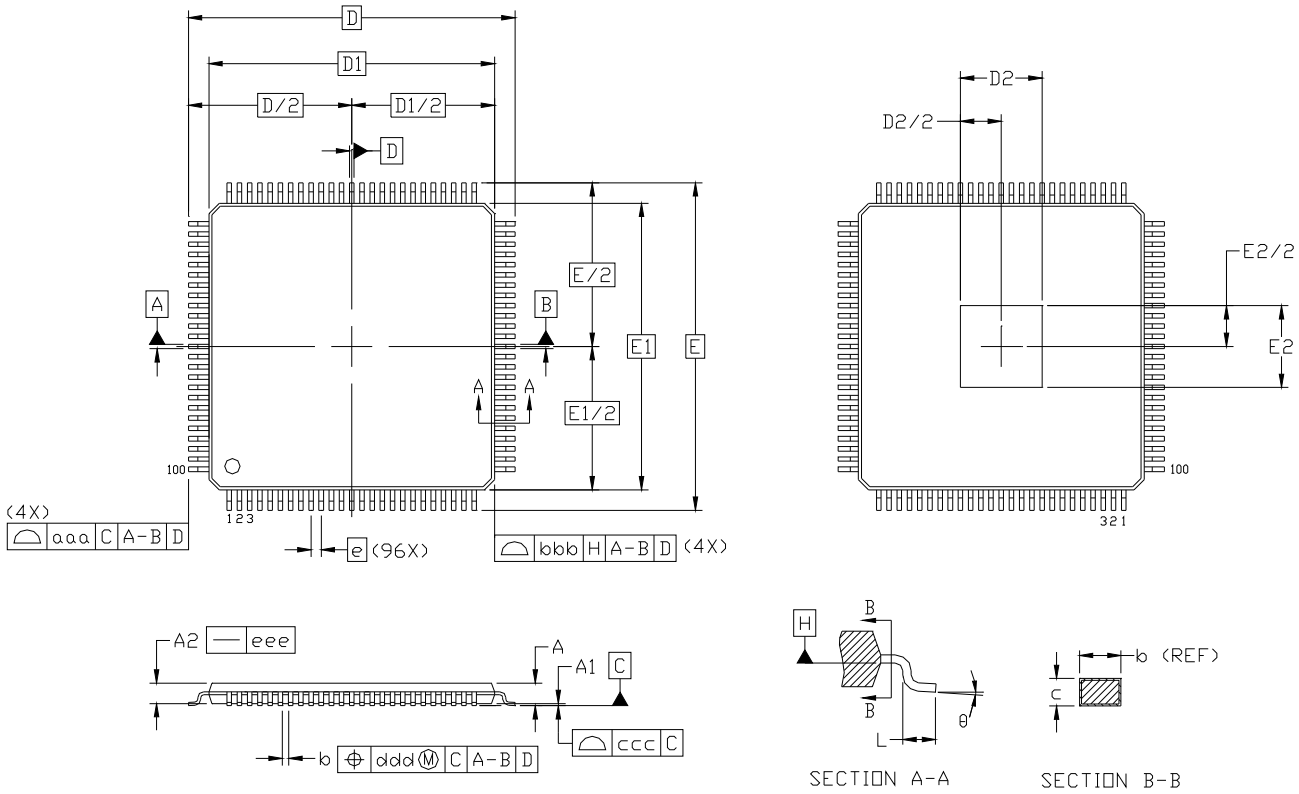


Figure 5. 100-Pin Thin Quad Flat Package (TQFP)

Table 9. 100-Pin Package Diagram Dimensions

Dimension	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	—	0.20
D	16.00 BSC		
D1	14.00 BSC		
D2	3.85	4.00	4.15
e	0.50 BSC		

Dimension	Min	Nom	Max
E	16.00 BSC		
E1	14.00 BSC		
E2	3.85	4.00	4.15
L	0.45	0.60	0.75
aaa	—	—	0.20
bbb	—	—	0.20
ccc	—	—	0.08
ddd	—	—	0.08
θ	0°	3.5°	7°

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant AED-HD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. PCB Land Pattern

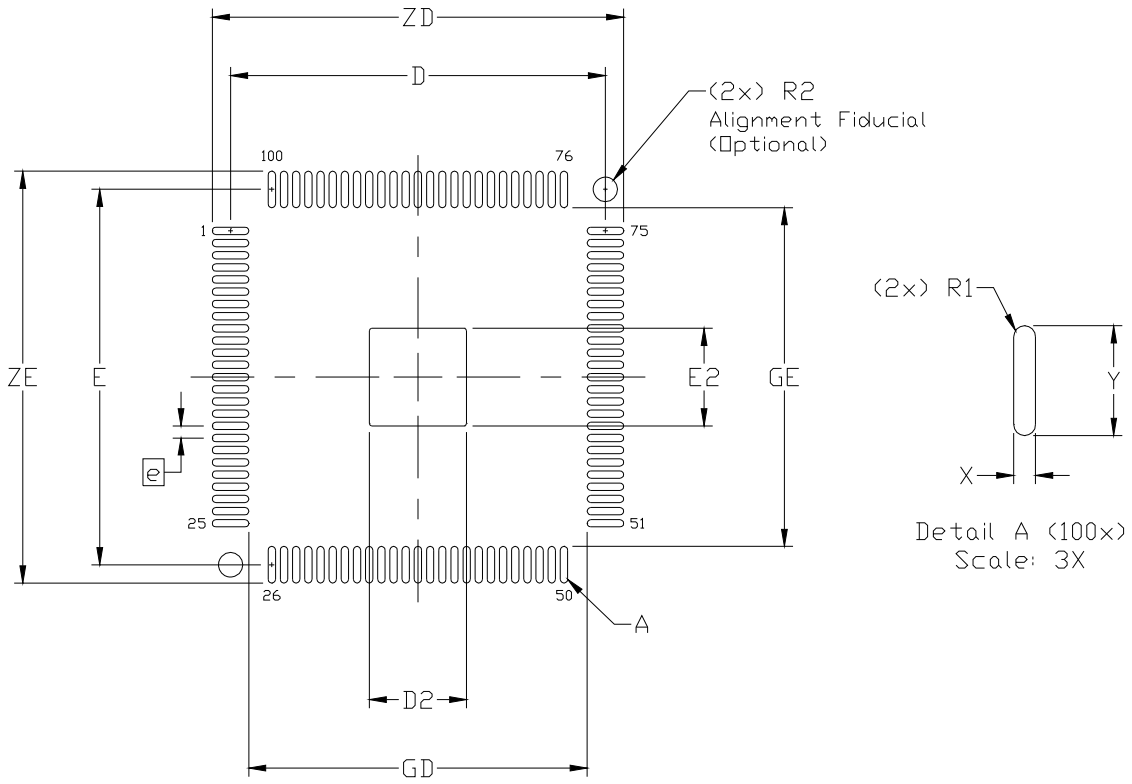


Figure 6. PCB Land Pattern Diagram

Table 10. PCB Land Pattern Dimensions

Dimension	MIN	MAX
e	0.50 BSC.	
E	15.40 REF.	
D	15.40 REF.	
E2	3.90	4.10
D2	3.90	4.10
GE	13.90	—
GD	13.90	—
X	—	0.30
Y	1.50 REF.	
ZE	—	16.90
ZD	—	16.90
R1	0.15 REF	
R2	—	1.00

Notes

General:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design:

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design:

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
9. A 4 x 4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

Card Assembly:

10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. Top Marking

8.1. Si5366 Top Marking (TQFP)

8.2. Top Marking Explanation

Mark Method:	Laser	
Logo Size:	9.2 x 3.1 mm Center-Justified	
Font Size:	3.0 Point (1.07 mm) Right-Justified	
Line 1 Marking:	Device Part Number Si5366-C-GQ	
Line 2 Marking:	YY = Year WW = Workweek	Assigned by the Assembly Supplier. Corresponds to the year and work-week of the mold date.
	R = Die Revision	
	TTTTT = Mfg Code	Manufacturing Code
Line 3 Marking:	Circle = 1.8 mm Diameter Center-Justified	“e3” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	

Document Change List

Revision 0.1 to Revision 0.2

- Updated Table 1, “Performance Specifications,” on page 4.
- Changed LVTTL to LVCMOS in Table 2, “Absolute Maximum Ratings,” on page 5.
- Added Figure 1, “Typical Phase Noise Plot,” on page 6.
- Updated “4. Pin Descriptions: Si5366”.
- Updated "5. Ordering Guide" on page 25.
- Added “7. PCB Land Pattern”.

Revision 0.2 to Revision 0.3

- Changed 1.8 V operating range to ±5%.
- Clarified "4. Pin Descriptions: Si5366" on page 17.
- Updated "6. Package Outline: 100-Pin TQFP" on page 26.

Revision 0.3 to Revision 1.0

- Expanded spec tables (1, 2, 3, 4, and 5).
- Changed “any-rate” to “any-frequency” throughout.
- Added 3.3 V operation.
- Added note about bypass with CMOS outputs.
- Added device top mark.

NOTES:

ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

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Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

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