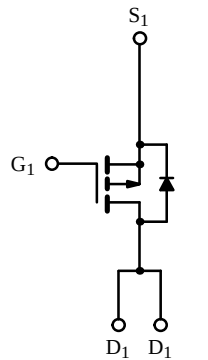
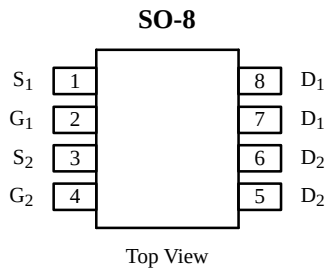


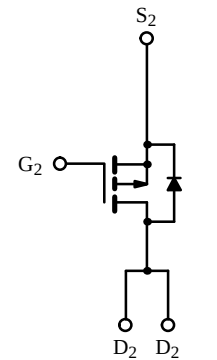
Dual P-Channel Enhancement-Mode MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-30	0.053 @ $V_{GS} = -10$ V	± 4.9
	0.095 @ $V_{GS} = -4.5$ V	± 3.6



P-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	± 4.9	A
		± 3.9	
Pulsed Drain Current	I_{DM}	± 30	
Continuous Source Current (Diode Conduction) ^a	I_S	-1.7	W
Maximum Power Dissipation ^a	P_D	2.0	
		1.3	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1235. A SPICE Model data sheet is available for this product (FaxBack document #5152).

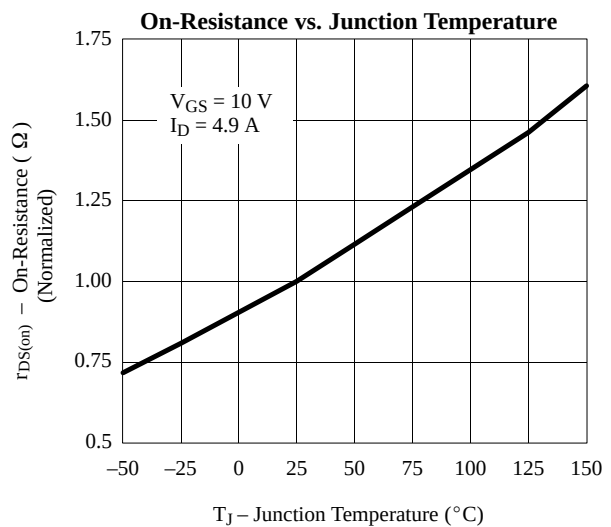
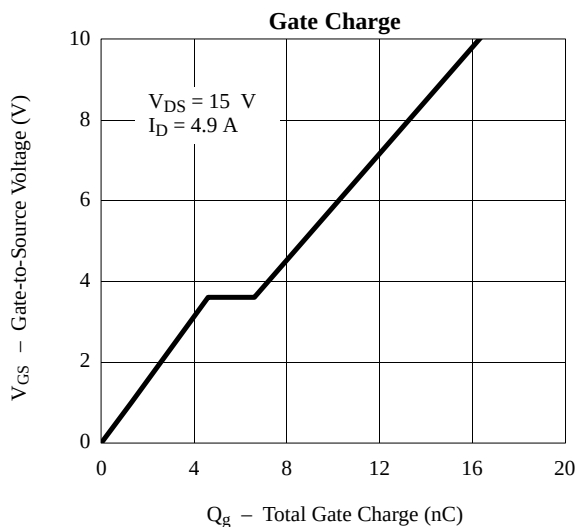
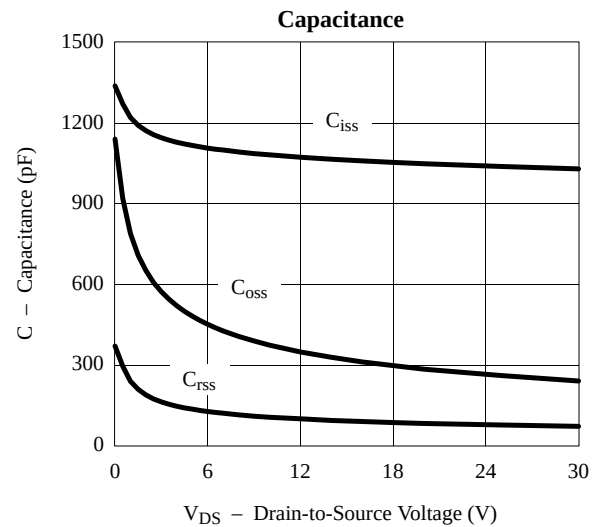
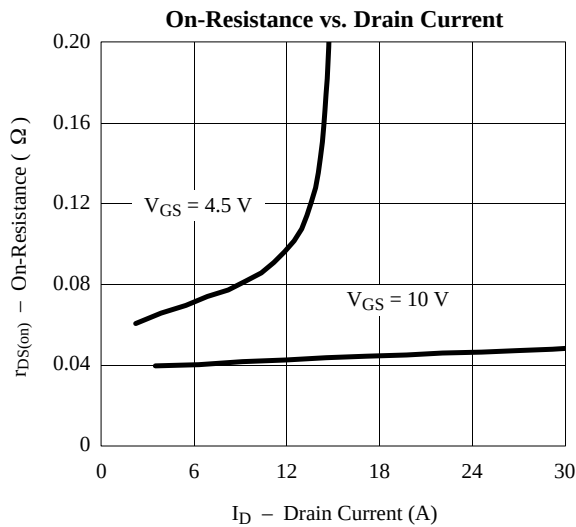
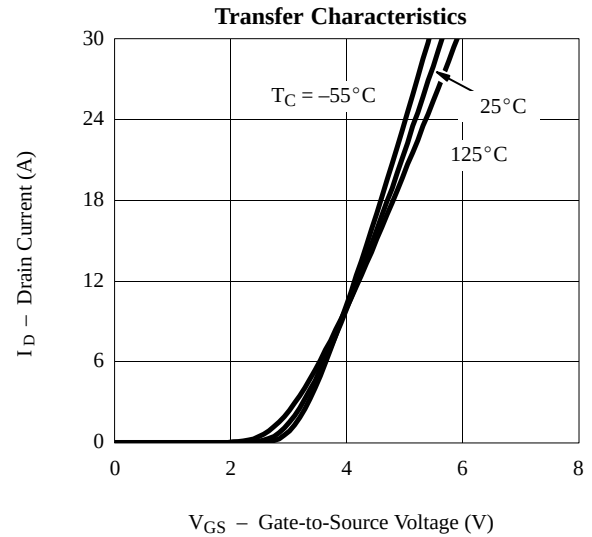
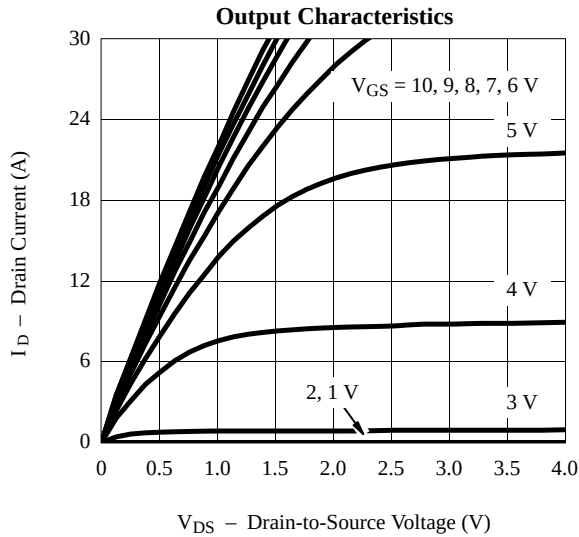
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -30\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			-25	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \leq -5\ \text{V}, V_{GS} = -10\ \text{V}$	-20			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = -10\ \text{V}, I_D = -4.9\ \text{A}$		0.043	0.053	Ω
		$V_{GS} = -4.5\ \text{V}, I_D = -3.6\ \text{A}$		0.070	0.095	
Forward Transconductance ^b	g_{fs}	$V_{DS} = -15\ \text{V}, I_D = -4.9\ \text{A}$		10		S
Diode Forward Voltage ^b	V_{SD}	$I_S = -1.7\ \text{A}, V_{GS} = 0\ \text{V}$		0.8	-1.2	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = -15\ \text{V}, V_{GS} = -10\ \text{V}, I_D = -4.9\ \text{A}$		16	25	nC
Gate-Source Charge	Q_{gs}			5		
Gate-Drain Charge	Q_{gd}			2		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15\ \text{V}, R_L = 15\ \Omega$ $I_D \cong -1\ \text{A}, V_{GEN} = -10\ \text{V}, R_G = 6\ \Omega$		9	15	ns
Rise Time	t_r			13	20	
Turn-Off Delay Time	$t_{d(off)}$			25	40	
Fall Time	t_f			15	25	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.7\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		60	90	

Notes

- a. For design aid only; not subject to production testing.
 b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Noted)



Typical Characteristics (25°C Unless Noted)

