SYVANTEK

SYC74HCT612
Memory Mapper

Features:

- Designed for paged memory mapping
- Expands 4 address lines to 12 address lines
- Single +5V power supply
- Totally TTL compatible: All inputs and outputs
- High-current three-state output

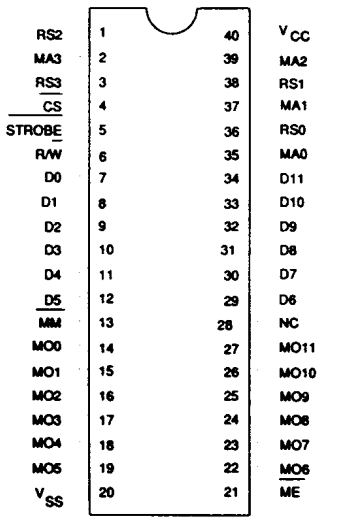
Description:

The SYC74HCT612 is a high-speed memory mapper, fabricated using high-performance, high-reliability CMOS technology. it is designed to expand a microprocessor's memory address capability by 8 bits (from 4 to 12). It contains a 4-line to 16-line decoder, a 16-word by 12-bit RAM and 16 channels of 2-line to 1-line multiplexers. Four bits of the memory address bus can be used to select one of 16 map registers that contain 12 bits each. These 12 bits are presented to the system memory address bus along with the unused memory address bit from the CPU.

There are four modes of operation (read, write, map and pass), When the chip select ($\overline{CS}$) is low, data may be read or written into the map register through data I/O (D0 ~ D7) selected by the register select inputs (RS0 ~ RS3) under the control of R/$\overline{W}$. When $\overline{CS}$ is high and Map Mode Control ($\overline{MM}$) is low, the map operation will output the contents of map register selected by the map address input (MA0 ~ MA3). When $\overline{CS}$ and $\overline{MM}$ are both high (pass mode), the address bit on MA0 ~ MA3 appears at MO8 ~ MO11, respectively, with low levels on the other map outputs (MO0 ~ MO7).

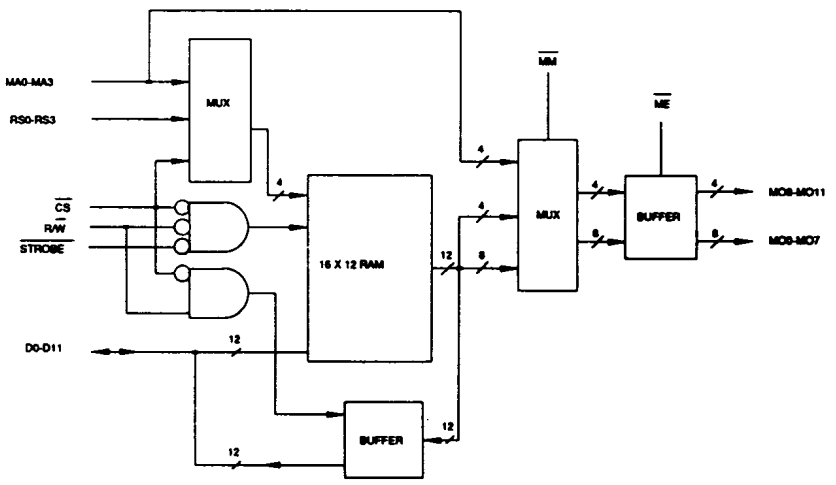
The $\overline{STROBE}$ input is used to enter data into the selected map register during I/O operations. Map Enable ($\overline{ME}$) is used to enable the map outputs. All outs are tri-state outputs with high current driving capability.

PIN CONFIGURATION



NOTE:
Pin 28 has no internal connection

FUNCTIONAL BLOCK DIAGRAM



Pin Description:

Pin #	Pin Name	Functional Description
7-12 29-34	D0 ~ D11	I/O connections to data used for reading from or writing to the map register.
1,3, 36,38	RS0 ~ RS3	Register selects inputs for I/O operations.
6	R/$\overline{W}$	Read or write control pin is used in I/O operation. When high, the data bus is used to read from the register. When low, the data bus is used to write into the register.
5	$\overline{STROBE}$	$\overline{STROBE}$ input is used to enter data into the selected map register.
4	$\overline{CS}$	Chip select input for an I/O operation when input level is low.
2,35,37,39	MA0 ~ MA3	Map address inputs to select one of 16 registers when in map mode.
14-19 22-27	MO0 ~ MO11	Map data outputs. In the map mode, these outputs provide the map register contents to the system memory address bus. When is pass mode, these outputs present the map address data on MO8 ~ MO11 and low level on MO0 ~ MO7.
13	$\overline{MM}$	Map mode input. When low, the map mode is active. When high, it is in pass mode.
21	$\overline{ME}$	Map enable for the map outputs. When low, outputs MO0 ~ MO11 are active. When high, these outputs are at high impedance.

Function Table:

$\overline{CS}$	$\overline{MM}$	R/$\overline{W}$	$\overline{STROBE}$	MODE	Operation
0	X	0	0	Write	Write from data input (D0 ~ D7) to selected register.
0	X	1	X	Read	Read from selected register to data output (D0 ~ D7).
1	0	X	X	Map	Present the register contents to map outputs (MO0 ~ MO11). (If $\overline{ME}$=0)
1	1	X	X	Pass	Provide map address data (MA0 ~ MA3) on MO8 ~ MO11 and low level on MO0 ~ MO7. (If $\overline{ME}$=1)

Absolute Maximum Ratings: [1]

- Terminal Voltage with Respect to V_{SS}: . . . -0.5V to +7V
- Operating Temperature: . . . . . 0°C to 70°C
- Storage Temperature: . . . . . -65°C to 150°C

Note [1] *Stresses greater than those listed under the ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.*

DC Electrical Characteristics (T_A=25°C, V_{CC}=5V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{IL}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	-	-	± 1	uA
I_{OL}	Output Leakage Current	0V ≤ V_O ≤ V_{CC}	-	-	± 5	uA
I_{CC}	Standby Current	V_{IN} = 0.2V OR V_{CC} -0.2V	-	-	10	uA
V_{IH}	Input High-Level Voltage	-	2.0	-	-	V
V_{IL}	Input Low-Level Voltage	-	-	-	0.8	V
V_{OHD}	Output High-Level Voltage on D0 ~ D11	I_{OH}=-20uA I_{OH}=-6.0mA	4.4 3.8	4.9 4.0	- -	V V
V_{OHM}	Output High-Level Voltage on MO0 ~MO11	I_{OH}=-20uA I_{OH}=-8.0mA	4.4 3.8	4.9 4.3	- -	V V
V_{OLD}	Output Low-Level Voltage on D0 ~ D11	I_{OL}=20uA I_{OL}=12mA	- -	0.001 0.3	0.1 0.4	V V
V_{OLM}	Output Low-Level Voltage on MO0 ~ MO11	I_{OL}=20uA I_{OL}=20mA	- -	0.001 0.4	0.1 0.5	V V

Capacitance: [2]

Symbol	Parameter	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A=25°C, f=1MHZ, V_{CC}=5V	8	pF
C_{OUT}	Output Capacitance	T_A=25°C, f=1MHZ, V_{CC}=5V	10	pF

Note [2] *This Parameter is periodically sampled and is not 100% tested.*

AC Characteristics: (V_{CC}=5V, T_A=25°C)

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{SBW}	$\overline{STROBE}$ Pulse Width	75	-	-	ns
t_{CSSU}	$\overline{CS}$ Setup Time ($\overline{CS}$ low to $\overline{STROBE}$ low)	20	-	-	ns
t_{RWSU}	R/$\overline{W}$ Setup Time (R/$\overline{W}$ low to $\overline{STROBE}$ low)	20	-	-	ns
t_{RSSU}	RS Setup Time (RS Setup Time)	20	-	-	ns
t_{DASU}	DATA Setup Time (D0 ~ D11 valid to $\overline{STROBE}$ high)	75	-	-	ns
t_{CSHD}	$\overline{CS}$ Hold Time ($\overline{STROBE}$ high to $\overline{CS}$ high)	20	-	-	ns
t_{RWHD}	R/$\overline{W}$ Hold Time ($\overline{STROBE}$ High to R/$\overline{W}$ high)	20	-	-	ns
t_{RSHD}	RS Hold Time ($\overline{STROBE}$ high to RS invalid)	20	-	-	ns
t_{DAHD}	DATA Hold Time ($\overline{STROBE}$ high to D0 ~ D11 invalid)	20	-	-	ns
t_{RSDV}	RS to D0 ~ D11	-	39	75	ns
t_{CLDV}	$\overline{CS}$ to D0 ~ D11	-	26	50	ns
t_{CHDZ}	$\overline{CS}$ to D0 ~ D11, disable	-	38	65	ns
t_{WHDV}	R/$\overline{W}$ to D0 ~ D11	-	20	35	ns
t_{WLDZ}	R/$\overline{W}$ to D0 ~ D11, disable	-	30	50	ns
t_{CHQ}	$\overline{CS}$ to MO0 ~ MO11	-	48	85	ns
t_{MLQ}	$\overline{MM}$ to MO0 ~ MO11	-	20	40	ns
t_{MHQ}	$\overline{MM}$ to MO0 ~ MO11	-	22	40	ns
t_{AVQ1}	MA to MO0 ~ MO11, $\overline{MM}$=low	-	39	70	ns
t_{AVQ2}	MA to MO8 ~ MO11, $\overline{MM}$=high	-	13	30	ns
t_{ELQ}	$\overline{ME}$ to MO0 ~ MO11	-	17	30	ns
t_{EHQZ}	$\overline{ME}$ to MO0 ~ MO11, disable	-	14	25	ns

AC Test Conditions:

Output Load: . . . . . .50 pF
Input Pulse Levels: . . . . . .0V to 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

Package Availability:

- 40 Pin Plastic Dip
- 40 Pin CERDIP

Timing Diagrams

Read and Write Mode

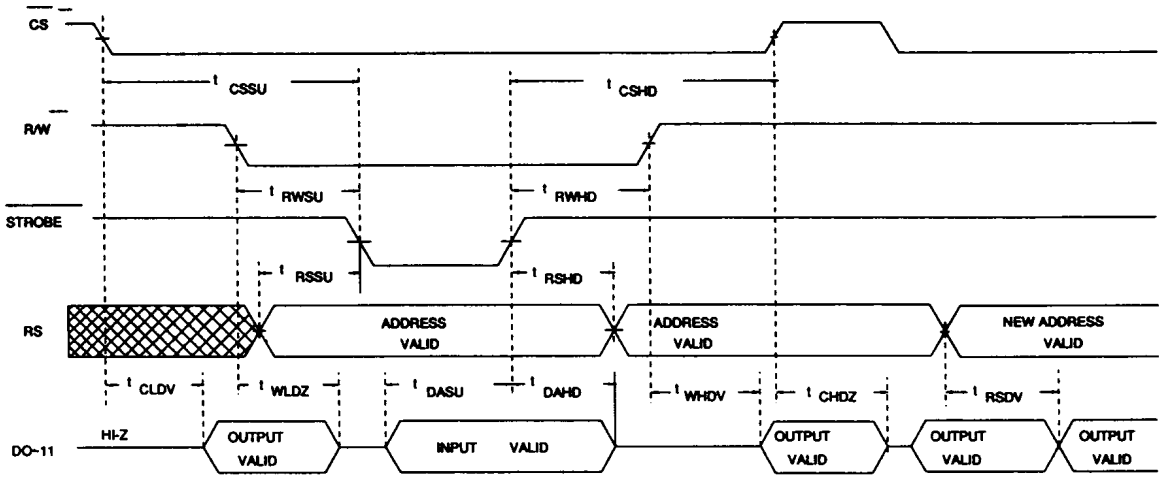


Figure 1

Map and Pass Mode

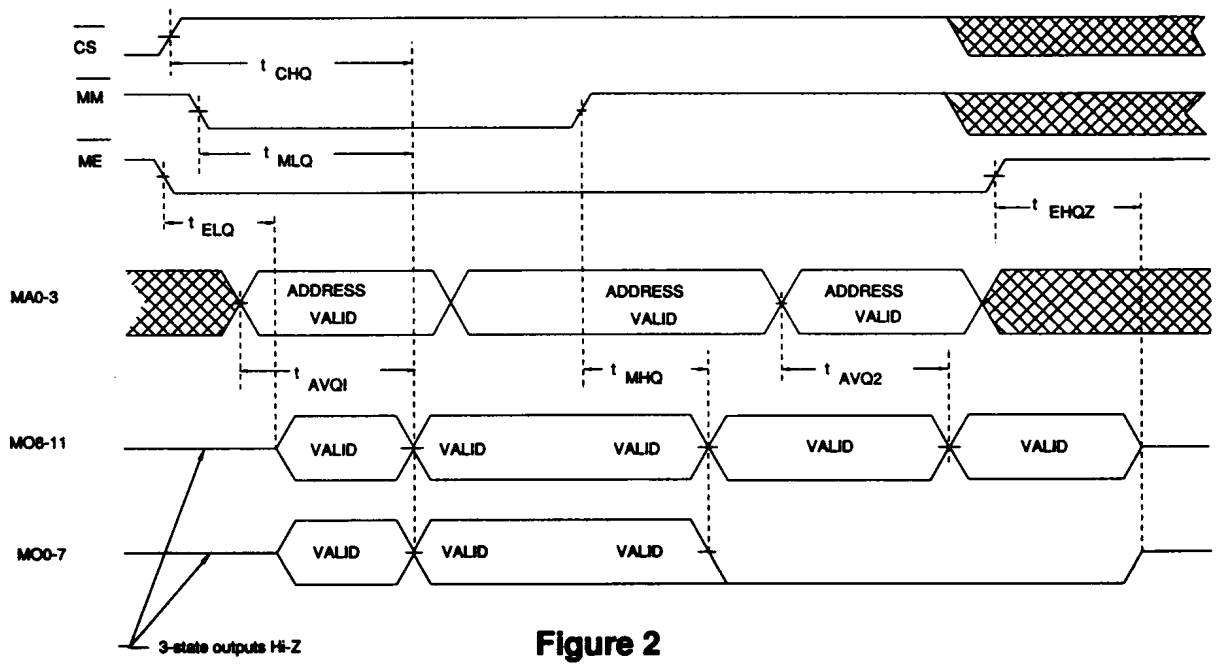


Figure 2

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