SY56016R

Low Voltage 1.2V/1.8V/2.5V CML Differential Line Driver/Receiver 6.4Gbps with Equalization

General Description

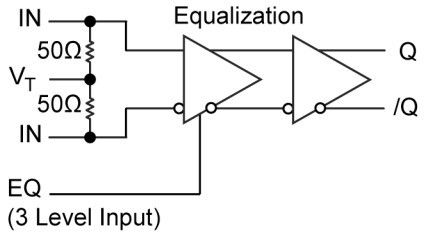
The SY56016R is a fully differential, low voltage 1.2V/1.8V/2.5V CML Line Driver/Receiver with input equalization. The SY56016R can process clock signals as fast as 5.0GHz or data patterns up to 6.4Gbps.

The differential input includes Micrel's unique, 3-pin input termination architecture that interfaces to CML differential signals, without any level-shifting or termination resistor networks in the signal path. The differential input can also accept AC-coupled CML, LVPECL, and LVDS signals. Input voltages as small as 200mV (400mV$_{PP}$) are applied before the 9", 18" or 27" FR4 transmission line. For AC-coupled input interface applications, an internal voltage reference is provided to bias the V_T pin. The outputs are CML, with extremely fast rise/fall times guaranteed to be less than 80ps.

The SY56016R operates from a 2.5V ±5% core supply and a 1.2V, 1.8V or 2.5V ±5% output supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). The SY56016R is part of Micrel's high-speed, Precision Edge® product line.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Functional Block Diagram



Precision Edge®

Features

- 1.2V/1.8V/2.5V CML Differential Line Driver/Receiver with Equalization
- Equalizes 9, 18, 27 inches of FR4
- Guaranteed AC performance over temperature and voltage:
  - DC-to >6.4Gbps Data throughput
  - DC-to >5.0GHz Clock throughput
  - <250ps propagation delay (IN-to-Q)
  - <80ps rise/fall times
- Ultra-low jitter design
  - <1ps$_{RMS}$ random jitter
- High-speed CML outputs
- 2.5V ±5% V_{CC}, 1.2V/1.8V/2.5V ±5% V_{CCO} power supply operation
- Industrial temperature range: –40°C to +85°C
- Available in 10-pin (2mm x 2mm) MLF® package

Applications

- Data Distribution:
- SONET clock and data distribution
- Fibre Channel clock and data distribution
- Gigabit Ethernet clock and data distribution

Markets

- Storage
- Test and measurement
- Enterprise networking equipment
- High-end servers
- Metro area network equipment

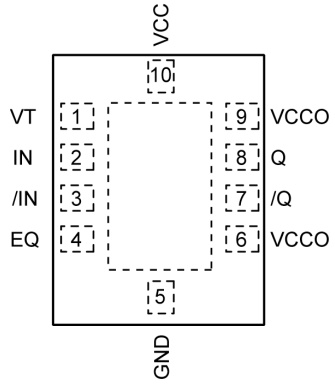
Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY56016RMG	MLF-10	Industrial	R016 with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY56016RMGTR[2]	MLF-10	Industrial	R016 with Pb-Free bar-line indicator	NiPdAu Pb-Free

Note:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.

Pin Configuration



10-Pin MLF® (MLF-10)

Truth Table

EQ	Equalization
LOW	9”
FLOAT	18”
HIGH	27”

Pin Description

Pin Number	Pin Name	Pin Function
2, 3	IN, /IN	Differential Input: Signals as small as 200mV V_{PK} (400mV_{PP}) can be applied to the input of 9, 18 or 27 inches 6 mil FR4 stripline transmission line. They are then terminated at the differential input internally with 50Ω to the VT pin.
1	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to VT pin. This pin provides a center-tap to a termination network for maximum interface flexibility. An internal high impedance resistor divider biases VT to allow input AC coupling. For AC coupling, bypass VT with 0.1µF low ESR capacitor to VCC. See “Interface Applications” subsection and Figure 2a.
4	EQ	Three level input for equalization control. High, float, low.
10	VCC	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors as close to the V_{CC} pin as possible. Supplies input and core circuitry.
6, 9	VCCO	Output Supply: Bypass with 0.1µF//0.01µF low ESR capacitors as close to the V_{CCO} pins as possible. Supplies the output buffer.
5	GND, Exposed pad	Ground: Exposed pad must be connected to a ground plane that is the same potential as the ground pin.
8, 7	Q0, /Q0	CML Differential Output Pair: Differential buffered copy of the input signal. The output swing is typically 390mV. See “Interface Applications” sub-section for termination information.

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Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +3.0V
Supply Voltage (V_{CCO}) ..... –0.5V to +3.0V
V_{CC} - V_{CCO} ..... <1.8V
V_{CCO} - V_{CC} ..... <0.5V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
CML Output Voltage (V_{OUT})..... 0.6V to V_{CCO}+0.5V
Current (V_T)
Source or sink current on VT pin ..... ±100mA
Input Current
Source or sink current on (IN, /IN) ..... ±50mA
Maximum operating Junction Temperature.....125°C
Lead Temperature (soldering, 20sec.) .....260°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... 2.375V to 2.625V
(V_{CCO}) ..... 1.14V to 2.625V
Ambient Temperature (T_A) .....–40°C to +85°C
Package Thermal Resistance [3]
MLF®
Still-air (θ_{JA}) ..... 93°C/W
Junction-to-board (ψ_{JB})..... 56°C/W

DC Electrical Characteristics[4]

T_A = –40°C to +85°C, unless otherwise stated

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage Range	V_{CC}	2.375	2.5	2.625	V
		V_{CCO}	1.14	1.2	1.26	V
		V_{CCO}	1.7	1.8	1.9	V
		V_{CCO}	2.375	2.5	2.625	V
I_{CC}	Power Supply Current	Max. V_{CC}		30	42	mA
I_{CCO}	Power Supply Current	No Load. V_{CCO} >1.7V		16	21	mA
R_{IN}	Input Resistance (IN-to-V_T, /IN-to-V_T)		45	50	55	Ω
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input HIGH Voltage (IN, /IN)		1.42		V_{CC}	V
V_{IL}	Input LOW Voltage[5] (IN, /IN)	1.22V = 1.7V-0.475V	1.22		V_{IH}–0.2	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 3a, applied to input of transmission line.	0.2		1.0	V
V_{DIFF_IN}	Differential Input Voltage Swing (|IN - /IN|)	See Figure 3b, applied to input of transmission line.	0.4		2.0	V
V_{T_IN}	Voltage from Input to V_T				1.28	V

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. 1.7V represents the V_{CC} (min) value and 0.475V represents the maximum swing on a CML output. The difference between 1.7V and 0.475V is the V_{IL} (min) needed for normal operation.

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CML Outputs DC Electrical Characteristics[6]

V_{CCO} = 1.14V to 1.26V R_L = 50Ω to V_{CCO},
V_{CCO} = 1.7V to 1.9V, 2.375V to 2.625V, R_L = 50Ω to V_{CCO} or 100Ω across the outputs,
V_{CC} = 2.375V to 2.625V. T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	R_L = 50Ω to V_{CCO}	V_{CCO} -0.020	V_{CCO} -0.010	V_{CCO}	V
V_{OUT}	Output Voltage Swing	See Figure 3a	300	390	475	mV
V_{DIFF_OUT}	Differential Output Voltage Swing	See Figure 3b	600	780	950	mV
R_{OUT}	Output Source Impedance		45	50	55	Ω

Three Level EQ Input DC Electrical Characteristics[6]

V_{CC} = 2.375V to 2.625V. T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		V_{CC}-0.3		V_{CC}	V
V_{IL}	Input LOW Voltage		0		V_{EE}+ 0.3	V
I_{IH}	Input HIGH Current	V_{IH} = V_{CC}			400	µA
I_{IL}	Input LOW Current	V_{IL} = GND	-480			µA

Notes:

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

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AC Electrical Characteristics

V_{CCO} = 1.14V to 1.26V R_L = 50Ω to V_{CCO},
V_{CCO} = 1.7V to 1.9V, 2.375V to 2.625V, R_L = 50Ω to V_{CCO} or 100Ω across the outputs,
V_{CC} = 2.375V to 2.625V. T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Frequency	NRZ Data	6.4			Gbps
		V_{OUT} > 200mV Clock	5.0			GHz
t_{PD}	Propagation Delay IN-to-Q	Note 7, Figure 1	100	150	250	ps
t_{SKEW}	Part-to-Part Skew	Note 8			100	ps
t_{JITTER}	Data Random Jitter	Note 9			1	ps_{RMS}
t_r, t_f	Output Rise/Fall Times (20% to 80%)	At full output swing.	20	50	80	ps

Notes:

7. Propagation delay is measured with no attenuating transmission line connected to the input.
8. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and input transition.
9. Random jitter is measured with a K28.7 pattern, measured at ≤ f_{MAX}.

Timing Diagram

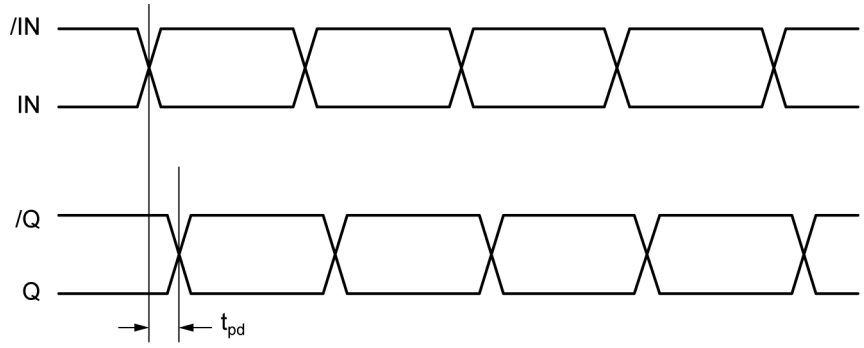

Figure 1. Propagation Delay

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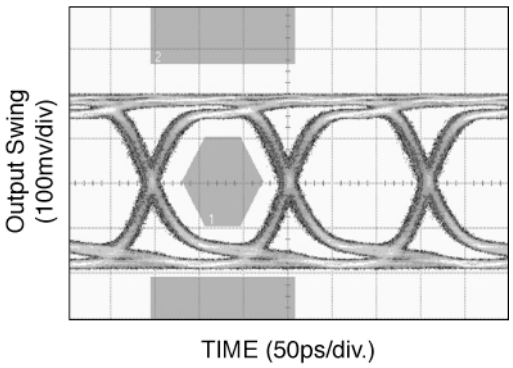
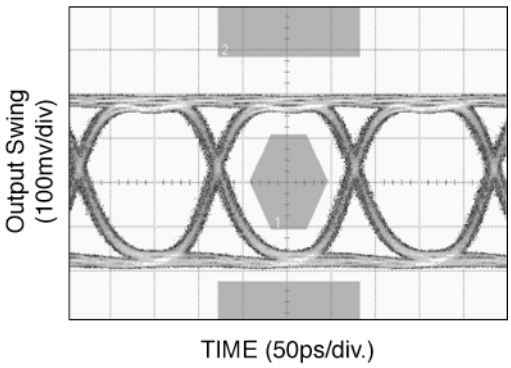
Typical Characteristics

V_{CC} = 2.5V, V_{CCO} = 1.2V, GND = 0V, V_{IN} = 400mV, R_L = 50Ω to 1.2V, Data Pattern: 2^{23}-1, T_A = 25°C, unless otherwise stated.

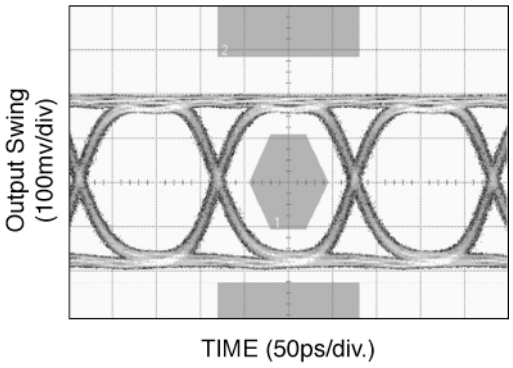
6.4Gbps, 24 inch FR4



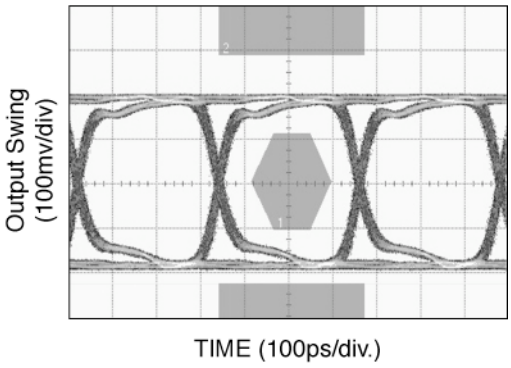
6.4Gbps, 18 inch FR4



6.4Gbps, 9 inch FR4



3.2Gbps, 24 inch FR4



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Input and Output Stage

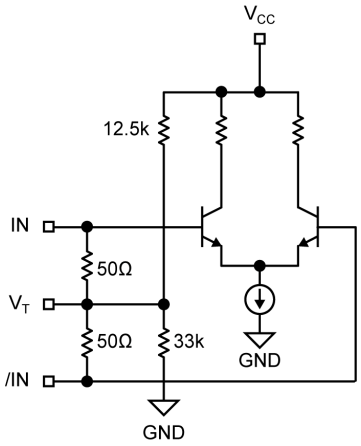

Figure 2a. Simplified Differential Input Buffer

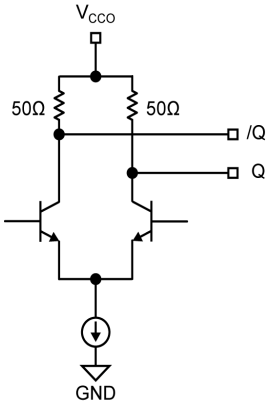

Figure 2b. Simplified CML Output Buffer

Single-Ended and Differential Swings

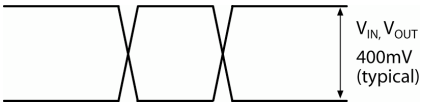

Figure 3a. Single-Ended Swing

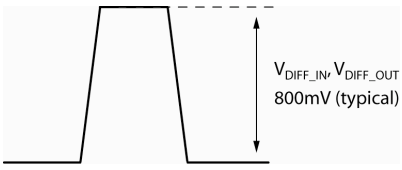

Figure 3b. Differential Swing

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Interface Applications

For Input Interface Applications see Figures 4a through 4e. For CML Output Termination, see Figures 5a through 5d.

CML Output Termination with 1.2V V_{CCO}

For VCCO of 1.2V, Figure 5a, terminate the output with 50Ω-to-1.2V, DC coupled, not 100Ω differentially across the outputs.

If AC-coupling is used, Figure 5d, terminate into 50Ω-to-1.2V before the coupling capacitor and then connect to a high value resistor to a reference voltage.

Do not AC couple with internally terminated receiver. For example, 50Ω ANY-IN input. AC-coupling will offset the output voltage by 200mV and this offset voltage will be too low for proper driver operation. Any unused output pair needs to be terminated when V_{CCO} is 1.2V, do not leave floating.

CML Output Termination with 1.8V/2.5V V_{CCO}

For V_{CCO} of 1.8V or 2.5V, Figures 5a and 5b, terminate with either 50Ω-to-V_{CCO} or 100Ω differentially across the outputs. AC- or DC-coupling is fine. See Figure 5c for AC-coupling.

Input AC-Coupling

The SY56016R input can accept AC-coupling from any driver with voltage swing between 0.2V to 1.0V (See DC Electrical Characteristics for more details). Bypass VT with a 0.1µF low ESR capacitor to VCC, as shown in Figures 4c and 4d. VT has an internal high impedance resistor divider as shown in Figure 2a, to provide a bias voltage for AC-coupling.

Input Termination

From 1.8V CML driver: Terminate with VT tied to 1.8V. Do not terminate 100Ω differentially.

From 2.5V CML driver: Terminate with either VT tied to 2.5V or 100Ω differentially.

The input cannot be DC-coupled from a 1.2V CML driver.

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Input Interface Applications

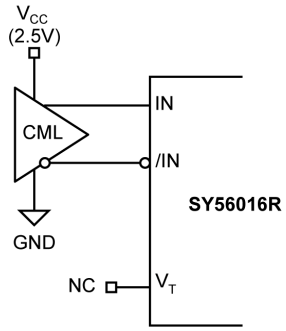


Figure 4a. CML Interface 100Ω Differential (DC-Coupled, 2.5V)

Option: May connect V_T to V_{CC}

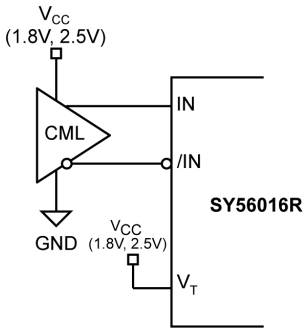


Figure 4b. CML Interface 50Ω to V_{CC} (DC-Coupled, 1.8V, 2.5V)

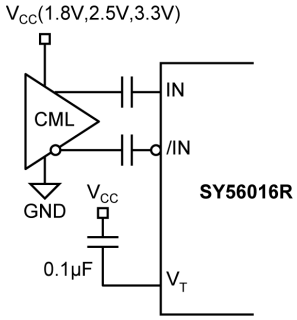


Figure 4c. CML Interface (AC-Coupled)

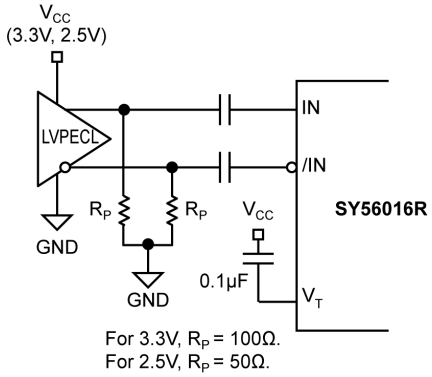


Figure 4d. LVPECL Interface (AC-Coupled)

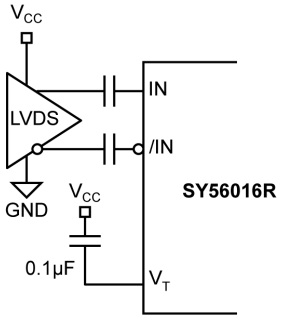


Figure 4e. LVDS Interface (AC-Coupled)

CML Output Termination

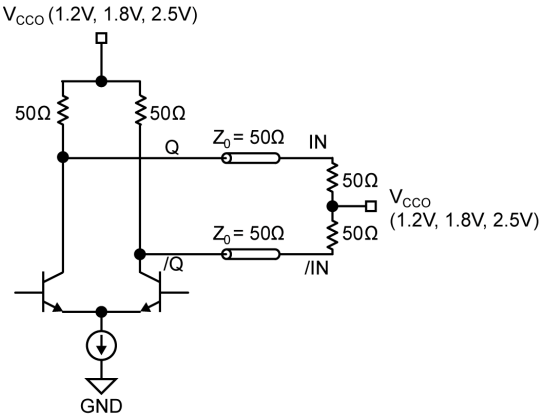


Figure 5a. 1.2V 1.8V or 2.5V CML DC-Coupled Termination

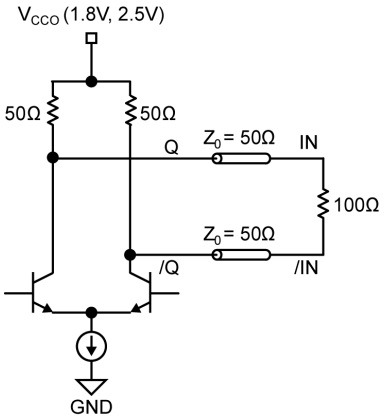


Figure 5b. 1.8V or 2.5V CML DC-Coupled Termination

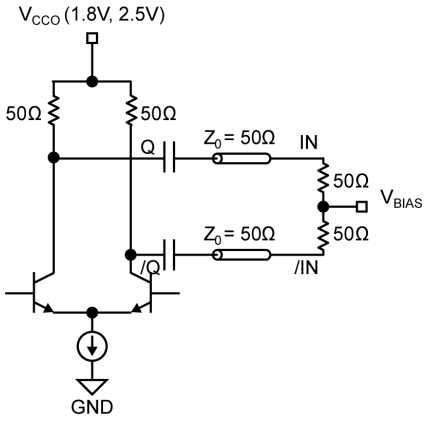


Figure 5c. CML AC-Coupled Termination (V_{CCO} 1.8V or 2.5V only)

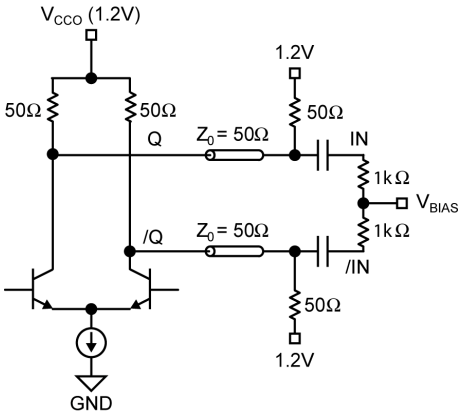
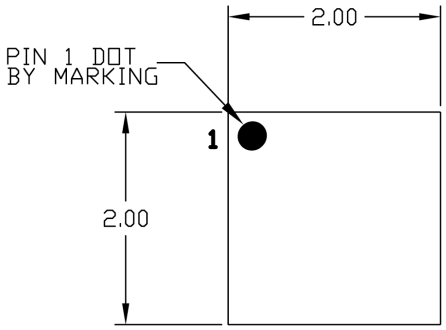


Figure 5d. CML AC-Coupled Termination V_{CCO} 1.2V Only

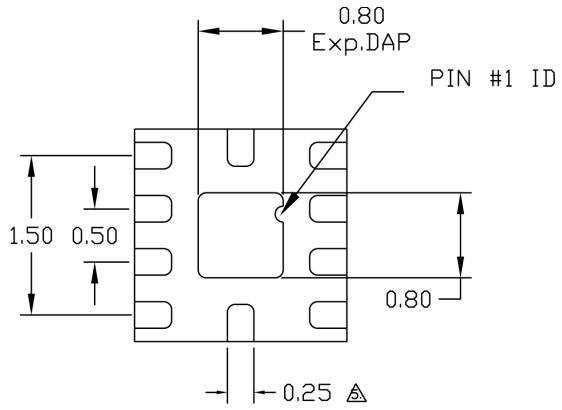
Related Product and Support Documents

Part Number	Function	Datasheet Link
HBW Solutions	New Products and Termination Application Notes	http://www.micrel.com/page.do?page=/product-info/as/HBWsolutions.shtml

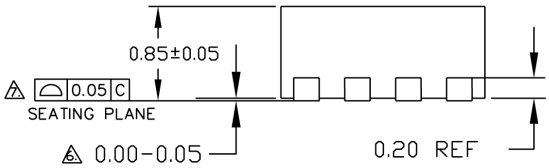
Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
7. APPLIED FOR EXPOSED PAD AND TERMINALS.

10-Pin *Micro*LeadFrame® (MLF-10)

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