

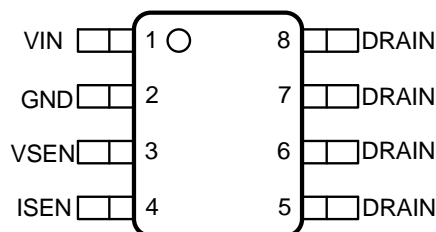


SY50133Z1 provides reliable protections including VIN Over Voltage Protection, Short Circuit Protection (SCP), Over Temperature Protection (OTP), Output voltage OVP protection (OVP), VSEN/ISEN pin short protection, VSEN pin upper divider resistor disconnect protection.

Recommended Operating Output Power		
Products	90~264Vac	176~264Vac
SY50133Z1	12W	15W

## Ordering Information

SY50133□(□□)□  
 └─ Temperature Code  
 └─ Package Code  
 └─ Optional Spec Code



Pinout (Top view)

Ordering Number	Package	Top Mark
SY50133Z1FAC	SO8	CTMxyz

x=year code, y=week code, z= lot number code

## Pinout

Pin Number	Pin Name	Pin Description
1	VIN	Power supply pin. Bypass this pin to the GND pin with a 4.7uF/50V ceramic capacitor.
2	GND	Ground pin.
3	VSEN	Output voltage sense pin. This pin receives the auxiliary winding voltage by a resistor divider. The value of the resistor divider also programs the cable impedance. This pin also senses the winding voltage to provide the QR operation.
4	ISEN	Current sense pin. The current sense resistor is placed between this pin and the GND pin.
5	DRAIN	Drain of the internal power MOSFET.
6	DRAIN	Drain of the internal power MOSFET.
7	DRAIN	Drain of the internal power MOSFET.
8	DRAIN	Drain of the internal power MOSFET.

## Absolute Maximum Ratings (Note 1)

VIN	-0.3V~26V
VSEN	-0.3V~3.6V
ISEN	-0.3V~3.6V
Supply Current I <sub>VIN</sub>	20mA
DRAIN	620V
Power Dissipation, @ T <sub>A</sub> = 25°C SO8	1.1W
Package Thermal Resistance (Note 2)	
SO8, θ <sub>JA</sub>	150°C/W
SO8, θ <sub>JC</sub>	60°C/W
Junction Temperature Range	-45°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	-65°C to 150°C

## Recommended Operating Conditions

VIN	9V~20V
ISEN	0V~1V
Junction Temperature Range	-40°C to 125°C
Ambient Temperature Range	-40°C to 105°C

## Electrical Characteristics

( $V_{VIN} = 12V$  (Note 3),  $T_A = 25^\circ C$  unless otherwise specified)

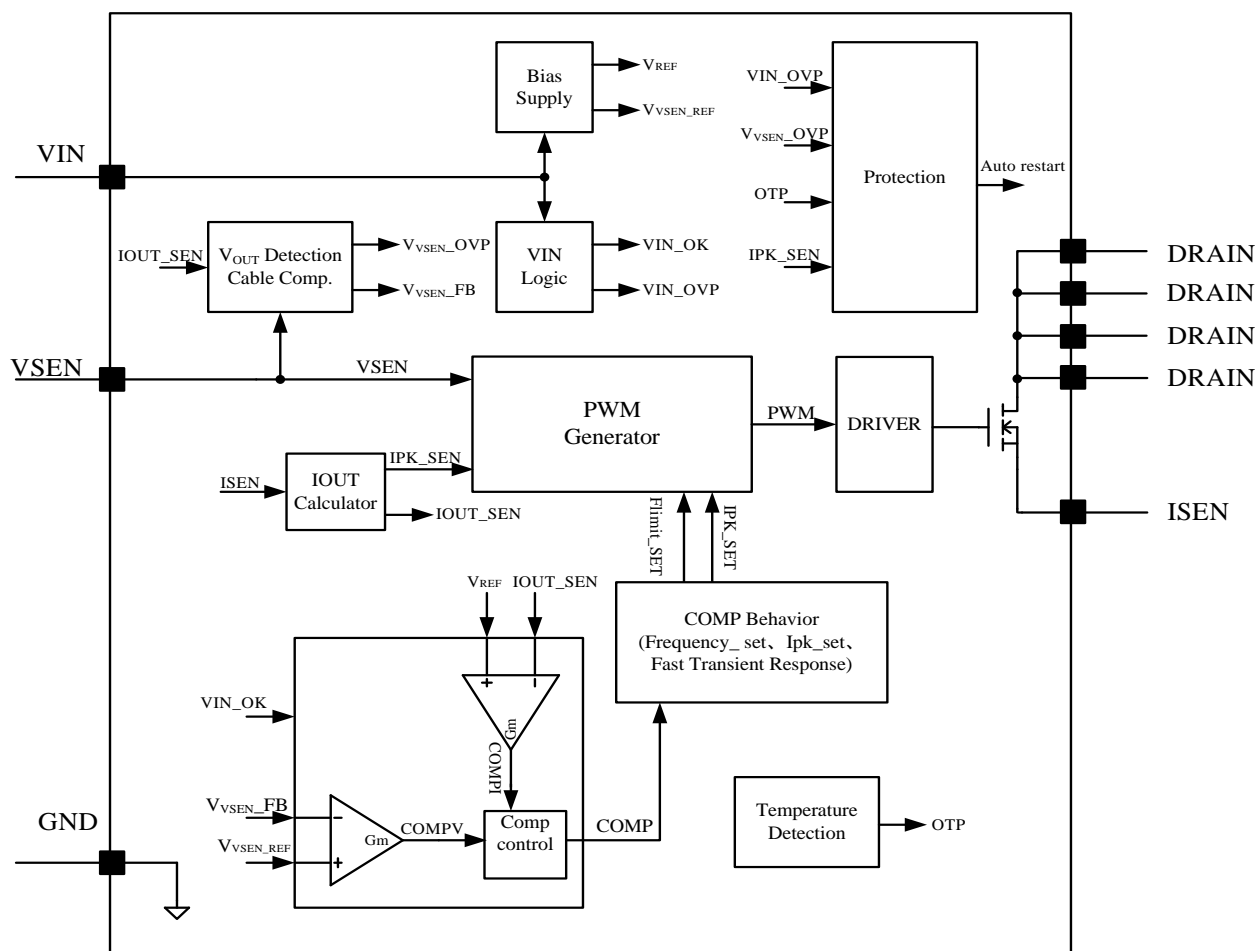
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VIN Turn-on Threshold	V <sub>VIN_ON</sub>		19.7	21.3	22.9	V
VIN Turn-off Threshold	V <sub>VIN_OFF</sub>		6.9	7.7	8.5	V
VIN OVP Voltage	V <sub>VIN_OVP</sub>			V <sub>VIN_ON</sub> +3		V
Start Up Current	I <sub>ST</sub>	V <sub>VIN</sub> <V <sub>VIN_OFF</sub>	0.5	2	5	μA
Operating Current	I <sub>VIN</sub>	f=100kHz		1.53		mA
Quiescent Current	I <sub>Q</sub>	f=500Hz		140		μA
Discharge Current in OVP Mode	I <sub>VIN_OVP</sub>	V <sub>VIN</sub> =12V		5.2		mA
Current Feedback Modulator Section						
Internal Reference Voltage	V <sub>REF</sub>		0.41	0.42	0.43	V
ISEN Pin Section						
Current Limit Voltage	V <sub>ISEN_LIM</sub>	V <sub>FBV</sub> <0.4V		0.7		V
		V <sub>FBV</sub> >0.4V	0.91	1.05	1.18	V
VSEN Pin Section						
OVP Voltage Threshold	V <sub>VSEN_OVP</sub>		1.4	1.5	1.6	V
Internal Reference Voltage	V <sub>VSEN_REF</sub>		1.232	1.25	1.268	V
Cable Compensation Coefficient	K <sub>3</sub>		16	25	31	μA/V
Integrated MOSFET Section						
Breakdown Voltage	V <sub>BV</sub>	V <sub>GS</sub> =0V,I <sub>DS</sub> =250μA	620			V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =12V,I <sub>DS</sub> =0.02A		4.4		Ω
Switching Section						
Max ON Time	T <sub>ON_MAX</sub>			24		μs
Min ON Time	T <sub>ON_MIN</sub>			360		ns
Max OFF Time	T <sub>OFF_MAX</sub>		1.58	2	2.42	ms
Min OFF Time	T <sub>OFF_MIN</sub>		1.3	1.8	2.3	μs
Minimum Switching Period	T <sub>PERIOD_MIN</sub>		6.9	8	9.1	μs
Thermal Section						
Thermal Shutdown Temperature	T <sub>SD</sub>			150		°C
Thermal Shutdown Temperature Hysteresis	T <sub>SD_HYS</sub>			20		°C

**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:**  $\theta_{JA}$  is measured in the natural convection at  $T_A = 25^\circ C$  on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on “2 x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal via to bottom layer ground plane.

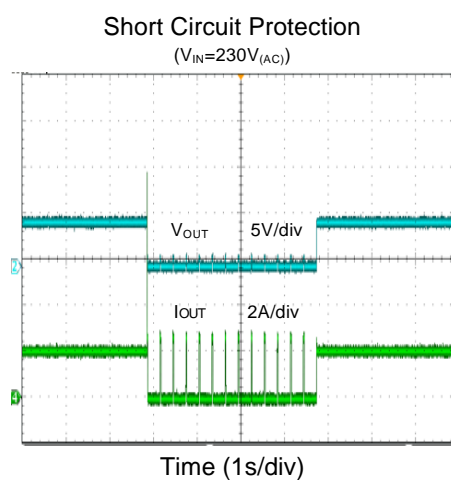
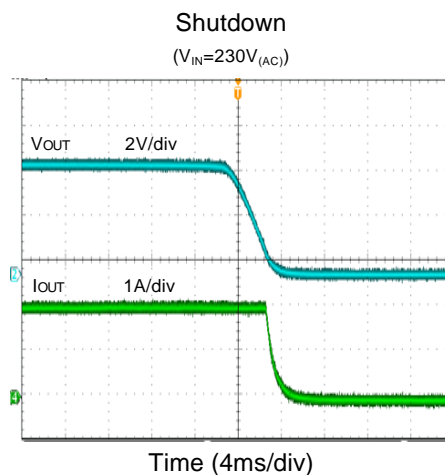
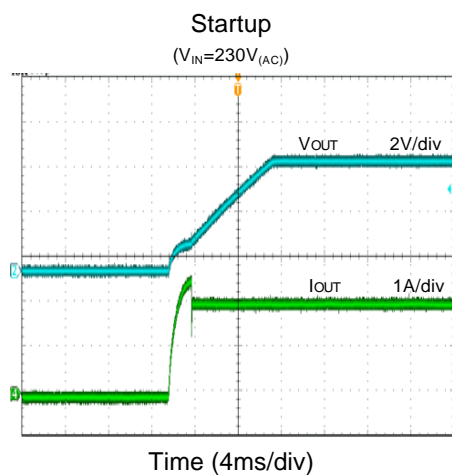
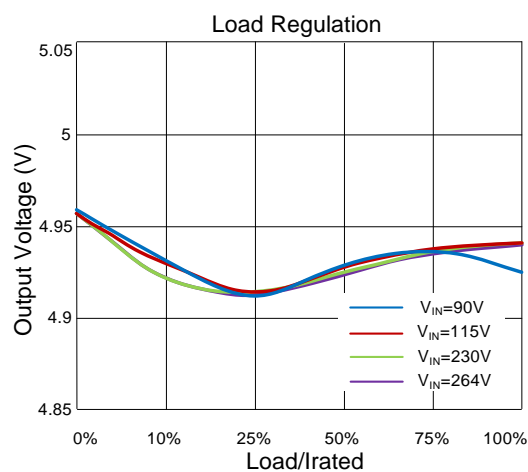
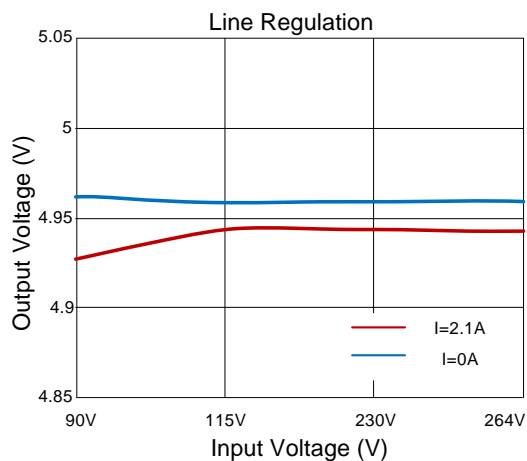
**Note 3:** Increase VIN pin voltage gradually higher than  $V_{VIN\_ON}$  voltage to start the IC first, then set VIN to 12V.

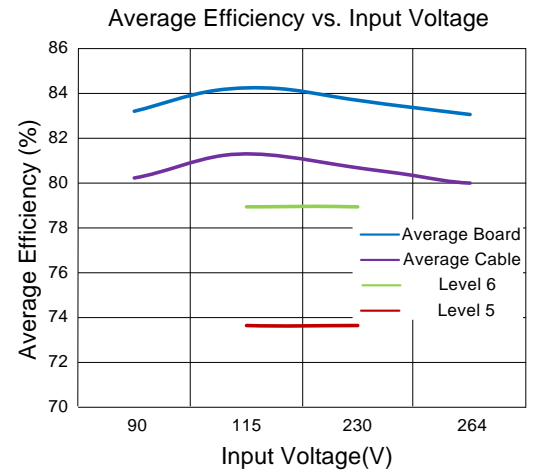
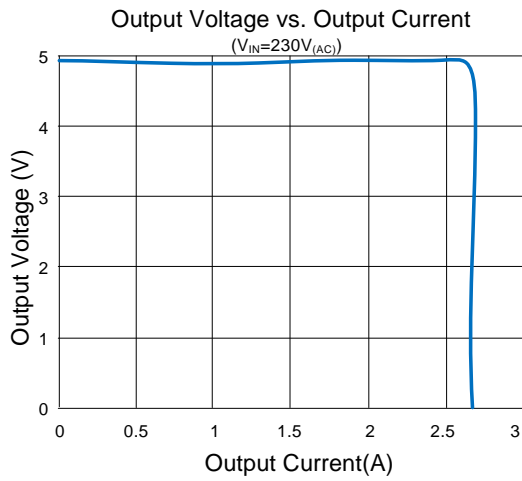
## Block Diagram



## Typical Performance Characteristics

(Test condition: input voltage: 90~264Vac; output spec: 5Vdc\_2.1A; output cable: 22AWG\_1.2m; Ambient temperature: 25±5 °C; Ambient humidity: 65±25 %.)





## Operation Principles

### Start-up Operation

After AC supply is powered on, the rectified BUS voltage ramps up. The capacitor across VIN and GND pins,  $C_{VIN}$ , is charged up by the BUS voltage through a start up resistor  $R_{ST}$ . Once  $V_{VIN}$ , the voltage on the VIN pin, rises up to  $V_{VIN\_ON}$ , the internal blocks starts the operation.  $V_{VIN}$  will subsequently be pulled down by the power consumption of the circuitry until the auxiliary winding of Flyback transformer can supply sufficient energy to maintain  $V_{VIN}$  above  $V_{VIN\_OFF}$ .

The start-up procedure is divided into two sections, as shown in Fig.1:  $t_{STC}$  is the  $C_{VIN}$  charged up section, and  $t_{STO}$  is the output voltage built-up section. The start up time  $t_{ST}$  composes of  $t_{STC}$  and  $t_{STO}$ , and usually  $t_{STO}$  is much smaller than  $t_{STC}$ .

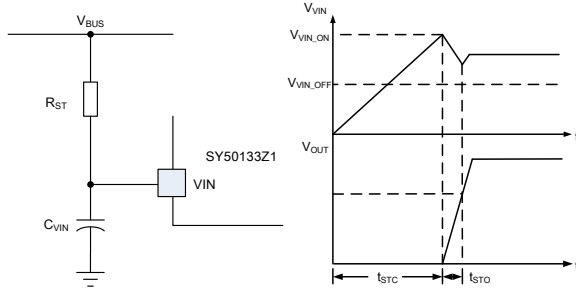


Fig.1 Start up

The start up resistor  $R_{ST}$  and  $C_{VIN}$  are designed by the following rules:

(a) Preset start-up resistor  $R_{ST}$ , make sure that the current through  $R_{ST}$  is larger than  $I_{ST}$  and smaller than  $I_{VIN\_OVP}$

$$\frac{V_{BUS\_MAX}}{I_{VIN\_OVP}} < R_{ST} < \frac{V_{BUS\_MIN}}{I_{ST}} \quad (1)$$

Where  $V_{BUS}$  is the BUS line voltage.

(b) Select  $C_{VIN}$  to obtain an ideal start-up time  $t_{ST}$ , and ensure the output voltage is built up with only one try.

$$C_{VIN} = \frac{(\frac{V_{BUS\_MIN}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}} \quad (2)$$

(c) If the  $C_{VIN}$  is not big enough to build up the output voltage with one try, increase  $C_{VIN}$  and decrease  $R_{ST}$ , go

back to step (a) and repeat the same design flow until the ideal start up procedure is obtained.

### Shut-down Operation

After AC supply is powered off, the energy stored in the BUS capacitor will be discharged. When the auxiliary winding of Flyback transformer cannot supply enough energy to the VIN pin,  $V_{VIN}$  will decrease. Once  $V_{VIN}$  is below  $V_{VIN\_OFF}$ , the IC will stop working.

### Quasi-Resonant Operation (valley detection)

The Quasi-Resonant switching mode is applied, which means to turn on the integrated MOSFET at voltage valley. QR mode operation provides the low turn-on switching losses for Flyback converter.

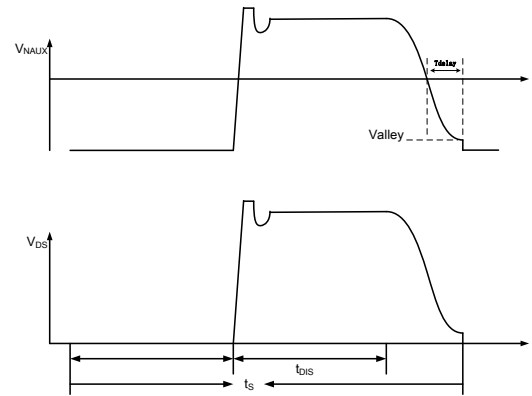


Fig.2 QR mode operation

The voltage across drain and source of the primary integrated MOSFET is reflected to the auxiliary winding of the Flyback transformer.  $V_{SEN}$  pin detects the voltage across the auxiliary winding by a resistor divider. As shown in Fig.2, when the voltage on  $V_{SEN}$  pin across zero, the MOSFET would be turned on after 400ns delay.

### Output voltage control (CV control)

In order to achieve primary side constant voltage control, the output voltage is sensed by the auxiliary winding.

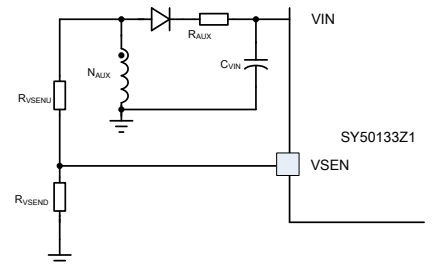


Fig.3 VSEN pin connection

As shown in Fig.4, during OFF time, the voltage across the auxiliary winding is

$$V_{AUX} = (V_{OUT} + V_{D_F}) \times \frac{N_{AUX}}{N_S} \quad (3)$$

$N_{AUX}$  is the turns of auxiliary winding;  $N_S$  is the turns of secondary winding;  $V_{D_F}$  is the forward voltage of the power diode.

At the current zero-crossing point,  $V_{D_F}$  is zero, so  $V_{OUT}$  is proportional to  $V_{AUX}$ . The voltage of this point is sampled by the IC as the feedback of output voltage. The resistor divider is designed by

$$\frac{V_{VSEN\_REF}}{V_{OUT}} = \frac{R_{VSEND}}{R_{VSENU} + R_{VSEND}} \times \frac{N_{AUX}}{N_S} \quad (4)$$

where  $R_{VSEND}$  and  $R_{VSENU}$  are the low side and high resistors at the VSEN pin, respectively, and  $V_{VSEN\_REF}$  is the internal voltage reference at 1.25V

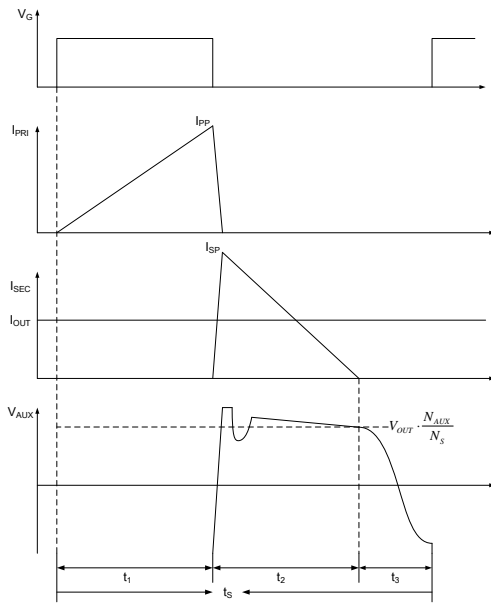


Fig.4 Auxiliary winding voltage waveforms

### Output current control (CC control)

The output current is regulated by SY50133Z1 with primary side detection technology, the maximum output current  $I_{OUT\_LIM}$  can be set by

$$I_{OUT\_LIM} = \frac{k_1 \times V_{REF} \times N_{PS}}{R_S} \quad (5)$$

Where  $k_1$  is the output current weight coefficient;  $V_{REF}$  is the internal reference voltage;  $R_S$  is the current sense resistor.

$k_1$  and  $V_{REF}$  are all internal constant parameters,  $I_{OUT\_LIM}$  can be programmed by  $N_{PS}$  and  $R_S$ .

$$R_S = \frac{k_1 \times V_{REF} \times N_{PS}}{I_{OUT\_LIM}} \quad (6)$$

$K_1$  is set to 0.5

When the over current operation or short circuit operation takes place, the output current will be limited at  $I_{OUT\_LIM}$ . The V-I curve is shown as Fig.5.

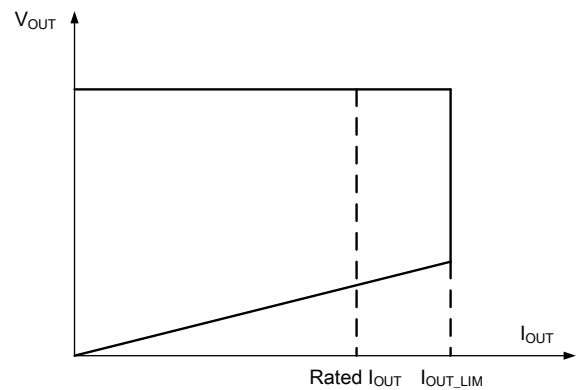


Fig.5 V-I curve

The IC provides line regulation modification function to improve line regulation performance of the output current limit.

### Cable impedance compensation

SY50133Z1 incorporates the cable impedance compensation to provide a better load regulation of output voltage at cable terminals. When the converter output load increases from no load to full load, the resulting voltage decrease on the output cables are compensated by decreasing the voltage feedback signals, which is shown by Fig. 6.

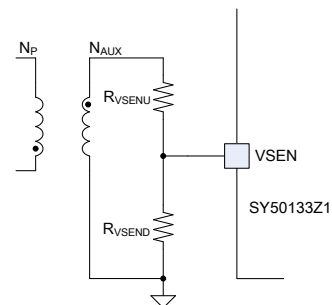


Fig. 6 Cable compensation



$$R_{VSEN} = \frac{R_{Cable}}{2k_3 \cdot R_s} \cdot \frac{N_P}{N_s} \cdot \frac{N_{AUX}}{N_s} \quad (7)$$

where  $k_3$  is set to 25uA/V,  $R_s$  is the current sense resistor connecting to the ISEN pin.

$R_{cable}$  is the resistance on the cable. The cable compensation effect can be adjusted by change the resistance of  $R_{VSEN}$  to achieve good load regulation of different output cables. The larger  $R_{VSEN}$ , the stronger cable compensation effect will be.

If the output current is below 10% the OCP point, the cable compensation is disabled.

## Fault Protection modes

### Over-temperature Protection (OTP)

SY50133Z1 includes over-temperature protection (OTP) circuitry to prevent the overheating due to the excessive power dissipation. It will shut down the switching operation when the junction temperature exceeds the OTP threshold, about 150°C. In OTP mode, if the junction temperature decreases by approximately 20°C, the IC will resume the normal operation. For a continuous normal operation, provide an adequate cooling so that the junction temperature does not exceed the OTP threshold.

### Short Circuit Protection (SCP)

When the output is shorted to ground, the output voltage is clamped to zero. The valley signal of the auxiliary winding voltage might not be detected by the VSEN pin. In this case, MOSFET cannot be turned on until maximum off time is reached. IC will shut down until  $V_{IN}$  is below  $V_{VIN\_OFF}$ , and then enter the hiccup mode.

When the output voltage is not low enough to disable the valley detection in short condition, SY50133Z1 will operate in CC mode until  $V_{IN}$  decreases below  $V_{VIN\_OFF}$ . As shown in Fig.7, a filter resistor  $R_{AUX}$  is needed to prevent the SCP function from being affected by the voltage spikes of the auxiliary winding,

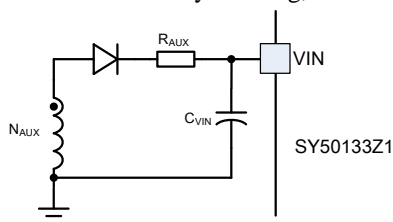


Fig. 7 Filter resistor  $R_{AUX}$

### VIN voltage OVP protection

When the  $V_{IN}$  voltage exceeds  $V_{VIN\_OVP}$  threshold, SY50133Z1 will stop switching and discharge the  $V_{IN}$

voltage. Once  $V_{VIN}$  is below  $V_{VIN\_OFF}$ , the SY50133Z1 will shut down and  $V_{IN}$  will be charged again.

### Output voltage OVP protection

When the VSEN pin signal exceeds 1.5V, reflecting an output over-voltage conditions, SY50133Z1 will stop switching and discharge the  $V_{IN}$  voltage. Once  $V_{VIN}$  is below  $V_{VIN\_OFF}$ , the IC will shut down and then enter the hiccup mode.

### VSEN pin short protection

The SY50133Z1 has a protection against the faults caused by shorting VSEN pin to GND. When the VSEN voltage does not reach the sense protection trigger level at the end of startup, the VSEN pin is deemed shorting to GND, and the protection is activated: the IC stops switching and discharge the  $V_{IN}$  voltage. Once  $V_{VIN}$  decreases below  $V_{VIN\_OFF}$ , the IC will shut down and then enter the hiccup mode. In order to ensure reliable detection, the pull-down resistor at VSEN pin should be larger than 2kΩ.

### ISEN pin short protection

The SY50133Z1 has a protection against the faults caused by shorting ISEN pin to GND. If ISEN short is detected at startup the IC stops switching and discharge the  $V_{IN}$  voltage. Once  $V_{VIN}$  decreases below  $V_{VIN\_OFF}$ , the IC will shut down and then enter the hiccup mode.

### VSEN pin upper divider resistor disconnect protection

If the upper divider resistor disconnected lasting for 8 switching cycles, the IC will stop switching and discharge the  $V_{IN}$  voltage. Meanwhile, limit the  $V_{ISEN}$  at  $V_{L\_MIN}$ . Once  $V_{VIN}$  is below  $V_{VIN\_OFF}$ , the SY50133Z1 will shut down and  $V_{IN}$  will be charged again.

## Power Supply Design Considerations

### Power Rating

A few applications are shown as below.

Products	Input range	Output		Temperature rise
SY50133Z1	90Vac~264Vac	10.5W	5V/2.1A	40°C
	90Vac~264Vac	12.5W	5V/2.5A	50°C
	90Vac~264Vac	13W	5V/2.6A	60°C
	90Vac~264Vac	12W	12V/1A	40°C

The test is conducted in a natural cooling condition at

25 °C ambient temperature.

## Transformer Design Considerations ( $N_{PS}$ and $L_M$ )

$N_{PS}$  is limited by the electrical stress of the internal power MOSFET:

$$N_{PS} \leq \frac{V_{MOS(BR)DS} \times 90\% - \sqrt{2}V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (8)$$

where  $V_{MOS(BR)DS}$  is the breakdown voltage of the integrated MOSFET.  $V_{D\_F}$  is the forward voltage of secondary power diode;  $\Delta V_S$  is the overshoot voltage clamped by RCD snubber during OFF time.

In Quasi-Resonant mode, each switching period cycle,  $t_s$ , consists of three parts: current rising time  $t_1$ , current falling time  $t_2$  and quasi-resonant time  $t_3$  shown in Fig.8.

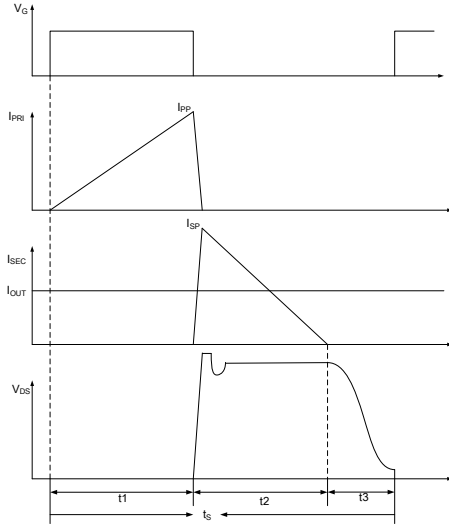


Fig.8 switching waveforms

Under the conditions of the minimum input AC RMS voltage and full load, the switching frequency is minimum while the peak current through integrated MOSFET is maximum.

Once the minimum frequency  $f_{S\_MIN}$  is set, the inductance of the transformer could be designed. The design flow is shown below:

(a) Select  $N_{PS}$

$$N_{PS} \leq \frac{V_{MOS(BR)DS} \times 90\% - \sqrt{2}V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (9)$$

(b) Preset minimum frequency  $f_{S\_MIN}$

(c) Compute inductor  $L_M$  and maximum primary peak current  $I_{P\_PK\_MAX}$

$$I_{P\_PK\_MAX} = \frac{2P_{OUT}}{\eta \times V_{DC\_MIN}} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D\_F})} + \pi \sqrt{\frac{2P_{OUT}}{\eta} \times C_{Drain} \times f_{S\_MIN}} \quad (10)$$

$$L_M = \frac{2P_{OUT}}{\eta \times I_{P\_PK\_MAX}^2 \times f_{S\_MIN}} \quad (11)$$

where  $C_{Drain}$  is the parasitic capacitance at drain of integrated MOSFET,  $\eta$  is the efficiency, and  $P_{OUT}$  is the rated full load power

(d) Compute current rising time  $t_1$  and current falling time  $t_2$

$$t_1 = \frac{L_M \times I_{P\_PK\_MAX}}{V_{BUS}} \quad (12)$$

$$t_2 = \frac{L_M \times I_{P\_PK\_MAX}}{N_{PS} \times (V_{OUT} + V_{D\_F})} \quad (13)$$

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}} \quad (14)$$

$$t_s = t_1 + t_2 + t_3 \quad (15)$$

(e) Compute primary maximum RMS current  $I_{P\_RMS\_MAX}$  for the transformer fabrication.

$$I_{P\_RMS\_MAX} = \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_1}{t_s}} \quad (16)$$

(f) Compute secondary maximum peak current  $I_{S\_PK\_MAX}$  and RMS current  $I_{S\_RMS\_MAX}$  for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (17)$$

$$I_{S\_RMS\_MAX} = \frac{\sqrt{3}}{3} N_{PS} \times I_{P\_PK\_MAX} \times \sqrt{\frac{t_2}{t_s}} \quad (18)$$

## Transformer Design Considerations

The key transformer parameters are shown below:

Necessary parameters	
Primary to Secondary Turns ratio	$N_{PS}$
Inductance	$L_M$
Primary maximum current	$I_{P\_PK\_MAX}$

Primary maximum RMS current	$I_{P\_RMS\_MAX}$
Secondary maximum RMS current	$I_{S\_RMS\_MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area  $A_e$ .

(b) Preset the maximum magnetic flux  $\Delta B$

$$\Delta B = 0.22 \sim 0.28 T$$

(c) Compute primary turn  $N_p$

$$N_p = \frac{L_M \times I_{P\_PK\_MAX}}{\Delta B \times A_e} \quad (19)$$

(d) Compute secondary turn  $N_s$

$$N_s = \frac{N_p}{N_{PS}} \quad (20)$$

(e) Compute auxiliary turn  $N_{AUX}$

$$N_{AUX} = N_s \times \frac{V_{VIN}}{V_{OUT}} \quad (21)$$

where  $V_{VIN}$  is the working voltage of VIN pin (9V~20V is recommended).

(f) Select an appropriate wire diameter

With  $I_{P\_RMS\_MAX}$  and  $I_{S\_RMS\_MAX}$ , select appropriate wire to achieve the current density from 4A/mm<sup>2</sup> to 10A/mm<sup>2</sup>.

(g) If the window area of the core and bobbin is not enough, reselect the core style, go to (a) and redesign the transformer until the ideal transformer is achieved.

## Diode Selection

Under the conditions of the maximum input voltage and full load, the voltage stress of secondary power diode is maximum;

$$V_{D\_R\_MAX} = \frac{\sqrt{2} V_{AC\_MAX}}{N_{PS}} + V_{OUT} \quad (22)$$

where  $V_{AC\_MAX}$  is maximum input AC RMS voltage,  $N_{PS}$  is the primary to secondary turns ratio of the Flyback transformer and  $V_{OUT}$  is the rated output voltage.

Under the conditions of the minimum input voltage and full load, the current stress of power diode is maximum.

$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (23)$$

$$I_{D\_AVG} = I_{OUT} \quad (24)$$

where  $I_{P\_PK\_MAX}$  is maximum primary peak current.

## Input Capacitor $C_{BUS}$ Selection

Generally, the input capacitor  $C_{BUS}$  is selected by

$$C_{BUS} = 2 \sim 3 \mu F / W,$$

or more accurately by

$$C_{BUS} = \frac{\arcsin(1 - \frac{\Delta V_{BUS}}{\sqrt{2} V_{AC\_MIN}}) + \frac{\pi}{2}}{\pi} \times \frac{P_{OUT}}{\eta} \times \frac{1}{2 f_{IN} V_{AC\_MIN}^2 [1 - (1 - \frac{\Delta V_{BUS}}{\sqrt{2} V_{AC\_MIN}})^2]} \quad (25)$$

Where  $\Delta V_{BUS}$  is the voltage ripple of BUS line.

## RCD snubber for MOSFET selection

The power loss of the snubber  $P_{RCD}$  is evaluated as:

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT} \quad (26)$$

where  $V_{OUT}$  is the output voltage,  $V_{D\_F}$  is the forward voltage of the power diode,  $\Delta V_S$  is the overshoot voltage clamped by RCD snubber,  $L_K$  is the leakage inductor,  $L_M$  is the inductance of the Flyback transformer and  $P_{OUT}$  is the output power.

The  $R_{RCD}$  is calculated as:

$$R_{RCD} = \frac{(N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S)^2}{P_{RCD}} \quad (27)$$

The  $C_{RCD}$  is calculated as:

$$C_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{R_{RCD} f_S \Delta V_{C\_RCD}} \quad (28)$$

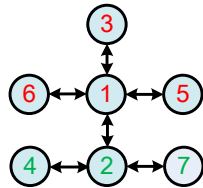
## Layout Considerations

A proper PCB design must follow the below guidelines:

(a) To achieve a good EMI performance and to reduce the line frequency voltage ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

(b) The circuit loop of all switching circuit should be kept as small as possible: primary power loop, secondary loop and auxiliary power loop.

(c) The connection of primary ground is recommended as:



Ground ①: ground of BUS line capacitor

Ground ②: ground of bias supply capacitor

Ground ③: ground node of auxiliary winding

Ground ④: ground node of divider resistor

Ground ⑤: primary ground node of Y capacitor

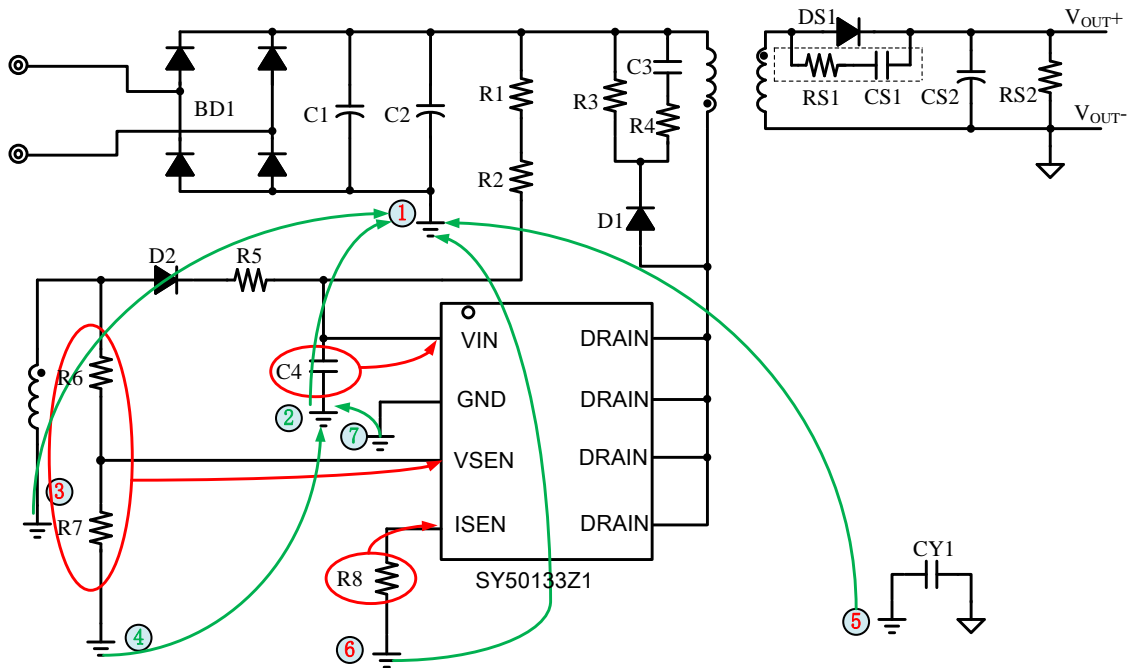
Ground ⑥: ground node of current sample resistor.

Ground ⑦: ground of IC GND.

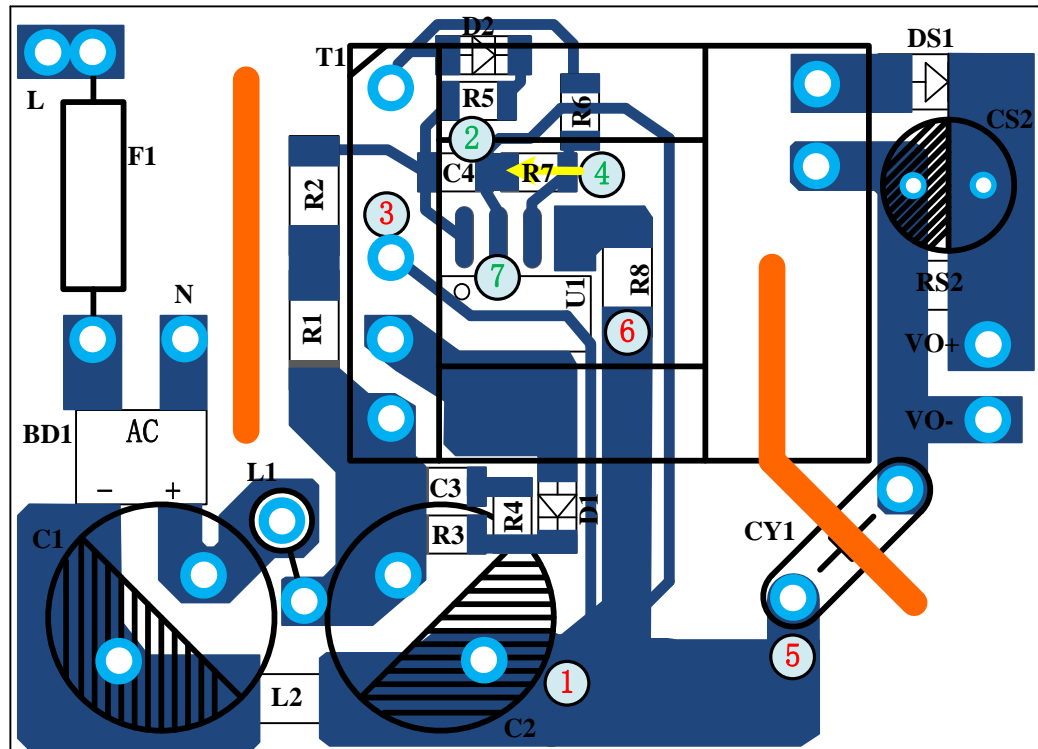
(d) Bias supply trace should be connected to the bias supply capacitor first and then to the GND pin. The bias supply capacitor should be put right beside the IC.

(e) The loop consisting of 'Source pin – current sense resistor – GND pin' should be kept as small as possible.

(f) The resistor divider connected to VSEN pin is recommended to be put close to the IC.



Note : Ground node of current sample resistor must be connected to the ground of bus line capacitor



Example layout

## Design Notes

1. At no load, the secondary side diode freewheeling time should be more than 1.8us.
2. VIN voltage should be designed to higher than 11V for all conditions.
3. RCD snubber's influence:  
At no load or light load, the off-time of main switch is very long and the snubber capacitor's voltage may be discharged to a small value. When the primary switch turns on and then turns off, the primary winding current needs a longer than normal time to charge up the snubber capacitor. This might affect the feedback voltage sensing. If Imin ( $I_{min}=0.24V/R_s$ ) is 0.1A, the snubber capacitor should be no larger than 470pF.
4. At heavy load, the peak-to-peak voltage at the Vsen pin should be less than approximately 100mVp-p after off-min time (1.8us). This can be guaranteed by decreasing the leakage inductance and using proper RCD snubber.
5.  $R_{VSEN}$  is the upper resistor of the divider. Normally, its value is recommended between 30k $\Omega$ ~91k $\Omega$ .
6. In order to ensure the CC/CV loop stability, the output capacitor should use the following formula to estimate:  
 $C_{out} = 3.7m * I_{ou} t / V_{out}$ .  
For example, in the 5V/2A output case,  $C_{out}=3.7*2/5=1.48mF$ . The output capacitor can choose from 1270uF to 1680uF. On the other hand, switching frequency ripple should also be considered. If the switching frequency ripple is too large, increase the capacitance of Cout properly or use low ESR capacitor.

## Design Example

A design example of typical application is shown below step by step. (Cable Test)

Note: All selected parameter (set value) need to adjust according to the practical condition.

### #1. Identify design specification

Design Specification			
V <sub>AC(RMS)</sub>	90V~264V	V <sub>OUT</sub>	5V
I <sub>OUT</sub>	2.1A	η	85%

### #2. Transformer design (N<sub>PS</sub>, L<sub>M</sub>, N<sub>P</sub>, N<sub>S</sub>, N<sub>AUX</sub>)

(1) Refer to **Transformer selection (N<sub>PS</sub> and L<sub>M</sub>)**

Conditions			
V <sub>AC_MIN</sub>	90V	V <sub>AC_MAX</sub>	264V
ΔV <sub>S</sub>	75V	V <sub>MOS(BR)DS</sub>	620V
P <sub>OUT (Max)</sub>	10.5W	V <sub>D_F</sub>	1V
C <sub>Drain</sub>	100pF	f <sub>S_MIN</sub>	60kHz
ΔV <sub>BUS</sub>	30% V <sub>BUS_MIN</sub>		

(a) Compute turns ratio N<sub>PS</sub> first

$$\begin{aligned}
 N_{PS} &\leq \frac{V_{MOS(BR)DS} \times 90\% - \sqrt{2} V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \\
 &= \frac{620V \times 0.9 - \sqrt{2} \times 264V - 75V}{5V + 1.0V} \\
 &= 18.275
 \end{aligned}$$

N<sub>PS</sub> is set to

$$N_{PS} = 15$$

(b) f<sub>S\_MIN</sub> is preset

$$f_{S\_MIN} = 60kHz$$

(c) Compute inductor L<sub>M</sub> and maximum primary peak current I<sub>P\_PK\_MAX</sub>

$$\begin{aligned}
 I_{P\_PK\_MAX} &= \frac{2P_{OUT}}{\eta \times (\sqrt{2} V_{AC\_MIN} - \Delta V_{BUS})} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D\_F})} + \pi \sqrt{\frac{2P_{OUT}}{\eta} \times C_{Drain} \times f_{S\_MIN}} \\
 &= \frac{2 \times 10.5W}{0.85 \times (\sqrt{2} \times 90V - 0.3 \times \sqrt{2} \times 90V)} + \frac{2 \times 10.5W}{0.85 \times 15 \times (5V + 1V)} + \pi \times \sqrt{\frac{2 \times 10.5W}{0.85} \times 100pF \times 60kHz} \\
 &= 0.59A
 \end{aligned}$$

$$L_M = \frac{2P_{OUT}}{\eta \times I_{P\_PK\_MAX}^2 \times f_{S\_MIN}}$$

$$= \frac{2 \times 10.5W}{0.85 \times (0.59A)^2 \times 60kHz}$$

$$= 1.183mH$$

Set:  $L_M = 1.1mH$ . (Note: the actual value generally less than the compute value)

(d) Compute current rising time  $t_1$  and current falling time  $t_2$

$$t_1 = \frac{L_M \times I_{P\_PK\_MAX}}{V_{BUS\_MIN}} = \frac{1.1mH \times 0.59A}{\sqrt{2} \times 90V} = 5.1\mu s$$

$$t_2 = \frac{L_M \times I_{P\_PK\_MAX}}{N_{PS} \times (V_{OUT} + V_{D\_F})} = \frac{1.10mH \times 0.59A}{15 \times (5V + 1V)} = 7.212\mu s$$

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}} = \pi \times \sqrt{1.1mH \times 100pF} = 1.042\mu s$$

$$t_s = t_1 + t_2 + t_3 = 5.1\mu s + 7.212\mu s + 1.042\mu s = 13.354\mu s$$

(e) Compute primary maximum RMS current  $I_{P\_RMS\_MAX}$  for the transformer fabrication.

$$I_{P\_RMS\_MAX} = \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_1}{t_s}} = \frac{\sqrt{3}}{3} \times 0.59A \times \sqrt{\frac{5.1\mu s}{13.354\mu s}} = 0.211A$$

(f) Compute secondary maximum peak current  $I_{S\_PK\_MAX}$  and RMS current  $I_{S\_RMS\_MAX}$  for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 15 \times 0.59A = 8.851A$$

$$I_{S\_RMS\_MAX} = N_{PS} \times \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_2}{t_s}} = 15 \times \frac{\sqrt{3}}{3} \times 0.59A \times \sqrt{\frac{7.212}{13.354}} = 3.755A$$

(2) Refer to **Transformer number of turn's selection ( $N_P$ ,  $N_S$ ,  $N_{AUX}$ )**

(a) Select the magnetic core style, identify the effective area  $A_e$ . There select EF17 for compute example. Its  $A_e$  is 24.4 mm<sup>2</sup>. The EF17 can be replaced by other reasonable magnetic core style.

(b) Preset the maximum magnetic flux  $\Delta B$ . Usually  $\Delta B = 0.22 \sim 0.28T$ .

Set:  $\Delta B = 0.25T$ .

(c) Compute primary turn  $N_P$

$$N_P = \frac{L_M \times I_{P\_PK\_MAX}}{\Delta B \times A_e} = \frac{1.1 \times 10^{-3} \times 0.59A}{0.25 \times 24.4 \times 10^{-6}} = 106$$

Set:  $N_P = 105$



(d) Compute secondary turn  $N_s$

$$N_s = \frac{N_p}{N_{PS}} = \frac{105}{15} = 7$$

Set:  $N_s=7$

(e) Compute auxiliary turn  $N_{AUX}$

$$N_{AUX} = N_s \times \frac{V_{VIN}}{V_{OUT}} = 7 \times \frac{12.5}{5} = 17.5$$

Set:  $N_{AUX}=18$

Where  $V_{VIN}$  is the working voltage of VIN pin (9V~20V is recommended).

(f) Select an appropriate wire diameter

With  $I_{P\_RMS\_MAX}$  and  $I_{S\_RMS\_MAX}$ , select appropriate wire to make sure the current density ranges from 4A/mm<sup>2</sup> to 10A/mm<sup>2</sup>.

Primary wire diameter selection: current density  $j$  is set to 5 A/mm<sup>2</sup>.

$$\text{The compute primary wire cross-sectional area } S1 = \frac{I_{P\_RMS\_MAX}}{j} = \frac{0.211}{5} = 0.042\text{mm}^2$$

$$\text{The compute primary wire diameter } D1 = 2 \times \sqrt{\frac{S1}{\pi}} = 2 \times \sqrt{\frac{0.042}{\pi}} = 0.231\text{mm}$$

Set:  $D1=0.23\text{mm}$ .

Secondary wire diameter selection: current density  $j$  is set to 10 A/mm<sup>2</sup>.

$$\text{The compute secondary wire cross-sectional area } S2 = \frac{I_{S\_RMS\_MAX}}{j} = \frac{3.755}{10} = 0.376\text{mm}^2$$

$$\text{The compute secondary wire diameter } D2\_1 = 2 \times \sqrt{\frac{S2/2}{\pi}} = 2 \times \sqrt{\frac{0.376/2}{\pi}} = 0.489\text{mm}$$

Set:  $D2=D2\_1 \times 2=0.5\text{mm} \times 2$ .

Consider transformer style, the actual primary and secondary wire diameter can be adjusted for best production.

(g) If the winding area of the core and bobbin is not enough, reselect the core style, go to (a) and redesign the transformer until the ideal transformer is achieved.

## (h) Other usually transformer inductance

	Specification	Remark
<b>Thickened EE16 (90~264Vac,5V2.1A)</b>		
Primary-Side Inductance	1.2mH ± 5%	40kHz,1V,25 ± 5 °C, Hum:65 ± 25%
Primary-Side Leakage Inductance	50μH Maximum	Short One of Secondary Winding
N <sub>P</sub>		96
N <sub>S</sub>		6
N <sub>A</sub>		15
<b>EF1510 (90~264Vac,5V2.1A)</b>		
Primary-Side Inductance	1.2mH ± 5%	40kHz,1V,25 ± 5 °C, Hum:65 ± 25%
Primary-Side Leakage Inductance	50μH Maximum	Short One of Secondary Winding
N <sub>P</sub>		64
N <sub>S</sub>		4
N <sub>A</sub>		10
<b>Thickened EE16 (90~264Vac,12V1A)</b>		
Primary-Side Inductance	1.25mH ± 5%	40kHz,1V,25 ± 5 °C, Hum:65 ± 25%
Primary-Side Leakage Inductance	50μH Maximum	Short One of Secondary Winding
N <sub>P</sub>		105
N <sub>S</sub>		15
N <sub>A</sub>		16

## #3. Select secondary power diode

Refer to **Diode selection**

Compute the voltage and the current stress of secondary power diode

$$V_{D\_R\_MAX} = \frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}} + V_{OUT} = \frac{\sqrt{2} \times 264V}{15} + 5V = 29.89V$$

$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 15 \times 0.59A = 8.851A$$

$$I_{D\_AVG} = 2.1A$$

## #4. Select the input capacitor CIN

Refer to **Input capacitor C<sub>BUS</sub>**

Known conditions at this step			
V <sub>AC_MIN</sub>	90V	ΔV <sub>BUS</sub>	30% V <sub>BUS_MIN</sub>

$$C_{BUS} = \frac{\arcsin(1 - \frac{\Delta V_{BUS}}{\sqrt{2}V_{AC\_MIN}}) + \frac{\pi}{2}}{\pi} \times \frac{P_{OUT}}{\eta} \times \frac{1}{2f_{IN} V_{AC\_MIN}^2 [1 - (1 - \frac{\Delta V_{BUS}}{\sqrt{2}V_{AC\_MIN}})^2]}$$

$$= \frac{\arcsin(1 - \frac{0.3 \times \sqrt{2} \times 90V}{\sqrt{2} \times 90V}) + \frac{\pi}{2}}{\pi} \times \frac{10.5W}{0.85} \times \frac{1}{2 \times 50 \times 90V^2 \times [1 - (1 - \frac{0.3 \times \sqrt{2} \times 90V}{\sqrt{2} \times 90V})^2]}$$

$$= 22.33\mu F$$

Set:  $C_{BUS}=20\mu F$

Where  $\Delta V_{BUS}$  is the voltage ripple of BUS line.

## #5. Set VIN pin

Refer to **Start up**

Conditions			
$V_{BUS\_MIN}$	$90V \times \sqrt{2}$	$V_{BUS\_MAX}$	$264V \times \sqrt{2}$
$I_{ST}$	$5\mu A$ (max)	$V_{VIN\_ON}$	21.3V (typical)
$I_{VIN\_OVP}$	5.2mA (typical)	$t_{ST}$	3s (designed by user)

(a)  $R_{ST}$  is preset

$$R_{ST} < \frac{V_{BUS\_MIN}}{I_{ST}} = \frac{90V \times \sqrt{2}}{5\mu A} = 25.452M\Omega,$$

$$R_{ST} > \frac{V_{BUS\_MAX}}{I_{VIN\_OVP}} = \frac{264V \times \sqrt{2}}{5.2mA} = 71.78k\Omega$$

Set  $R_{ST}$

$$R_{ST}=4M$$

(b) Design  $C_{VIN}$

$$C_{VIN} = \frac{(\frac{V_{BUS\_MIN}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}} = \frac{(\frac{90V \times \sqrt{2}}{4M\Omega} - 5\mu A) \times 3s}{21.3V} = 3.77\mu F$$

Set  $C_{VIN}$

$$C_{VIN}=4.7\mu F$$

## #6. Set current sense resistor to achieve ideal output current

Refer to **Output current control (CC control)**

Known conditions at this step			
$k_I$	0.5	$N_{PS}$	15
$V_{REF}$	0.42V	$I_{OUT\_LIM}$	2.52A

The current sense resistor is

$$R_s = \frac{k_I \times V_{REF} \times N_{PS}}{I_{OUT\_LIM}}$$

$$= \frac{0.5 \times 0.42V \times 15}{2.52A}$$

$$= 1.25\Omega$$

Set  $R_s$

$$R_s = 1.2\Omega$$

## #7. Set VSEN pin

Refer to **Output voltage control (CV control)**

First compute  $R_{VSENU}$

Conditions			
$V_{OUT}$	5V	$V_{VSEN\_REF}$	1.25V
$R_{Cable}$	0.13Ω(22AWG 1.2m)	$N_s$	7
$N_{AUX}$	18	$K_3$	25uA/V

$$R_{VSENU} = \frac{N_p}{N_s} \cdot R_{Cable} \cdot \frac{N_{AUX}}{N_s} \cdot \frac{1}{2K_3 \cdot R_s} = 83.57K\Omega$$

Set  $R_{VSENU}$

$$R_{VSENU} = 51k\Omega$$

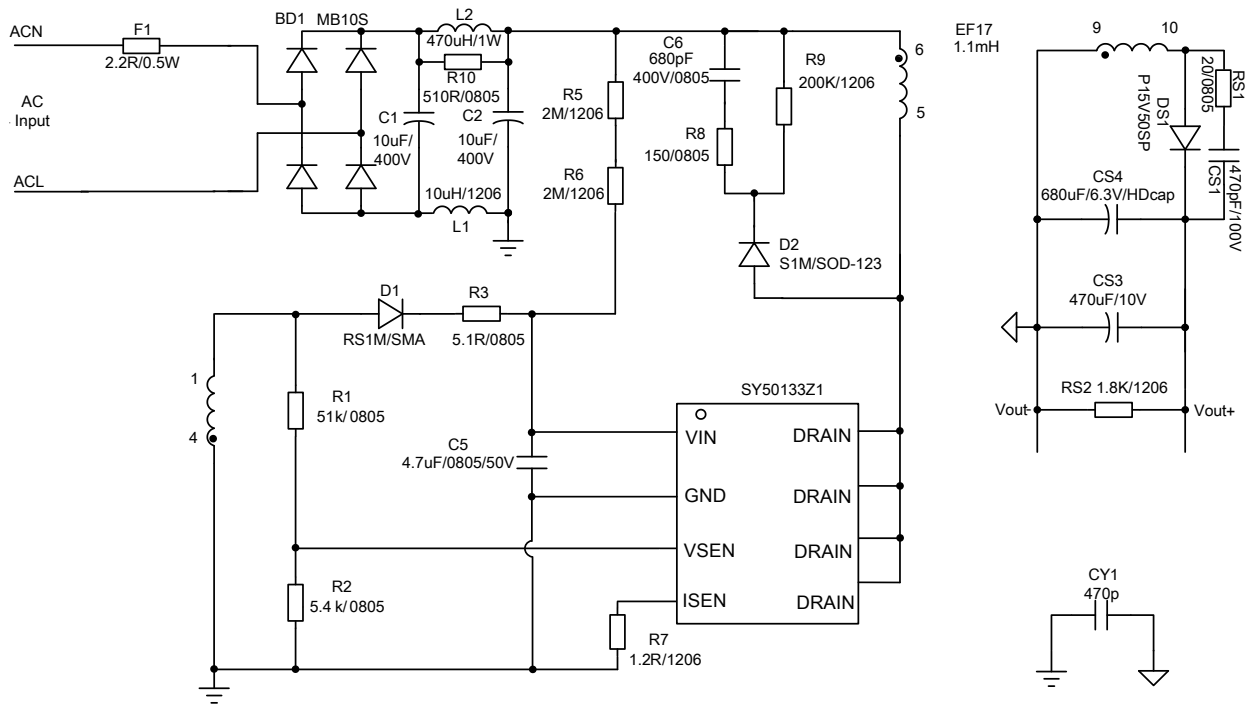
Then compute  $R_{VSEND}$

$$R_{VSEND} = \frac{R_{VSENU}}{\frac{V_{OUT} N_{AUL}}{V_{VSEN\_REF} N_s} - 1} = \frac{51K}{\left(\frac{5V \times 18}{1.25V \times 7} - 1\right)} = 5.492k\Omega$$

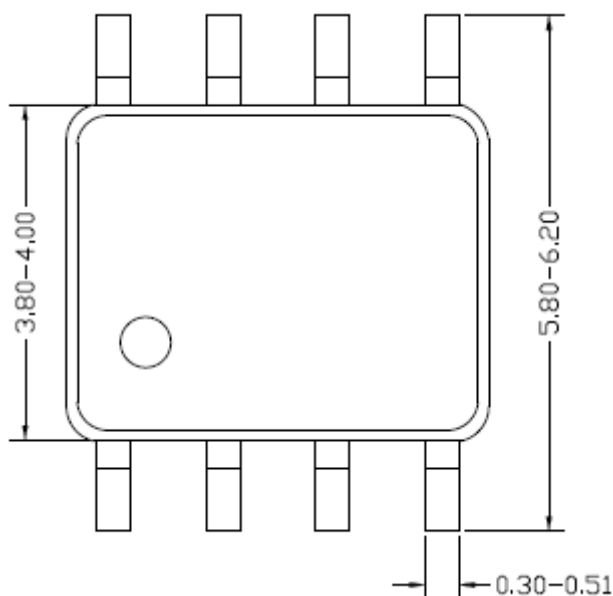
Set  $R_{VSEND}$

$$R_{VSEND} = 5.6//150k\Omega$$

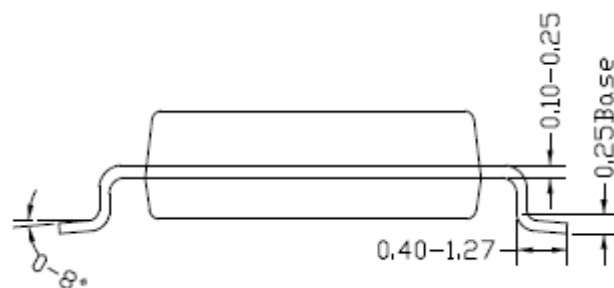
## #8. Final result



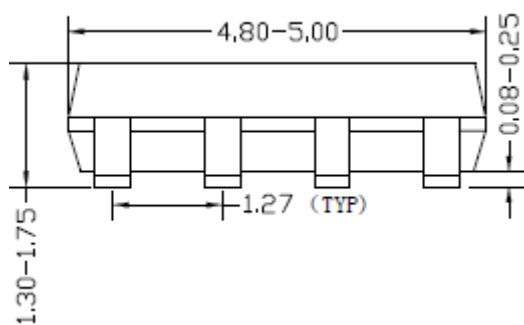
## SO8 Package outline & PCB layout design



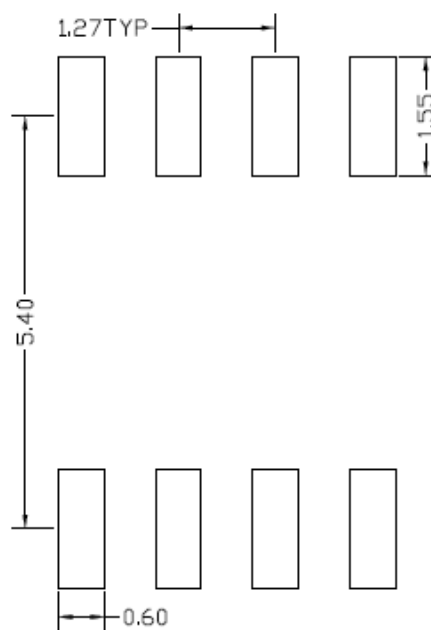
**Top view**



**Side view**



**Front view**

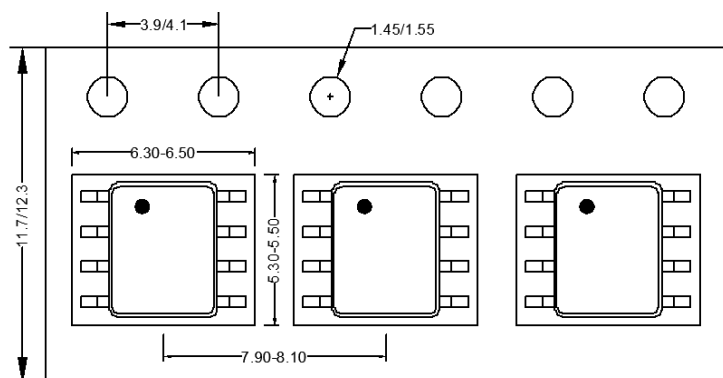


**Recommended Pad Layout  
(Reference only)**

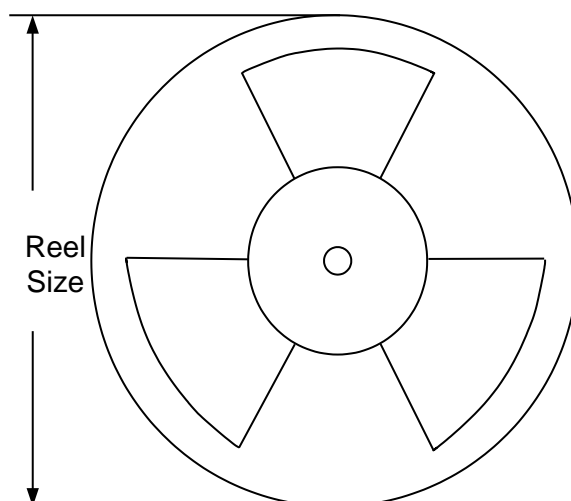
**Notes:** All dimension in millimeter and exclude mold flash & metal burr.

## Taping & Reel Specification

### 1. Taping orientation for packages (SO8)



### 2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8	12	8	13"	400	400	2500

## **Revision History**

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

<b>Date</b>	<b>Revision</b>	<b>Change</b>
May 5, 2019	Revision 0.9	Initial Release



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