SY26024

21µA Ultra-Low I_Q, 2.2MHz Synchronous Step-Down Regulator

General Description

The SY26024 is a high-efficiency 2.2MHz synchronous step-down DC/DC regulator capable of delivering up to 4A output current. It operates over an input voltage range of 2.5V to 5.5V, and integrates very low $R_{DS\ (ON)}$ main and synchronous switches to minimize conduction loss.

The SY26024 is available in a space-saving, low-profile DFN1.5mm×1.5mm-6 package.

Applications

- Portable Electronics
- Industrial PC
- Smart Phone

Features

- 2.5V to 5.5V Input Voltage Range
- Fast Load-Transient Response
- Low $R_{DS(ON)}$ for Internal Switches: 38mΩ Top, 30mΩ Bottom
- 2.2MHz Switching Frequency
- ±1% Output Voltage Accuracy (Full Temperature Range)
- PFM Mode for Light-Load Efficiency
- 21µA Operating Quiescent Current
- Internal Soft-Start Limits Inrush Current
- 100% Duty Cycle Enables Dropout Operation
- Output Auto-Discharge Function
- Power-Good Indicator
- Autorecovery for Short-Circuit, Overvoltage, and Overtemperature Protection
- RoHS-Compliant and Halogen-Free
- Compact Package: DFN1.5mm×1.5mm-6

Typical Applications

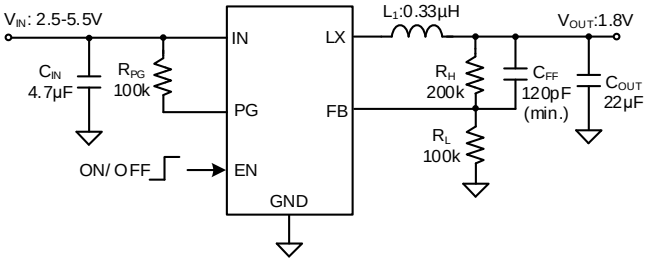


Figure 1. Schematic Diagram

Table 1. Inductor and C_{OUT} Selection

V_{OUT} (V)	L(µH)	C_{OUT} (µF)		
		10	22	44
1.2	0.33		*	✓
	0.47		✓	✓
1.8	0.33		*	✓
	0.47		✓	✓
2.5	0.47		*	✓
	0.68		✓	✓

Note: '*' indicates recommended for most applications.

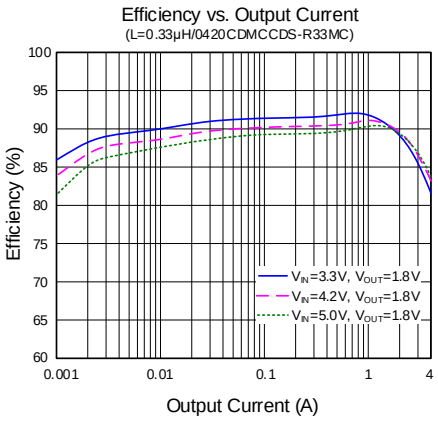


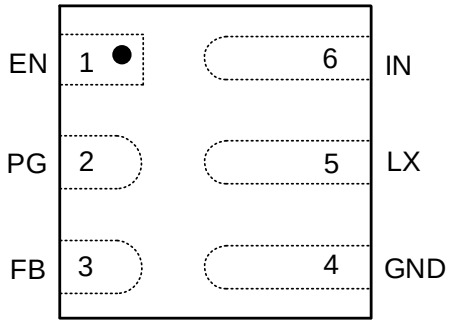
Figure 2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package type	Top Mark
SY26024DQD	DFN1.5×1.5-6 RoHS-Compliant and Halogen-Free	**f9*xyz***

***x* = year code, *y* = week code, *z* = lot number code**

Pinout (top view)



Pin Description

Pin Name	Pin Number	Pin Description
EN	1	Enable control. Pull high to turn on. Do not leave floating.
PG	2	Power-good indicator. Power good indicator (open drain output). Low if the V_{FB} < 92% or the V_{FB} > 109% of V_{REF}, high otherwise. Connect a pullup resistor to the desired voltage level.
FB	3	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: V_{OUT} = 0.6 × (1 + R_H/R_L).
GND	4	Power return path ground pin.
LX	5	Inductor pin. Connect this pin to the switching node of the inductor.
IN	6	Input pin. Decouple this pin to the GND pin with at least a 4.7µF ceramic capacitor.

Block Diagram

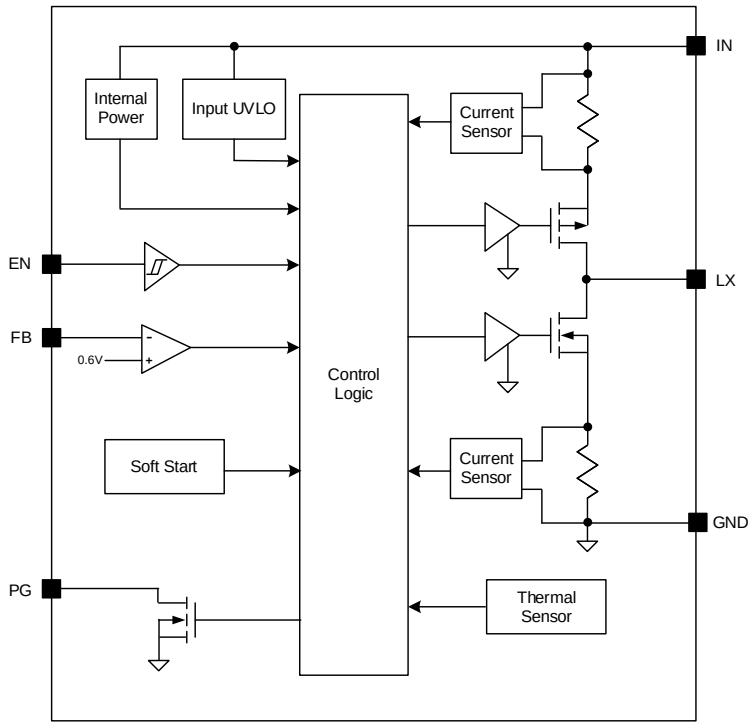


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	6	V
FB, EN, PG	-0.3	V_{IN} + 0.6	
LX (tested down to -3V <20ns and up to +7V <20ns)	-0.3	6	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	62	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	8	
P_D Power Dissipation T_A = 25°C	1.6	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Supply Input Voltage	2.5	5.5	V
Junction Temperature	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(T_J = -40°C–125°C, and V_{IN} = 2.5V to 5.5V. Typical values are at T_J = 25°C and V_{IN} = 5V, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.5		5.5	V
Input UVLO Threshold	V_{UVLO}	V_{IN} falling	2.1	2.2	2.3	V
Input UVLO Hysteresis	V_{HYS}			160		mV
Quiescent Current	I_Q	V_{FB} = 105% × V_{REF}		21		μA
Shutdown Current	I_{SHDN}	V_{EN} = 0V, T_A = 25℃		0.05	0.5	μA
Feedback Reference Voltage	V_{REF}	I_{OUT} = 1A, CCM	0.594	0.6	0.606	V
Output Voltage Load Regulation (Note 4)	ΔV_{LDR}	I_{OUT} = 0.5A to 4A, V_{OUT} = 1.8V		0.1		%/A
Output Discharge FET R_{ON}	R_{DIS}	V_{EN} = 0V		8		Ω
Top FET R_{ON}	$R_{DS(ON)1}$			38		mΩ
Bottom FET R_{ON}	$R_{DS(ON)2}$			30		mΩ
EN Input Voltage High	$V_{EN, H}$		1.0			V
EN Input Voltage Low	$V_{EN, L}$				0.4	V
EN Leakage Current	$I_{EN, LKG}$	EN = high		0.01		μA
Power-Good Threshold	V_{PG}	V_{FB} falling, PG from high to low		92		%
		V_{FB} rising, PG from low to high		95.5		%
		V_{FB} rising, PG from high to low		109		%
		V_{FB} falling, PG from low to high		105		%
Power-Good Delay	$t_{PG,R}$	PG from low to high		100		μs
	$t_{PG,F}$	PG from high to low		20		μs
Power-Good Output Low	$V_{PG, L}$	I_{PG} = 1mA			0.4	V
Power-Good Leakage Current	$I_{PG, LKG}$	V_{PG} = 5V		0.01		μA
Min ON Time (Note 4)	$t_{ON,MIN}$			50		ns
Maximum Duty Cycle (Note 4)	D_{MAX}		100			%
Soft-Start Time	t_{SS}	From EN high to 95% of V_{OUT} nominal, T_A = 25°C		1.75		ms
Switching Frequency	f_{SW}	I_{OUT} = 1A, V_{OUT} = 1.8V		2.2		MHz
Top FET Current Limit	$I_{LMT, TOP}$		5			A
Bottom FET Current Limit	$I_{LMT, BOT}$		4			A
Thermal Shutdown Temperature (Note 4)	T_{SD}			150		°C
Thermal Shutdown Hysteresis (Note 4)	T_{HYS}			20		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Package thermal resistance is measured in the natural convection at TA = 25°C on a 6cm×6cm size 2-oz two-layer Silergy Evaluation Board.

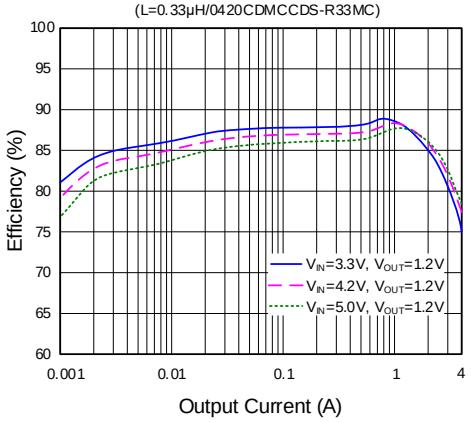
Note 3: The device is not guaranteed to function outside its operating condition.

Note 4: Guaranteed by design.

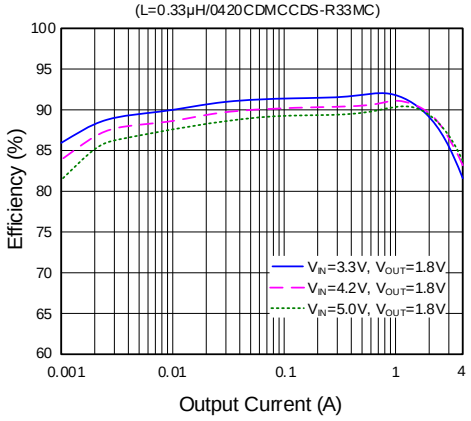
Typical Performance Characteristics

(T_A = 25°C, V_{IN} = 5V, L = 0.33μH, C_{OUT} = 2×10μF, unless otherwise specified.)

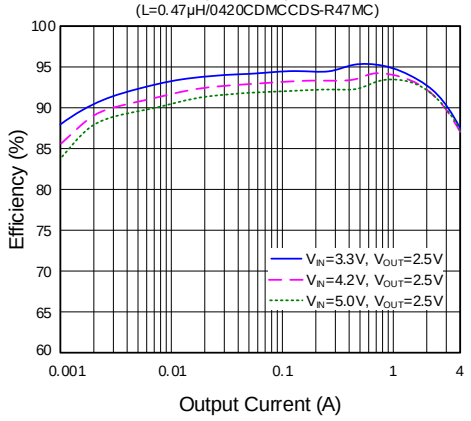
Efficiency vs. Output Current
(L=0.33μH/0420CDMCCDS-R33MC)



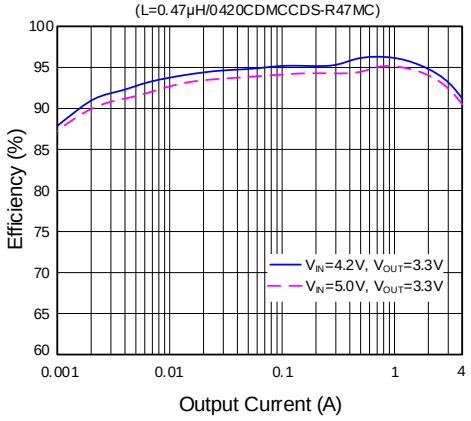
Efficiency vs. Output Current
(L=0.33μH/0420CDMCCDS-R33MC)



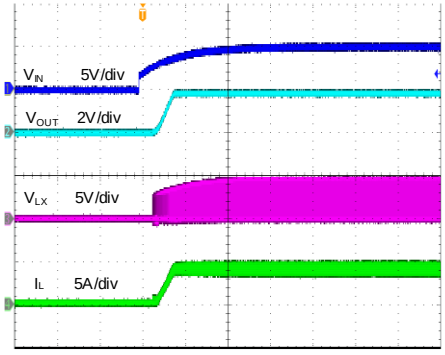
Efficiency vs. Output Current
(L=0.47μH/0420CDMCCDS-R47MC)



Efficiency vs. Output Current
(L=0.47μH/0420CDMCCDS-R47MC)

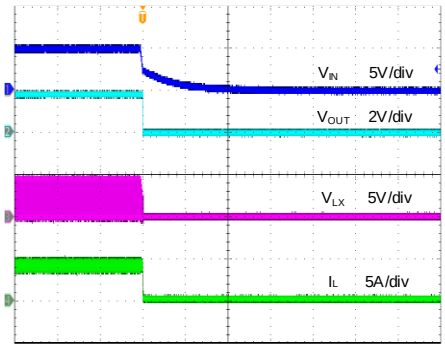


Startup from V_{IN}
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=4A)



Time (4ms/div)

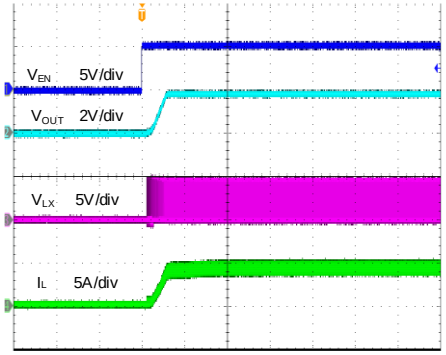
Shutdown from V_{IN}
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=4A)



Time (4ms/div)

Startup from EN

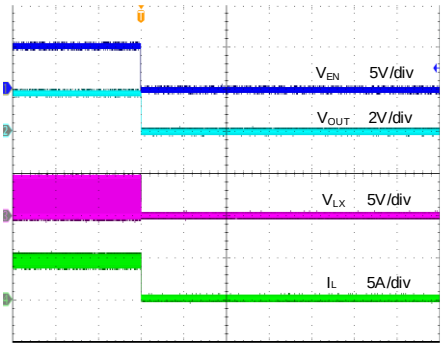
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=4A)



Time (4ms/div)

Shutdown from EN

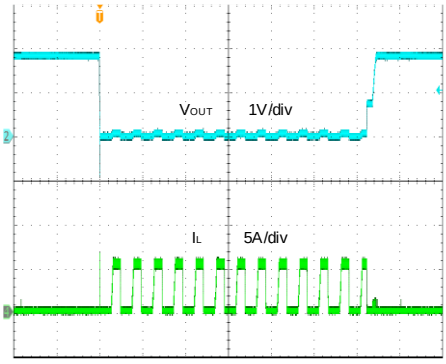
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=4A)



Time (4ms/div)

Short Circuit Protection

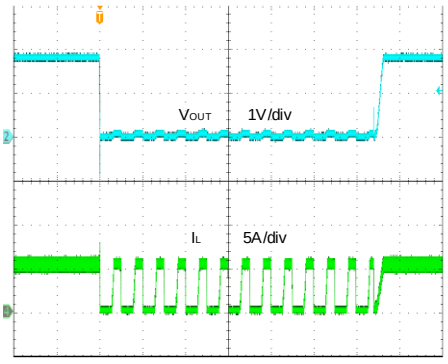
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0A~short)



Time (10ms/div)

Short Circuit Protection

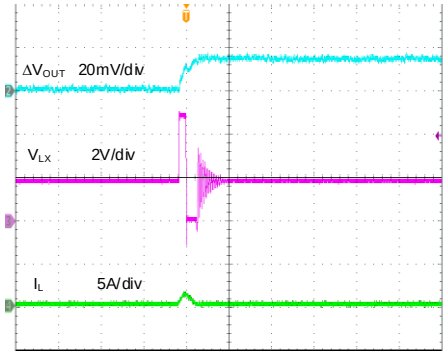
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=4A~short)



Time (10ms/div)

Output Ripple

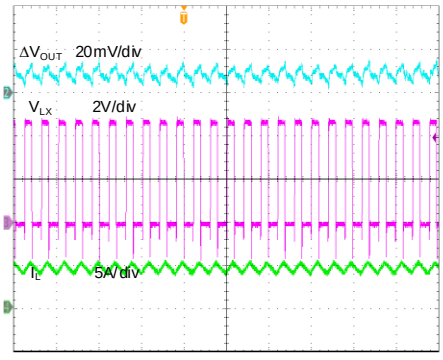
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0A)



Time (1μs/div)

Output Ripple

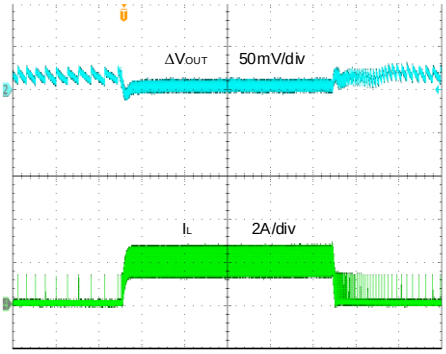
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=4A)



Time (1μs/div)

Load Transient

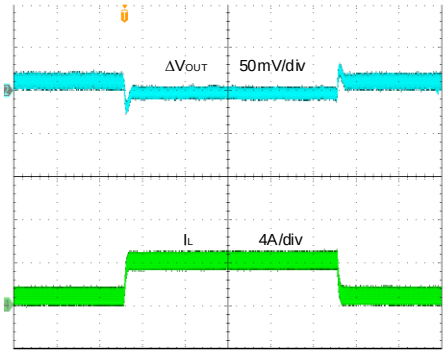
(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0~2A)



Time (100μs/div)

Load Transient

(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0.4~4A)



Time (100μs/div)

Operation

The SY26024 is a high-efficiency 2.2MHz synchronous step-down DC/DC regulator capable of delivering up to 4A output current. It operates over an input voltage range of 2.5V to 5.5V, and integrates very low $R_{DS\ (ON)}$ main and synchronous switches to minimize conduction loss.

The SY26024 uses instant-PWM architecture to achieve fast transient responses for step-down applications and high efficiency at light loads.

The SY26024 provides cycle-by-cycle current limiting and thermal shutdown protections.

The 2.2MHz switching frequency allows low-output voltage ripple and small external inductor and capacitor sizes.

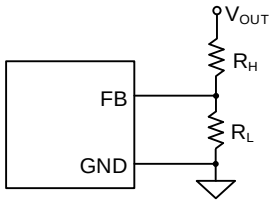
Application Information

The following sections describe the selection process for the input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L, and feedback resistors (R_H and R_L) for meeting the targeted application specifications.

Feedback Resistor Dividers R_H and R_L

Choose R_H and R_L to program the proper output voltage. To minimize power consumption under light loads, choose large resistance values between 10kΩ and 1MΩ for both R_H and R_L. For V_{OUT} = 1.8V and R_H = 100kΩ, the calculated R_L value is 49.9kΩ, as shown in the following equation:

$$R_L = \frac{0.6V}{V_{OUT}-0.6V} R_H$$



Input Capacitor C_{IN}

The ripple current through the input capacitor can be estimated using the following formula：

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1-D)}$$

For normal operation, a typical X5R or better grade ceramic capacitor with 6.3V rating should be placed close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN} and the IN/GND pins. A 4.7μF low-ESR ceramic capacitor is recommended for most applications.

Output Capacitor C_{OUT}

Select the output capacitor to handle the output ripple requirements, considering both steady-state ripple and transient requirements. For the best performance, it is recommended to use X5R or better grade ceramic capacitors with 6.3V rating and more than 2×10μF capacitance.

Output Inductor L

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The inductance is calculated as follows:

$$L = \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 40\%}$$

where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY26024 is tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,\ MIN} > I_{OUT,\ MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Choose an inductor with DCR less than 25mΩ to achieve good overall efficiency.

Inductor vs. Output Capacitor

The ripple base control strategy needs very little C_{OUT} for stable operation. An inductor that is too large and C_{OUT} capacitance can lead to unstable operation. The

recommended inductance and output capacitance are shown in the table below.

Table 2. Inductance vs. Output Capacitance Selection Table (Note 5)

L (µH)	C_{OUT} (µF)					
	22	44	88	120	180	220
0.33	**Note 6**	✓	✓	✓	✓	✓
0.47	✓	✓	✓	✓	✓	✓
0.68	✓	✓	✓	✓	×	×

Note 5: Tested with 120pF feed-forward capacitor.

Note 6: Only suitable for V_{OUT} < 2.0V application.

Minimum Duty Cycle and Maximum Duty Cycle

In the COT architecture, there is no limitation for low duty cycles, since even at very low duty cycles, the switching frequency can be reduced as needed as long as the on-time is close to the minimum, to ensure proper operation.

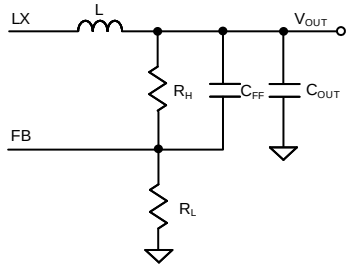
The device will enter 100% dropout mode if the output voltage is very close to the input voltage, In this mode of operation the top FET is constantly turned on, and the bottom FET is turned off.

Power-Good Indicator

The power-good indicator is an open-drain output controlled by a window comparator connected to the feedback signal. If V_{FB} is greater than $V_{PG, R}$ and less than V_{OVP} for at least the power-good delay time (low to high), PG will be high-impedance. Otherwise, it is pulled low. PG should be connected to V_{IN} or another voltage source through a resistor (e.g., 10kΩ–100kΩ).

Load-Transient Considerations

The SY26024 integrates the compensation components to achieve good stability and fast transient responses. Adding a small feed-forward ceramic capacitor with more than 120pF capacitance in parallel with R_H helps improve the load-transient response and is therefore highly recommended.



Overcurrent and Undervoltage Protection

The SY26024 uses cycle-by-cycle current limiting for both the high-side and low-side MOSFETs. If the high-side power FET current exceeds the peak current-limit threshold, the high-side power FET will turn off and the low-side power FET will turn on. If the low-side FET current exceeds the valley current-limit threshold, the low-side FET will stay on until the current decreases below the valley current-limit threshold. If the load current continues to increase in these conditions, the output voltage will drop. When the output voltage falls below 33% of the regulation level, the undervoltage protection (UVP) will be triggered, and the IC will start operating in hiccup mode. The hiccup on-time and hiccup off time ratio is 1:1. If the hard short is removed, the IC will return to normal operation.

Layout Design

To achieve optimal design, follow these PCB layout considerations:

- For maximum efficiency and stable operation, the following components should be placed close to the device: C_{IN}, L, R_H, R_L, and C_{FF}.
- Maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance. Using a ground plane is highly recommended. Place an adequate number of vias on the GND copper to improve heat distribution.
- Place C_{IN} close to IN and GND pins. Minimize the loop area formed by C_{IN} and GND.
- Minimize the PCB copper area associated with the LX pin.
- The components R_H and R_L, and the trace connecting to the FB pin must not be adjacent to the LX net on the PCB layout to avoid noise coupling.
- The feedback sampling point should be connected at the C_{OUT} terminal rather than the inductor output terminal.
- If the system chip interfacing with the EN pin has a high impedance state during shutdown mode, and the IN pin is connected directly to a power source such as a Li-ion battery, add a 1MΩ pulldown resistor between the EN and GND pins to prevent noise from falsely turning on while the regulator is in shutdown mode.

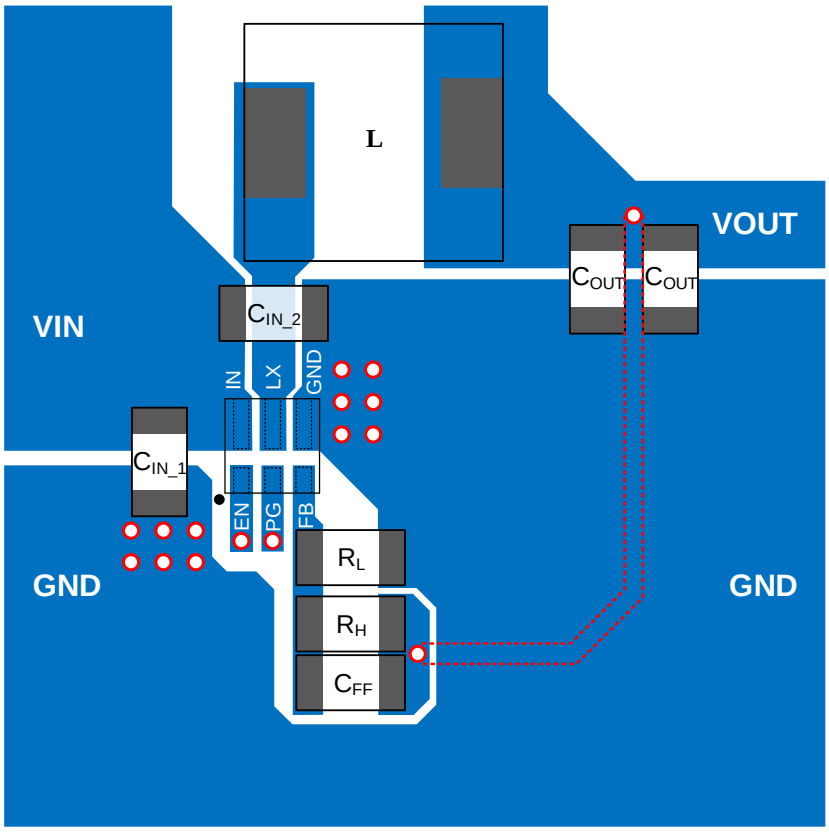
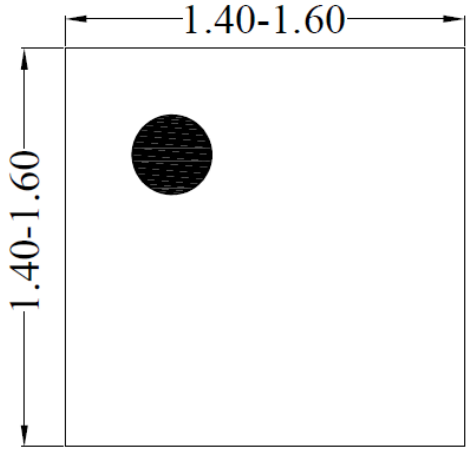
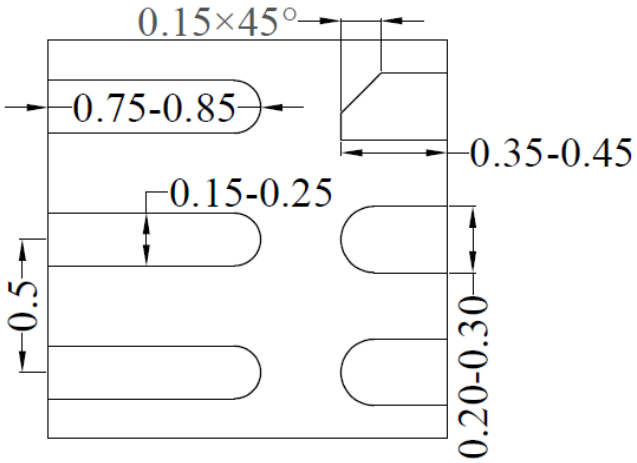


Figure 4. PCB Layout Suggestion

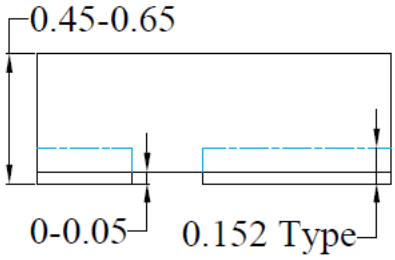
DFN1.5x1.5-6 Package Outline



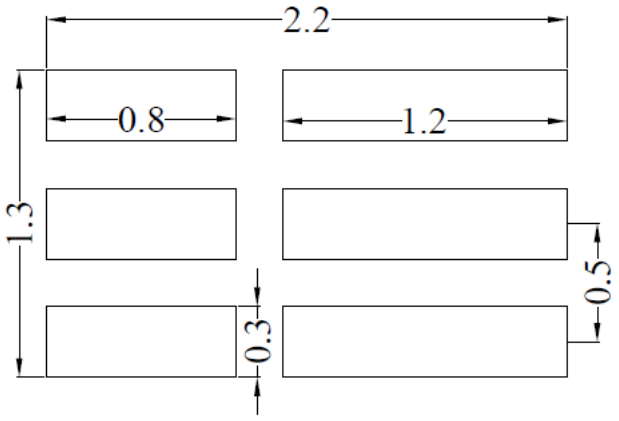
Top View



Bottom View



Front View

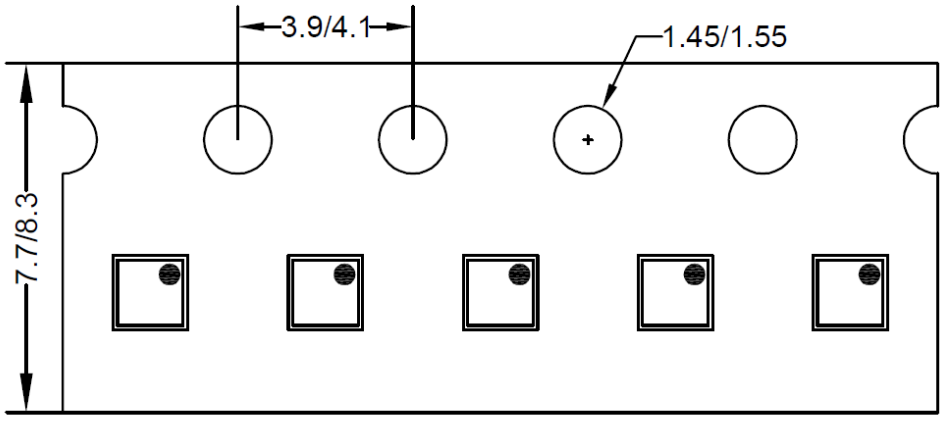


Recommended PCB Layout
(reference only)

Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

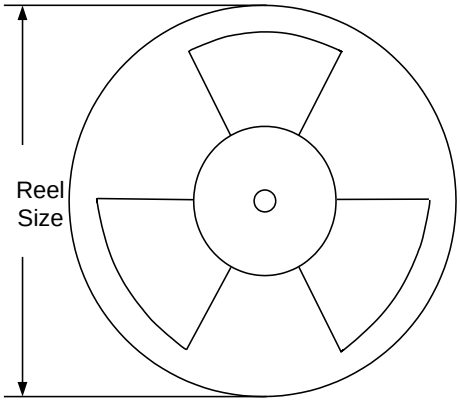
Taping and Reel Specification

DFN1.5×1.5 taping orientation



Feeding direction →

Carrier tape and reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN1.5×1.5	8	4	7"	400	160	3000

Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Dec.14, 2022	Revision 1.0	Language improvements for clarity.
Nov.17, 2022	Revision 0.9A	Update the Package outline (page 11)
Dec.14, 2021	Revision 0.9	Initial Release

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