SY26023E

High Efficiency, 2.2MHz, 3A, 5.5V Input Synchronous Buck Converter

General Description

The SY26023E high efficiency 2.2MHz synchronous buck converter operates over a wide input voltage range of 2.5V to 5.5V, and can deliver an output current up to 3A. It integrates a top MOSFET and a bottom MOSFET with very low $R_{DS(ON)}$ to minimize conduction loss. The 2.2MHz pseudo-constant switching frequency enables using small external inductor and capacitor values.

The SY26023E uses advanced constant on-time and ripple-based control strategy to achieve fast transient response. It also provides cycle-by-cycle current limit protection, output under voltage protection and over temperature protection.

Only the input and output capacitors, inductor, feedback resistor divider and feedforward capacitor need to be selected for the targeted application specifications.

The SY26023E is available in a compact DFN1.5×1.5-6 package. The device is part of a family which shares the same package and pinout. The other parts in the family are: SY26023, 3A output current, PFM (Pulse Frequency Modulation), and SY26024 4A output current, PFM.

Features

- Low $R_{DS(ON)}$ for Internal MOSFETs: 38mΩ Top, 30mΩ Bottom
- Wide Input Voltage Range: 2.5V ~ 5.5V
- Up to 3A Output Current
- ±1% 0.6V Reference over Temperature from -40°C to 125°C
- 2.2MHz High Switching Frequency Minimizes the External Components
- Advanced Constant On-time and Ripple-Based Control to Achieve Fast Transient Responses
- Forced Continuous Conduction Mode (FCCM) Operation
- Internal Soft-Start Limits the Inrush Current
- 100% Dropout Operation
- Power Good Indicator
- Cycle-by-Cycle Valley, Peak and Reverse Current Limit Protection
- Hic-Cup Mode Output Under Voltage Protection
- Auto-Recovery Mode Over Temperature Protection
- RoHS-Compliant and Halogen-Free
- Compact Package: DFN1.5×1.5-6

Applications

- Portable Electronics
- Industrial PC
- Smart Phone

Typical Application

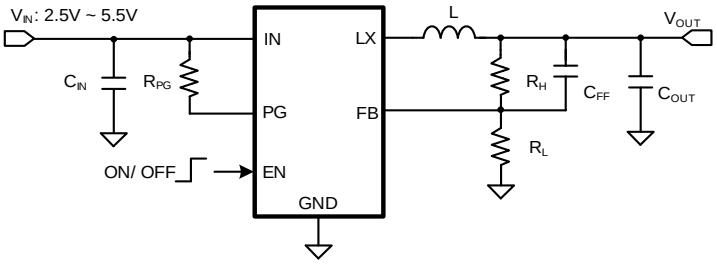


Figure 1. Schematic Diagram

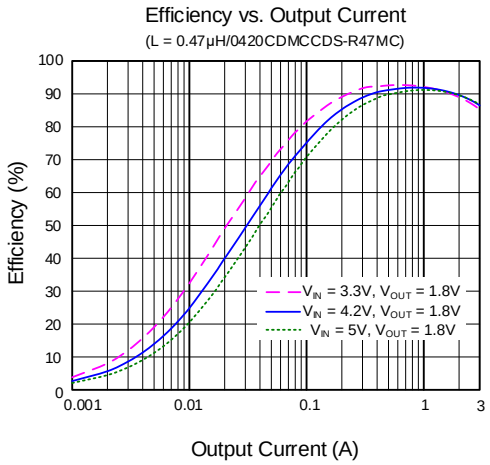


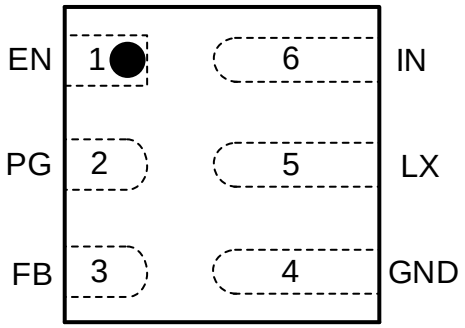
Figure 2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY26023EDQD	DFN1.5×1.5-6 RoHS-Compliant, Halogen-Free	**9f*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	EN	Enable pin. Pull this pin high to turn on the device and pull this pin low than to turn off the device. Do not leave this pin floating.
2	PG	Power good indicator pin. PG pin should be connected to V_{IN} or another voltage source through a resistor (e.g., 10kΩ ~ 100kΩ). This pin becomes low when the output voltage is within 95.5% to 109% of regulated value under normal operation.
3	FB	Output feedback pin. Connect this pin to the center point of the output resistor divider as shown in Figure 1. $V_{OUT} = 0.6 \times (1 + R_H/R_L)$.
4	GND	Ground pin.
5	LX	Inductor pin. Connect this pin to the switching node of the inductor.
6	IN	Input pin. Decouple this pin from the GND pin with at least a 10μF ceramic capacitor.

Block Diagram

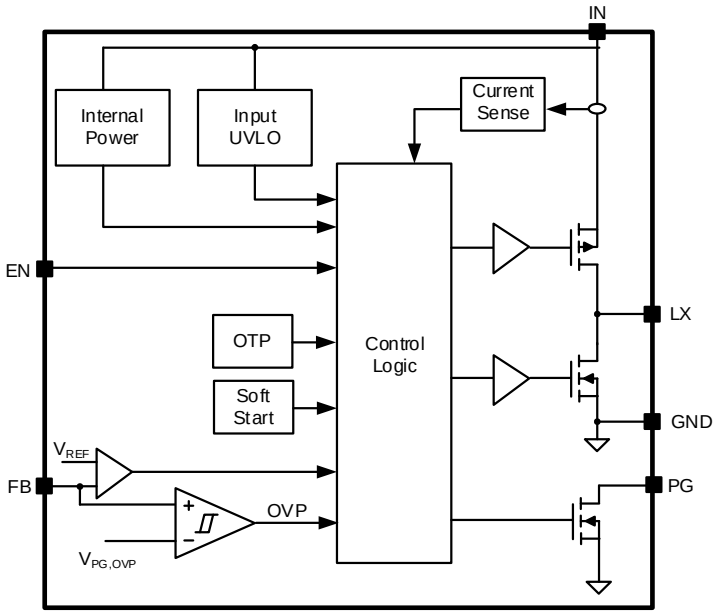


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	6	V
EN, FB, PG	-0.3	IN + 0.6	
LX	-0.3	6	
LX, 40ns duration	-3	7	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	62	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	8	
P_D Power Dissipation T_A = 25°C	1.6	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Input Voltage	2.5	5.5	V
Output Voltage	0.6	5.5	
Continuous Output Current		3	A
Ambient Temperature	-40	85	°C
Junction Temperature	-40	125	

Electrical Characteristics

(T_J = -40°C ~ 125°C, and V_{IN} = 2.5V to 5V, typical values are at T_J = 25°C and V_{IN} = 5V, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage Range	V_{IN}		2.5		5.5	V
	UVLO Falling Threshold	$V_{IN,UVLO}$	V_{IN} falling, T_J = 25°C	2.1	2.2	2.3	
	UVLO Hysteresis	$V_{IN,HYS}$			160		mV
	Shutdown Current	I_{SHDN}	V_{EN} = 0V, T_J = 25°C		0.05	0.5	μA
Output	FB Reference Voltage	V_{REF}		0.594	0.6	0.606	V
	Turn On Delay Time	$t_{ON,DLY}$	From EN high to LX starts switching (Note 4)		160		μs
	Soft-Start Time	t_{SS}	V_{OUT} from 0% to 95% V_{SET}		1.75		ms
	UVP Hiccup On-Time	$t_{HICCUP,ON}$	(Note 4)		2		
	UVP Hiccup Off-Time	$t_{HICCUP,OFF}$	(Note 4)		2.5		
	UVP Threshold	V_{UVP}	(Note 4)		33		$\%V_{REF}$
	Discharge on Resistance	R_{DIS}	V_{EN} = 0V		8		Ω
MOSFET	Top MOSFET $R_{DS(ON)}$	$R_{DS(ON),TOP}$			38		mΩ
	Bottom MOSFET $R_{DS(ON)}$	$R_{DS(ON),BOT}$			30		
	Top MOSFET Current Limit Threshold	$I_{LMT,TOP}$		4			A
	Bottom MOSFET Current Limit Threshold	$I_{LMT,BOT}$		3			
	Bottom MOSFET Reverse Current Limit Threshold	$I_{LMT,RVS}$		0.7	1.2		
Enable (EN)	Input Voltage High	$V_{EN,H}$		1			V
	Input Voltage Low	$V_{EN,L}$				0.4	
Power Good	Thresholds	$V_{PG,R}$	V_{FB} rising, PG from low to high		95.5		$\%V_{REF}$
		$V_{PG,F}$	V_{FB} falling, PG from high to low		92		
		$V_{PG,OVP}$	V_{FB} rising, PG from high to low		109		
		$V_{PG,REC}$	V_{FB} falling, PG from low to high		105		
	Delay Time	$t_{PG,R}$	Low to high		100		μs
		$t_{PG,F}$	High to low		20		
	Leakage Current	$I_{PG,LKG}$	V_{PG} = 5V		0.01		μA
Frequency	Switching Frequency	f_{SW}			2.2		MHz
	Minimum On-Time	$t_{ON,MIN}$			50		ns
	Maximum Duty Cycle	D_{MAX}	(Note 4)	100			%
OTP	Temperature	T_{OTP}	(Note 4)		150		°C
	Temperature Hysteresis	T_{HYS}	(Note 4)		20		

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} of SY26023EDQD is measured in the natural convection at T_A = 25°C on a 2-oz two-layer Silergy evaluation board. Pin 5 is the case position for SY26023EDQD θ_{JC} measurement.

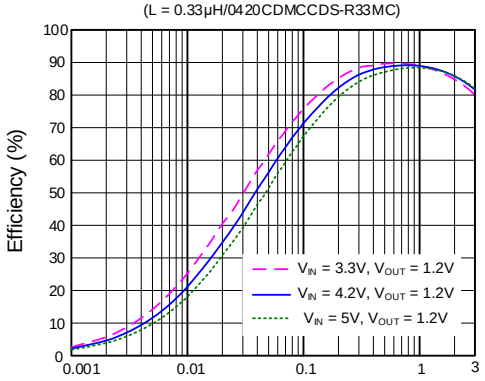
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Guaranteed by design.

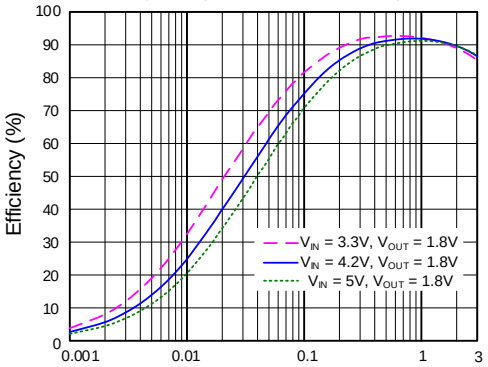
Typical Performance Characteristics

(T_A = 25°C, V_{IN} = 5V, V_{OUT} = 1.8V, L = 0.47μH, C_{OUT} = 20μF, unless otherwise noted)

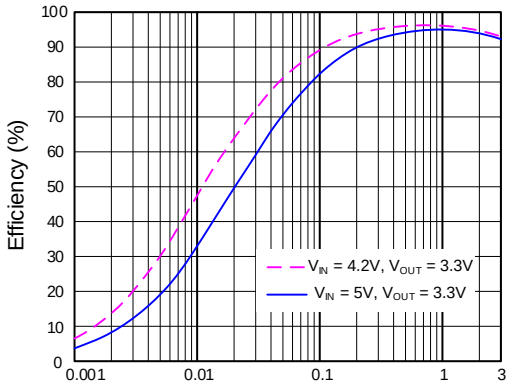
Efficiency vs. Output Current
(L = 0.33μH/0420CDMCCDS-R33MC)



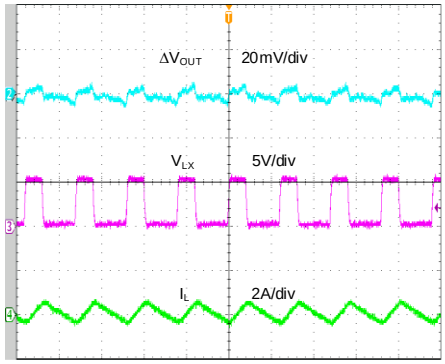
Efficiency vs. Output Current
(L = 0.47μH/0420CDMCCDS-R47MC)



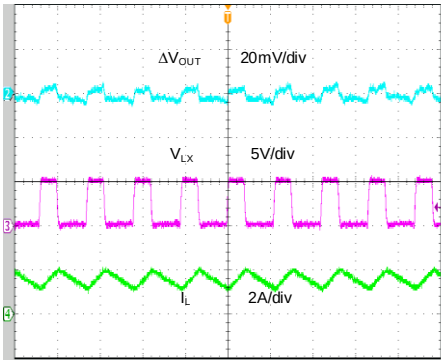
Efficiency vs. Output Current
(L = 0.47μH/0420CDMCCDS-R47MC)



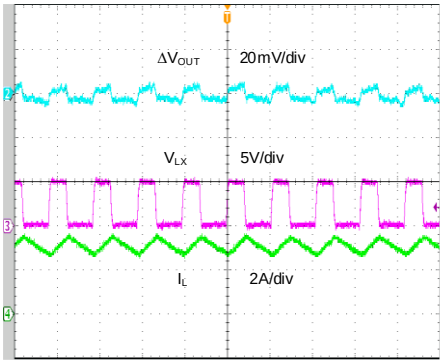
Output Ripple
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 0A)



Output Ripple
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 1.5A)

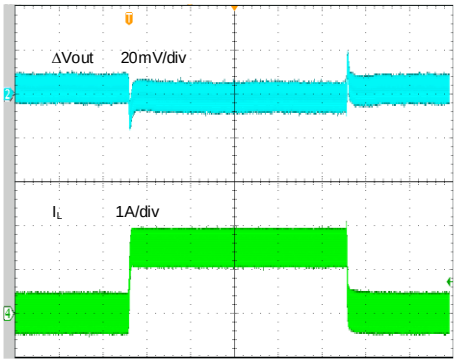


Output Ripple
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 3A)



Load Transient

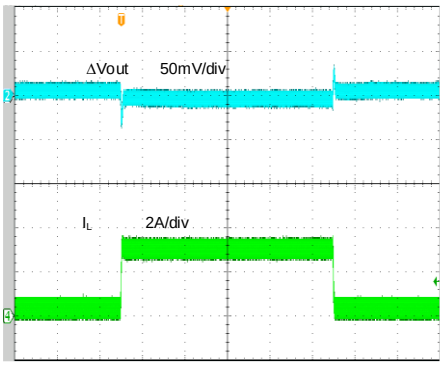
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 0A ~ 1.5A)



Time (200μs/div)

Load Transient

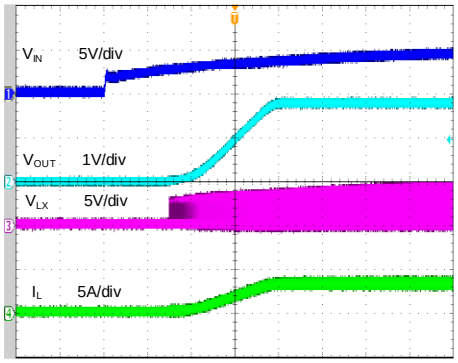
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 0.3A ~ 3A)



Time (200μs/div)

Startup from V_{IN}

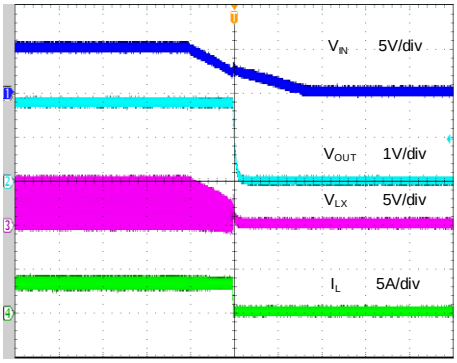
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 3A)



Time (800μs/div)

Shutdown from V_{IN}

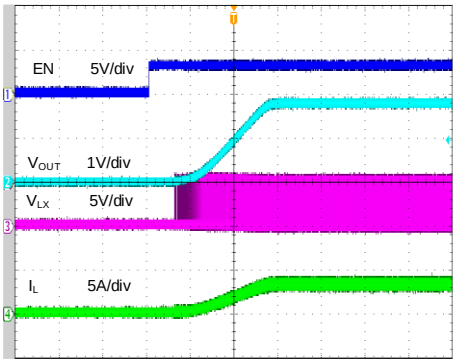
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 3A)



Time (200μs/div)

Startup from Enable

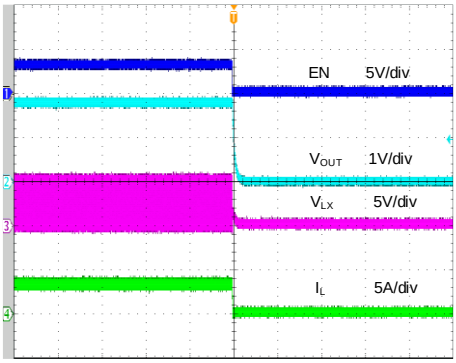
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 3A)



Time (800μs/div)

Shutdown from Enable

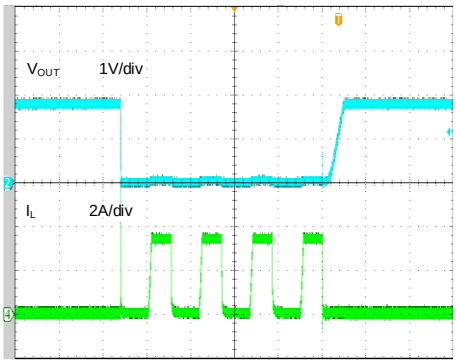
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 3A)



Time (200μs/div)

Short Circuit Protection

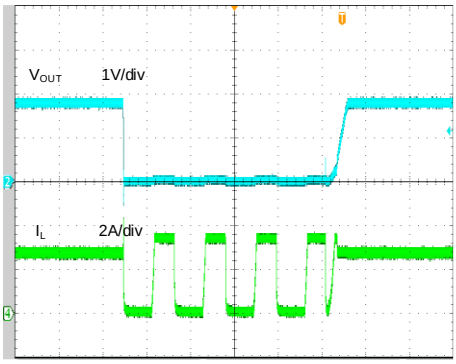
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 0A ~ short)



Time (4ms/div)

Short Circuit Protection

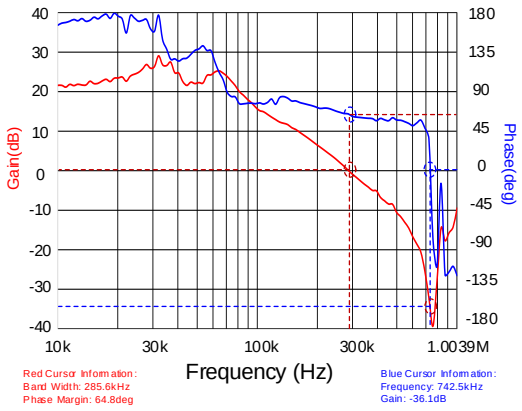
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 3A ~ short)



Time (4ms/div)

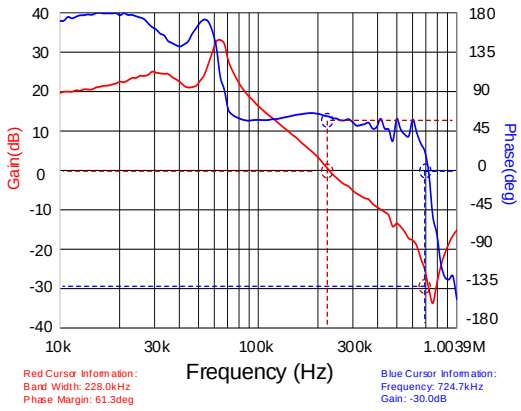
Bode Plot

(V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 3A)



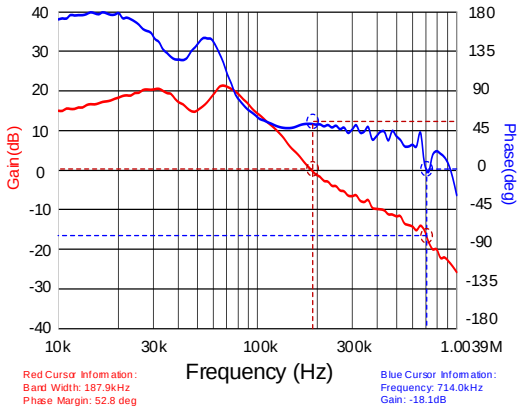
Bode Plot

(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 3A)



Bode Plot

(V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 3A)



Detailed Description

The SY26023E high efficiency 2.2MHz synchronous buck converter operates over a wide input voltage range of 2.5V to 5.5V, and can deliver an output current up to 3A. It integrates a top MOSFET and a bottom MOSFET with very low $R_{DS(ON)}$ to minimize conduction loss. The 2.2MHz pseudo-constant switching frequency allows small external inductor and capacitor values.

The SY26023E also provides cycle-by-cycle current limit protection output under voltage protection and over temperature protection.

Constant On-Time and Ripple-based Control Strategy

The device uses instant PWM architecture to achieve fast transient response. It uses an advanced constant on-time and ripple-based control strategy in which a virtual replica of the inductor current signal is synthesized internally and combined with the feedback voltage. When the sum voltage is lower than the reference voltage, the bottom MOSFET turns off and the top MOSFET turns on for a fixed period of time (Constant t_{ON}). t_{ON} is internally calculated according to the input voltage, output voltage, and desired switching frequency (f_{SW}):

$$t_{ON} = \frac{V_{OUT}/V_{IN}}{f_{SW}}$$

The top MOSFET turns off after a period of t_{ON}.

Input Under Voltage Lockout (UVLO)

To prevent operation before the internal circuitry is ready and to ensure that the top and bottom MOSFETs can be properly driven, the device incorporates an input under voltage lockout protection. The SY26023E remains in a low current state and all LX node switching actions are inhibited until V_{IN} exceeds $V_{IN,UVLO}$ + $V_{IN,HYS}$. At that time, if EN is enabled, the device will startup. If V_{IN} falls below falling threshold $V_{IN,UVLO}$, the LX node switching actions will again be suppressed.

Enable Control

The EN input is a high-voltage input with logic-compatible threshold. When EN is driven above 1V, normal device operation is enabled. When EN is driven to less than 0.4V, the device will shut down, reducing the input current to less than 0.5μA.

Output Power Good Indicator

PG is an open drain output controlled by a window comparator connected to FB. If the voltage is higher than $V_{PG,R}$ and less than $V_{PG,OVP}$ for at least the power good delay time (low to high), PG will be set to high-impedance state.

PG should be connected to V_{IN} or another voltage source through a resistor (e.g., 100kΩ). After V_{IN} rises until the internal initial power is ready, the PG internal MOSFET is turned on so that PG is actively driven low before output voltage is ready. After the feedback voltage V_{FB} reaches $V_{PG,R}$, PG is set to high-impedance state after a delay time of 100μs (typ.). When V_{FB} drops to $V_{PG,F}$, or rises above $V_{PG,OVP}$, PG is driven low after a delay time of 20μs (typ.).

Fault-Protection Modes

Cycle-by-Cycle Current Limit Protection

If the top MOSFET current exceeds the top current limit threshold, it will turn off and the bottom MOSFET will turn on. If the bottom MOSFET current exceeds the bottom current limit threshold, it will stay on until the current decreases below its current limit threshold. As a result, both inductor peak and valley currents are limited.

Reverse Current Limit

When the output voltage is higher than the target output voltage, the device will operate with reverse current limit until the condition disappears. In this case, a cycle-by-cycle reverse current limit protects the bottom MOSFET from excessive negative current. When $I_{LMT,RVS}$ threshold is reached, the bottom MOSFET is turned off, and a new t_{ON} cycle is triggered.

Output Under Voltage Protection (UVP)

With output current increasing, as soon as the bottom MOSFET current exceeds its current limit threshold, the top MOSFET will not be allowed to turn on any more. If the load current continues to increase, the output voltage will drop. When the output voltage falls below 33% of the regulated level, the output under voltage protection will be activated and the device will operate in hiccup mode. The hiccup on-time is 2ms, and the hiccup off-time is 2.5ms. If the hard short condition is removed, the device will return to normal operation.

Over Temperature Protection (OTP)

The device includes over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. When the junction temperature is reduced by approximately 20°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate thermal dissipation so that the junction temperature does not exceed the OTP threshold.

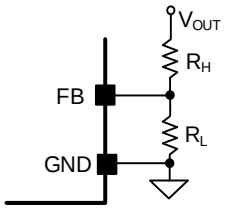
Application Information

The following paragraphs provide information on the selection of the external components needed to meet the targeted application specifications.

Feedback Resistor-Divider R_H and R_L

Choose R_H and R_L to program the proper output voltage. A value between 1kΩ and 1MΩ is recommended for both resistors to minimize power consumption under light loads. As an example, if V_{OUT} = 1.8V and R_H selected value is 100kΩ, R_L can be calculated as follows:

$$R_L = \frac{0.6}{V_{OUT} - 0.6V} \times R_H$$



With a calculated value of 50kΩ for R_L, a standard 1% 49.9kΩ resistor is selected.

Input Capacitor C_{IN}

For the best performance, select a typical X5R or better grade ceramic capacitor with a 16V rating, and at least 10µF capacitance. The capacitor should be placed as close as possible to the device, while also minimizing the loop area formed by C_{IN} and the IN/GND pins.

When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability, and high RMS current rating over a wide temperature and voltage range.

In situations where the input rail is supplied through long wires, it is recommended to add some bulk capacitance like electrolytic, tantalum or polymer type capacitors to reduce the overshoot and ringing caused by the added parasitic inductance.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current. The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1 - D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 10µF X5R capacitor is sufficient for most applications.

Output Inductor L

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT} / V_{IN,MAX})}{f_{sw} \times I_{OUT,MAX} \times 0.4}$$

Where, f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The device has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Use an inductor with DCR less than 50mΩ to achieve good overall efficiency.

Output Capacitor C_{OUT}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady state ripple and transient

requirements must be taken into consideration when selecting C_{OUT}. For the best performance, use a X5R or better grade ceramic capacitor with a 16V rating, and capacitance of at least 10μF.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed.

The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, consider both.

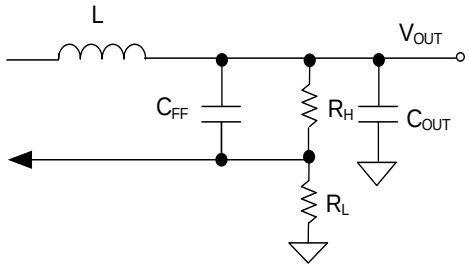
$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

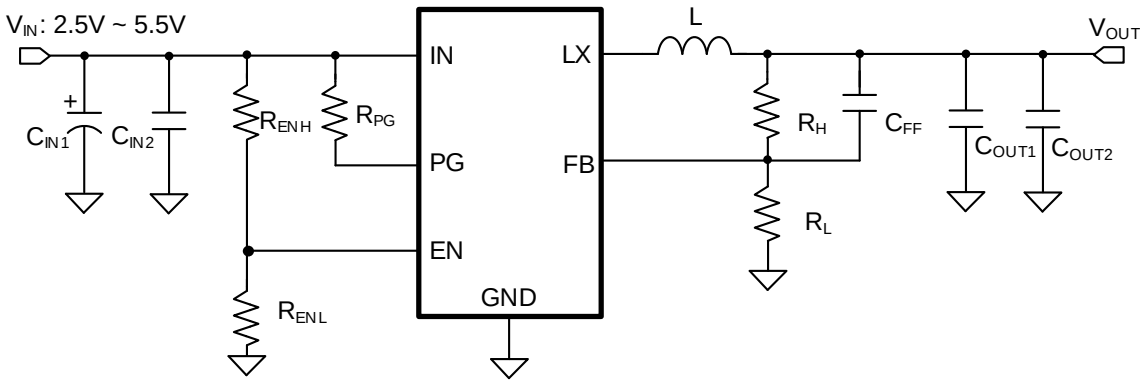
The measured capacitive ripple might be higher than the theoretical value because the effective capacitance for ceramic capacitors decreases with the voltage across its terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Feedforward Capacitor C_{FF}

The device integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a ceramic capacitor (feedforward capacitor C_{FF}) in parallel with R_H may further speed up the load transient response. It is recommended at least 220pF for most applications. Note that when the output LC parameter is large, the feedforward capacitor can be increased for provide sufficient ripple to FB for small output ripple and good transient behavior.



Application Schematic (V_{OUT} = 1.8V)



BOM List

Reference Designator	Description	Part Number	Manufacturer
C_{IN1}	100µF/25V(electrolytic capacitor)		
C_{IN2}, C_{OUT1}, C_{OUT2}	10µF/16V/X5R, 1206	GRM319R61C106KE15D	mµRata
C_{FF}	220pF/50V/C0G, 0603	GRM1885C1H221JA01D	mµRata
L	0.47µH/inductor	0420CDMCCDS-R47MC	Sumida
R_H	100kΩ, 1%, 0603		
R_L	49.9kΩ, 1%, 0603		
R_{PG}	100kΩ, 1%, 0603		
R_{ENH}	10kΩ, 1%, 0603		
R_{ENL}	1MΩ, 1%, 0603		

Recommended Component Values for Typical Applications

V_{OUT}(V)	R_H(kΩ)	R_L(kΩ)	C_{FF}(pF)	L/Part Number	C_{OUT}
1.2	100	100	220	0.33µH/0420CDMCCDS-R33MC	10µF/16V/X5R, 1206
1.8	100	49.9	220	0.47µH/0420CDMCCDS-R47MC	10µF/16V/X5R, 1206
3.3	100	22.1	220	0.47µH/0420CDMCCDS-R47MC	10µF/16V/X5R, 1206

Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

Input Capacitors: Place the input capacitors very close to IN and GND pins, minimizing the loop formed by these connections. The input capacitor should be connected to the IN and GND pins using a wide copper area.

Output Capacitors: Connect the C_{OUT} negative terminal to the GND pin using wide copper traces instead of vias, in order to achieve better accuracy and stability of the output voltage.

Feedback Network: Place the feedback components (R_H, R_L and C_{FF}) as close to the FB pin as possible. Avoid routing the feedback line near LX, or other high-frequency signals as it is noise-sensitive. Use a Kelvin connection to connect with C_{OUT} rather than the inductor output terminal.

LX Connection: Keep the LX area small to prevent excessive EMI, while providing a wide copper trace to minimize parasitic resistance and inductance.

EN Signal: It is not recommended to connect EN pin directly to V_{IN} or another voltage source. A resistor in a range of 1kΩ to 1MΩ should be used if EN pin is pulled high.

GND Vias: Place an adequate number of vias on the GND layer around the device for better thermal performance.

PCB Board: To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if possible. Connect the ground pad to a large copper area to enhance thermal performance.

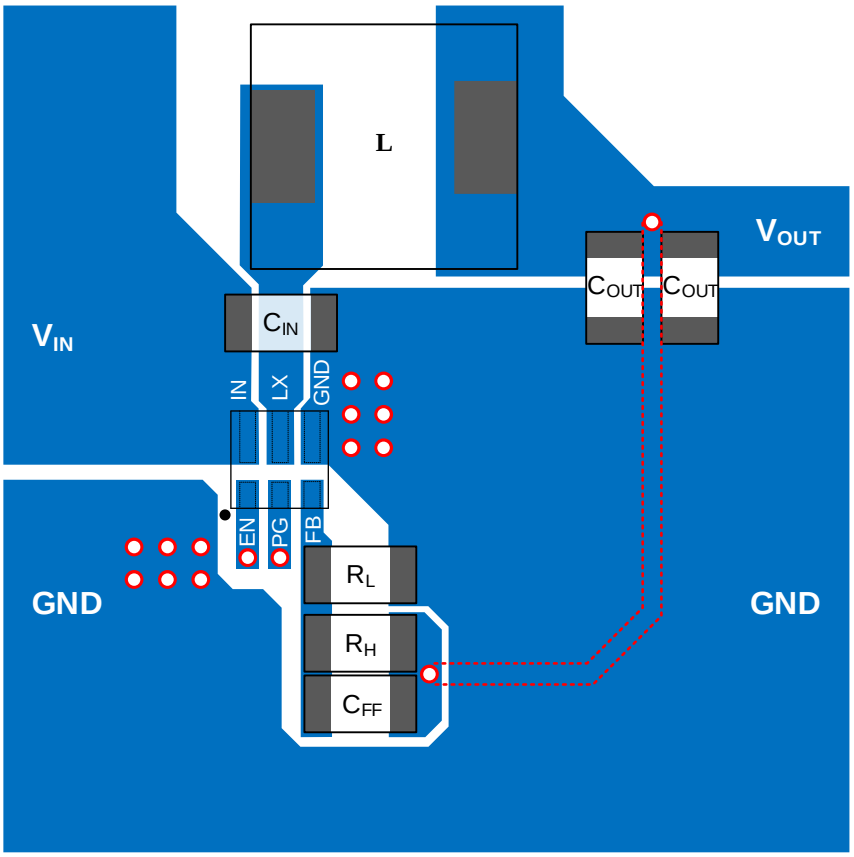
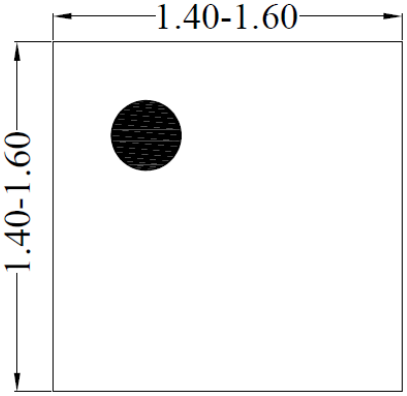
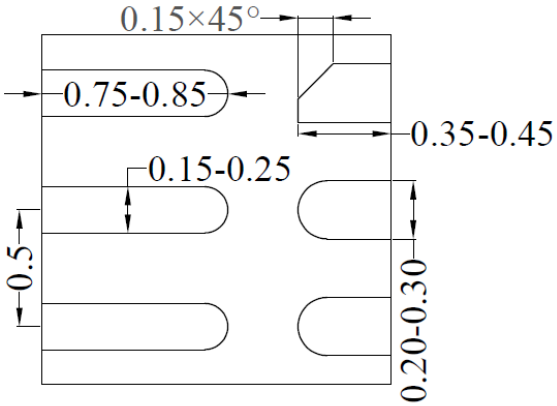


Figure 4. Suggested PCB Layout

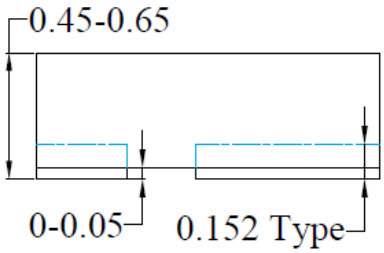
DFN1.5×1.5-6 Package Outline



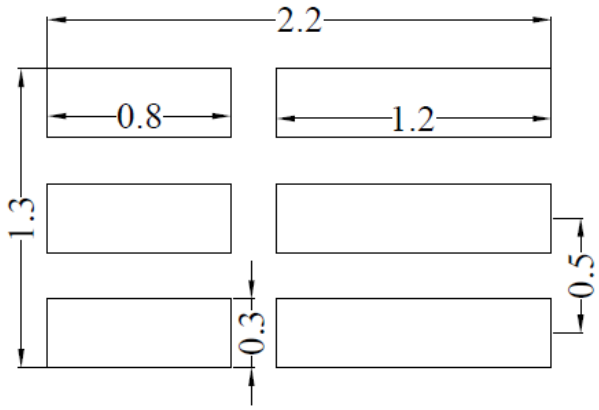
Top View



Bottom View



Front View



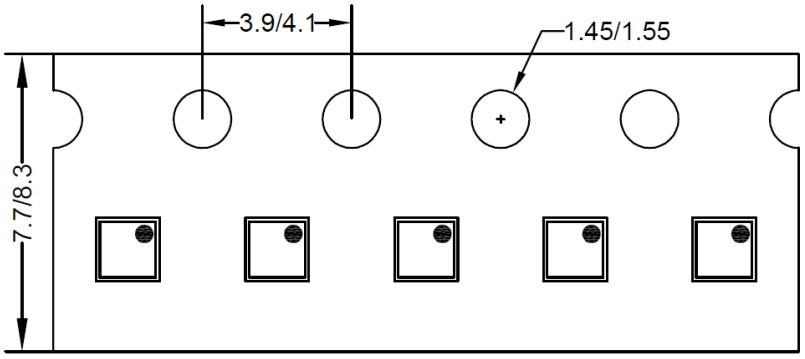
Recommended PCB layout
(only for reference)

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr;

Taping & Reel Specification

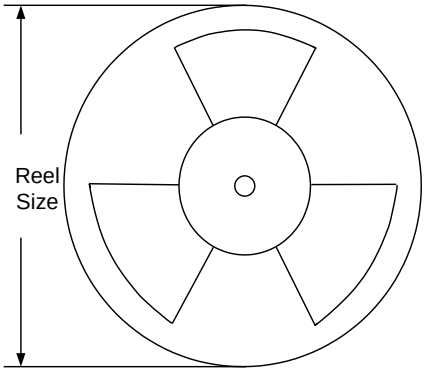
1. Taping orientation

DFN1.5×1.5



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN1.5×1.5	8	4	7"	400	160	3000

3. Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, it is not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Mar. 14, 2024	Revision 1.0	Initial Release

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