SY22312CS42-J10

11-Channel Multi-Spectrum Sensor

General Description

The SY22312CS42-J10 is an 11-channel multi-spectrum light sensor, for the spectrum identification and color matching applications. The SY22312CS42-J10 can detect eight channels which cover visible range from 380nm to 780nm, along with Flicker channel to detect low frequency ambient light flicker.

The SY22312CS42-J10 also integrates a near infrared channel which can sense the 800~1100nm infrared light. The NIR channel combined with all other visible channels can provide surrounding ambient light information and help to distinguish light source type. The flicker sensing engine can calculate whether it is 100Hz or 120Hz via relative flag bit through internal algorithm and can also buffer data to calculate the flicker frequency through the external logic algorithm.

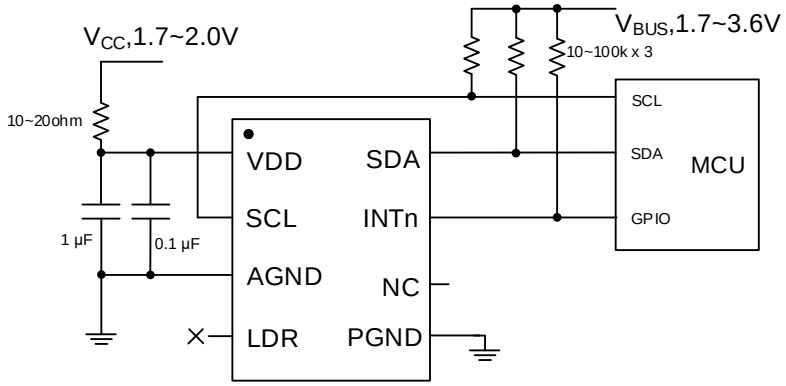
The SY22312CS42-J10 provides a separate pin for various types of interrupt schemes, which simplifies system design complexity by eliminating the need to poll sensor readings. A SMBus compatible with I^2C interface is also integrated for easy connection to a microcontroller or embedded controller.

The SY22312CS42-J10 featuring high SNR performance, high data uniformity, user-friendly interface and wide operating temperature range, is suitable for battery-powered equipment with the requirements of ambient light sensing and proximity sensing.

Features

- Spectral Sensing
  - 16-bit Resolution for all Channels
  - Wide Detection Range: Larger than 100k lux
  - Indoor Light Source Flicker Noise Rejection (50Hz and 60Hz)
  - Programmable Integration Time and Gain Settings from 1x to 2048x
- CCT (Correlated Color Temperature)
  - Detection CCT Range from 2000k to 13000k
- Flicker
  - 16 Bit Resolution
  - Sensitivity Less than 1lux/count, Detection Range from 1 to 10k lux
  - Sampling Rate Higher than 2kHz, can Detect Flicker from 50Hz to 400Hz
  - FIFO Depth 512 bytes
- Interrupt Source Selectable, FIFO Buffer Depth can also Generate an Interrupt
- Operation Range
  - 1.7V-2.0V
  - 490μA (typ.) for Normal Operation Mode, 5μA (typ.) Shutdown Current
  - -40°C to +85°C Operating Temperature
- Package Information
  - Size: 3.1mm×2.0mm×1.0mm

Typical Application



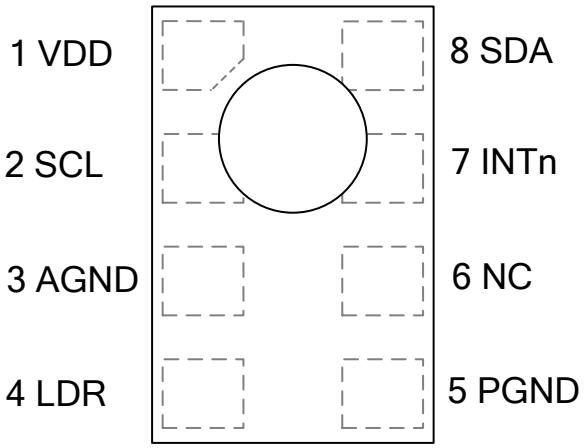
Note 1: Capacitors shall be placed as close as possible to V_{DD} pin.

Note 2: LDR pin can be floated. Recommend to be connected to GND if not used.

Ordering Information

Part Number	Package Type	Top Mark	MSL	Delivery Quantity
SY22312CS42-J10	LGA3.1×2.0-8 RoHS-Compliant and Halogen-Free	N/A	3	3000 pcs/reel

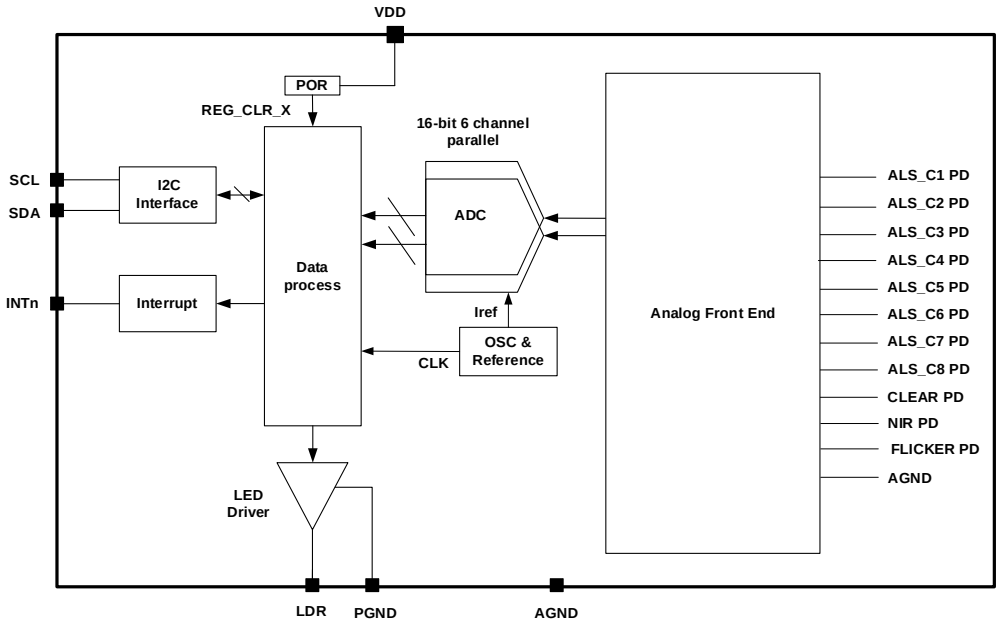
Pinout (Top View)



Top Mark: 1C1xyz (**Device code:** 1C1, x=year code, y=week code, z=lot number code)

Pin No.	Pad Name	Pin Description
1	VDD	Positive supply: 1.7V to 2.0V.
2	SCL	I^2C clock line. The I^2C bus lines can be pulled from 1.7V to above VDD, 3.6V max.
3	AGND	Ground. All voltages are referenced to AGND/PGND and both ground pins must be connected to ground.
4	LDR	LED current sink input.
5	PGND	Ground. All voltages are referenced to AGND/PGND and both ground pins must be connected to ground.
6	NC	No connection.
7	INTn	Interrupt output with open-drain configuration, active low level.
8	SDA	I^2C data line. The I^2C bus lines can be pulled from 1.7V to above VDD, 3.6V max.

Block Diagram



Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	2.3	V
I^2C Bus Voltage	V_{I^2C}	-0.3	4	
INTn and driving terminal Voltage	V_{INTn}, V_{IRDRV}	-0.3	4	
HBM (Human Body Model)		±2		kV
CDM (Charged Device Model)		±500		V

Recommended Operating Conditions (Note 3)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	1.7		2.0	V
Storage Temperature	T_{STG}	-40		+100	°C
Operating Temperature	T_{OPR}	-40		+85	°C

Electrical and Optical Characteristics

V_{DD} = 1.8V, T_A = 25°C, unless otherwise specified (Note 4)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Range	VDD		1.7	1.8	2.0	V
Supply Current when Powered down	IDD_SD	Spectral sensing disabled， Flicker sensing disabled	-	5	20	μA
Supply Current Spectral in Normal Mode	IDD_Spectral sensor	Spectral sensing enabled, Flicker sensing disabled	338	450	563	μA
	IDD_Total	Spectral sensing and Flicker sensing enabled	368	490	613	
Flicker Channel Integration Time	T	FLK_INT_TIME=16ms	15.2	16	16.8	ms
Full Scale of Spectral Sensor Output	DATA_FS	ALS_INT_TIME>=12.5ms	-	-	65535	counts
C1_count(Wp423nm)	DATA_C1	IT=50ms, Gain=1024x, Spectral sensing enabled, White LED 2700K, Ev=200lux	1989	2550	3111	counts
C2_count(Wp448nm)	DATA_C2		10199	13076	15953	
C3_count(Wp468nm)	DATA_C3		2404	3082	3760	
C4_count(Wp516nm)	DATA_C4		4541	5822	7103	

C5_count(Wp545nm)	DATA_C5		33189	36877	40565	
C6_count(Wp601nm)	DATA_C6		12882	16515	20148	
C7_count(Wp626nm)	DATA_C7		9233	11838	14442	
C8_count(Wp685nm)	DATA_C8		624	800	976	
NIR_count(Wp850nm)	DATA_NIR		353	453	553	
Flicker_count(Wp525nm)	DATA_Flicker	IT=1ms, Gain=4x, White LED 2700K, Ev=200lux	541	795	1050	
Channel Ratio of C1/C2		IT=50ms, Gain=1024x,Spectral sensing enabled, White LED 2700K, Ev=200lux	0.1755	0.1950	0.2145	
Channel Ratio of C2/C5			0.3191	0.3546	0.3900	
Channel Ratio of C3/C2			0.2121	0.2357	0.2593	
Channel Ratio of C4/C2			0.4007	0.4452	0.4898	
Channel Ratio of C6/C2			1.1367	1.2630	1.3893	
Channel Ratio of C7/C2			0.8148	0.9053	0.9959	
Channel Ratio of C8/C2			0.0538	0.0612	0.0685	
Channel Ratio of NIR/C2			0.0305	0.0346	0.0388	
Dark Count	C1 channel	IT=100ms, Gain=1024x, Spectral sensing enabled, Ev=0lux. Calculated by algorithm or by actual test(C8 and NIR channels)	-35		35	counts
	C2 channel		-25		20	
	C3 channel		-25		25	
	C4~C8, NIR channels		-15		15	
	Flicker channel	FLK_IT=64ms,FLK_Gain=32x,Spectral sensing enabled, Ev=0lux	-45		45	
Gain Ratio	C2~C7,C8, NIR channels gain ratio	1024x/512x,512x/256x,256x/128x,128x/64x,64x/32x,32x/16x	1.8	2.0	2.2	
	C2~C7,C8, NIR channels gain ratio	2048x/1024x	1.7	2.0	2.3	
	C1 channel gain ratio	512x/256x,256x/128x,128x/64x,64x/32x,32x/16x	1.8	2.0	2.2	
	C1 channel gain ratio	2048x/1024x,1024x/512x	1.7	2.0	2.3	

I^2C Electrical Specifications V_{DD} = 1.8V, T_A = 25°C, unless otherwise specified (Note 2)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Range for I^2C Interface	V_{I^2C}		1.7	-	3.6	V
SCL Clock Frequency	f_{SCL}		-	-	1000	kHz
Low Level Input Voltage of SCL and SDA	V_{IL}		-	-	0.55	V
High Level Input Voltage of SCL and SDA	V_{IH}		1.25	-	-	V
SDA Current Sinking Capability	I_{SDA}	V_{OL} = 0.4V	2.7	5	-	mA
Hysteresis of Schmitt Trigger Input	V_{hys}		0.05 V_{DD}	-	-	V
Low-level Output Voltage of SDA	V_{OL}	I_{OL}=4mA	-	-	0.4	V
Input Leakage for SDA, SCL	I_i		-10	-	10	μA
Pulse Width of Spikes Suppressed by the Input Filter	t_{SP}		-	-	50	ns
SCL Falling Edge to SDA Output Data Valid	t_{AA}		-	-	0.9	μs
Capacitance for Each SDA and SCL Pin	C_i		-	-	10	pF
Hold Time (repeated) START Condition	$t_{HD:STA}$		0.26	-	-	μs
Low Period of the SCL Clock	t_{LOW}		0.5	-	-	μs
High Period of the SCL Clock	t_{HIGH}		0.26	-	-	us
Set-up Time for a Repeated START Condition	$t_{SU:STA}$		0.26	-	-	μs
Data Hold Time	$t_{HD:DAT}$		0	-	-	ns
Data Set-up Time	$t_{SU:DAT}$		50	-	-	ns
Set-up Time for STOP Condition	$t_{SU:STO}$		0.26	-	-	μs
Bus Free Time between a STOP and START Condition	t_{BUF}		0.5	-	-	μs
Rise Time of Both SDA and SCL	t_R		-	-	120	ns
Fall Time of SDA and SCL	t_F		-	-	120	ns
Capacitive Load for Each Bus Line	C_b		-	-	0.55	nF
SDA and SCL System Bus Pull-up Resistor	$R_{pull-up}$	Maximum is	-	10	-	kΩ

		determined by t_R and t_F (Note 5)				
Data Valid Time	$t_{VD:DAT}$		-	-	0.45	μs
Data Valid to Acknowledge Time	$t_{VD:ACK}$		-	-	0.45	μs
Noise Margin at the LOW Level	V_{nL}		$0.1V_{DD}$	-	-	V
Noise Margin at the HIGH Level	V_{nH}		$0.2V_{DD}$	-	-	V

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The I^2C bus protocol was developed by Philips (now NXP). For a complete description of the I^2C protocol, please review the NXP I^2C design specification at http://www.i2c−bus.org/references/.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that TA ≅ TJ = 25C.

Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production teste

Register Map

The SY22312CS42-J10's I²C target address is 0x46. Below is the register map details of sensor.

Table 1. Registers and Register Bits

REG Addr	REG Name	Bit								
		7	6	5	4	3	2	1	0	Default
0x00	COM_TEST	Chip ID								0x32
0x01	ALS_CON1	ADC5_EN	ADC4_EN	ADC3_EN	ADC2_EN	ADC1_EN	Reserved			0x00
0x02	ALS_CON2	ALS_INT_TIME[3:0]				ALS_GAIN[3:0]				0x00
0x03	ALS_CON3	ALS_MODE[1:0]		MODE1_INT_TIME	Reserved	MODE1_CYC[3:0]				0x00
0x04	ALS_CON4	Reserved			MODE2_CYC[4:0]					0x00
0x05	ALS_CON5	Must Write 0x93 to this register								0x00
0x06	ALS_CON6	FLK_EN	FLK_INT_TIME[2:0]			Reserved	FLK_GAIN[2:0]			0x00
0x07	AINT_CON	AINT_EN	Reserved	AINT_SOURCE[3:0]				AINT_PRST[1:0]		0x00
0x08	FINT_CON	FLV_INT_EN	OVERWR_EN	Reserved	FIFO_CAL_EN	FLK_INT_EN	FLK_TYPE	FINT_PRST[1:0]		0x00
0x0A	DRV_CON	DRV_EN	DRV_CUR[6:0]							0x00
0x0B	ALS_LTL	ALS_LTL[7:0]								0x00
0x0C	ALS_LTH	ALS_LTH[15:8]								0x00
0x0D	ALS_HTL	ALS_HTL[7:0]								0xFF
0x0E	ALS_HTH	ALS_HTH[15:8]								0xFF
0x0F	FLK_FIFO_TH	FLK_FIFO_LEVEL[7:0]								0x00
0x10	C1_DATAL	C1_DATA[7:0]								0x00
0x11	C1_DATAH	C1_DATA[15:8]								0x00
0x12	C2_DATAL	C2_DATA[7:0]								0x00
0x13	C2_DATAH	C2_DATA[15:8]								0x00
0x14	C3_DATAL	C3_DATA[7:0]								0x00
0x15	C3_DATAH	C3_DATA[15:8]								0x00
0x16	C4_DATAL	C4_DATA[7:0]								0x00
0x17	C4_DATAH	C4_DATA[15:8]								0x00
0x18	C5_DATAL	C5_DATA[7:0]								0x00
0x19	C5_DATAH	C5_DATA[15:8]								0x00
0x1A	C6_DATAL	C6_DATA[7:0]								0x00
0x1B	C6_DATAH	C6_DATA[15:8]								0x00
0x1C	C7_DATAL	C7_DATA[7:0]								0x00
0x1D	C7_DATAH	C7_DATA[15:8]								0x00
0x1E	CLEAR_DATAL	CLEAR_DATA[7:0]								0x00
0x1F	CLEAR_DATAH	CLEAR_DATA[15:8]								0x00
0x20	C8_DATAL	C8_DATA[7:0]								0x00
0x21	C8_DATAH	C8_DATA[15:8]								0x00
0x22	NIR_DATAL	NIR_DATA[7:0]								0x00

0x23	NIR_DATAH	NIR_DATA[15:8]								0x00
0x2C	FLK_DATAL	FLK_DATA[7:0]								0x00
0x2D	FLK_DATAH	FLK_DATA[15:8]								0x00
0x2F	INT_FLAG	AINT_FLAG	ALS_VALID	Unused						0x00
0x30	FIFO_LVL_CNT	FIFO_LV_CNT[7:0]								0x00
0x31	FIFO_FLAG	FINT_FLAG	FIFO_EMPTY	FIFO_FULL	Unused	CAL_INT	100HZ_FLAG	120HZ_FLAG	Unused	0x00
0x33	FIFO_R_CLR	FIFO_R_CNT_CLR								0xAA
0x34	FIFO_DATAL	FIFO_DATA[7:0]								0x00
0x35	FIFO_DATAH	FIFO_DATA[15:8]								0x00
0x36	FIFO_R_CNT	FIFO_R_CNT[7:0]								0x00
0x3A	LOG_CODE1	LOG_CODE1[7:0]								0x00
0x3B	LOG_CODE2	LOG_CODE2[7:0]								0x00
0x3C	LOG_CODE3	LOG_CODE3[7:0]								0x00

Table 2. Command Code

Bit #	Access	Default	Name	Function / Operation
7				Unused register bits - write 0
6:4				111, special function others, register address
3:0			Register address / Special function register	Special function: 0000:clears FIFO level interrupt flag and FIFO data 0010:clears Flicker calculation interrupt flag(CAL_INT) 0100:clears ALS interrupt flag 1010:restart all ADCs 1101:set registers to default value others: reserved

Chip ID Register (0x00)

This read-only register contains a fixed data 0x32. Read this register through I^2C interface to identify the product. It can also help to test whether the communication link is established or not.

Table 3. Register 0x01 (ALS_CON1) – ALS Sensing Configuration 1

Bit #	Access	Default	Name	Function / Operation
7	RW	0x00	ADC5_EN	When specific bit is 1, related ADC is enabled When specific bit is 0, related ADC is disabled ADC5 for C8/NIR channels ADC4 for C6/C5 channels ADC3 for C4/C7 channels ADC2 for C2/C3 channels ADC1 for C1/CLEAR channels
6	RW	0x00	ADC4_EN	
5	RW	0x00	ADC3_EN	
4	RW	0x00	ADC2_EN	
3	RW	0x00	ADC1_EN	
2:0	RW	0x00	Reserved	Reserved. Write as 0

Table 4. Register 0x02 (ALS_CON2) – ALS Sensing Configuration 2

Bit #	Access	Default	Name	Function / Operation
7:4	RW	0x00	ALS_INT_TIME[3:0]	For bit 7:4 = (see the following) 0000, integration time of color sensing is 1.56ms 0001, integration time is 3.12ms 0010, integration time is 6.25ms 0011, integration time is 12.5ms 0100, integration time is 25ms 0101, integration time is 50ms 0110, integration time is 100ms 0111, integration time is 200ms 1000, integration time is 400ms
3:0	RW	0x00	ALS_GAIN[3:0]	For bit 3:0 = (see the following) 0000, gain setting of C1~C8, CLEAR and NIR ADCs is 2048x 0001, gain is 1024x 0010, gain is 512x 0011, gain is 256x 0100, gain is 128x 0101, gain is 64x 0110, gain is 32x 0111, gain is 16x 1000, gain is 8x 1001, gain is 4x 1010, gain is 2x 1011, gain is 1x others, reserved

Table 5. Register 0x03 (ALS_CON3) – ALS Sensing Configuration 3

Bit #	Access	Default	Name	Function / Operation
7:6	RW	0x00	ALS_MODE[1:0]	For bit 7:6 = (see the following) MODE1: Dummy channels are working MODE2:C1~C8, CLEAR and NIR channels are working 00, MODE1 & MODE2 are OFF 01, MODE1 is ON 10, MODE2 is ON 11, MODE1 & MODE2 alternate operation
5	RW	0x00	MODE1_INT_TIME	When =0, integration time for MODE1 is 12.5ms When =1, integration time for MODE1 is 25ms
4	RW	0x00	Reserved	Reserved. Write as 0
3:0	RW	0x00	MODE1_CYC[3:0]	MODE1 operates for (MODE1_CYC+1) cycles and output the last cycle data for dummy data, then switch to MODE2

Table 6. Register 0x04 (ALS_CON4) – ALS Sensing Configuration 4

Bit #	Access	Default	Name	Function / Operation
7:5	RW	0x00	Reserved	Reserved. Write as 0
4:0	RW	0x00	MODE2_CYC[4:0]	For bit 4:0 = (see the following) MODE 2 operates for (MODE2_CYC+1)*2 cycles and then switches to MODE1

Table 7. Register 0x05 (ALS_CON5) – ALS Averaging

Bit #	Access	Default	Name	Function / Operation
7:0	RW	0x00		User MUST write 0x93 to this byte when initialization

Table 8. Register 0x06 (ALS_CON6) – Flicker Configuration

Bit #	Access	Default	Name	Function / Operation
7	RW	0x00	FLK_EN	When =0, Flicker channel ADC is disabled When =1, Flicker channel ADC is enabled
6:4	RW	0x00	FLK_INT_TIME[2:0]	For bit 6:4 = (see the following) 000, integration time of Flicker detection is 0.25ms 001, integration time is 0.5ms 010, integration time is 1ms 011, integration time is 2ms 100, integration time is 4ms 101, integration time is 8ms 110, integration time is 16ms others, reserved
3	RW	0x00	Reserved	Reserved. Write as 0
2:0	RW	0x00	FLK_GAIN[2:0]	For bit 3:1 = (see the following) 000, gain setting of Flicker ADC is 64x 001, gain is 32x 010, gain is 16x 011, gain is 8x 100, gain is 4x 101, gain is 2x 110, gain is 1x others, reserved

Table 9. Register 0x07 (AINT_CON) – Color Sensing Interrupt Configuration

Bit #	Access	Default	Name	Function / Operation
7	RW	0x00	AINT_EN	When = 0, interrupt pin is HZ and irrelevant to AINT_FLAG bit When = 1, interrupt pin shall react according to AINT_FLAG bit
6	RW	0x00	Reserved	Reserved. Write as 0
5:2	RW	0x00	AINT_SOURCE[3:0]	For bit 5:2 = (see the following) 0000, interrupt source is C1 data 0001, interrupt source is C2 data 0010, interrupt source is C3 data 0011, interrupt source is C4 data 0100, interrupt source is C5 data 0101, interrupt source is C6 data 0110, interrupt source is C7 data 0111, interrupt source is CLEAR data 1000, interrupt source is C8 data others, reserved
1:0	RW	0x00	AINT_PRST[1:0]	For bits 1:0 = (see the followings) 00: set AINT_FLAG if 1 reading trips the threshold value 01: set AINT_FLAG if 4 readings trip the threshold value 10: set AINT_FLAG if 8 readings trip the threshold value 11: set AINT_FLAG if 16 readings trip the threshold value

Table 10. Register 0x08 (FINT_CON) – Flicker Interrupt Configuration

Bit #	Access	Default	Name	Function / Operation
7	RW	0x00	FLV_INT_EN	When = 0, interrupt pin is HZ and irrelevant to FINT_FLAG bit When = 1, interrupt pin shall react according to FINT_FLAG bit
6	RW	0x00	OVERWR_EN	When = 0, FIFO data shall be overwritten once all FIFO are filled with new data When = 1, FIFO data shall not be overwritten once all FIFO are filled with new data
5	RW	0x00	Reserved	Reserved. Write as 0

4	RW	0x00	FIFO_CAL_EN	When = 0, internal Flicker calculation is disabled When = 1, internal Flicker calculation is enabled
3	RW	0x00	FLK_INT_EN	When = 0, interrupt pin is HZ and irrelevant to CAL_INT bit When = 1, interrupt pin shall react according to CAL_INT bit
2	RW	0x00	FLK_TYPE	When = 0, Flicker detection target is not 100Hz and 120Hz When = 1, Flicker detection target is 100Hz or 120Hz
1:0	RW	0x00	FINT_PRST	For bits 1:0 = (see the followings) 00: set CAL_INT if 1 reading trips the FLK_type range 01: set CAL_INT if 2 readings trip the FLK_type range 10: set CAL_INT if 4 readings trip the FLK_type range 11: set CAL_INT if 8 readings trip the FLK_type range

Table 11. Register 0x0A (DRV_CON1) – Driver Configuration 1

Bit #	Access	Default	Name	Function / Operation
7	RW	0x00	DRV_EN	When = 0, internal driver is shut down When = 1, internal driver is enabled
6:0	RW	0x00	DRV_CUR[6:0]	These 7 bits configure driving current of internal driver. 3mA * (1+DRV_CUR[6:0]) 0000000, 3mA 0000001, 6mA …… 1111111, 384mA

Table 12. Registers 0x0B to 0x0E – Interrupt Threshold Registers for Color Sensing

Addr #	Access	Default	Name	Function / Operation
0x0B	RW	0x00	ALS_LTL	Lower byte of ambient light sensing interrupt low threshold
0x0C	RW	0x00	ALS_LTH	Upper byte of interrupt low threshold
0x0D	RW	0xFF	ALS_HTL	Lower byte of interrupt high threshold
0x0E	RW	0xFF	ALS_HTH	Upper byte of interrupt high threshold

Table 13. Register 0x0F (FLK_FIFO_TH) – FIFO Level for Interrupt

Bit #	Access	Default	Name	Function / Operation
7:0	RW	0x00	FLK_FIFO_LEVEL[7:0]	These 8 bits configure how many cycles of FIFO data are updated before FINT_FLAG is set

Table 14. Registers 0x10 to 0x2D – All Channel Output Data Registers

Addr #	Access	Default	Name	Function / Operation
0x10	RO	0x00	C1_DATAL	Lower byte of Color channel 1 data
0x11	RO	0x00	C1_DATAH	Upper byte of Color channel 1 data
0x12	RO	0x00	C2_DATAL	Lower byte of Color channel 2 data
0x13	RO	0x00	C2_DATAH	Upper byte of Color channel 2 data
0x14	RO	0x00	C3_DATAL	Lower byte of Color channel 3 data
0x15	RO	0x00	C3_DATAH	Upper byte of Color channel 3 data
0x16	RO	0x00	C4_DATAL	Lower byte of Color channel 4 data
0x17	RO	0x00	C4_DATAH	Upper byte of Color channel 4 data
0x18	RO	0x00	C5_DATAL	Lower byte of Color channel 5 data
0x19	RO	0x00	C5_DATAH	Upper byte of Color channel 5 data
0x1A	RO	0x00	C6_DATAL	Lower byte of Color channel 6 data
0x1B	RO	0x00	C6_DATAH	Upper byte of Color channel 6 data

0x1C	RO	0x00	C7_DATAL	Lower byte of Color channel 7 data
0x1D	RO	0x00	C7_DATAH	Upper byte of Color channel 7 data
0x1E	RO	0x00	CLEAR_DATAL	Lower byte of CLEAR channel data
0x1F	RO	0x00	CLEAR_DATAH	Upper byte of CLEAR channel data
0x20	RO	0x00	C8_DATAL	Lower byte of Color channel 8 data
0x21	RO	0x00	C8_DATAH	Upper byte of Color channel 8 data
0x22	RO	0x00	NIR_DATAL	Lower byte of NIR channel data
0x23	RO	0x00	NIR_DATAH	Upper byte of NIR channel data
0x2C	RO	0x00	FLK_DATAL	Lower byte of Flicker channel data
0x2D	RO	0x00	FLK_DATAH	Upper byte of Flicker channel data

Table 15. Register 0x2F (INT_FLAG) – Color Sensing Interrupt Flag

Bit #	Access	Default	Name	Function / Operation
7	RO	0x00	AINT_FLAG	When =0, no color sensing interrupt has occurred since power-on or last “clear” When =1, a color sensing interrupt event occurred
6	RO	0x00	ALS_VALID	When =0, color data is not updated after enabled or last data reading When =1, color data is updated after enabled or last data reading
5:0	RO	0x00	Unused	Unused

Table 16. Register 0x31 (FIFO_FLAG) – FIFO Flag

Bit #	Access	Default	Name	Function / Operation
7	RO	0x00	FINT_FLAG	When =0, no FIFO level interrupt has occurred since power-on or last “clear” When =1, a FIFO level interrupt event occurred
6	RO	0x00	FIFO_EMPTY	When =0, no FIFO empty interrupt has occurred since power-on or last ”clear” When =1, all data in FIFO are read and FIFO becomes empty
5	RO	0x00	FIFO_FULL	When =0, no FIFO full interrupt has occurred since power-on or last “clear” When =1, all data in FIFO are fresh that have never been accessed
4	RO	0x00	Unused	Unused
3	RO	0x00	CAL_INT	When =0, no calculation interrupt has occurred since power-on or last “clear” When =1, a calculation interrupt event occurred
2	RO	0x00	100HZ_FLAG	When =0, calculated flicker frequency is not within the range of 100Hz +/-10% When =1, calculated flicker frequency is 100Hz (tolerance is +/-10%)
1	RO	0x00	120HZ_FLAG	When =0, calculated flicker frequency is not within the range of 120Hz +/-8% When =1, calculated flicker frequency is 120Hz (tolerance is +/-8%)
0	RO	0x00	Unused	Unused

Table 17. Registers 0x30 & 0x33~0x36 – FIFO Related Registers

Addr #	Access	Default	Name	Function / Operation
0x30	RW	0x00	FIFO_LV_CNT	Number of available FIFO data samples
0x33	RW	0xAA	FIFO_R_CNT_CL	Reading this register will clear FIFO reading counter

			R	(FIFO_R_CNT) in register 0x36
0x34	RW	0x00	FIFO_DATAL	Lower byte of FIFO buffer
0x35	RW	0x00	FIFO_DATAH	Upper byte of FIFO buffer
0x36	RW	0x00	FIFO_R_CNT	Number of data samples which have been read

I²C Read / Write Register Data

The SY22312CS42-J10's I²C target address is 0x46. Figures 1 and 2 graphically depict the protocol of writing or reading register data. The first 8-bit data following the write-operation can be either the register address or special function. Referring to Table 2 for details.

A : Acknowledge (0)
NA : Not Acknowledged (1)
P : Stop Condition
R : Read (1)
W : Write (0)
S : Start Condition
Sr : Repeat Start
... : Continuation of Protocol
□ : Controller to Target
▯ : Target to Controller

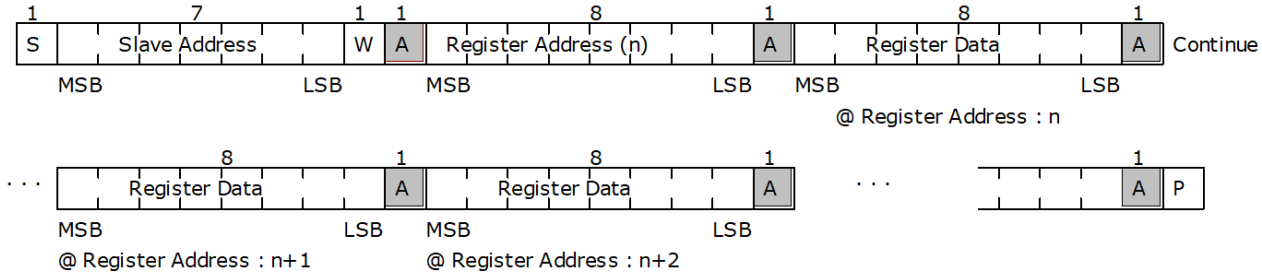


Figure 1. I²C Write-Register-Data Protocol

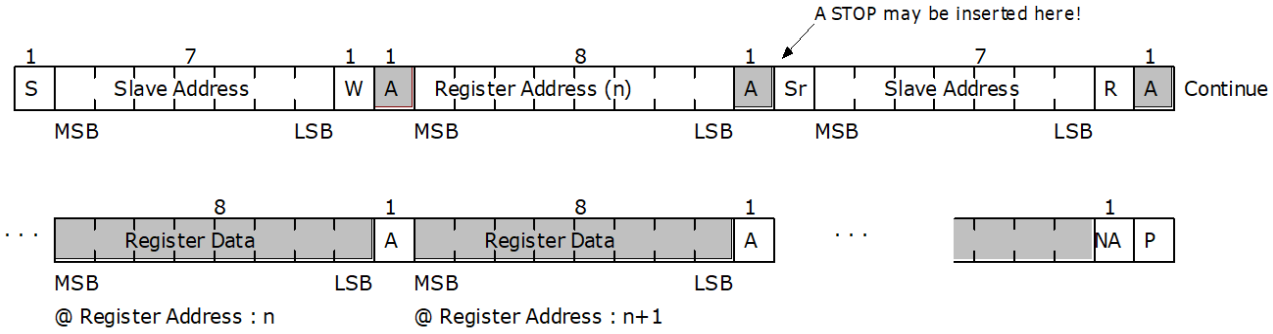
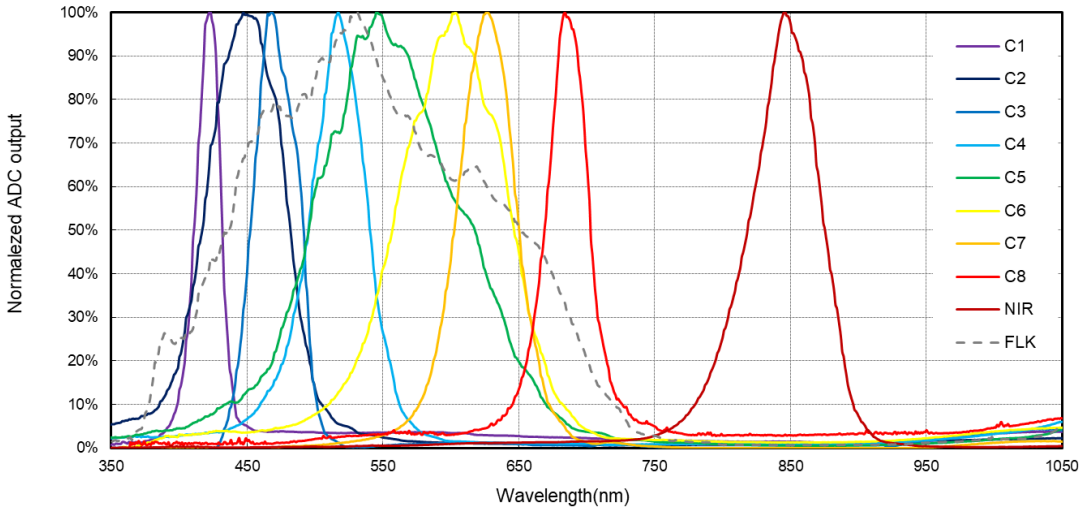


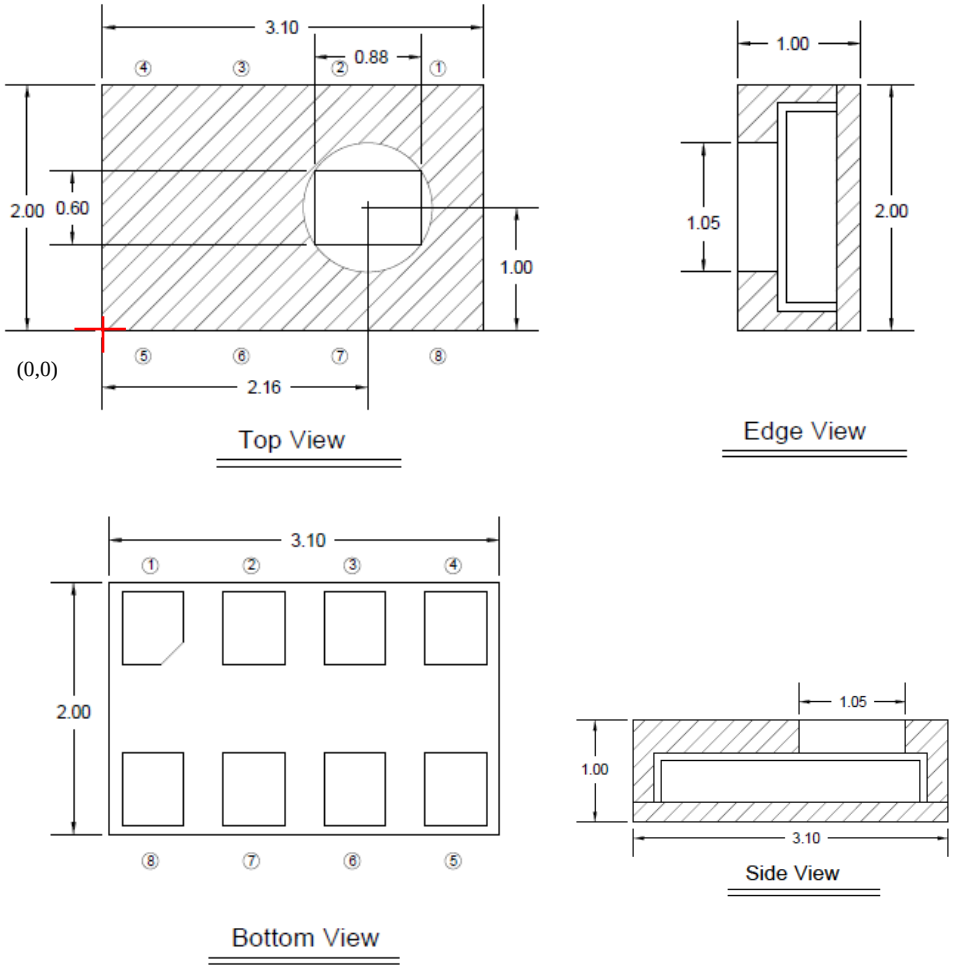
Figure 2. I²C Read-Register-Data Procotol

Typical Characteristics

Relative Spectral Response

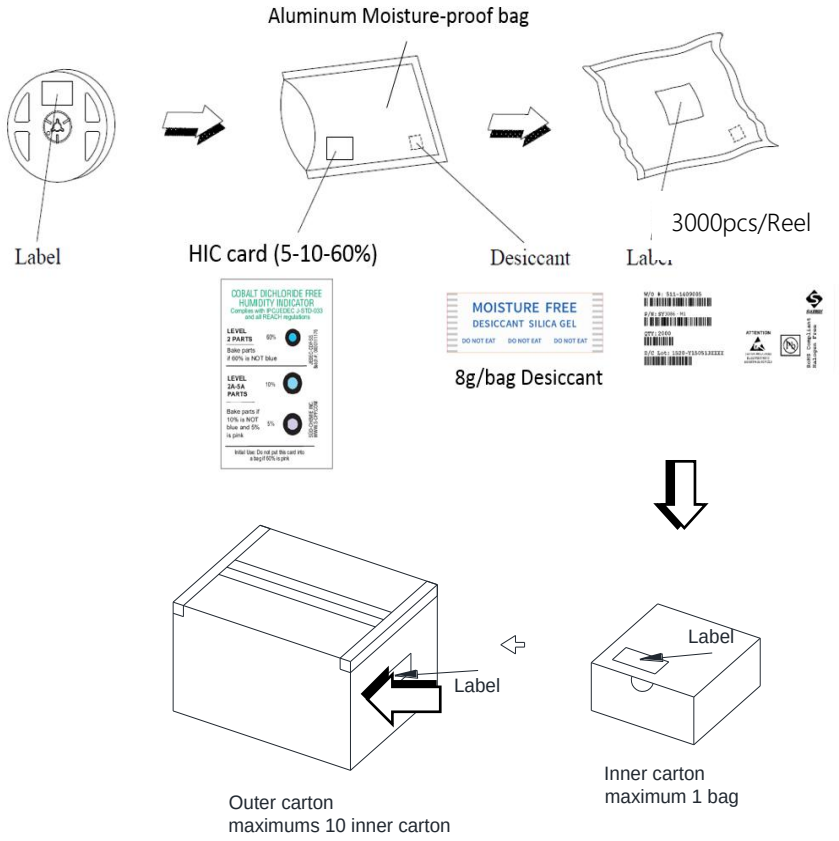


Package Outline Drawings



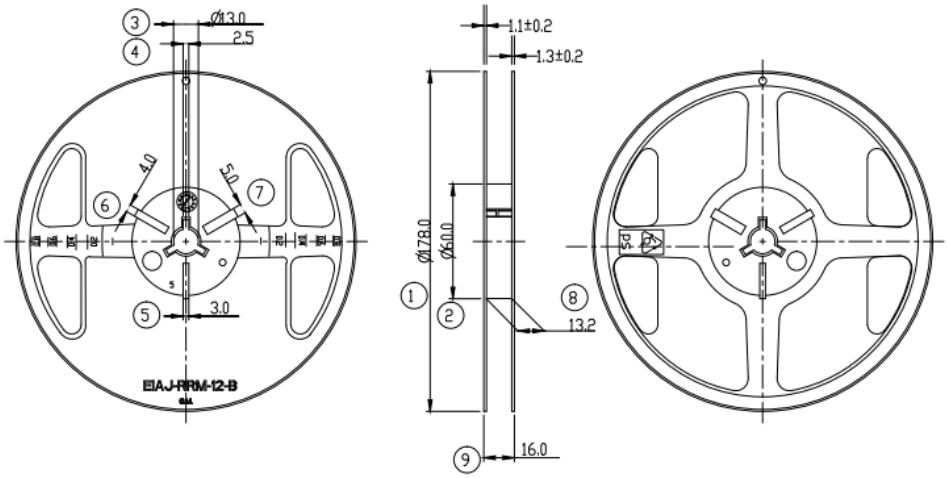
Note 1: All tolerances are ± 0.1mm, unless otherwise noted
Note 2: Sensing center is at point (x, y) = (2.16, 1.00)
Note 3: Sensing area: 880μm x 600μm
Note 4: Unit is in mm

Packaging Quantity Specifications

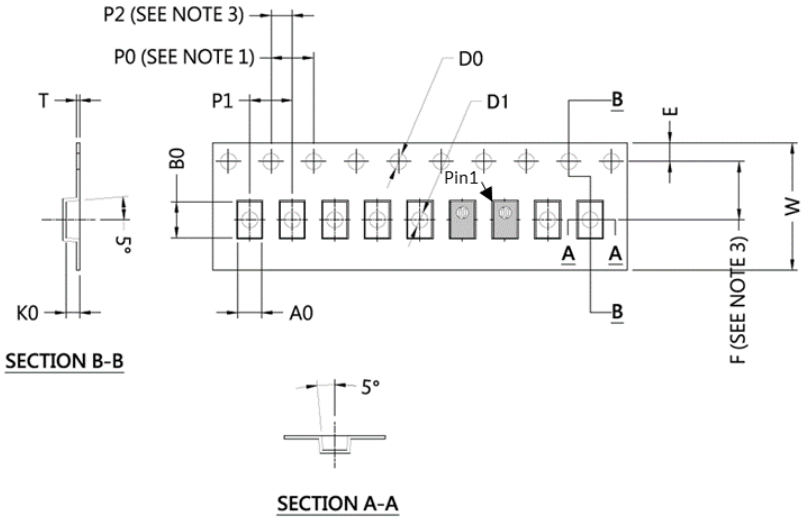


- Dimensions of Reel (Unit: mm)

Width	1	2	3	4	5	6	7	8	9
7"	178±1	60±0.5	13±0.5	2.5±0.5	$3^{+0.5}_{-0}$	$4^{+0.5}_{-0}$	$5^{+0.5}_{-0}$	13.2±1.5	16±1



- Dimensions of Tape (Unit: mm)



Item	Specification	Tol. (+/-)	Item	Specification	Tol. (+/-)
W	12.00	±0.3	P1	4.00	±0.10
E	1.75	±0.10	P2	2.00	±0.05
F	5.50	±0.05	A0	2.25	±0.10
D0	1.50	+0.1/-0.0	B0	3.40	±0.10
D1	1.50	+0.1/-0.0	K0	1.30	±0.10
P0	4.00	±0.10	T	0.30	±0.05

Recommended Method of Storage

Storage is recommended as soon as the bag has been opened to prevent moisture absorption. The following conditions should be observed if bags are not available:

- Storage temperature: 10°C to 30°C.
- Storage humidity: ≦60%RH max.
- Storage Time: ≦168hr max.

Moisture-Proof Package

To avoid moisture absorption by the resin, the product should be stored under the following conditions:

- Temperature: 23 ± 5°C.
- Relative humidity: 60% (max).
- Baking is required if the devices have been stored unopened for more than 24 months and the HIC card is not discolored.

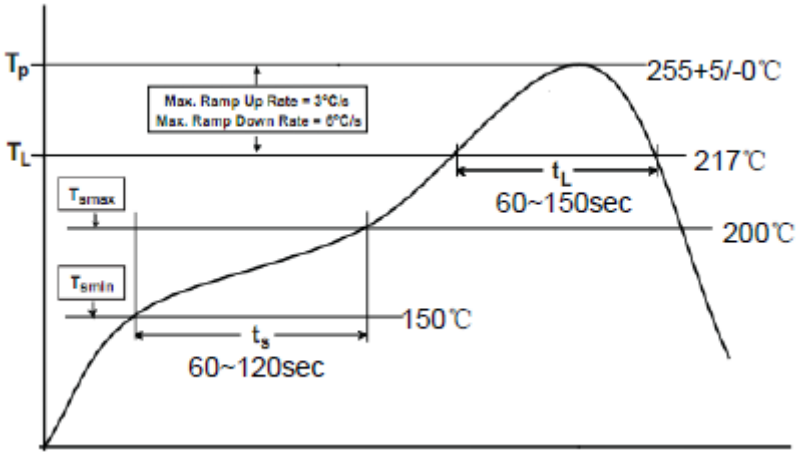
ESD Precaution

Proper storage and handling procedures should be followed to prevent ESD damage to the devices especially when they are removed from the anti-static bag. Electro-Static Sensitive Devices warning labels are on the package.

Make any necessary soldering correction manually

- Temperature shall be no more than 350°C (25W for soldering iron) within 3 seconds.
- Make sure do not do this more than one time for any given pin.

Recommended Soldering Profile



Note 1: Do not put stress on the devices during heating stage while soldering.

Note 2: Do not warp the circuit board after soldering.

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description
1.0	Dec 20, 2023	Initial Release
1.0	Nov.04,2024	Language Improvements for clarity

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