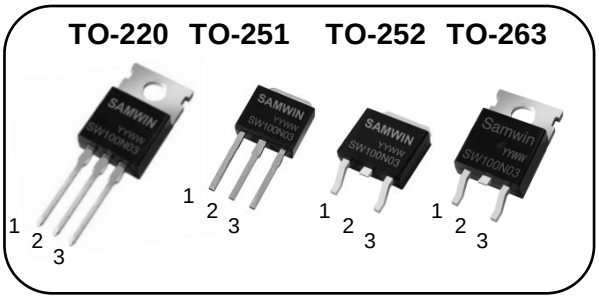
N-channel MOSFET

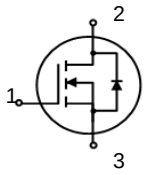
Features

- High ruggedness
- $R_{DS(ON)}$ (Max 5.3mΩ)@V_{GS}=10V
- Gate Charge (Typical 69nC)
- Improved dv/dt Capability
- 100% Avalanche Tested



1. Gate 2. Drain 3. Source

BV_{DSS} : 30V
I_D : 100A
$R_{DS(ON)}$: 5.3 mΩ



General Description

This N-channel enhancement mode field-effect power transistor using SAMWIN semiconductor's advanced planar stripe, DMOS technology intended for battery Operated systems like a DC-DC converter motor control , ups ,audio amplifier. Also, especially designed to minimize $R_{DS(ON)}$, low gate charge and high rugged avalanche characteristics.

Order Codes

Item	Sales Type	Marking	Package	Packaging
1	SW P 100N03	SW100N03	TO-220	TUBE
2	SW I 100N03	SW100N03	TO-251	TUBE
3	SW D 100N03	SW100N03	TO-252	REEL
4	SW B 100N03	SW100N03	TO-263	REEL

Absolute maximum ratings

Symbol	Parameter		Value				Unit
V_{DSS}	Drain to Source Voltage		30				V
I_D	Continuous Drain Current		100*				A
I_{DM}	Drain current pulsed	(note 1)	400*				A
V_{GS}	Gate to Source Voltage		±20				V
E_{AS}	Single pulsed Avalanche Energy	(note 2)	507				mJ
E_{AR}	Repetitive Avalanche Energy	(note 1)	39				mJ
			TO-220	TO-251	TO-252	TO-263	
P_D	Total power dissipation (@T_C=25°C)		113	96	83	96	W
	Derating Factor above 25°C		0.9	0.77	0.67	0.77	W/°C
T_{STG}, T_J	Operating Junction Temperature & Storage Temperature		-55 ~ + 150				°C
T_L	Maximum Lead Temperature for soldering purpose, 1/8 from Case for 5 seconds.		300				°C

*. Drain current is limited by junction temperature.

Thermal characteristics

Symbol	Parameter	Value				Unit
		TO220	TO251	TO252	TO263	
R_{thjc}	Thermal resistance, Junction to case	1.1	1.3	1.5	1.3	°C/W
R_{thcs}	Thermal resistance, Case to Sink	0.5	-	-	-	°C/W
R_{thja}	Thermal resistance, Junction to ambient	62.5	100	100	62.5	°C/W

Electrical characteristic (T_C = 25ºC unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Off characteristics						
BV_{DSS}	Drain to source breakdown voltage	V_{GS}=0V, I_D=250uA	30	-	-	V
ΔBV_{DSS} / ΔT_J	Breakdown voltage temperature coefficient	I_D=250uA, referenced to 25ºC	-	0.16	-	V/ºC
I_{DSS}	Drain to source leakage current	V_{DS}=30V, V_{GS}=0V	-	-	1	uA
		V_{DS}=24V, T_C=125ºC	-	-	100	uA
I_{GSS}	Gate to source leakage current, forward	V_{GS}=20V, V_{DS}=0V	-	-	100	nA
	Gate to source leakage current, reverse	V_{GS}=-20V, V_{DS}=0V	-	-	-100	nA
On characteristics						
$V_{GS(TH)}$	Gate threshold voltage	V_{DS}=V_{GS}, I_D=250uA	1.0	-	3.0	V
$R_{DS(ON)}$	Drain to source on state resistance	V_{GS}=10V, I_D = 50A	-	4.0	5.3	mΩ
Dynamic characteristics						
C_{iss}	Input capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz	-	9500	-	pF
C_{oss}	Output capacitance		-	800	-	
C_{rss}	Reverse transfer capacitance		-	300	-	
$t_{d(on)}$	Turn on delay time	V_{DS}=15V, I_D=100A, R_G=25Ω (note 4, 5)	-	14.5	50	ns
tr	Rising time		-	100	150	
$t_{d(off)}$	Turn off delay time		-	212	250	
t_f	Fall time		-	156	200	
Q_g	Total gate charge	V_{DS}=24V, V_{GS}=10V, I_D=100A, (note 4, 5)	-	69	100	nC
Q_{gs}	Gate-source charge		-	13	-	
Q_{gd}	Gate-drain charge		-	195	-	

Source to drain diode ratings characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Continuous source current	Integral reverse p-n Junction diode in the MOSFET	-	-	90	A
I_{SM}	Pulsed source current		-	-	360	A
V_{SD}	Diode forward voltage drop.	I_S=100A, V_{GS}=0V	-	-	1.5	V
T_{rr}	Reverse recovery time	I_S=100A, V_{GS}=0V, dI_F/dt=100A/us	-	12	-	ns
Q_{rr}	Reverse recovery charge		-	4.2	-	nC

※. Notes

1. Repeatitive rating : pulse width limited by junction temperature.
2. L = 105uH, I_{AS} = 100A, V_{DD} = 25V, R_G=25Ω, Starting T_J = 25ºC
3. I_{SD} ≤ 100A, di/dt = 100A/us, V_{DD} ≤ BV_{DSS}, Staring T_J =25ºC
4. Pulse Test : Pulse Width≤ 300us, duty cycle ≤ 2%
5. Essentially independent of operating temperature.

Fig. 1. Output Characteristics

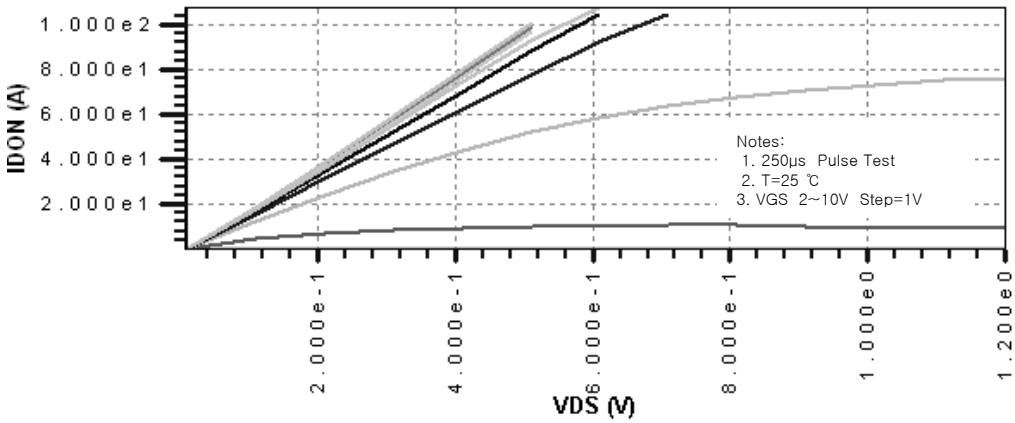


Fig. 2. Gate-Charge characteristics

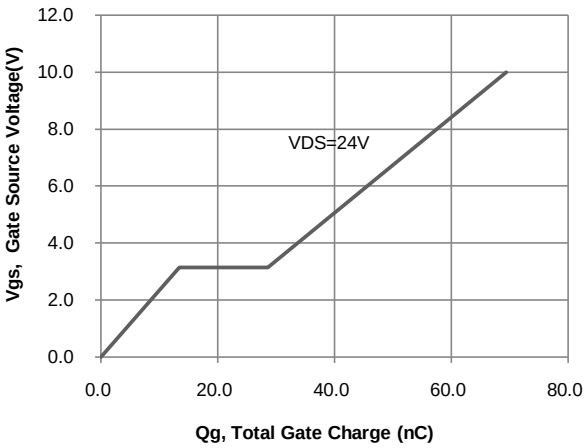


Fig. 3. On state current vs. diode forward voltage

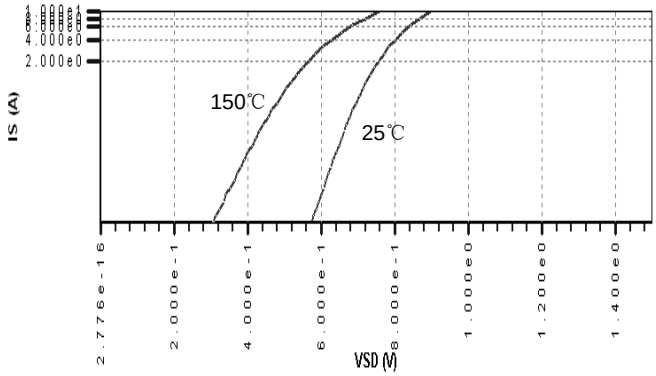


Fig 4. Breakdown Voltage Variation vs. Junction Temperature

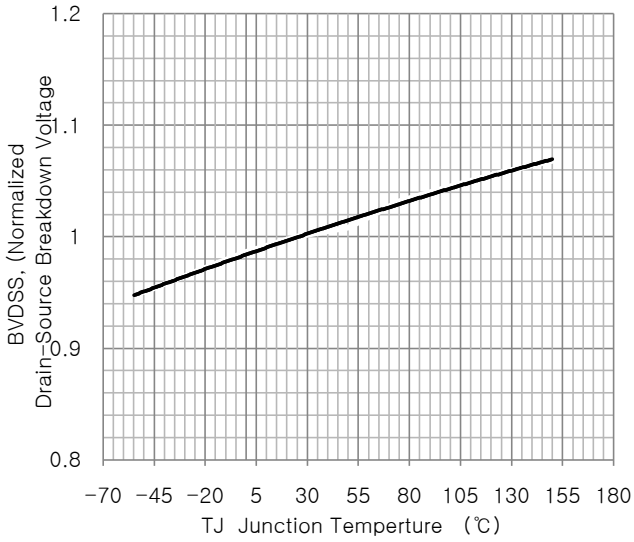


Fig. 5. On resistance variation vs. junction temperature

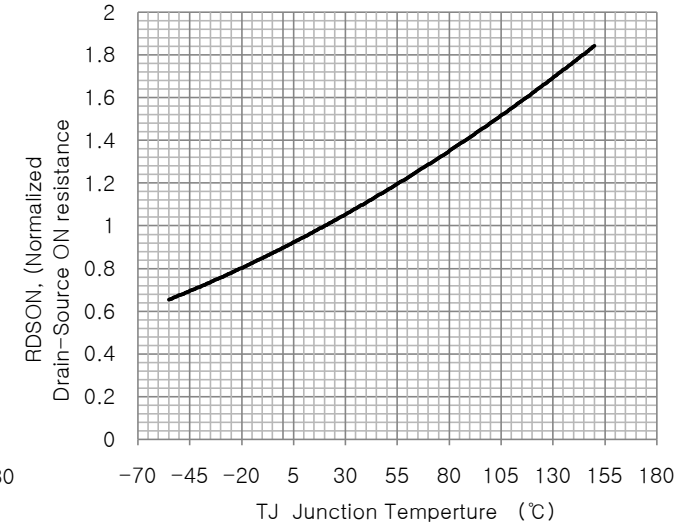


Fig. 6. Maximum Safe Operating Area

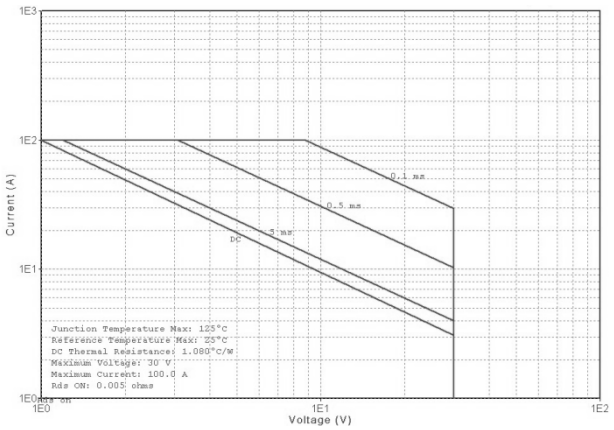


Fig. 7. Transient thermal response curve

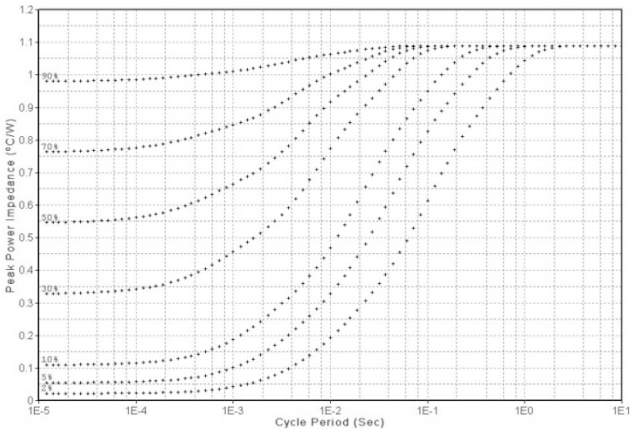


Fig. 8. Peak diode recovery dv/dt test circuit & waveform

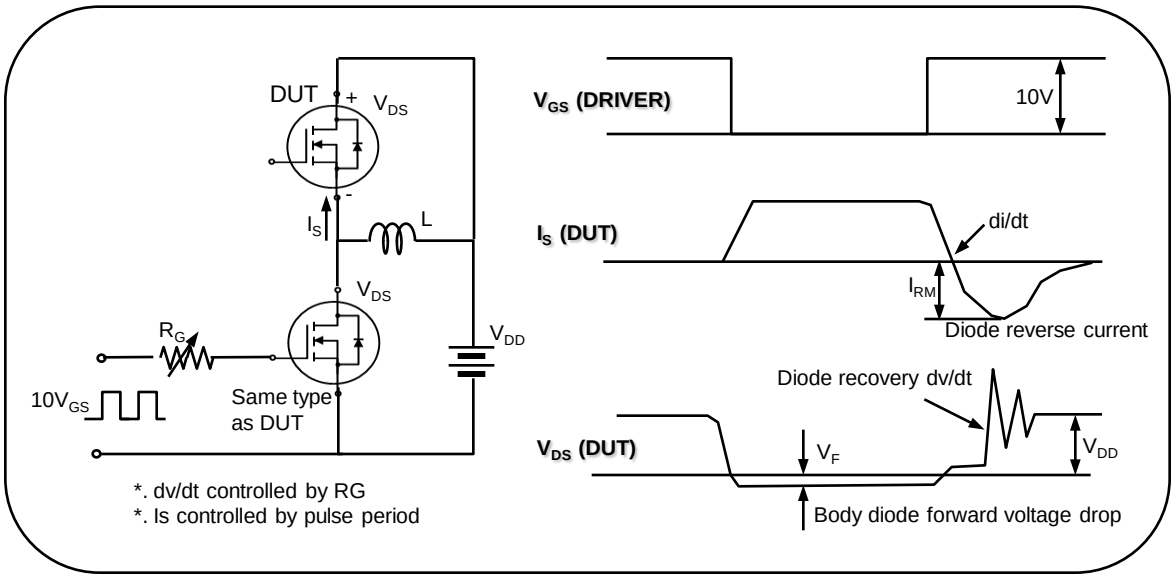


Fig. 9. Switching time test circuit & waveform

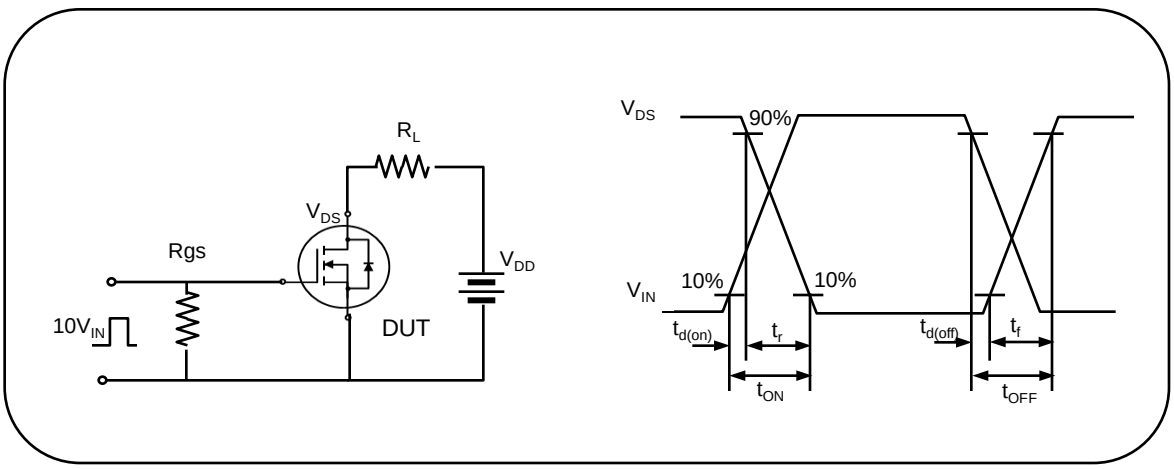


Fig. 10. Unclamped Inductive switching test circuit & waveform