

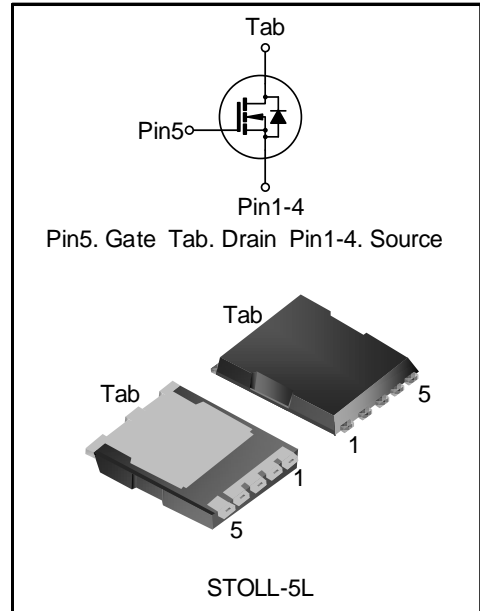
255A, 40V N-CHANNEL MOSFET

DESCRIPTION

SVGQ041R2NLS-2HF is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan's LVMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance and high avalanche breakdown tolerance.

FEATURES

- ◆ Compliant with AEC-Q101 standards.
- ◆ 255A, 40V, $R_{DS(on)(typ.)}=1.0m\Omega@V_{GS}=10V$
- ◆ Low gate charge
- ◆ Low C_{rss}
- ◆ Fast switching
- ◆ Extreme dv/dt rated
- ◆ 100% avalanche tested
- ◆ Pb-free lead plating
- ◆ RoHS compliant
- ◆ Max. junction temperature: $T_{jmax.}=175\text{ }^{\circ}C$



KEY PERFORMANCE PARAMETERS

Characteristics	Ratings	Unit
V_{DS}	40	V
$V_{GS(th)}$	2.4~3.4	V
$R_{DS(on),max}$	1.2	$m\Omega$
I_D	255	A
$Q_{g,typ}$	66	nC

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVGQ041R2NLS-2HFTR	STOLL-5L	Q41R2-2HF	Halogen free	Tape & Reel

ABSOLUTE MAXIMUM RATINGS (UNLESS OTHERWISE NOTED, T_J=25°C)

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Gate-source Voltage	V _{GS}	--	-20	--	20	V
Drain Current (Note 1)	I _D	T _C =25°C	--	--	255	A
		T _C =100°C	--	--	180	A
Drain Current Pulsed (Note 2)	I _{DM}	T _C =25°C	--	--	1020	A
Power Dissipation (Note 3)	P _D	T _C =25°C	--	--	150	W
Single Pulsed Avalanche Energy	E _{AS}	L=0.1mH, V _{DD} =32V, R _G =25Ω, starting temperature T _J =25°C	--	--	281	mJ
Single Pulsed Avalanche Current	I _{AS}	--	--	--	75	A
Operation Junction Temperature Range	T _J	--	-55	--	175	°C
Storage Temperature Range	T _{stg}	--	-55	--	175	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Thermal Resistance, Junction-case, Bottom	R _{θJC}	--	--	--	1.0	°C/W
Thermal Resistance, Junction-ambient	R _{θJA}	--	--	--	60	°C/W
Soldering Temperature(SMD)	T _{sold}	Reflow soldering: 10±1 sec, 3times	--	--	260	°C

ELECTRICAL CHARACTERISTICS (UNLESS OTHERWISE NOTED, $T_J=25^{\circ}\text{C}$)

Static characteristics

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Drain-source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	40	--	--	V
Drain-source Leakage Current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V, T_J=25^{\circ}\text{C}$	--	--	1.0	μA
		$V_{DS}=40V, V_{GS}=0V, T_J=150^{\circ}\text{C}$	--	12	--	
Gate-source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	--	--	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	2.4	--	3.4	V
Static Drain-source On State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=90A$	--	1.0	1.2	m Ω
Gate Resistance	R_g	$f=1\text{MHz}$	--	3.1	--	Ω

Dynamic characteristics

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Input Capacitance	C_{iss}	$f=1\text{MHz}, V_{GS}=0V, V_{DS}=25V$	--	4020	--	pF
Output Capacitance	C_{oss}		--	1143	--	
Reverse Transfer Capacitance	C_{rss}		--	39	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=20V, V_{GS}=10V, R_G=3.5\Omega, I_D=90A$ (Notes 4, 5)	--	18	--	ns
Turn-on Rise Time	t_r		--	30	--	
Turn-off Delay Time	$t_{d(off)}$		--	49	--	
Turn-off Fall Time	t_f		--	26	--	
Total Gate Charge	Q_g	$V_{DD}=32V, V_{GS}=10V, I_D=90A$ (Notes 4, 5)	--	66	--	nC
Gate-source Charge	Q_{gs}		--	23	--	
Gate-drain Charge	Q_{gd}		--	19	--	
Gate-plateau Voltage	$V_{plateau}$		--	5.5	--	V

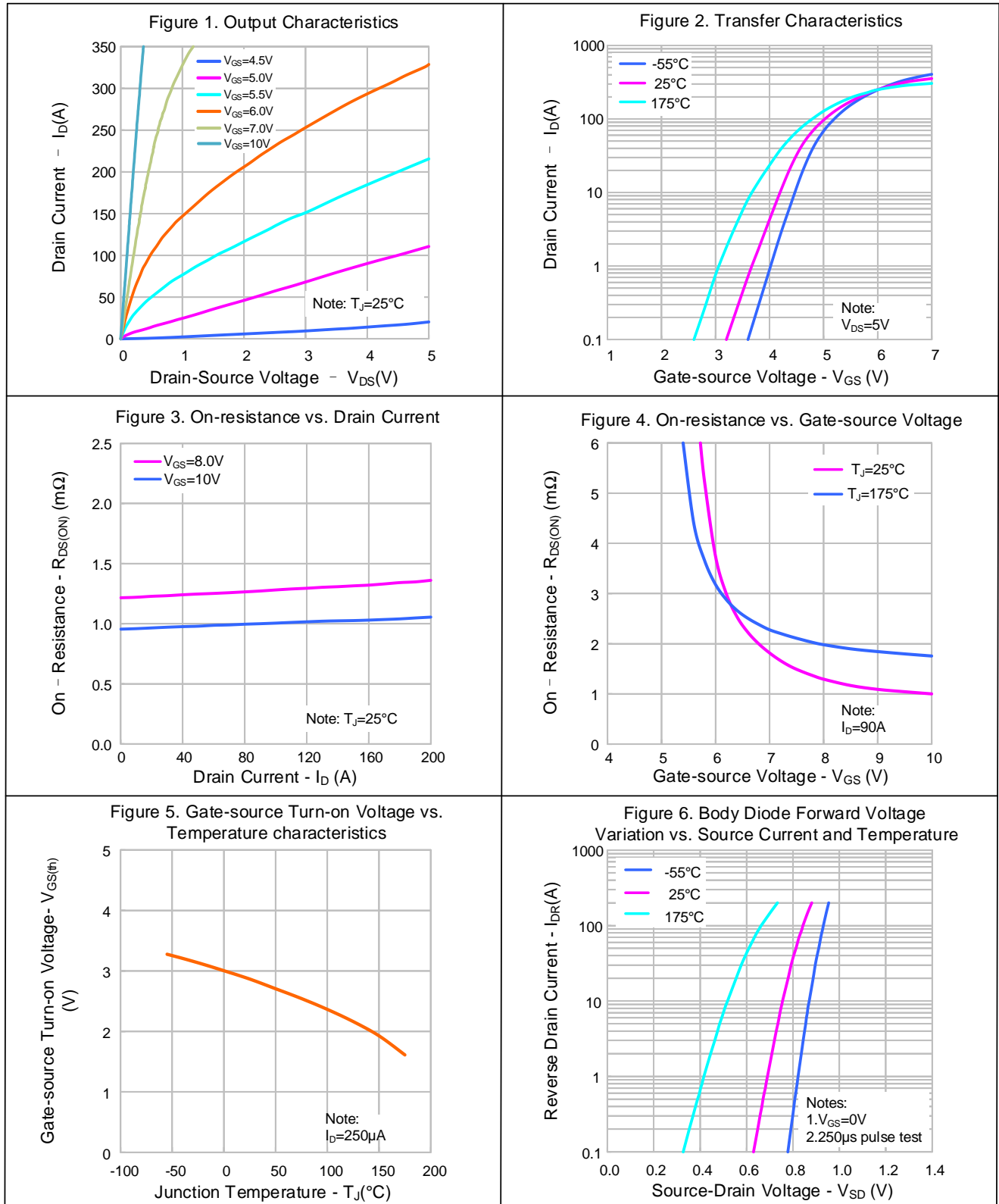
Reverse diode characteristics

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Diode Forward Current	I_S	Integral reverse P-N junction diode in the MOSFET	--	--	255	A
Diode Pulse Current	$I_{S,pulse}$		--	--	1020	
Source-Drain Diode Voltage Drop	V_{SD}	$I_S=90A, V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	T_{rr}	$I_S=50A, V_{GS}=0V, V_R=40V$	--	62	--	ns
Reverse Recovery Charge	Q_{rr}	$dI_F/dt=100A/\mu s$ (Note 4)	--	74	--	nC

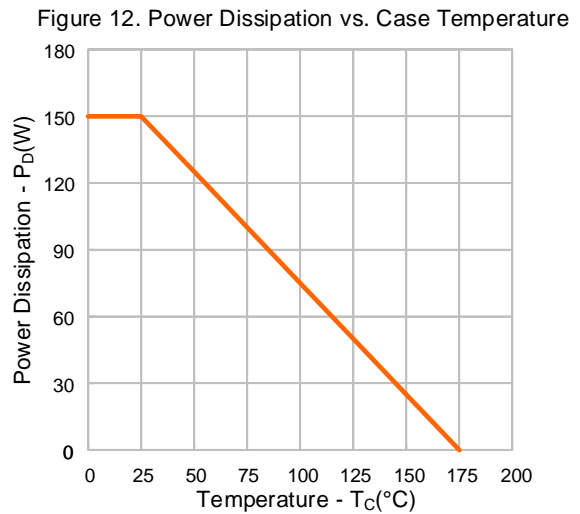
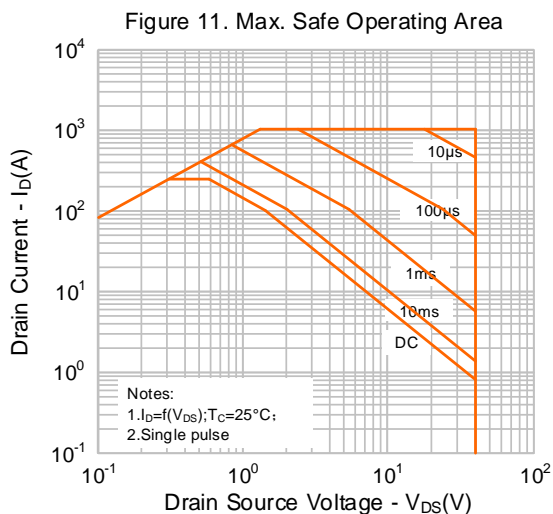
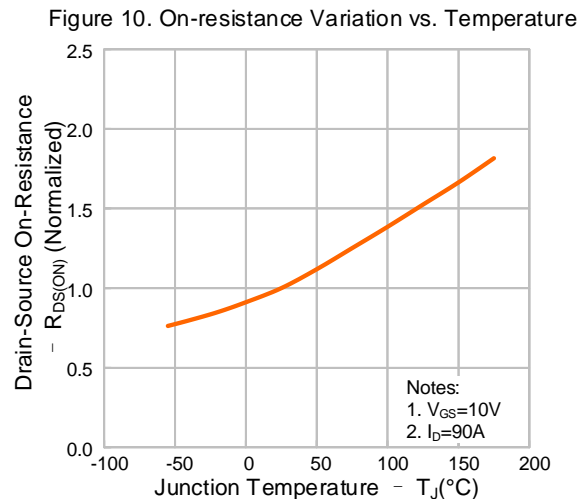
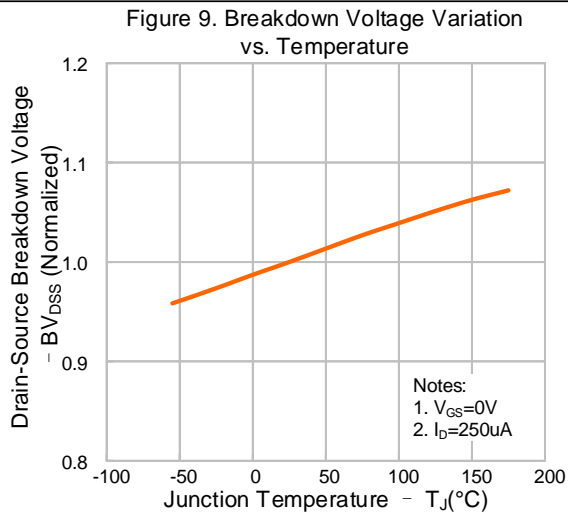
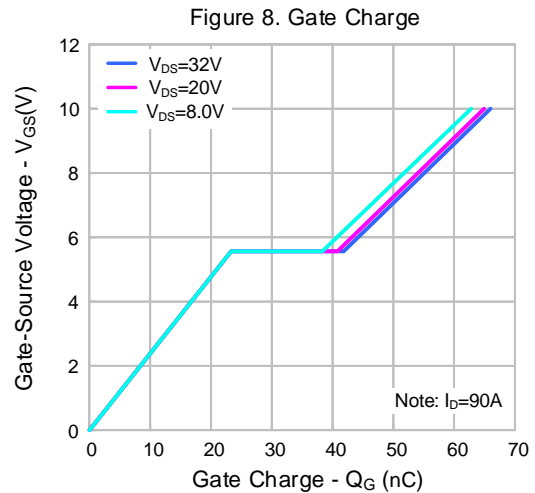
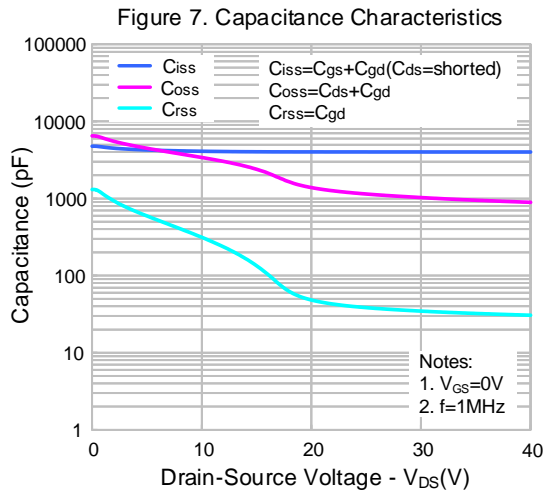
Notes:

- The rated value only refers to the maximum absolute value at the case temperature of 25°C in the specification. If the case temperature is higher than 25°C , it should be derated according to the actual environmental conditions;
- Pulse time $5\mu s$;
- The dissipation power will change with temperature, derating above 25°C : $1.0W/^{\circ}\text{C}$;
- Pulse Test: Pulse width $\leq 300\mu s$, Duty cycles $\leq 2\%$;
- Essentially independent of operating temperature.

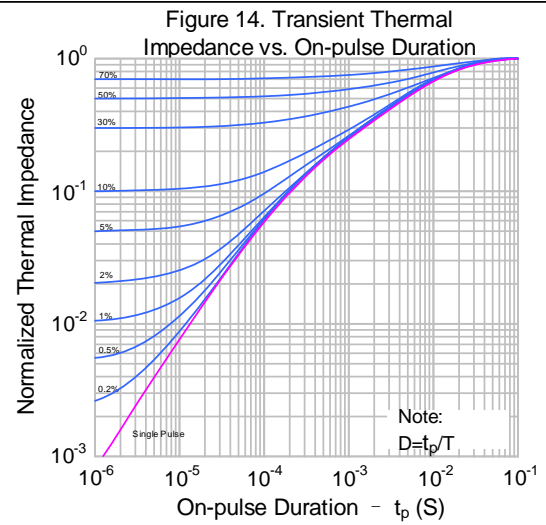
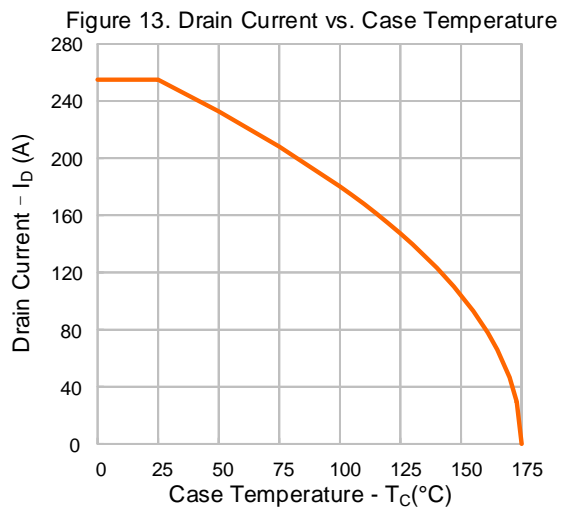
TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS (CONTINUED)

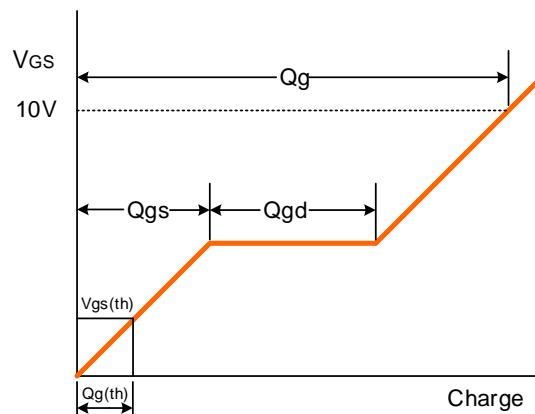
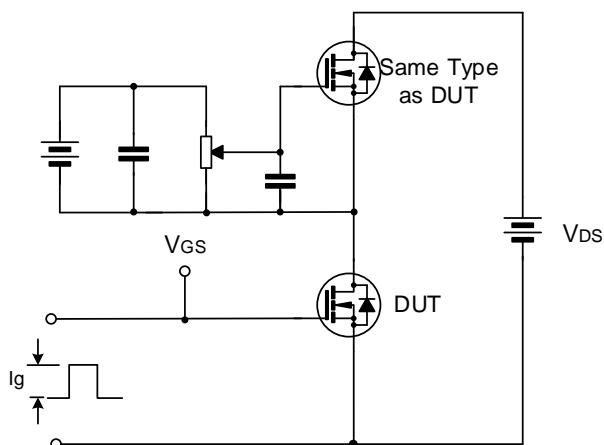


TYPICAL CHARACTERISTICS (CONTINUED)

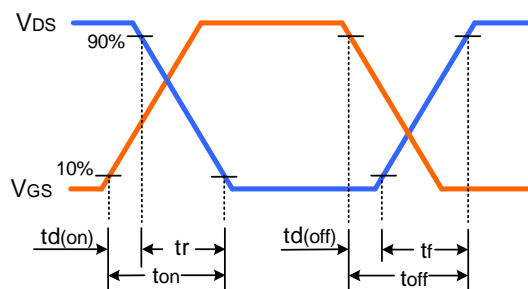
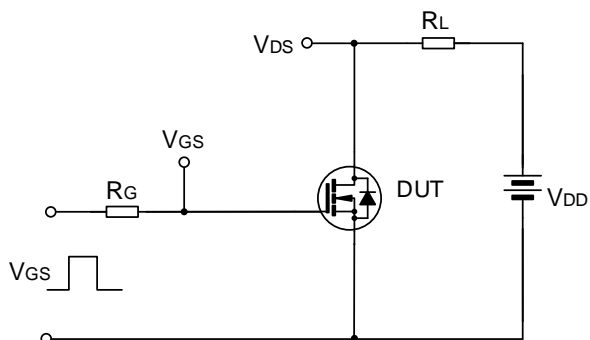


TYPICAL TEST CIRCUIT

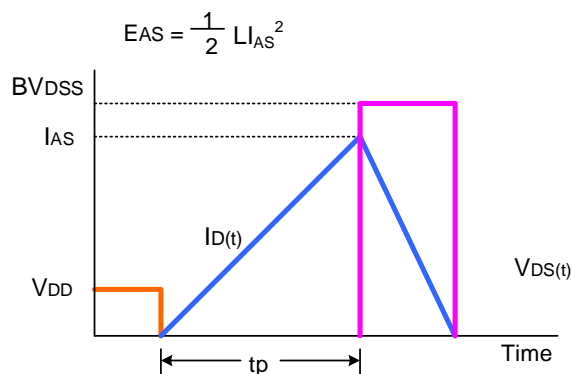
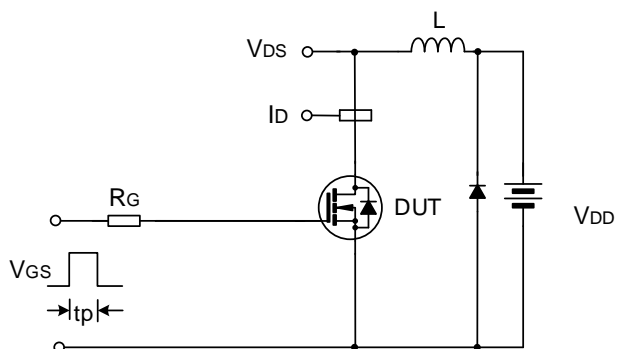
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



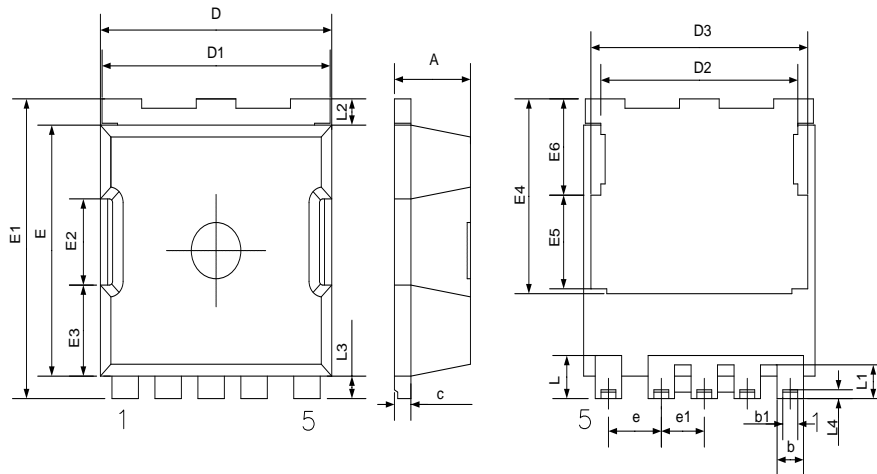
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

STOLL-5L

UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.15	2.30	2.45
b	0.70	0.80	0.90
b1	0.40	0.45	0.50
c	0.45	0.50	0.60
D	6.80	7.00	7.20
D1	6.75	6.90	7.05
D2	5.96 BSC		
D3	6.56 BSC		
E	6.50	6.70	6.90
E1	7.80	8.00	8.20
E2	2.15	2.30	2.45
E3	2.43 BSC		
E4	5.20 BSC		
E5	2.50 BSC		
E6	2.57 BSC		
e	1.60 BSC		
e1	1.30 BSC		
L	0.95	1.15	1.35
L1	0.80	0.90	1.00
L2	0.50	0.70	0.90
L3	0.45	0.60	0.75
L4	0.10	0.235	0.37



MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

Important notice:

1. Silan reserves the right to make changes of this instruction without notice.
2. Customers should obtain the latest relevant information when purchasing and should verify whether such information is latest and complete. Please read this instruction and application manual and related materials carefully before using products, including the circuit operation precautions, etc.
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Rev.: 1.2

Revision History:

1. Update features
 2. Update the curve
-

Rev.: 1.1

Revision History:

1. Update package stereogram
 2. Update important notice
-

Rev.: 1.0

Revision History:

1. First release
-
-