

# 87A, 150V N-CHANNEL MOSFET

### **DESCRIPTION**

SVGP159R3NL5A(L5) is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan's LVMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance.

This device is widely used in power management for UPS and Inverter Systems.

#### **FEATURES**

- 87A, 150V,  $R_{DS(on)(typ.)}$ =7.9m $\Omega@V_{GS}$ =10V
- Low gate charge
- Low Crss
- Fast switching
- Extreme dv/dt rated
- 100% avalanche tested
- Pb-free lead plating
- RoHS compliant

# PDFN-8-5×6×0.9-1.27

## **KEY PERFORMANCE PARAMETERS**

Characteristics	Ratings	Unit
V <sub>DS</sub>	150	V
V <sub>GS(th)</sub>	3.0~4.6	V
R <sub>DS(on),max.</sub>	9.3	mΩ
I <sub>D.pulse</sub>	87	Α
Q <sub>g.typ.</sub>	40	nC

#### **ORDERING INFORMATION**

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVGP159R3NL5ATR	DFN-8-5X6X0.9-1.27	P159R3N	Halogen free	Tape&reel
SVGP159R3NL5TR	PDFN-8-5X6X0.95-1.27	P159R3NL5	Halogen free	Tape&reel

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# ABSOLUTE MAXIMUM RATINGS (UNLESS OTHERWISE NOTED, TJ=25°C)

Obanastanistica	Comple ed	vmbol Test conditions	Ratings			- Unit	
Characteristics	Symbol Test conditions		Min.	Тур.	Max.	Oille	
Drain-source Voltage	$V_{DS}$		150			V	
Gate-source Voltage	$V_{GS}$		-20		20	V	
Drain Current (Note 1)	ı	T <sub>C</sub> =25°C			87	Α	
Drain Current (Note 1)	I <sub>D</sub>	T <sub>C</sub> =100°C			55	Α	
Drain Current Pulsed (Note 2)	I <sub>DM</sub>	T <sub>C</sub> =25°C			348	Α	
Power Dissipation (Note 3)	P <sub>D</sub>	T <sub>C</sub> =25°C			142	W	
Single Pulsed Avalanche Energy	E <sub>AS</sub>	L=0.5mH, $V_{DD}$ =50V, $R_{G}$ =25 $\Omega$ , starting temperature $T_{J}$ =25 $^{\circ}$ C			193	mJ	
Single Pulsed Avalanche Current	I <sub>AS</sub>				27.8	А	
Operation Junction Temperature Range	TJ		-55		150	°C	
Storage Temperature Range	T <sub>stg</sub>		-55		150	°C	

## THERMAL CHARACTERISTICS

Characteristics	Symbol	Test conditions	Ratings			Unit
	Symbol		Min.	Тур.	Max.	Offic
Thermal Resistance,	D				0.88	°C/W
Junction-case, Bottom	$R_{\theta JC}$					
Thermal Resistance,	5				50	0000
Junction-ambient	$R_{\theta JA}$				50	°C/W
Soldering Temperature	т	T <sub>sold</sub> Reflow soldering: 10±1 sec, 3times	1		260	°C
(SMD)	I sold					

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# ELECTRICAL CHARACTERISTICS (UNLESS OTHERWISE NOTED, TJ=25°C)

#### Static characteristics

Characteristics	Cumbal	Symbol Test conditions		Ratings			
Characteristics	Syllibol	rest conditions	Min.	Тур.	Max.	Unit	
Drain-source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	150			V	
Drain-source Leakage Current	1	V <sub>DS</sub> =150V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C			1.0	^	
	I <sub>DSS</sub>	V <sub>DS</sub> =150V, V <sub>GS</sub> =0V, T <sub>J</sub> =125°C		5.0		μΑ	
Gate-source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			±100	nA	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}$ , $I_{D}=250\mu A$	3.0		4.6	V	
Static Drain-source	D	V <sub>GS</sub> =10V, I <sub>D</sub> =44A		7.9	9.3	mΩ	
On State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =8V, I <sub>D</sub> =22A		8.7	10.5	11122	
Transconductance	g <sub>fs</sub>	V <sub>DS</sub> =2V, I <sub>D</sub> =20A		41		S	
Gate Resistance	R <sub>G</sub>	f=1MHz		1.6		Ω	

### **Dynamic characteristics**

Chamatanistica	Sumbol	Symbol Test conditions		Ratings		
Characteristics	Symbol			Тур.	Max.	Unit
Input Capacitance	C <sub>iss</sub>			2800		
Output Capacitance	C <sub>oss</sub>	f=1MHz, V <sub>GS</sub> =0V, V <sub>DS</sub> =75V		710		pF
Reverse Transfer Capacitance	C <sub>rss</sub>			17		
Turn-on Delay Time	t <sub>d(on)</sub>	V 75V V 40V D 00		24		
Turn-on Rise Time	t <sub>r</sub>	$V_{DD}$ =75V, $V_{GS}$ =10V, $R_{G}$ =3 $\Omega$ ,		91		
Turn-off Delay Time	t <sub>d(off)</sub>	I <sub>D</sub> =44A		27		ns
Turn-off Fall Time	t <sub>f</sub>	(Notes 4,5)		32		
Total Gate Charge	$Q_g$			40		
Gate-source Charge	Q <sub>gs</sub>	V <sub>DD</sub> =75V, V <sub>GS</sub> =10V, I <sub>D</sub> =44A		23		nC
Gate-drain Charge	$Q_{gd}$	(Notes 4,5)		6.6		
Gate-plateau Voltage	V <sub>plateau</sub>			7.3		V

### Reverse diode characteristics

Characteristics	Cumbal	Symbol Test conditions		Ratings			
Gnaracteristics	Symbol Test conditions		Min.	Тур.	Max.	Unit	
Continuous Source Current	Is	T <sub>C</sub> =25°C, Integral Reverse P-N			87	^	
Diode pulse current	I <sub>S,pulse</sub>	Junction Diode in the MOSFET			348	A	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =44A, V <sub>GS</sub> =0V			1.4	V	
Reverse Recovery Time	Trr	I <sub>S</sub> =44A, V <sub>GS</sub> =0V,		48		ns	
Reverse Recovery Charge	Qrr	dIF/dt=100A/µs (Note 4)		58		nC	

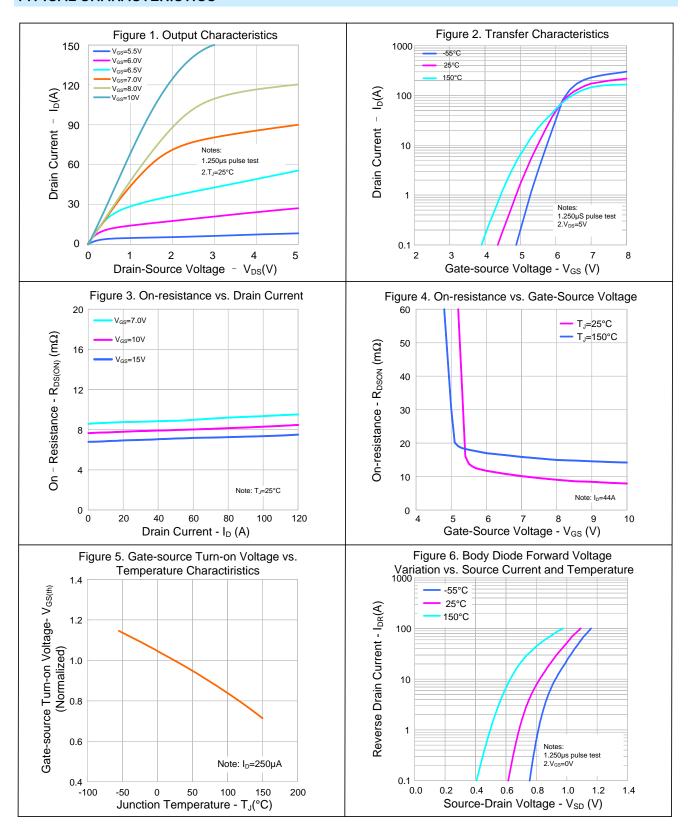
### Notes:

- 1. The rated value only refers to the maximum absolute value at the case temperature of 25°C in the specification. If the case temperature is higher than 25°C, it should be derated according to the actual environmental conditions;
- 2. Pulse time 5µs, pulse width is limited by the maximum junction temperature;
- The dissipation power will change with temperature, derating above 25°C: 1.14W/°C; 3.
- 4. Pulse Test: Pulse width ≤300µs, Duty cycle≤2%;
- 5. Essentially independent of operating temperature.

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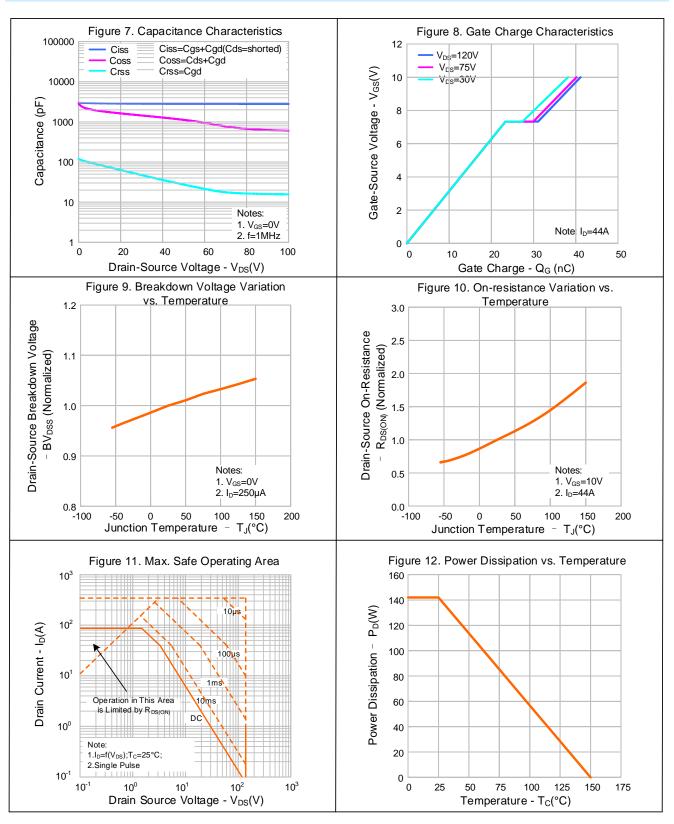
#### TYPICAL CHARACTERISTICS



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## **TYPICAL CHARACTERISTICS (CONTINUED)**

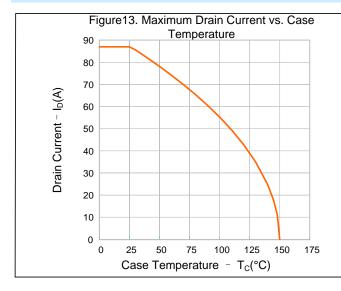


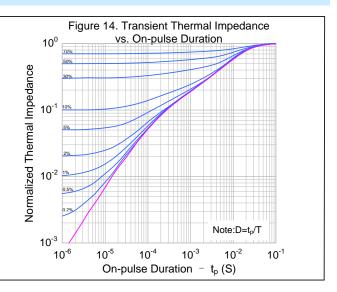
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# **TYPICAL CHARACTERISTICS (CONTINUED)**



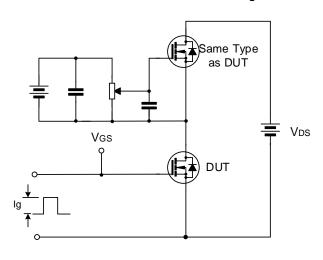


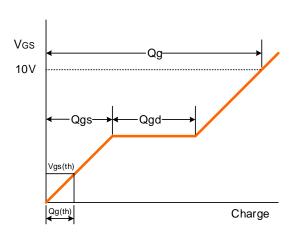
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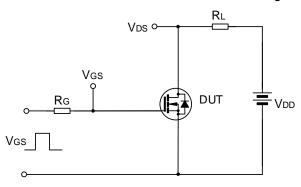
## **TYPICAL TEST CIRCUIT**

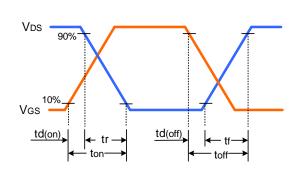
## Gate Charge Test Circuit & Waveform



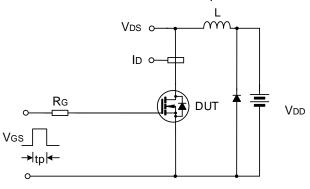


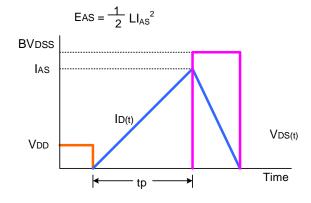
## Resistive Switching Test Circuit & Waveform





# Unclamped Inductive Switching Test Circuit & Waveform





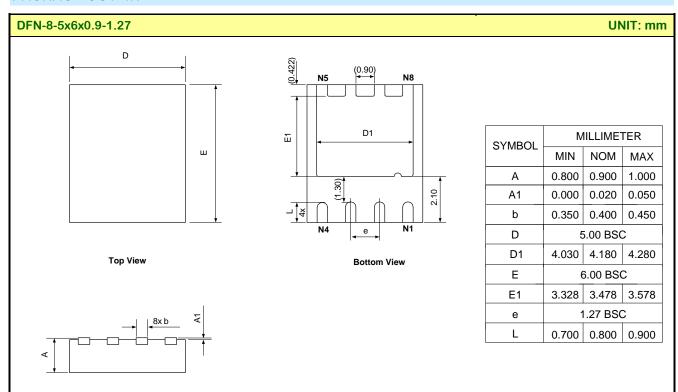
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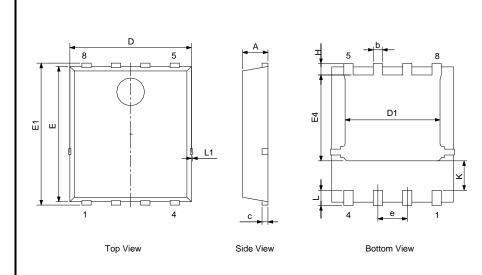
Side View

# SVGP159R3NL5A(L5)\_Datasheet

#### **PACKAGE OUTLINE**



PDFN-8-5x6x0.95-1.27 **UNIT: mm** 



SYMBOL	MI	LLIMETE	R
STIVIBUL	MIN NOM		MAX
Α	0.90	_	1.20
С	0.154	0.25	0.354
D	4.80	_	5.40
Е	5.66		6.06
D1	3.76	_	4.30
E1	5.90	_	6.35
b	0.30	_	0.55
K	1.10	1.30	1.50
е	1.07	1.27	1.37
E4	3.34		3.92
L	0.30	0.60	0.71
L1			0.12
Н	0.40	_	0.71

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## **MOS DEVICES OPERATE NOTES:**

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

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#### Important notice:

- Silan reserves the right to make changes of this instruction without notice.
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Rev.: 1.5

Revision History:

- 1. Delete the wave soldering condition
- 2. Update the typical test circuit
- 3. Update the important notice

Rev.: 1.4

Revision History:

- 1. Update SOA
- 2. Update important notice

Rev.: 1.3

Revision History:

1. Add package of SVGP159R3NL5(PDFN-8-5x6x0.95-1.27)

Rev.: 1.2

Revision History:

1. Update package outline

Rev.: 1.1 Revision History:

- 1. Update electrical characteristics
- 2. Update figure 5 and figure 13

Rev.: 1.0

Revision History:

1. First release

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