

100A, 150V N-CHANNEL MOSFET

DESCRIPTION

SVGP157R5NT(P7) is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan's LVMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance.

This device is widely used in power management for UPS and Inverter Systems.

FEATURES

- 100A, 150V, $R_{DS(on)(typ.)}$ =6.2m $\Omega@V_{GS}$ =10V
- Low gate charge
- Low Crss
- Fast switching
- Extreme dv/dt rated
- 100% avalanche tested
- Pb-free lead plating
- · RoHS compliant

FEATURES

Characteristics	Ratings	Unit
V _{DS}	150	V
V _{GS(th)}	2.0~4.0	V
R _{DS(on),max.}	7.5	mΩ
I _D	100	А
Q _{g.typ.}	74	nC

1 2 3 TO-220-3L 1 2 3 TO-247-3L

ORDERING INFORMATION

Part No.	Package	Marking Hazardous Substance Control		Packing Type
SVGP157R5NT	TO-220-3L	P157R5NT	Halogen free	Tube
SVGP157R5NP7	TO-247-3L	P157R5	Halogen free	Tube

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ABSOLUTE MAXIMUM RATINGS (UNLESS OTHERWISE NOTED, TJ=25°C)

Chamastanistica	Symbol Test conditions	Ratings			Unit		
Characteristics	Symbol Test conditions		Min.	Тур.	Max.	Oille	
Drain-source Voltage	V_{DS}		150			V	
Gate-source Voltage	V_{GS}		-20		20	V	
Drain Current		T _C =25°C			100	Α	
Drain Current	I _D	T _C =100°C			63	Α	
Drain Current Pulsed (Note 1)	I _{DM}	T _C =25°C			400	Α	
Power Dissipation (Note 2)	P_D	T _C =25°C			260	W	
Single Duleed Avelenabe Energy	F	$L=0.5 mH, V_{DD}=100 V, R_G=25 \Omega,$			825	mJ	
Single Pulsed Avalanche Energy	E _{AS}	starting temperature T _J =25°C					
Single Pulsed Avalanche Current	I _{AS}				57.4	Α	
Operation Junction	T_J		-55		150	Ŝ	
Temperature Range	IJ		-35		150	J	
Storage Temperature Range	T_{stg}		-55		150	°C	

THERMAL CHARACTERISTICS

Characteristics	Symbol	ool Test conditions	Ratings			Unit
Characteristics	Test conditions		Min.	Тур.	Max.	Oill
Thermal Resistance,	$R_{ heta JC}$				0.48	°C/W
Junction-case, Bottom	NθJC				0.46	-C/VV
Thermal Resistance,	В				62.5	°C/W
Junction-ambient	$R_{\theta JA}$				02.5	-0/٧٧
Soldering Temperature (in line)	T _{sold}	15 ⁺² ₋₀ sec, 1time			260	°C

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ELECTRICAL CHARACTERISTICS (UNLESS OTHERWISE NOTED, TJ=25°C)

Static characteristics

Characteristics	Symbol	Symbol Test conditions		Ratings		
Onaracteristics	Symbol Test conditions		Min.	Тур.	Max.	Unit
Drain-source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	150			V
Drain-source Leakage Current	1	V _{DS} =150V, V _{GS} =0V, T _J =25°C		1	1.0	
	I _{DSS}	V _{DS} =150V, V _{GS} =0V, T _J =125°C		10		μΑ
Gate-source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V		1	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}$, $I_{D}=250\mu A$	2.0	1	4.0	V
Static Drain-source	D-ac	V _{GS} =10V, I _D =100A		6.2	7.5	mΩ
On State Resistance	R _{DS(on)}	V _{GS} =8V, I _D =50A		6.4	7.7	mΩ
Gate Resistance	R_{G}	f=1MHz		4.6		Ω

Dynamic characteristics

Characteristics	Cumbal	Test conditions	Ratings		Unit		
Characteristics	Symbol	Symbol Test conditions		Тур.	Max.	Oille	
Input Capacitance	C _{iss}			5223			
Output Capacitance	Coss	f=1MHz, V _{GS} =0V, V _{DS} =75V		689		pF	
Reverse Transfer Capacitance	C _{rss}			14			
Turn-on Delay Time	t _{d(on)}	V 75V V 40V		23			
Turn-on Rise Time	t _r	V_{DD} =75V, V_{GS} =10V,		48			
Turn-off Delay Time	t _{d(off)}	$R_G=1.6\Omega$, $I_D=50A$		61		ns	
Turn-off Fall Time	t _f	(Notes 3,4)		22			
Total Gate Charge	Qg			74			
Gate-source Charge	Q _{gs}	V _{DD} =75V, V _{GS} =10V, I _D =100A		34		nC	
Gate-drain Charge	Q_{gd}	(Notes 3,4)		13			
Gate-plateau Voltage	V _{plateau}			6.5		V	

Reverse diode characteristics

Characteristics	Symbol	Symbol Test conditions		Ratings		
Characteristics	Symbol	rest conditions	Min.	Тур.	Max.	Unit
Continuous Diode		T 0500 into and account B.N.			100	
Forward Current	I _S	T _C =25°C, integral reverse P-N			100	Α
Diode Pulse Current	I _{S,pulse}	junction diode in the MOSFET			400	
Diode Forward Voltage	V_{SD}	I _S =100A, V _{GS} =0V			1.4	V
Reverse Recovery Time	T _{rr}	I _S =100A, V _{GS} =0V, dI _F /dt=100A/μs		119		ns
Reverse Recovery Charge	Q _{rr}	(Note 3)		421		nC

Notes:

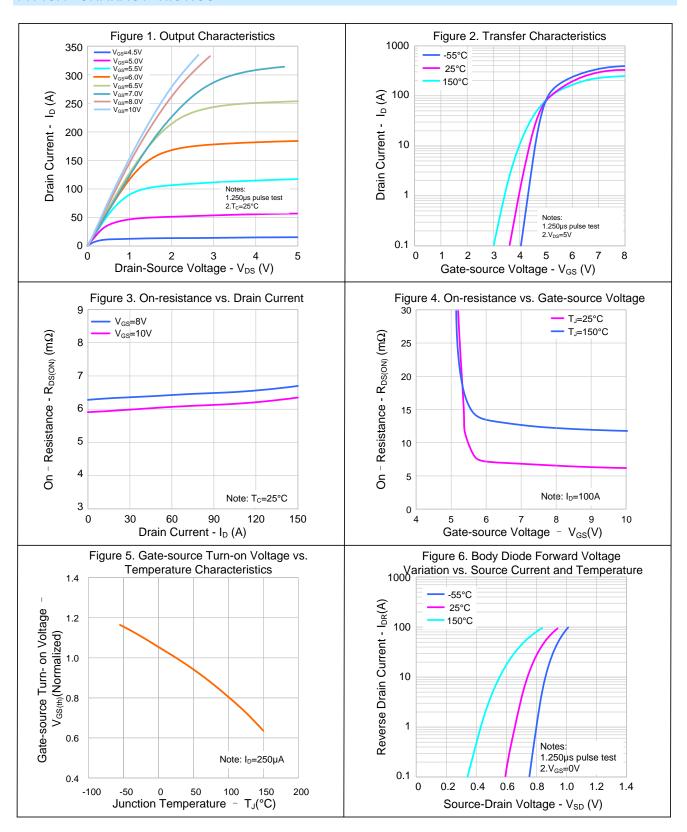
- 1.
- 2. The dissipation power will change with temperature, derating above 25°C:2.1W/°C;
- 3. Pulse Test: Pulse width ≤300µs, Duty cycle≤2%;
- Essentially independent of operating temperature.

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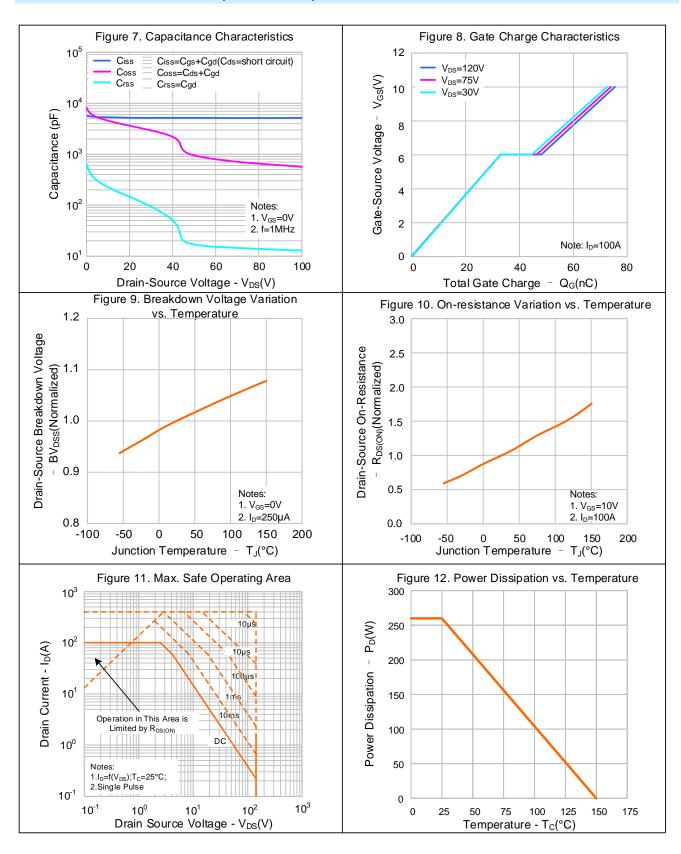
TYPICAL CHARACTERISTICS



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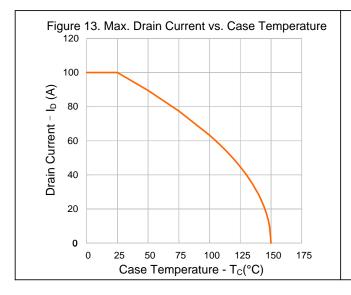
TYPICAL CHARACTERISTICS (CONTINUED)

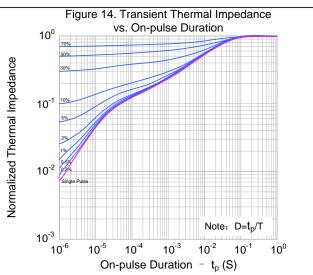


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TYPICAL CHARACTERISTICS (CONTINUED)



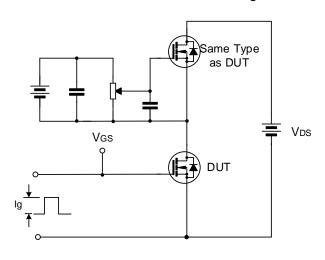


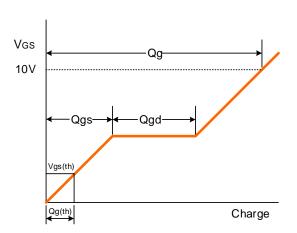
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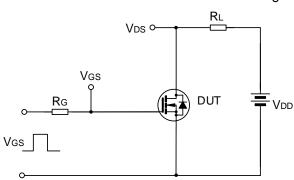
TYPICAL TEST CIRCUIT

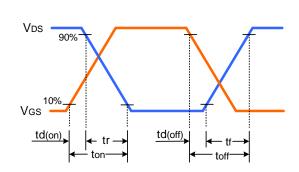
Gate Charge Test Circuit & Waveform



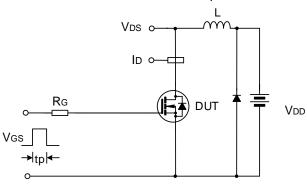


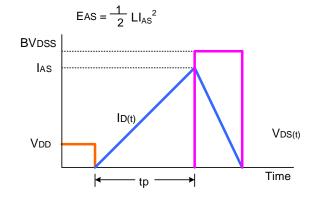
Resistive Switching Test Circuit & Waveform





Unclamped Inductive Switching Test Circuit & Waveform



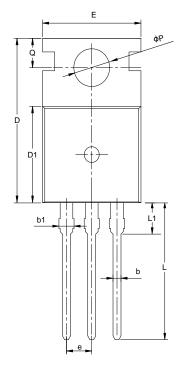


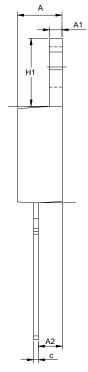
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PACKAGE OUTLINE

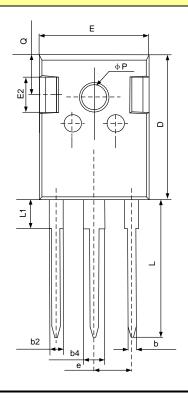
TO-220-3L UNIT: mm

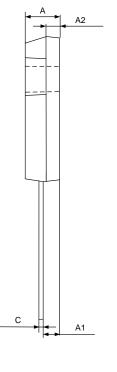




SYMBOL	MILLIMETER				
STIVIBUL	MIN	NOM	MAX		
Α	4.30	4.50	4.70		
A1	1.00	1.30	1.50		
A2	1.80	2.40	2.80		
b	0.60	0.80	1.00		
b1	1.00	_	1.60		
С	0.30	_	0.70		
D	15.10	15.70	16.10		
D1	8.10	9.20	10.00		
Е	9.60	9.90	10.40		
е		2.54BSC			
H1	6.10	6.50	7.00		
L	12.60	13.08	13.60		
L1	_	_	3.95		
ФΡ	3.40	3.70	3.90		
Q	2.60	_	3.20		

TO-247-3L UNIT: mm





SYMBOL	MILLIMETER				
OTMBOL	MIN	NOM	MAX		
Α	4.80	5.00	5.20		
A1	2.21	2.41	2.59		
A2	1.85	2.00	2.15		
b	1.11	-	1.36		
b2	1.91	_	2.25		
b4	2.91	_	3.25		
С	0.51	_	0.75		
D	20.80	21.00	21.30		
E	15.50	15.80	16.10		
E2	4.40	5.00	5.20		
е		5.44 BS	С		
L	19.72	19.92	20.22		
L1	_	_	4.30		
Q	5.60	5.80	6.00		
Р	3.40	_	3.80		

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MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

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- 1. Silan reserves the right to make changes of this instruction without notice.
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Part No.: SVGP157R5NT(P7) Document Type: Datasheet

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Rev.: 1.3 Revision History:

1. Add SVGP157R5NP7(TO-247-3L) package

Rev.: 1.2

Revision History:

1. Update SOA

2. Update typical test circuit

Rev.: 1.1

Revision History:

1. Add figures 4, 5, 12, 13 and 14

2. Update SOA

Rev.: 1.0

Revision History:

1. First release

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