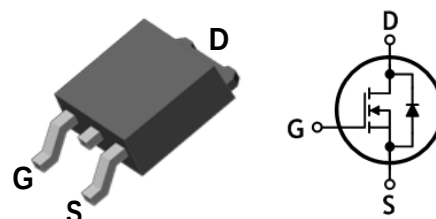


HIGH SPEED SWITCHING APPLICATION

Features

- Low drain-source On resistance: $R_{DS(on)}=1.2\Omega$ (Typ.)
- Low gate charge: $Q_g=21nC$ (Typ.)
- Low reverse transfer capacitance: $C_{rss}=5pF$ (Typ.)
- Lower EMI noise
- RoHS compliant device
- 100% avalanche tested

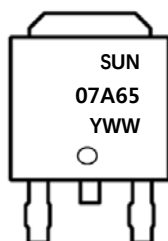


Ordering Information

Part Number	Marking	Package
SUN07A65D	SUN07A65	TO-252

TO-252

Marking Information



Column 1, 2: Device Code
Column 3: Production Information
e.g.) YWW
-. YWW: Date Code (year, week)

Absolute maximum ratings ($T_c=25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	V_{DS}	650	V
Gate-source voltage	V_{GS}	± 30	V
Drain current (DC) *	I_D	$T_c=25^\circ C$	7
		$T_c=100^\circ C$	4.43
Drain current (Pulsed) *	I_{DM}	28	A
Single avalanche energy (Note 2)	E_{AS}	92.9	mJ
Repetitive avalanche current (Note 1)	I_{AR}	7	A
Repetitive avalanche energy (Note 1)	E_{AR}	65	mJ
Power dissipation	P_D	65	W
Junction temperature	T_J	150	$^\circ C$
Storage temperature range	T_{stg}	-55~150	$^\circ C$

* Limited only maximum junction temperature

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 1.9	°C/W
Thermal resistance, junction to ambient	$R_{th(j-pcb)}$	Max. 50	

Electrical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0$	650	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}$, $V_{DS}=V_{GS}$	3	-	5	V
Drain-source cut-off current	I_{DSS}	$V_{DS}=650\text{V}$, $V_{GS}=0\text{V}$	-	-	1	μA
		$V_{DS}=650\text{V}$, $T_c=150^\circ\text{C}$	-	-	100	μA
Gate leakage current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 30\text{V}$	-	-	± 100	nA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}$, $I_D=3.5\text{A}$	-	1.2	1.4	Ω
Forward transfer conductance (Note 3)	g_{fs}	$V_{DS}=10\text{V}$, $I_D=3.5\text{A}$	-	8.7	-	S
Input capacitance	C_{iss}	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$	-	1380	-	pF
Output capacitance	C_{oss}		-	90	-	
Reverse transfer capacitance	C_{rss}		-	9	-	
Turn-on delay time (Note 3,4)	$t_{d(on)}$	$V_{DS}=325\text{V}$, $I_D=7\text{A}$, $R_G=25\Omega$	-	69	-	ns
Rise time (Note 3,4)	t_r		-	37	-	
Turn-off delay time (Note 3,4)	$t_{d(off)}$		-	130	-	
Fall time (Note 3,4)	t_f		-	25	-	
Total gate charge (Note 3,4)	Q_g	$V_{DS}=520\text{V}$, $V_{GS}=10\text{V}$, $I_D=7\text{A}$	-	21	26	nC
Gate-source charge (Note 3,4)	Q_{gs}		-	9	-	
Gate-drain charge (Note 3,4)	Q_{gd}		-	5	-	

Source-Drain Diode Ratings and Characteristics ($T_c=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	7	A
Source current (Pulsed)	I_{SM}		-	-	28	A
Forward voltage	V_{SD}	$V_{GS}=0\text{V}$, $I_{SD}=7\text{A}$	-	-	1.4	V
Reverse recovery time (Note 3,4)	t_{rr}	$I_{SD}=7\text{A}$, $V_{GS}=0\text{V}$ $dI_F/dt=100\text{A}/\mu\text{s}$	-	410	-	ns
Reverse recovery charge (Note 3,4)	Q_{rr}		-	1.7	-	μC

Note:

1. Repeated rating: Pulse width limited by safe operating area
2. $L=3.5\text{mH}$, $I_{AS}=7\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$
3. Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
4. Essentially independent of operating temperature typical characteristics

Typical Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

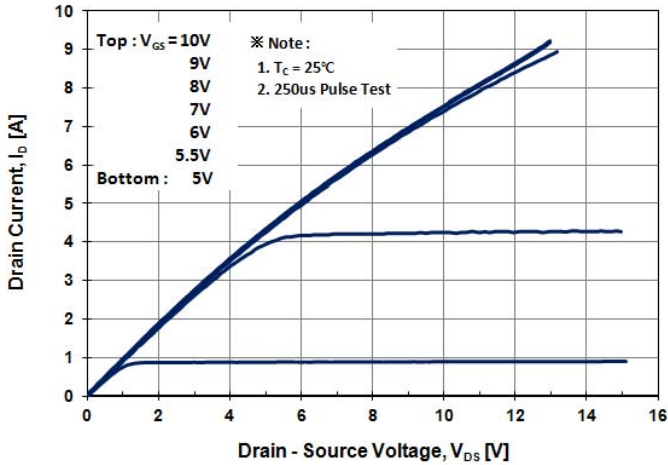


Fig. 2 Typical Output Characteristics

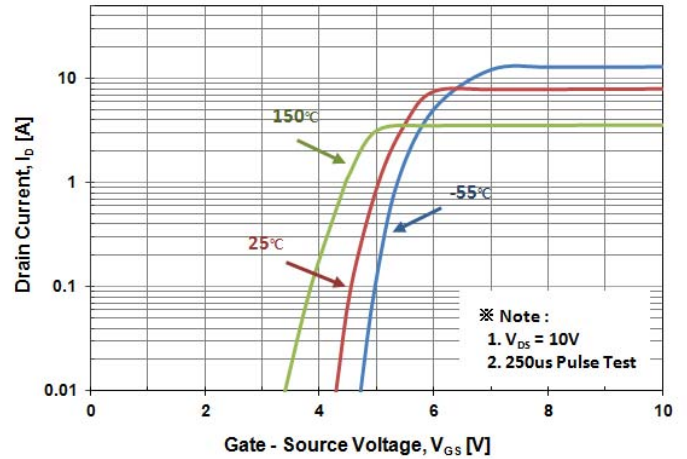


Fig.3 On-Resistance Variation with Drain Current and Gate Voltage

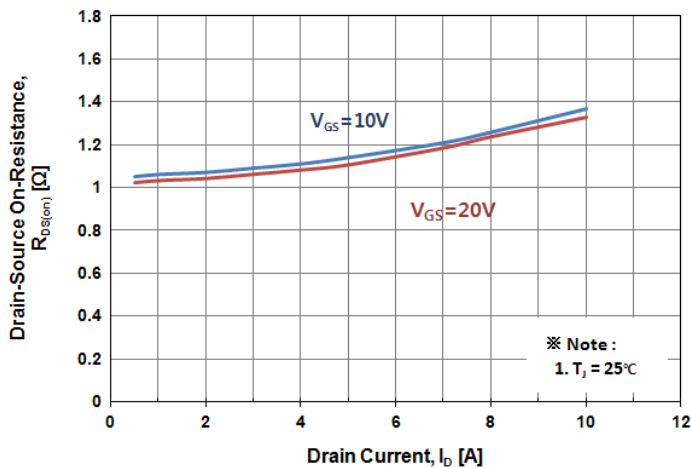


Fig. 4 Body Diode Forward Voltage Variation with Source Current

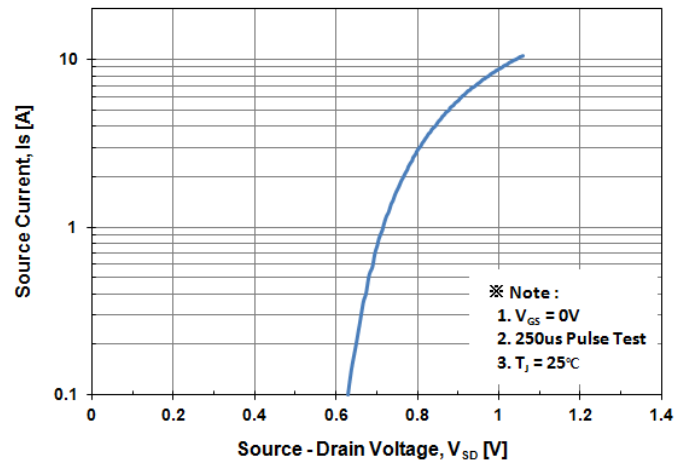


Fig. 5 Typical Capacitance Characteristics

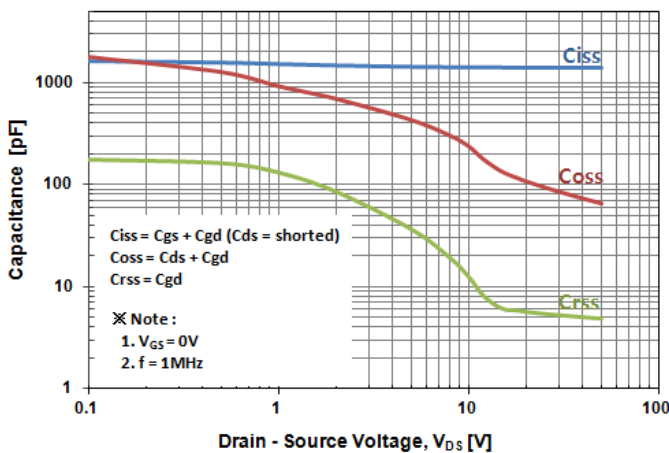


Fig. 6 Typical Total Gate Charge Characteristics

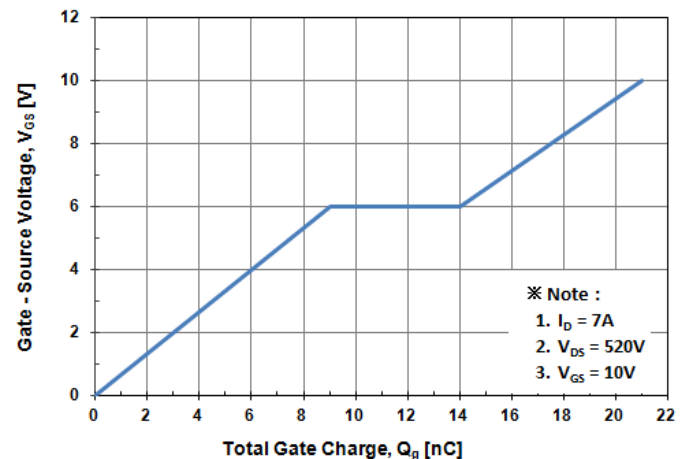


Fig. 7 Breakdown Voltage Variation vs. Temperature

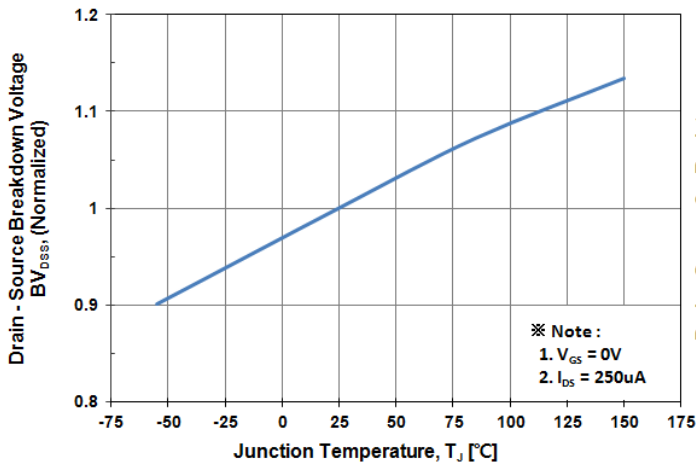


Fig. 8 On-Resistance Variation vs. Temperature

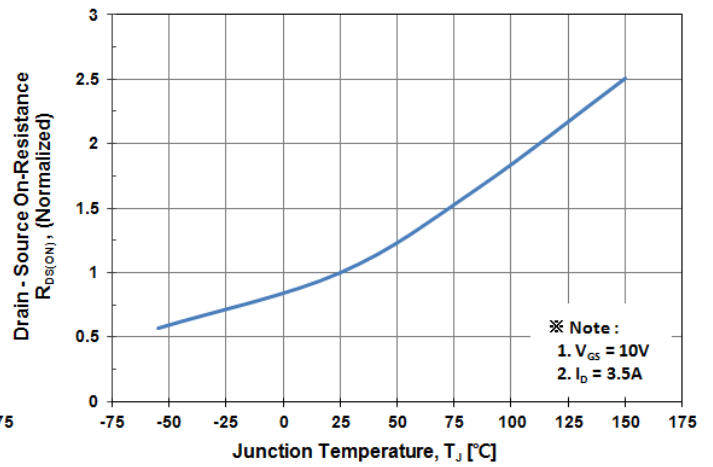


Fig. 9 Maximum Drain Current vs. Case Temperature

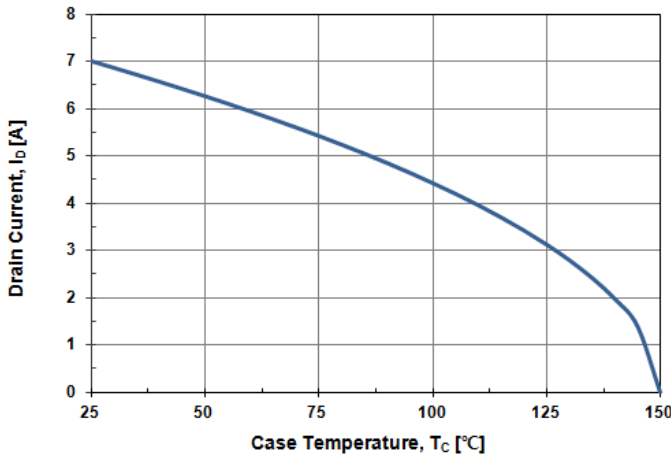


Fig. 10 Maximum Safe Operating Area

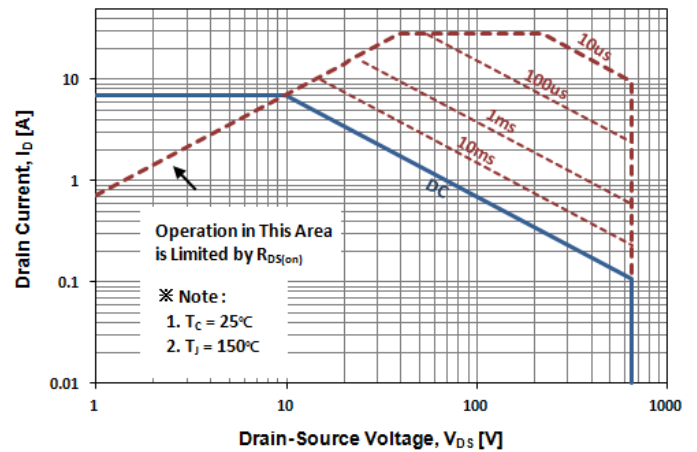


Fig. 11 Transient Thermal Impedance

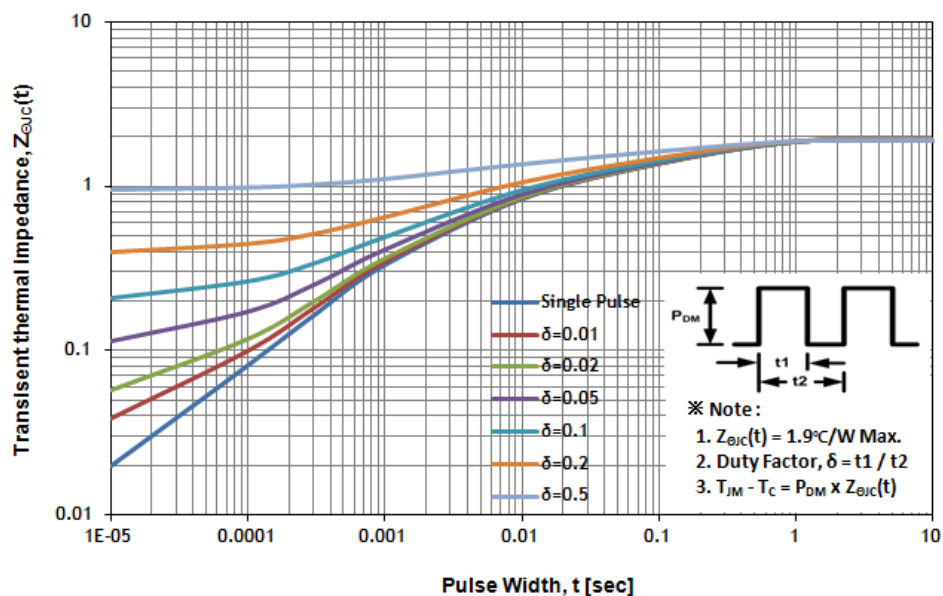


Fig. 12 Gate Charge Test Circuit & Waveform

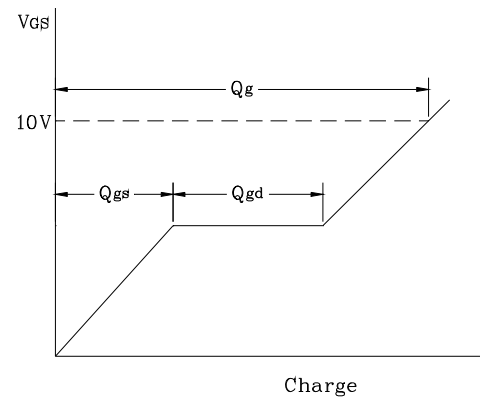
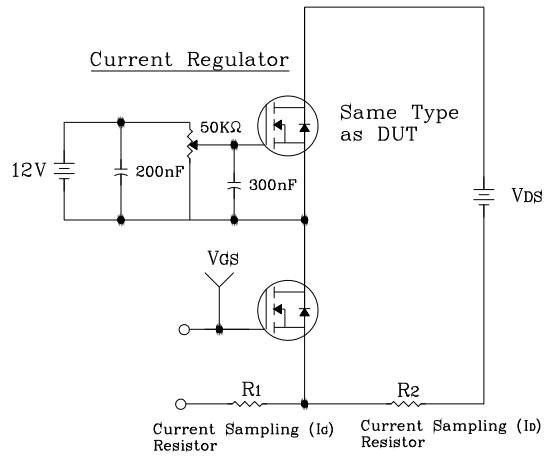


Fig. 13 Resistive Switching Test Circuit & Waveform

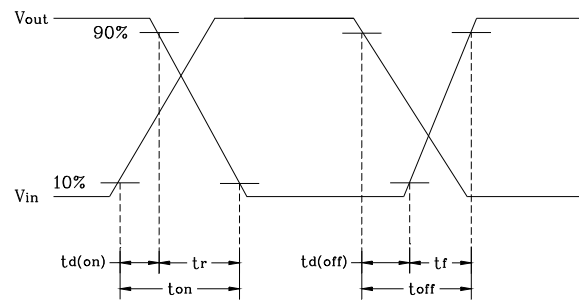
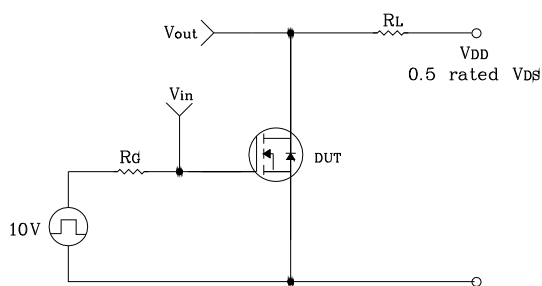


Fig. 14 E_{AS} Test Circuit & Waveform

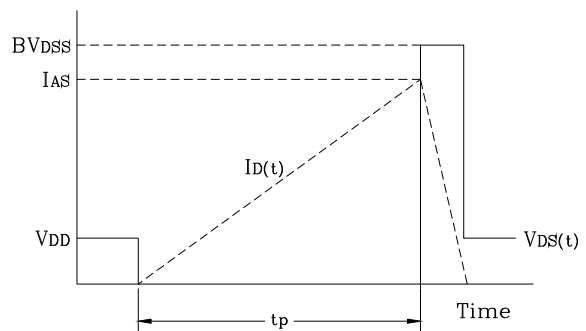
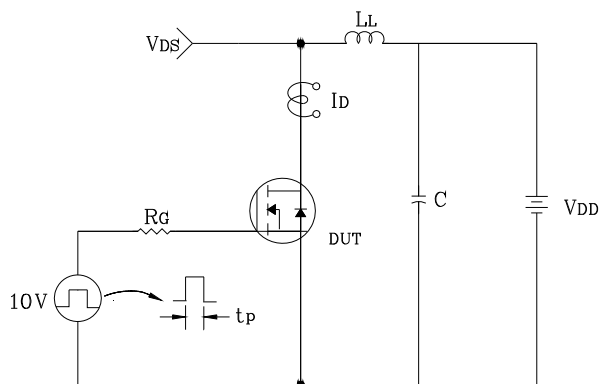
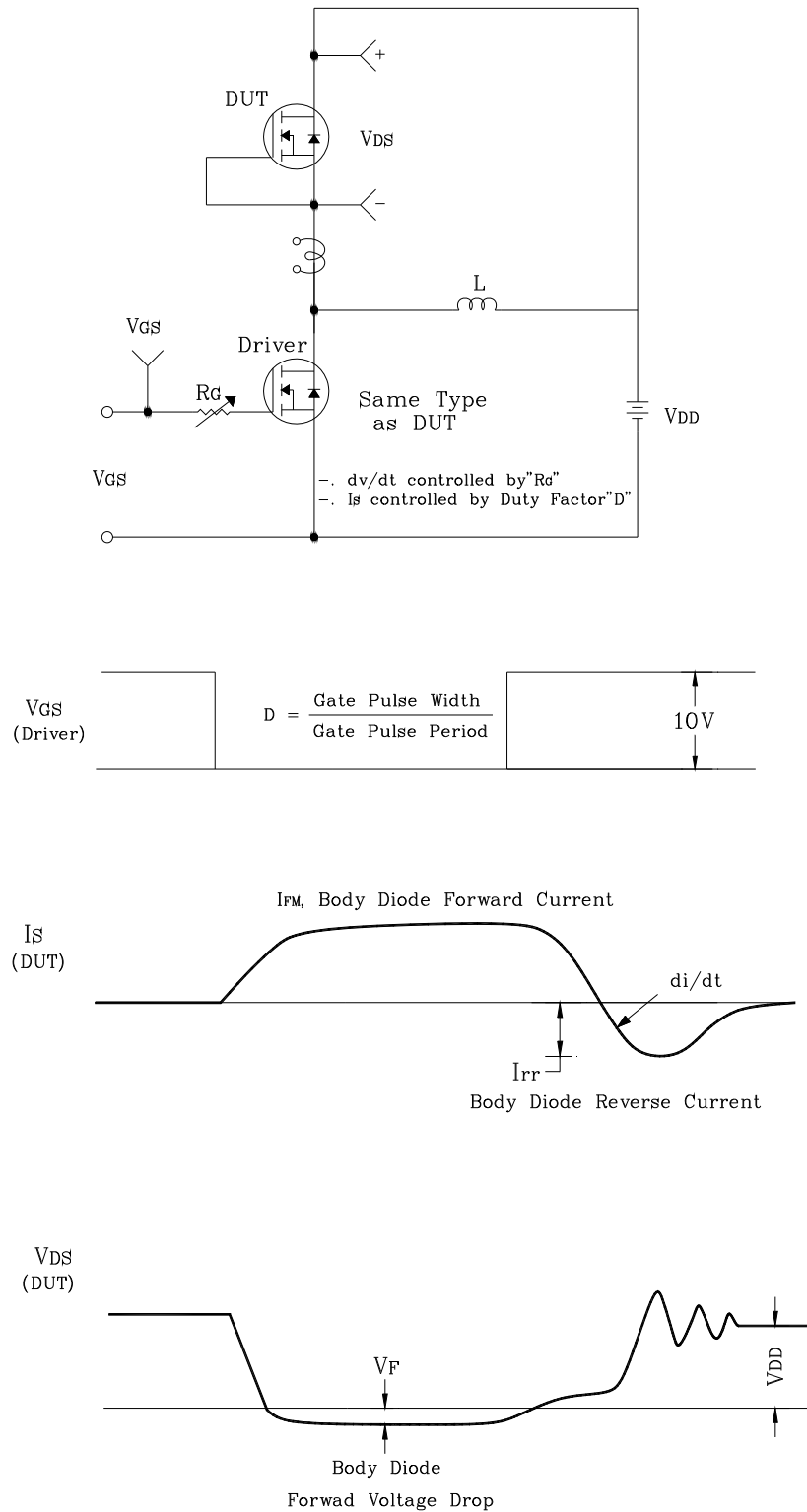
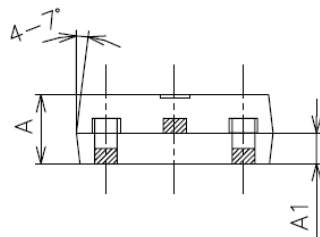
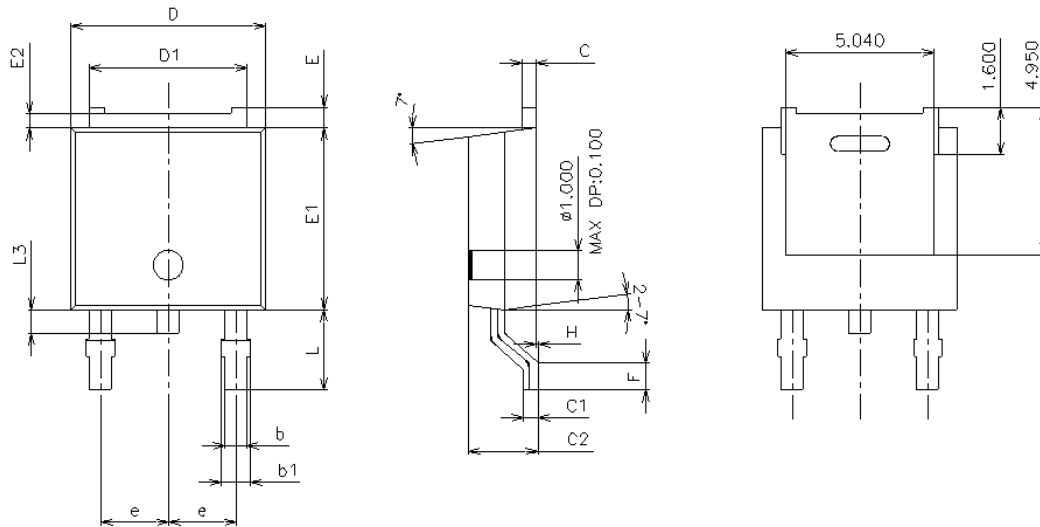


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform

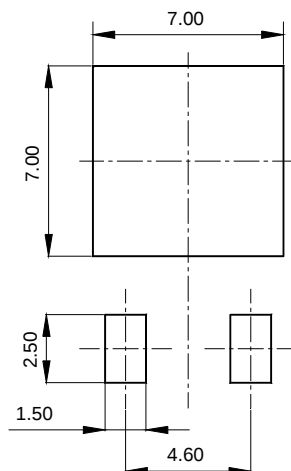


Package Outline Dimensions



SYMBOL	MILLIMETERS			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
D	6.40	6.60	6.80	
D1	5.14	5.34	5.54	
E	0.50	0.70	0.90	
E1	5.90	6.10	6.30	
E2	0.50 TYP			
A	2.20	2.30	2.40	
A1	0.87	1.07	1.27	
C	0.40	0.50	0.60	
C1	0.40	0.50	0.60	
C2	2.10	2.30	2.50	
L	2.50	2.70	2.90	
L3	0.60	0.80	1.00	
b	0.66	0.76	0.86	
b1	0.96 MAX			
e	2.10	2.30	2.50	
F	0.80 MIN			
H	0.00	-	0.10	

Recommended Land Pattern [unit: mm]



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