N-Channel 25-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[a, d]	Q_g (Typ.)
25	0.0045 at V_{GS} = 10 V	50	36.25 nC
	0.0060 at V_{GS} = 4.5 V	50	

FEATURES

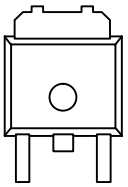
- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested

RoHS COMPLIANT

APPLICATIONS

- DC/DC Conversion, Low-Side
  - Desktop PC
  - Server

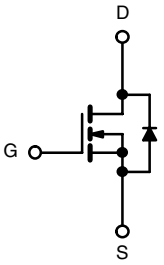
TO-252



Drain Connected to Tab

Top View

Ordering Information: SUD50N025-4m5P-E3 (Lead (Pb)-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	25	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 175 °C)	T_C = 25 °C	I_D	50[a, d]	A
	T_C = 70 °C		50[a, d]	
	T_A = 25 °C		18[b, c]	
	T_A = 70 °C		15[b, c]	
Pulsed Drain Current		I_{DM}	100	
Avalanche Current	L = 0.1 mH	I_{AS}	28	
Repetitive Avalanche Energy		E_{AS}	39	V
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	50[a, d]	A
	T_A = 25 °C		2.1[b, c]	
Maximum Power Dissipation	T_C = 25 °C	P_D	108[a]	W
	T_C = 70 °C		75.6[a]	
	T_A = 25 °C		2.5[b, c]	
	T_A = 70 °C		1.75[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[b, c]	t ≤ 10 s	R_{thJA}	48	60	°C/W
Maximum Junction-to-Case	Steady State	R_{thJC}	1.6	2	

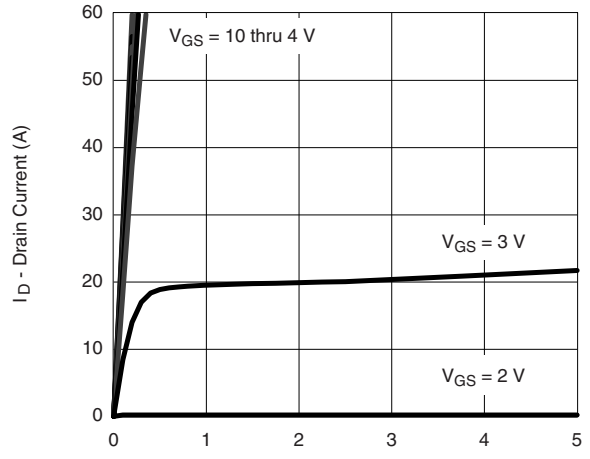
Notes:
a. Based on T_C = 25 °C.
b. Surface Mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. Calculated based on maximum junction temperature. Package limitation current is 50 A.
e. Maximum under Steady State conditions is 90 °C/W.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	25			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA		25.7		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 6.6		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1		3	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 25 V, V_{GS} = 0 V			1	µA
		V_{DS} = 25 V, V_{GS} = 0 V, T_J = 55 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	50			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 18 A		0.0037	0.0045	Ω
		V_{GS} = 4.5 V, I_D = 15 A		0.005	0.006	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 18 A		98		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 12 V, V_{GS} = 0 V, f = 1 MHz		5102		pF
Output Capacitance	C_{oss}			1025		
Reverse Transfer Capacitance	C_{rss}			525		
Total Gate Charge	Q_g	V_{DS} = 13 V, V_{GS} = 10 V, I_D = 18 A		76.3	115	nC
		V_{DS} = 13 V, V_{GS} = 4.5 V, I_D = 15 A		36.3	55	
Gate-Source Charge	Q_{gs}			10.2		
Gate-Drain Charge	Q_{gd}			7.6		
Gate Resistance	R_g	f = 1 MHz	0.53	1.05	1.58	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 13 V, R_L = 0.722 Ω $I_D \cong$ 18 A, V_{GEN} = 4.5 V, R_g = 1 Ω		48	72	ns
Rise Time	t_r			175	263	
Turn-Off Delay Time	$t_{d(off)}$			84	126	
Fall Time	t_f			51	77	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 13 V, R_L = 0.87 Ω $I_D \cong$ 15 A, V_{GEN} = 10 V, R_g = 1 Ω		24	36	
Rise Time	t_r			8	12	
Turn-Off Delay Time	$t_{d(off)}$			12	18	
Fall Time	t_f			8.5	13	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			50	A
Pulse Diode Forward Current[a]	I_{SM}				90	
Body Diode Voltage	V_{SD}	I_S = 15 A		0.9	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 5 A, dI/dt = 100 A/µs, T_J = 25 °C		26.3	40	ns
Body Diode Reverse Recovery Charge	Q_{rr}			16	24	nC
Reverse Recovery Fall Time	t_a			12.8		ns
Reverse Recovery Rise Time	t_b			13.5		

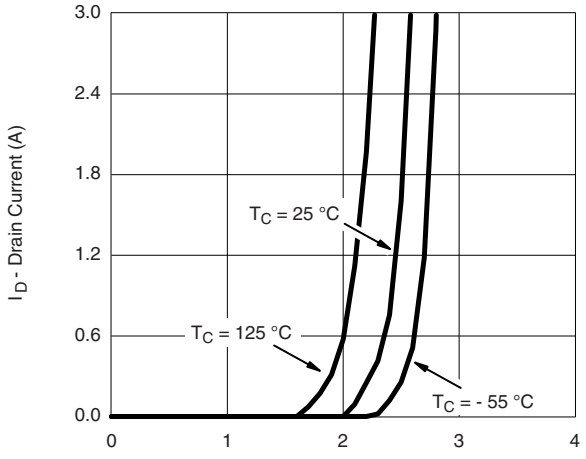
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

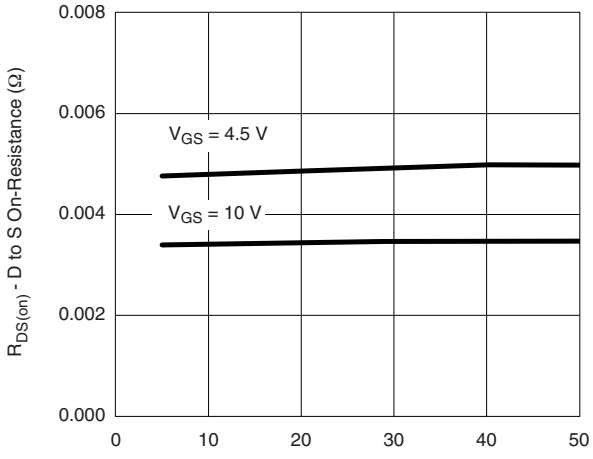
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



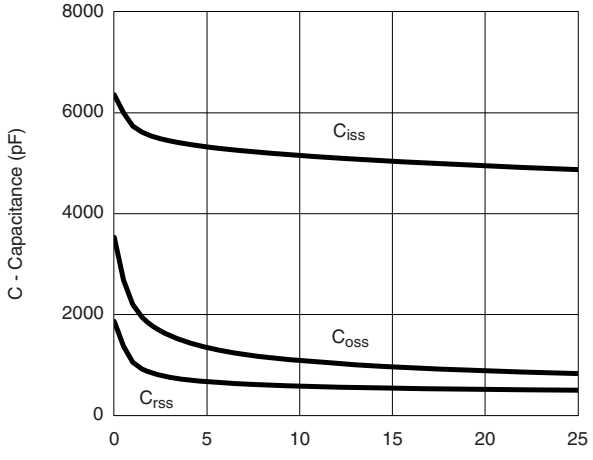
Output Characteristics



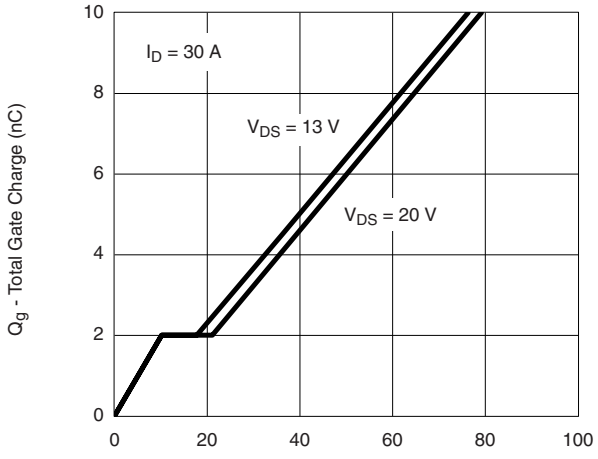
Transfer Characteristics



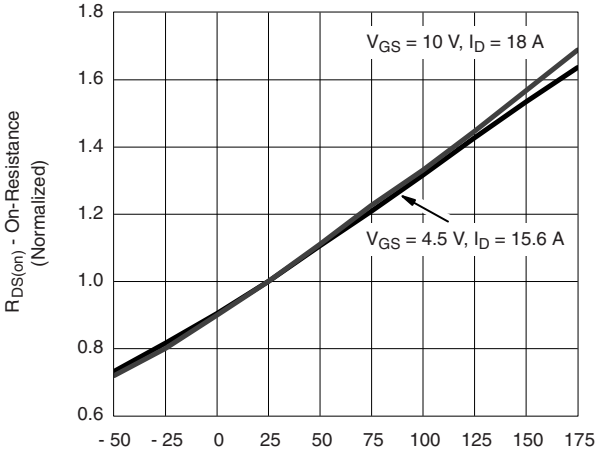
$r_{DS(on)}$ vs. Drain Current



Capacitance

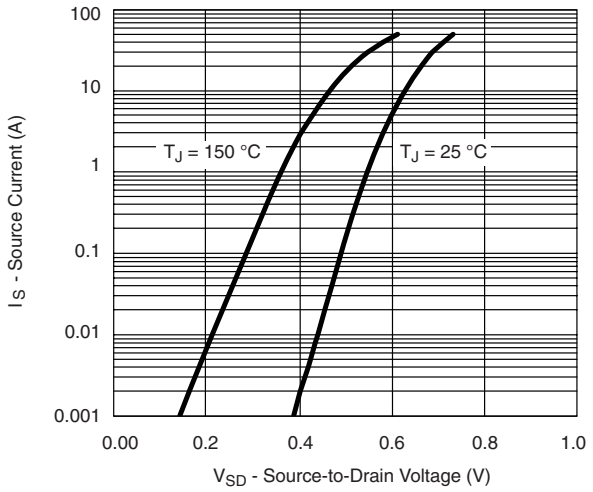


Gate Charge

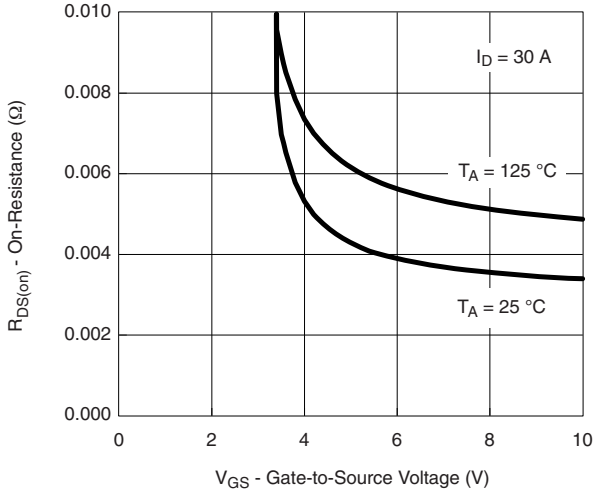


On-Resistance vs. Junction Temperature

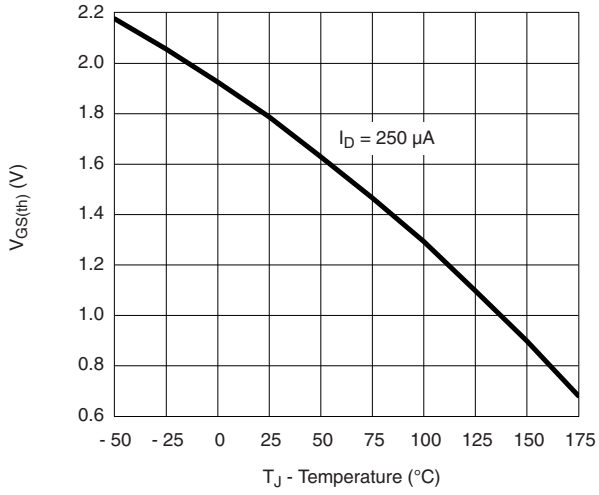
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



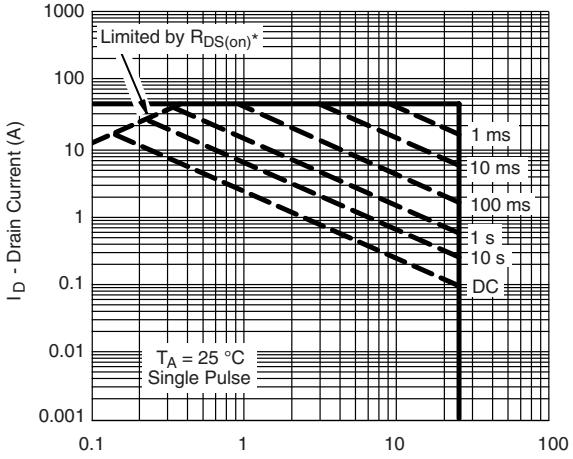
Forward Diode Voltage vs. Temperature



$R_{DS(on)}$ vs. V_{GS} vs. Temperature



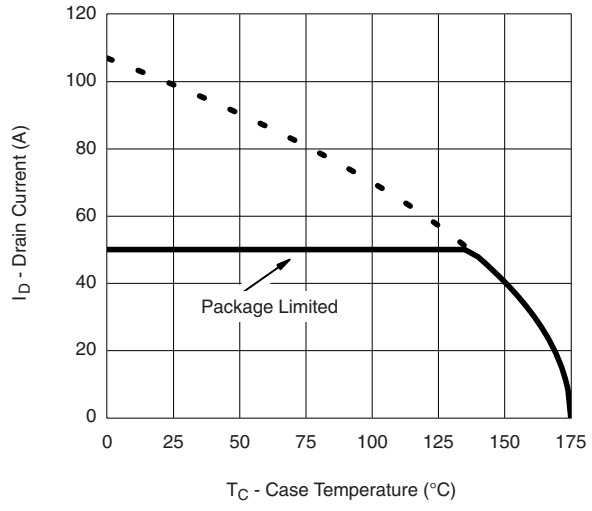
Threshold Voltage



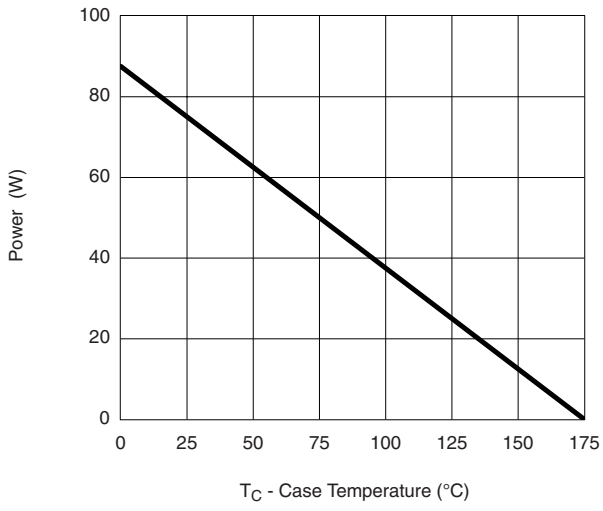
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

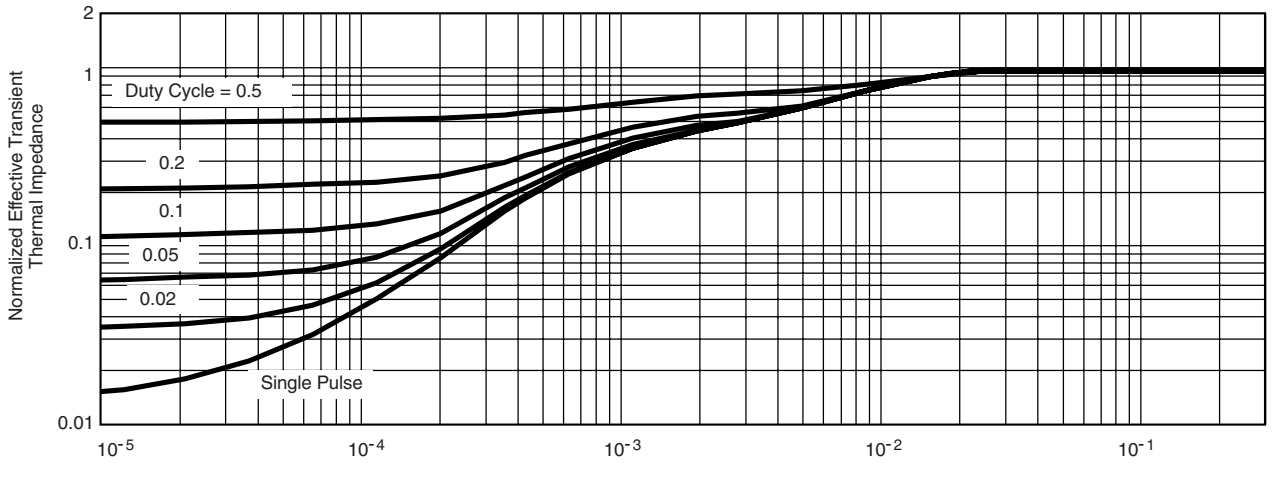


Current Derating*



Power Derating

* The power dissipation P_D is based on $T_{J(max)}$ = 175 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



Normalized Thermal Transient Impedance, Junction-to-Case

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